Stratix III Device Handbook, Volume 1

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Chapter Revision Dates

The chapters in this book, *Stratix III Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

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Chapter 9. High-Speed Differential I/O Interfaces and DPA in Stratix III Devices
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Chapter 13. IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices
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Chapter 14. Design Security in Stratix III Devices
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Chapter 15. SEU Mitigation in Stratix III Devices
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Chapter 16. Programmable Power and Temperature Sensing Diode in Stratix III Devices
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Chapter 17. Stratix III Device Packaging Information
Revised: *May 2007*
Part number: *SIII51017-1.1*

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® III family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section I. Device Core

This section provides a complete overview of all features relating to the Stratix® III device family, which is the most architecturally advanced, high performance, low power FPGA in the market place. This section includes the following chapters:

- Chapter 1, Stratix III Device Family Overview
- Chapter 2, Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices
- Chapter 3, MultiTrack Interconnect in Stratix III Devices
- Chapter 4, TriMatrix Embedded Memory Blocks in Stratix III Devices
- Chapter 5, DSP Blocks in Stratix III Devices
- Chapter 6, Clock Networks and PLLs in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. Stratix III Device Family Overview

SIII51001-1.1

Introduction

The Stratix® III family provides the most architecturally advanced, high performance, low power FPGAs in the market place.

Stratix III FPGAs lower power consumption through Altera's innovative Programmable Power Technology, which provides the ability to turn on the performance where needed and turn down the power consumption everywhere else. Selectable Core Voltage and the latest in silicon process optimizations are also employed to deliver the industry's lowest power, high performance FPGAs.

Specifically designed for ease of use and rapid system integration, the Stratix III FPGA family offers three family variants optimized to meet different application needs:

- The Stratix III *L* family provides balanced logic, memory, and multiplier ratios for mainstream applications.
- The Stratix III *E* family is memory and multiplier rich for data-centric applications.
- The Stratix III *GX* family contains embedded high-speed serial transceivers and extensive internal memory for high bandwidth applications.

Modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic on-chip termination, output delay and current strength control provide best-in-class signal integrity.

Based on a 1.1-V, 65-nm all-layer copper SRAM process, the Stratix III family is a programmable alternative to custom ASICs and programmable processors for high performance logic, digital signal processing (DSP), and embedded designs and architects.

Stratix III devices include optional configuration bit stream security through volatile or non-volatile 256-bit Advanced Encryption Standard (AES) encryption. Where ultra-high reliability is required, Stratix III devices include automatic error detection circuitry to detect data corruption by soft errors in the configuration random-access memory (CRAM) and user memory cells.

Features

Stratix III devices offer the following features:

- 48,000 to 338,000 equivalent logic elements (LEs), see Table 1–1
- 2,430 to 20,497 Kbits of enhanced TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of 9×9, 12×12, 18×18, 36×36 multipliers (at up to 550 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- I/O:GND:PWR ratio of 8:1:1 along with on-die and on-package decoupling for robust signal integrity
- Programmable Power Technology, which minimizes power while maximizing device performance
- Selectable Core Voltage, available in low-voltage devices (*L* ordering code suffix), enables selection of lowest power or highest performance operation
- Up to 16 global clocks, 88 regional clocks and 116 peripheral clocks per device
- Up to 12 phase-locked loops (PLLs) per device that support PLL reconfiguration, clock switchover, programmable bandwidth, clock synthesis and dynamic phase shifting
- Memory interface support with dedicated DQS logic on all I/O banks
- Support for high-speed external memory interfaces including DDR,DDR2,DDR3 SDRAM, RLDRAM II, QDR II and QDR II+ SRAM on up to 24 modular I/O banks
- Up to 1,104 user I/O pins arranged in 24 modular I/O banks that support a wide range of industry I/O standards
- Dynamic On-Chip Termination (OCT) with auto calibration support on all I/O banks
- High-speed differential I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry for 1.25 Gbps performance
- Support for high-speed networking and communications bus standards including SPI-4.2, SFI-4, SGMII, Utopia IV, 10 Gigabit Ethernet XSLI, Rapid I/O and NPSI
- The only high-density, high-performance FPGA with support for 256-bit (AES) volatile and non-volatile security key to protect designs
- Robust on-chip hot socketing and power sequencing support
- Integrated cyclical redundancy check (CRC) for configuration memory error detection with critical error determination for high availability systems support
- Built-in error correction coding (ECC) circuitry to detect and correct configuration or user memory error due to SEU events

- Nios II embedded processor support
- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP)

Table 1–1 lists the Stratix III FPGA family features.

Table 1–1. Stratix III FPGA Family Features

	Device/ Feature	ALMs	LEs	M9K blocks	M144K blocks	MLAB Blocks	Total Embedded RAM Kbits	MLAB Kbits	Total Memory Kbits	18×18-bit multipliers (FIR Mode)	PLLs
Stratix III Logic Family	EP3SL50	19K	47.5K	108	6	950	1,836	594	2,430	216	4
	EP3SL70	27K	67.5K	150	6	1,350	2,214	844	3,058	288	4
	EP3SL110	43K	107.5K	275	12	2,150	4,203	1,344	5,547	288	8
	EP3SL150	57K	142.5K	355	16	2,850	5,499	1,781	7,280	384	8
	EP3SL200	80K	200K	468	24	4,000	7,668	2,500	10,168	576	12
	EP3SE260	102K	255K	864	48	5,100	14,688	3,188	17,876	768	12
	EP3SL340	135K	337.5K	1,040	48	6,750	16,272	4,219	20,491	576	12
Stratix Enhanced Family	EP3SE50	19K	47.5K	400	12	950	5,328	594	5,922	384	4
	EP3SE80	32K	80K	495	12	1,600	6,183	1,000	7,183	672	8
	EP3SE110	43K	107.5K	639	16	2,150	8,055	1,344	9,399	896	8
	EP3SE260 *(1)*	102K	255K	864	48	5,100	14,688	3,188	17,876	768	12

Note to Table 1–1:

(1) The EP3SE260 device is rich in LE, memory, and multiplier resources. Hence, it aligns with both logic (*L*) and enhanced (*E*) variants.

The Stratix III logic family (*L*) offers balanced logic, memory, and multipliers to address a wide range of applications, while the enhanced family (*E*) offers more memory and multipliers per logic and is ideal for wireless, medical imaging, and military applications.

Stratix III devices are available in space-saving FineLine BGA packages (see Table 1–2 and Table 1–3).

Table 1–2 lists the Stratix III FPGA package options and I/O pin counts.

Table 1–2. Package Options and I/O Pin Counts *Note (1)*

Device	484-Pin FineLine BGA *(2)*	780-Pin FineLine BGA *(2)*	1152-Pin FineLine BGA *(2)*	1,517-Pin FineLine BGA *(3)*	1,760-Pin FineLine BGA *(3)*
EP3SL50	296	488	—	—	—
EP3SL70	296	488	—	—	—
EP3SL110	—	488	744	—	—
EP3SL150	—	488	744	—	—
EP3SL200	—	488	744	880 *(4)*	—
EP3SL340	—	—	744	976	1,120
EP3SE50	296	488	—	—	—
EP3SE80	—	488	744	—	—
EP3SE110	—	488	744	—	—
EP3SE260	—	488	744	976	—

Note to Table 1–2:

(1) The arrows indicate vertical migration.

(2) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p` and `CLK10n`) that can be used for data inputs.

(3) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

(4) I/O Bank 1B, 2B, 5B, and 6B are not available in the EP3SL200 F1517 FPGA.

All Stratix III devices support vertical migration within the same package (for example, you can migrate between the EP3SL50 and EP3SL70 devices in the 780-pin FineLine BGA package). Vertical migration allows you to migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus® II software (Assignments menu > Device > Migration Devices). You can migrate from the *L* family to the *E* family without increasing the number of LEs available. This minimizes the cost of vertical migration.

Table 1–3 lists the Stratix III FBGA package sizes.

Table 1–3. FineLine BGA Package Sizes

Dimension	484 Pin	780 Pin	1152 Pin	1,517 Pin	1760 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	529	841	1,225	1,600	1,849
Length/Width (mm/ mm)	23/23	29/29	35/35	40/40	43/43

Stratix III devices are available in up to three speed grades, -2, -3, and -4, with -2 being the fastest. Stratix III devices are offered in both commercial and industrial temperature range ratings with leaded and lead-free packages. Selectable Core Voltage is available in specially marked low-voltage devices (*L* ordering code suffix).

Architecture Features

The following section briefly describes the various features of the Stratix III family of FPGAs.

Logic Array Blocks and Adaptive Logic Modules

The Logic Array Block (LAB) is composed of basic building blocks known as Adaptive Logic Modules (ALMs) that can be configured to implement logic, arithmetic, and register functions. Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. ALMs are part of a unique, innovative logic structure that delivers faster performance, minimizes area, and reduces power consumption. ALMs expand the traditional 4-input look-up table architecture to 7 inputs, increasing performance by reducing LEs, logic levels, and associated routing. In addition, ALMs maximize DSP performance with dedicated functionality to efficiently implement adder trees and other complex arithmetic functions. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency.

The Logic Array Block (LAB) of Stratix-III has a new derivative called Memory LAB (or MLAB), which adds SRAM memory capability to the LAB. MLAB is a superset of the LAB and includes all LAB features. MLABs support a maximum of 640-bits of simple dual-port Static Random Access Memory (SRAM). Each ALM in an MLAB can be configured as either a 64×1 or 32×2 block, resulting in a configuration of 64×10 or 32×20 simple dual port SRAM block. MLAB and LAB blocks always co-exist as pairs in all Stratix-III families allowing up to 50% of the logic (LABs) to be traded for memory (MLABs).

For more information on LABs and ALMs, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

For more information on MLAB modes, features and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

MultiTrack Interconnect

In the Stratix III architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. The MultiTrack interconnect provides 1-hop connection to 34 adjacent LABs, 2-hop connections to 96 adjacent LABs and 3 hop connections to 160 adjacent LABs.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the reoptimization cycles that typically follow design changes and additions. The Quartus II Compiler also automatically places critical design paths on faster interconnects to improve design performance.

For more information, refer to the *MultiTrack Interconnect in Stratix III Devices* chapter of the *Stratix III Device Handbook, Volume 1*.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix III FPGA designs. TriMatrix memory includes the following blocks:

- 640-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers and shift registers
- 9-Kbit M9K blocks that can be used for general purpose memory applications
- 144-Kbit M144K blocks that are ideal for processor code storage, packet and video frame buffering

Each embedded memory block can be independently configured to be a single- or dual-port RAM, ROM, or shift register via the Quartus II MegaWizard. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of embedded SRAM at up to 600 MHz operation.

For more information on TriMatrix memory blocks, modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

DSP Blocks

Stratix III devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications requiring high data throughput. Stratix III devices provide you with the ability to implement various high performance DSP functions easily. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet protocol (VoIP), H.264 video compression and high-definition television (HDTV) require high performance DSP blocks to process data. These system designs typically use DSP blocks to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Stratix III devices have up to 112 DSP blocks. The architectural highlights of the Stratix III DSP block are the following:

- High performance, power optimized, fully pipelined multiplication operations
- Native support for 9-bit, 12-bit, 18-bit, 36-bit word lengths
- Native support for 18-bit complex multiplications
- Efficient support for floating point arithmetic formats (24-bit for Single Precision and 53-bit for Double Precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to efficiently combine multiplication results
- Cascading 18-bit input bus to form tap-delay lines
- Cascading 44-bit output bus to propagate output results from one block to the next block
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

DSP block multipliers can optionally feed an adder / subtractor or accumulator in the block depending on user configuration. This option saves ALM routing resources and increases performance, because all

connections and blocks are inside the DSP block. Additionally, the DSP Block input registers can efficiently implement shift registers for FIR filter applications, and the Stratix III DSP blocks support rounding and saturation. The Quartus II software includes megafunctions that control the mode of operation of the DSP blocks based on user parameter settings.

For more information, refer to the *DSP Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Clock Networks and PLLs

Stratix III devices provide dedicated Global Clock Networks (GCLKs), Regional Clock Networks (RCLKs), and Periphery Clock Networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 104 unique clock domains (16 GCLK + 88 RCLK) within the Stratix III device and allows for up to 38 (16 GCLK + 22 RCLK) unique GCLK/RCLK clock sources per device quadrant.

Stratix III delivers abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. Every output can be independently programmed creating a unique, customizable clock frequency with no fixed relation to any other input or output clock. Inherent jitter filtration and fine granularity control over multiply, divide ratios and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. Stratix III device PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management supporting multiplication, phase shifting, and programmable duty cycle. Stratix III PLLs also support external feedback mode, spread-spectrum input clock tracking and post-scale counter cascading.

For more information, refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

I/O Banks and I/O Structure

Stratix III devices contain up to 24 modular I/O banks, each of which contains 24, 32, 36, 40 or 48 I/Os. This modular bank structure improves pin efficiency and eases device migration. The left and right side I/O banks contain circuitry to support external memory interfaces at speeds up to 333 MHz and high-speed differential I/O interfaces meeting up to 1.25 Gbps performance. The top and bottom I/O banks contain circuitry to support external memory interfaces at speeds up to 400 MHz, high-speed differential inputs and outputs running at speeds up to 800 MHz and 500 MHz respectively.

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage referenced single-ended, and differential I/O standards. The Stratix III I/O supports programmable bus hold, programmable pull-up resistor, programmable slew rate, programmable output delay control, and open-drain output. Stratix III devices also support on-chip series (R_S) and on-chip parallel (R_T) termination with auto calibration for single-ended I/O standards and on-chip differential termination (R_D) for LVDS I/O standards on Left/Right I/O banks. Dynamic OCT is also supported on bi-directional I/O pins in all I/O banks.

For more information, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

External Memory Interfaces

The Stratix III I/O structure has been completely redesigned from the ground up to provide flexibility and enable high-performance support for existing and emerging external memory standards such as DDR, DDR2, DDR3, QDRII, QDRII+ and RLDRAMII at frequencies of up to 400 MHz.

Packed with features such as dynamic on-chip termination, trace mismatch compensation, read/write levelling, half-rate registers, 4- to 36-bit programmable DQ group widths, Stratix III I/O's supply the built in functionality required for rapid and robust implementation of external memory interfaces. Double data-rate support is found on all sides of the Stratix III device. Stratix III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces exactly where you want them.

A self-calibrating soft IP core (ALTMEMPHY) optimized to take advantage of Stratix III device I/O along with the new Quartus II timing analysis tool (TimeQuest) provide the total solution for the highest reliable frequency of operation across process voltage and temperature.

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

High Speed Differential I/O Interfaces with DPA

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSLI, Rapid I/O, and NPSI. Stratix III devices support 2×, 4×, 6×, 7×, 8× and 10× SERDES modes for high speed differential I/O interfaces and 4×, 6×, 7×, 8× and 10× SERDES modes when using the dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems. Soft CDR can also be implemented, enabling low-cost 1.25-Gbps clock embedded serial links.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Soft CDR functionality
- Synchronizer (FIFO buffer)
- PLLs

For more information, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Hot Socketing and Power-On Reset

Stratix III devices are hot-socketing compliant. Hot socketing is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence. You can insert or remove a Stratix III board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot-socketing feature also makes it easier to use Stratix III devices on printed circuit boards (PCBs) that also contain a mixture of 3.0-V, 2.5-V, 1.8-V, 1.5-V and 1.2-V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

For more information, refer to the *Hot Socketing and Power-On Reset in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Configuration

Stratix III devices are configured using one of the following four configuration schemes:

- Fast passive parallel (FPP)
- Fast active serial (AS)
- Passive serial (PS)
- Joint Test Action Group (JTAG)

All configuration schemes use either an external controller (for example, a MAX® II device or microprocessor), a configuration device, or a download cable.

Stratix III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Stratix III devices. During configuration, the Stratix III device decompresses the bitstream in real time and programs its SRAM cells.

Stratix III devices support decompression in the FPP when using a MAX II device / microprocessor + flash, fast AS, and PS configuration schemes. The Stratix III decompression feature is not available in the FPP when using the enhanced configuration device and JTAG configuration schemes.

For more information, refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Remote System Upgrades

Stratix III devices feature remote system upgrade capability, allowing error-free deployment of system upgrades from a remote location securely and reliably. Soft logic (either the Nios embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to Stratix series FPGAs and helps to avoid system downtime.

For more information refer to the *Remote System Upgrades with Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

IEEE 1149.1 (JTAG) Boundary Scan Testing

Stratix III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the Stratix III device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix III device in-circuit reconfiguration (ICR).

For more information refer to the *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Design Security

Stratix III devices are the only high-density, high-performance FPGAs with support for 256-bit volatile and non-volatile security keys to protect designs against copying, reverse engineering, and tampering. Stratix III devices have the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key.

The design security feature is available when configuring Stratix III FPGAs using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes.

For more information on the design security feature, refer to the *Design Security in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

SEU Mitigation

Stratix III devices have built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory (CRAM) cells. This feature allows all CRAM contents to be read and verified continuously during user mode operation to match a configuration-computed CRC value. The enhanced CRC circuit and frame-based configuration architecture allows detection and location of multiple, single, and adjacent bit errors which, in conjunction with a soft

circuit supplied as a reference design, allows don't-care soft errors in the CRAM to be ignored during device operation. This provides a step decrease in the effective soft error rate, increasing system reliability.

On-chip memory block SEU mitigation is also offered using the 9th bit and a configurable Megafunction in Quartus II for MLAB and M9K blocks while the M144K memory blocks have built-in error correction code (ECC) circuitry.

For more information on the dedicated error detection circuitry, refer to the *SEU Mitigation in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Programmable Power

Stratix III delivers Programmable Power, the only FPGA with user programmable power options balancing today's power and performance requirements. Stratix III devices utilize the most advanced power saving techniques including a variety of process, circuit, and architecture optimizations and innovations. In addition, user controllable power reduction techniques provide an optimal balance of performance and power reduction specific for each design configured into the Stratix III FPGA. The Quartus II software (starting from Version 6.1) automatically optimizes designs to meet the performance goals while simultaneously leveraging the programmable power saving options available in the Stratix III FPGA without the need for any changes to the design flow.

For more information on Programmable Power in Stratix III devices, refer to the following documents:

- *Programmable Power and Temperature Sensing Diode in Stratix III Devices* chapter of the *Stratix III Device Handbook, Volume 1*
- Power Optimization in the Stratix III Devices Application Note
- Stratix III Power White Paper

Signal Integrity

Stratix III devices simplify the challenge of signal integrity through a number of chip, package, and board level enhancements to enable efficient high speed data transfer into and out of the device. These enhancements include:

- 8:1:1 user I/O/Gnd/Vcc ratio to reduce the loop inductance in the package
- Dedicated power supply for each I/O bank, limit of I/Os is 24 to 48 I/Os per bank, to help limit simultaneous switching noise

- Programmable slew-rate support with up to 4 settings to match desired I/O standard, control noise, and overshoot
- Programmable output-current drive strength support with up to 4 settings to match desired I/O standard performance
- Programmable output-delay support to control rise/fall times and adjust duty cycle, compensate for skew and reduce simultaneous switching outputs (SSO) noise
- Dynamic OCT with auto calibration support for series and parallel OCT and differential OCT support for LVDS I/O standard on the left/right banks

For more information on SI support in Quartus II, refer to the *Quartus II Handbook*.

Reference and Ordering Information

The following section describes Stratix III device software support and ordering information.

Software

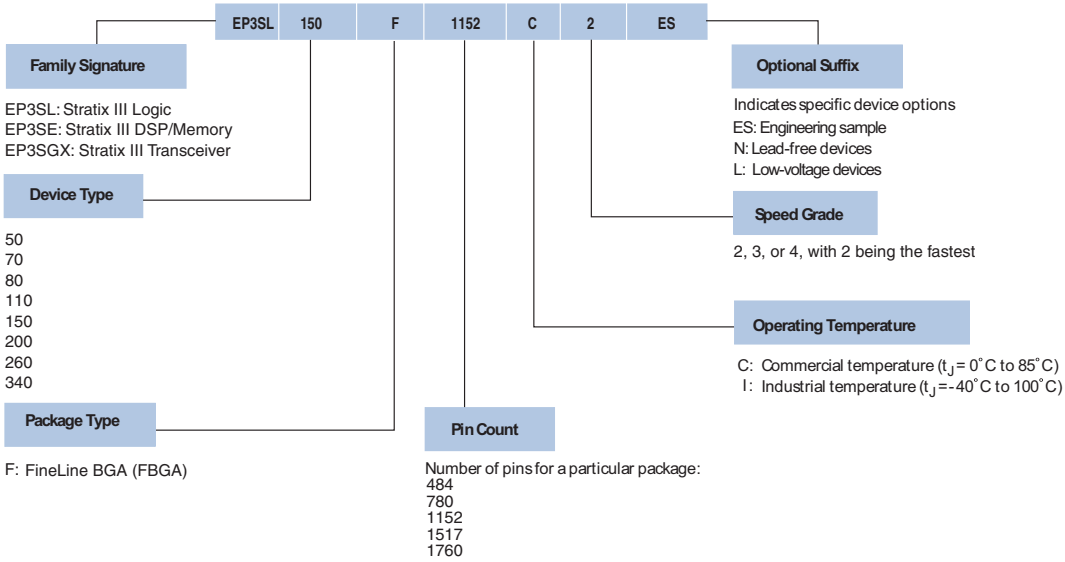
Stratix III devices are supported by the Altera Quartus II design software, version 6.1, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Quartus II Handbook* for more information on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Ordering Information

Figure 1–1 describes the ordering codes for Stratix III devices. For more information on a specific package, refer to the *Package Information for Stratix III Devices* chapter of the *Stratix III Device Handbook*.

Figure 1–1. Stratix III Device Packaging Ordering Information



Document Revision History

Table 1–4 shows the revision history for this document.

Table 1–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v 1.1	Minor formatting changes, fixed PLL numbers and ALM, LE and MLAB bit counts in Table 1–1.	—
November 2006 v1.0	Initial Release	—

2. Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices

SIII51002-1.1

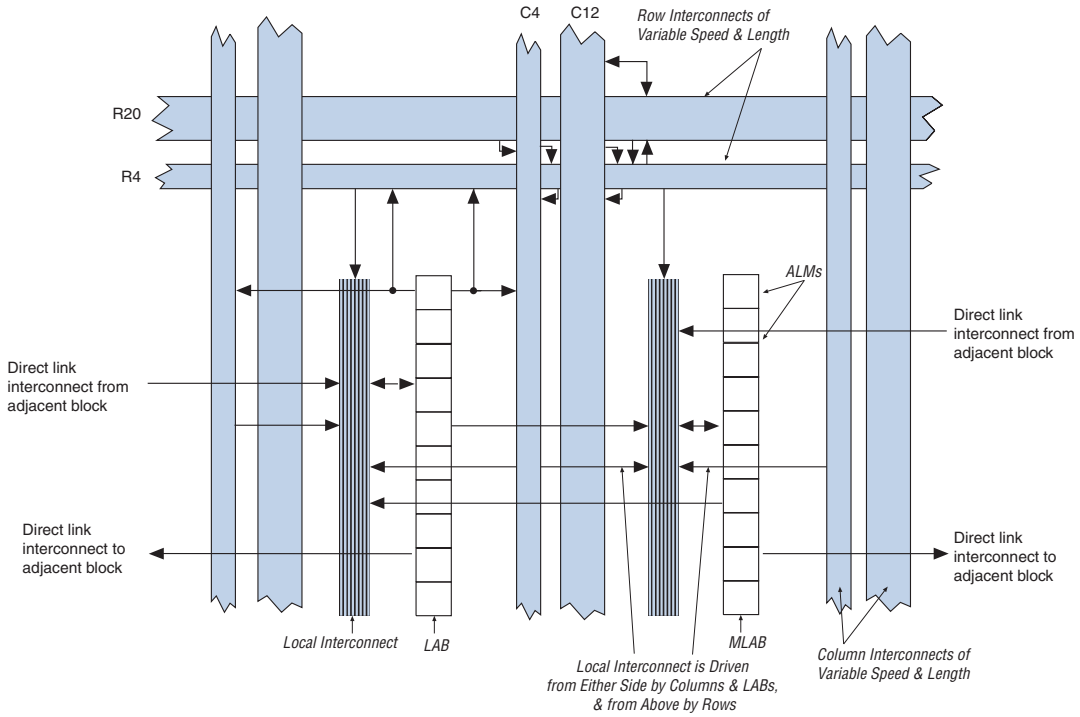
Introduction

This chapter describes the features of the logic array block (LAB) in the Stratix® III core fabric. The logic array block is composed of basic building blocks known as adaptive logic modules (ALMs) that can be configured to implement logic functions, arithmetic functions, and register functions.

Logic Array Blocks

Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. The direct link interconnect allows a LAB to drive into the local interconnect of its left and right neighbors. Register chain connections transfer the output of the ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2–1 shows the Stratix III LAB structure and the LAB interconnects.

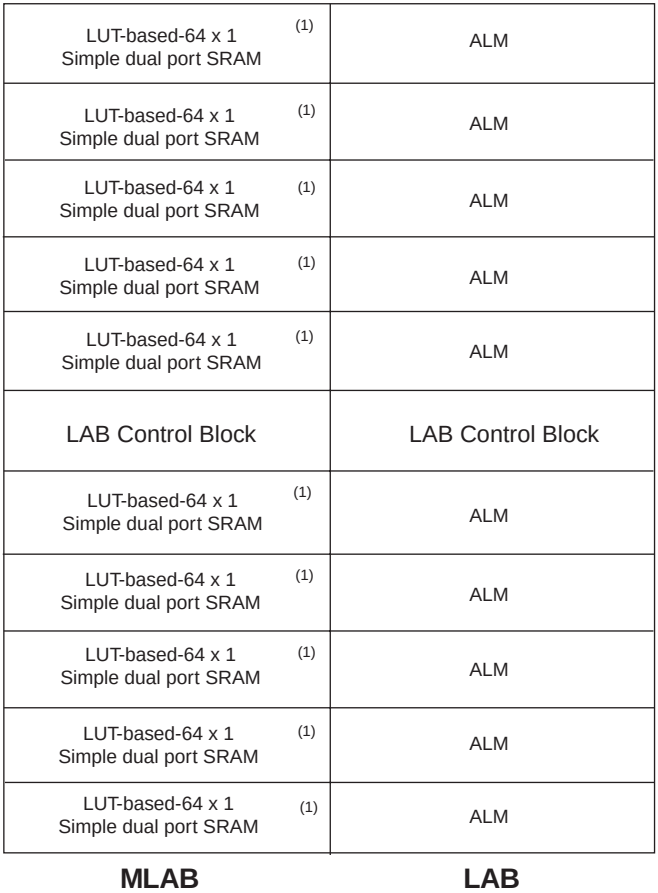
Figure 2–1. Stratix III LAB Structure



The LAB of Stratix III has a new derivative called Memory LAB (MLAB), which adds look-up table (LUT)-based SRAM capability to the LAB as shown in Figure 2–2. The MLAB supports a maximum of 640-bits of simple dual-port static random access memory (SRAM). You can configure each ALM in an MLAB as either a 64 × 1 or 32 × 2 block, resulting in a configuration of 64 × 10 or 32 × 20 simple dual port SRAM block. MLAB and LAB blocks always co-exist as pairs in all Stratix III families. MLAB is a superset of the LAB and includes all LAB features. Figure 2–2 shows an overview of LAB and MLAB topology.

The MLAB is described in detail in the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Figure 2–2. Stratix III LAB and MLAB Structure



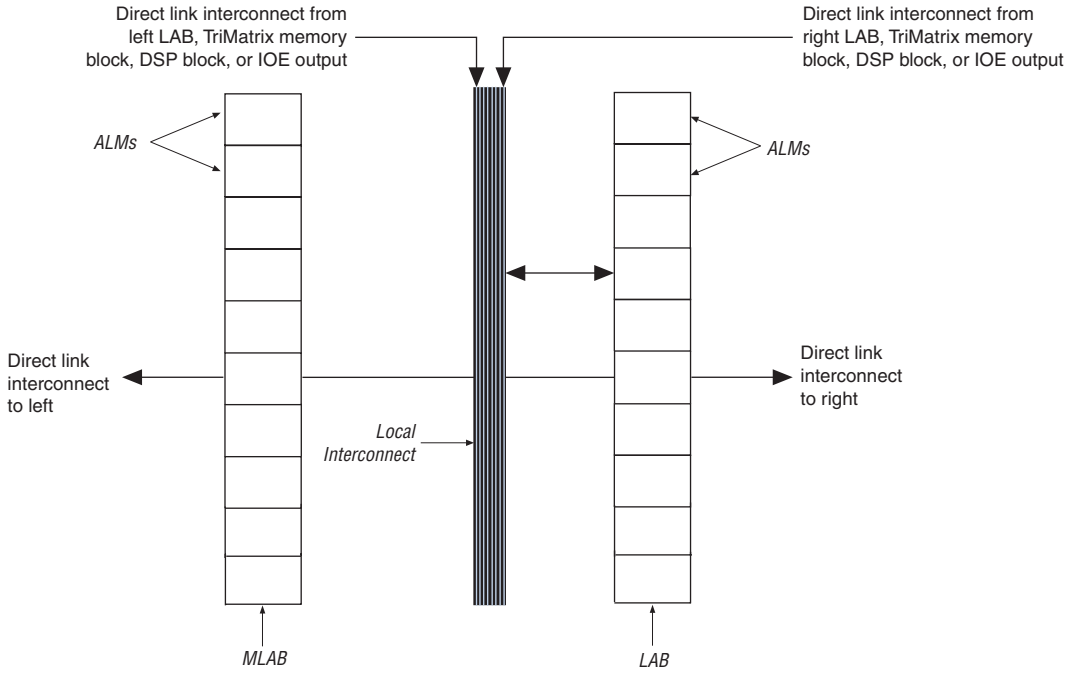
Note to Figure 2–2:
(1) You can use MLAB ALM as a regular LAB ALM or configure it as a dual-port SRAM, as shown.

LAB Interconnects

The LAB local interconnect can drive ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs / MLABs, M9K RAM blocks, M144K blocks, or DSP blocks from the left and right can also drive a LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 30 ALMs through fast local and direct link interconnects.

Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



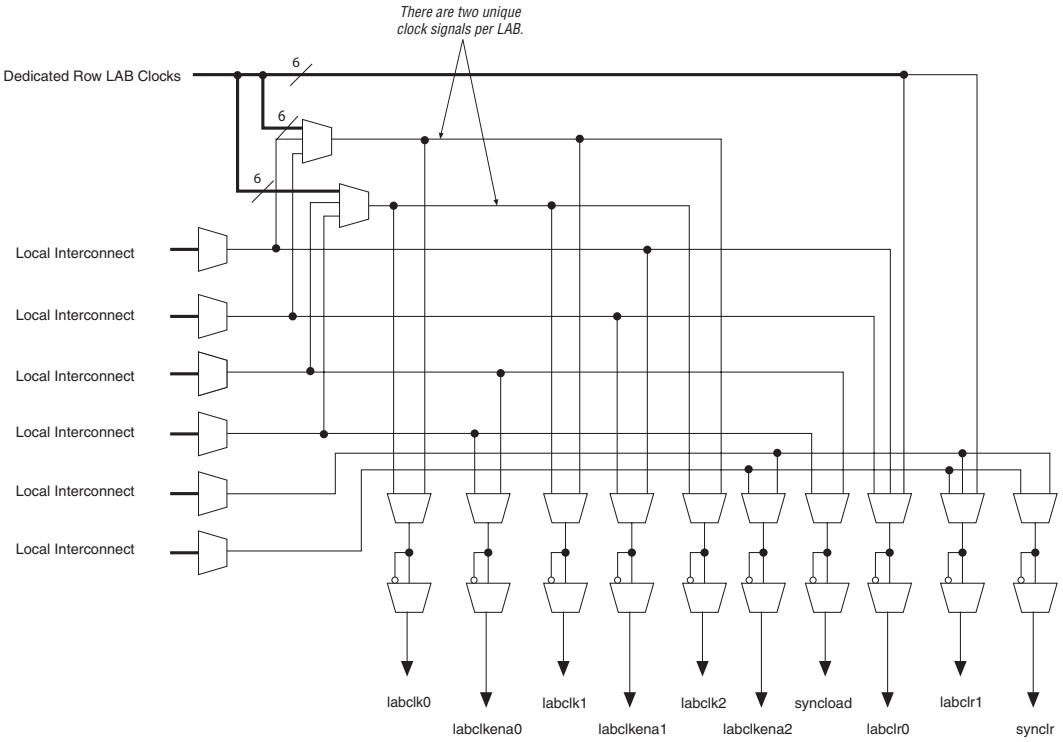
LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, a synchronous clear, and synchronous load control signals. This gives a maximum of 10 a control signals at a time. Although you generally use synchronous load and clear signals when implementing counters, you can also use them with other functions.

Each LAB has two unique clock sources and three clock enable signals, as shown in Figure 2–4. The LAB control block can generate up to three clocks using the two clock sources and three clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `labclk1` signal also uses `labclkena1` signal. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock.

The LAB row clocks [5..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

Figure 2–4. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Stratix III architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs) and two registers. With up to eight inputs to the two combinational ALUTs, one ALM can implement various combinations of two functions. This adaptability allows an ALM to be completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, an ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2–5 shows a high-level block diagram of the Stratix III ALM while Figure 2–6 shows a detailed view of all the connections in an ALM.

Figure 2–5. High-Level Block Diagram of the Stratix III ALM

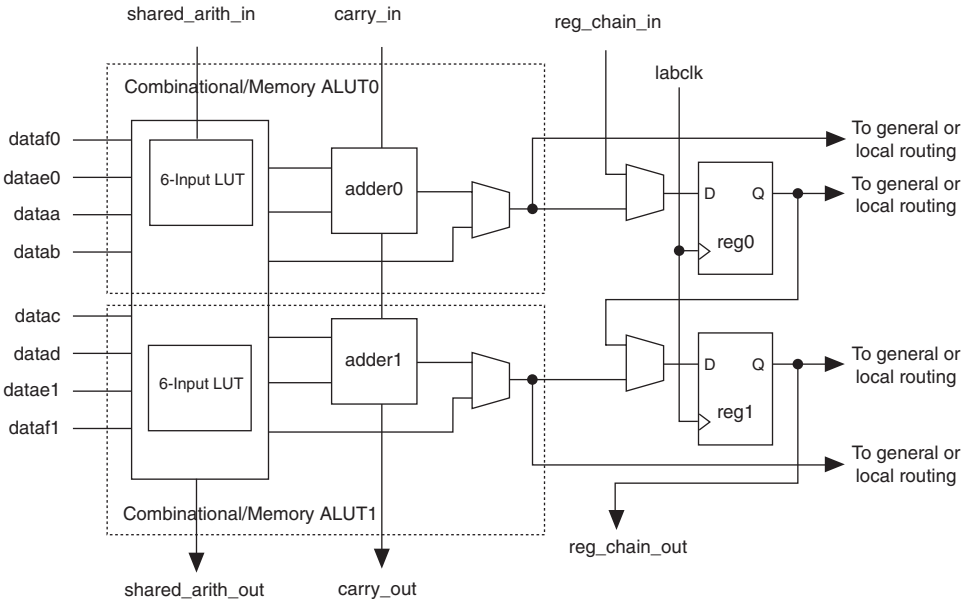
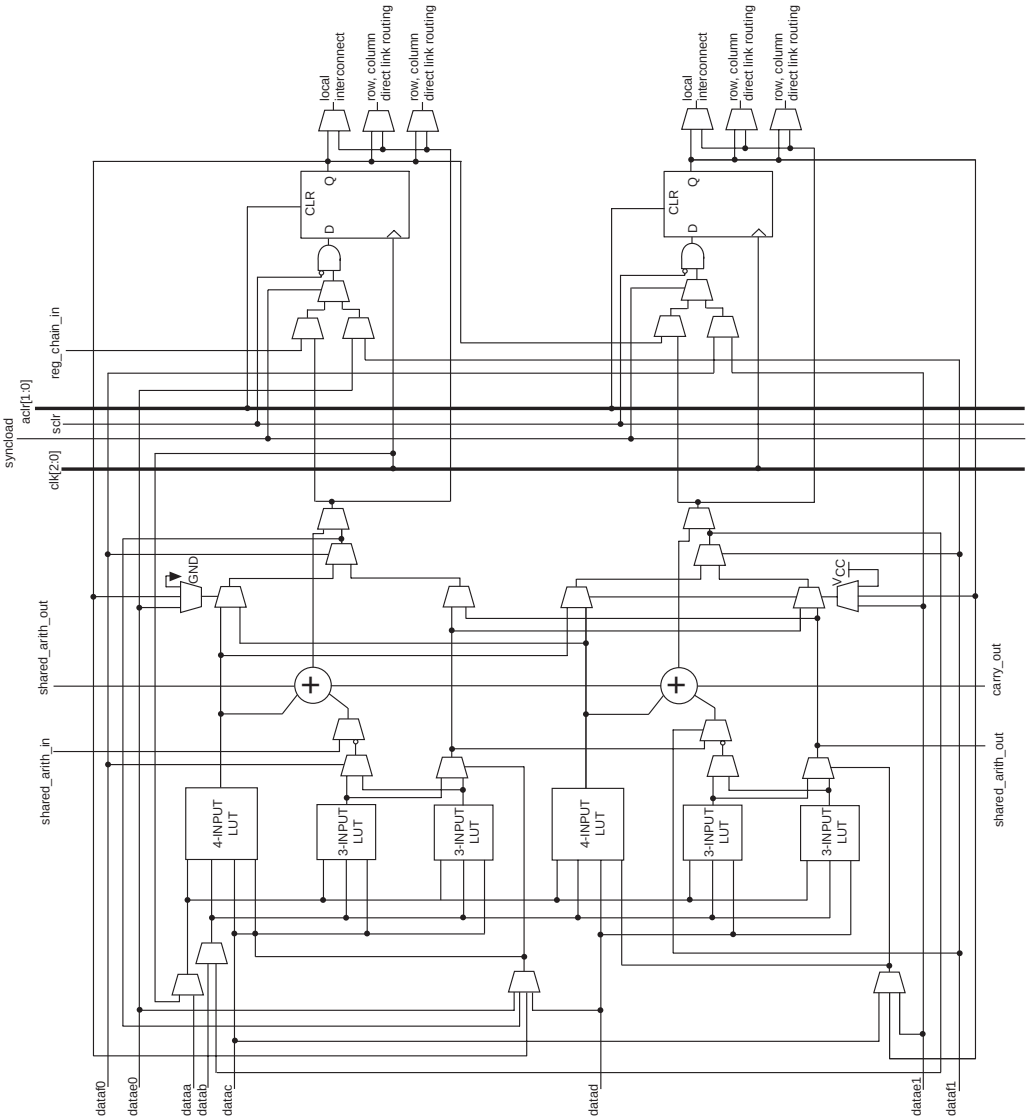


Figure 2–6. Stratix III ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, and synchronous load / clear inputs. Global signals, general-purpose I / O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I / O pins or internal logic can drive the clock enable. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of an ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers (refer to Figure 2–6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output.

This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.

ALM Operating Modes

The Stratix III ALM can operate in one of the following modes:

- Normal
- Extended LUT Mode
- Arithmetic
- Shared Arithmetic
- LUT-Register

Each mode uses ALM resources differently. In each mode, eleven available inputs to an ALM—the eight data inputs from the LAB local interconnect, carry-in from the previous ALM or LAB, the shared arithmetic chain connection from the previous ALM or LAB, and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes.

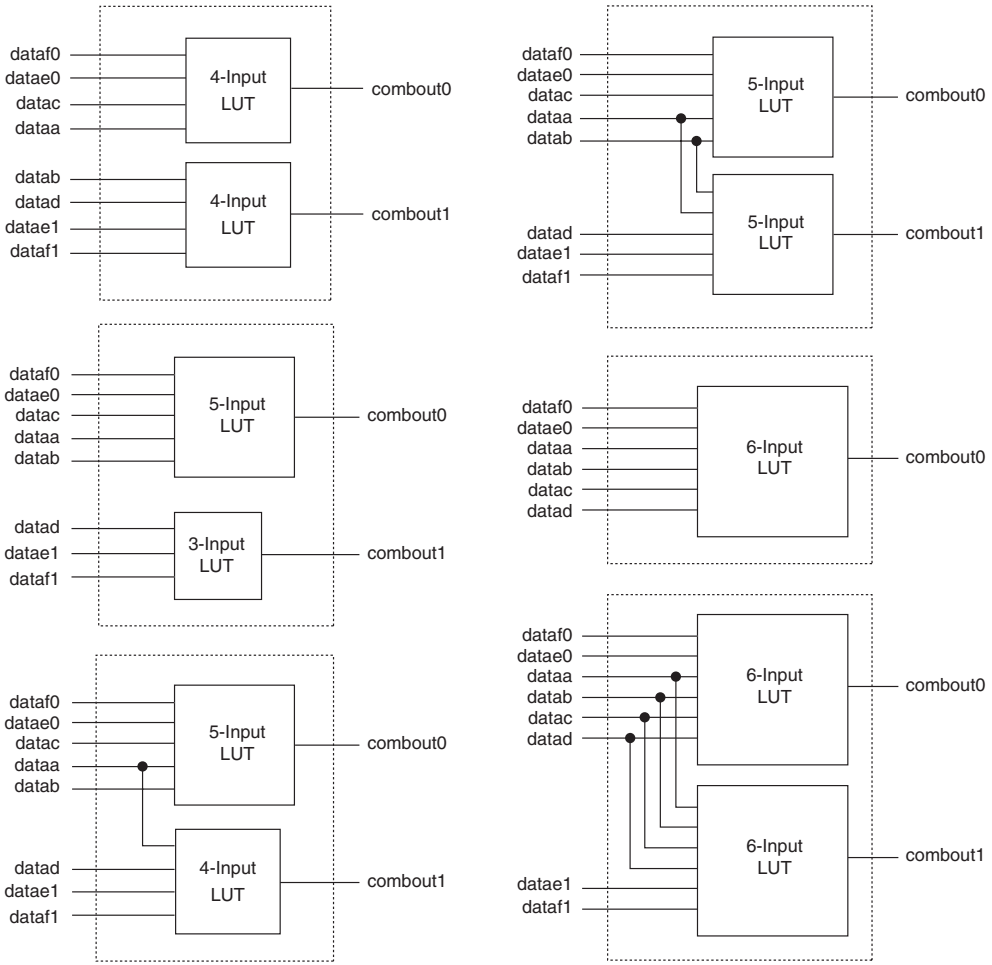
Refer to "LAB Control Signals" on page 2–4 for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as the library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix III ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions that have common inputs. Figure 2–7 shows the supported LUT combinations in normal mode.

Figure 2–7. ALM in Normal Mode *Note (1)*



Note to Figure 2–7:

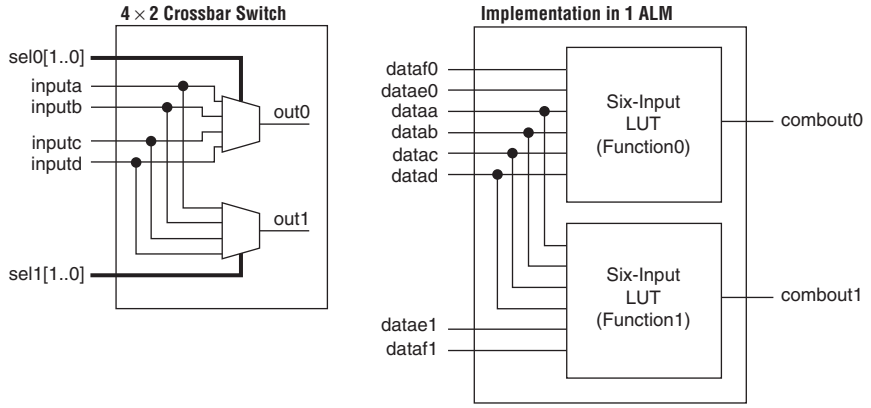
(1) Combinations of functions with fewer inputs than those shown are also supported. For example, combinations of functions with the following number of inputs are supported: 4 and 3, 3 and 3, 3 and 2, 5 and 2.

The normal mode provides complete backward compatibility with four-input LUT architectures.

For the packing of 2 five-input functions into one ALM, the functions must have at least two common inputs. The common inputs are `dataa` and `datab`. The combination of a four-input function with a five-input function requires one common input (either `dataa` or `datab`).

In the case of implementing 2 six-input functions in one ALM, four inputs must be shared and the combinational function must be the same. For example, a 4 × 2 crossbar switch (two 4-to-1 multiplexers with common inputs and unique select lines) can be implemented in one ALM, as shown in Figure 2–8. The shared inputs are dataa, datab, datac, and datad, while the unique select lines are datae0 and dataf0 for function0, and datae1 and dataf1 for function1. This crossbar switch consumes four LUTs in a four-input LUT-based architecture.

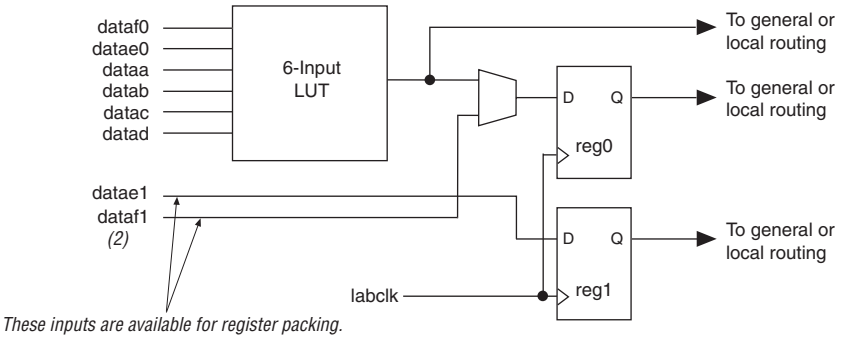
Figure 2–8. 4 × 2 Crossbar Switch Example



In a sparsely used device, functions that could be placed into one ALM may be implemented in separate ALMs by the Quartus II software in order to achieve the best possible performance. As a device begins to fill up, the Quartus II software automatically utilizes the full potential of the Stratix III ALM. The Quartus II Compiler automatically searches for functions of common inputs or completely independent functions to be placed into one ALM and to make efficient use of the device resources. In addition, you can manually control resource usage by setting location assignments.

Any six-input function can be implemented utilizing inputs dataa, datab, datac, datad, and either datae0 and dataf0 or datae1 and dataf1. If datae0 and dataf0 are utilized, the output is driven to register0, and/or register0 is bypassed and the data drives out to the interconnect using the top set of output drivers (refer to Figure 2–9). If datae1 and dataf1 are utilized, the output drives to register1 and/or bypasses register1 and drives to the interconnect using the bottom set of output drivers. The Quartus II Compiler automatically selects the inputs to the LUT. ALMs in normal mode support register packing.

Figure 2–9. Input Function in Normal Mode Note (1)



Notes to Figure 2–9:

(1) If `datae1` and `dataf1` are used as inputs to the six-input function, then `datae0` and `dataf0` are available for register packing.

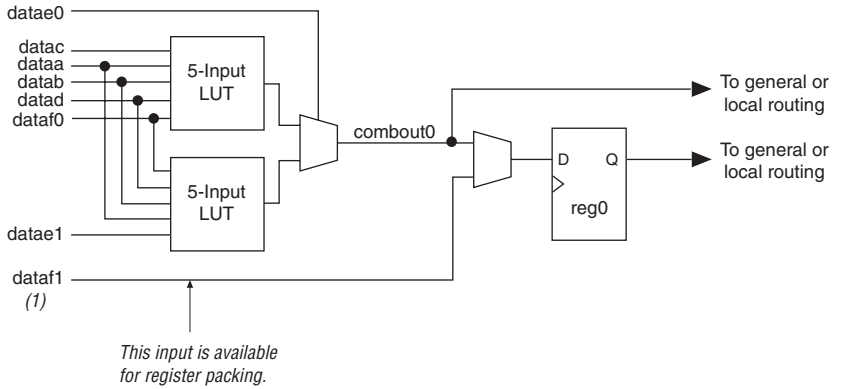
(2) The `dataf1` input is available for register packing only if the six-input function is un-registered.

Extended LUT Mode

Use the extended LUT mode to implement a specific set of seven-input functions. The set must be a 2-to-1 multiplexer fed by two arbitrary five-input functions sharing four inputs. Figure 2–10 shows the template of supported seven-input functions utilizing extended LUT mode. In this mode, if the seven-input function is unregistered, the unused eighth input is available for register packing.

Functions that fit into the template shown in Figure 2–10 occur naturally in designs. These functions often appear in designs as "if-else" statements in Verilog HDL or VHDL code.

Figure 2–10. Template for Supported Seven-Input Functions in Extended LUT Mode



Note to Figure 2–10:

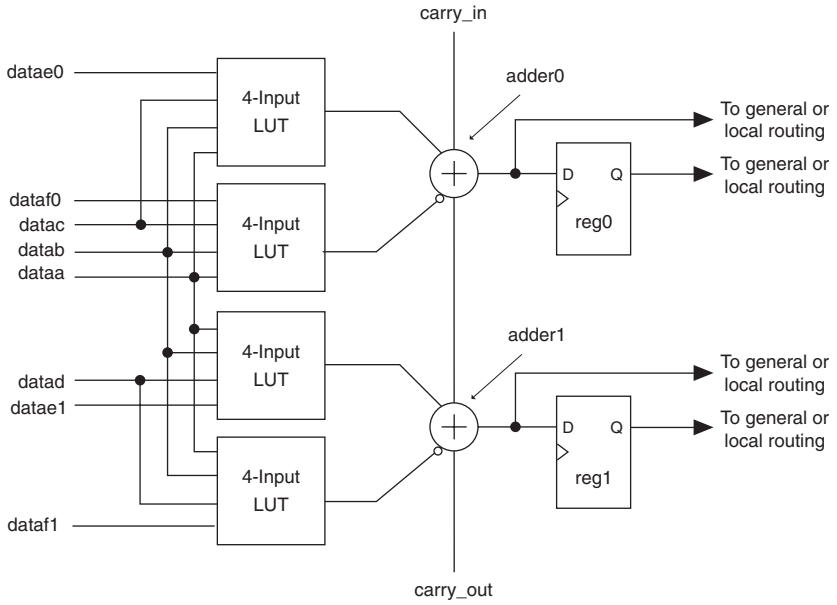
(1) If the seven-input function is unregistered, the unused eighth input is available for register packing. The second register, `reg1`, is not available.

Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. The ALM in arithmetic mode uses two sets of 2 four-input LUTs along with two dedicated full adders. The dedicated adders allow the LUTs to be available to perform pre-adder logic; therefore, each adder can add the output of 2 four-input functions.

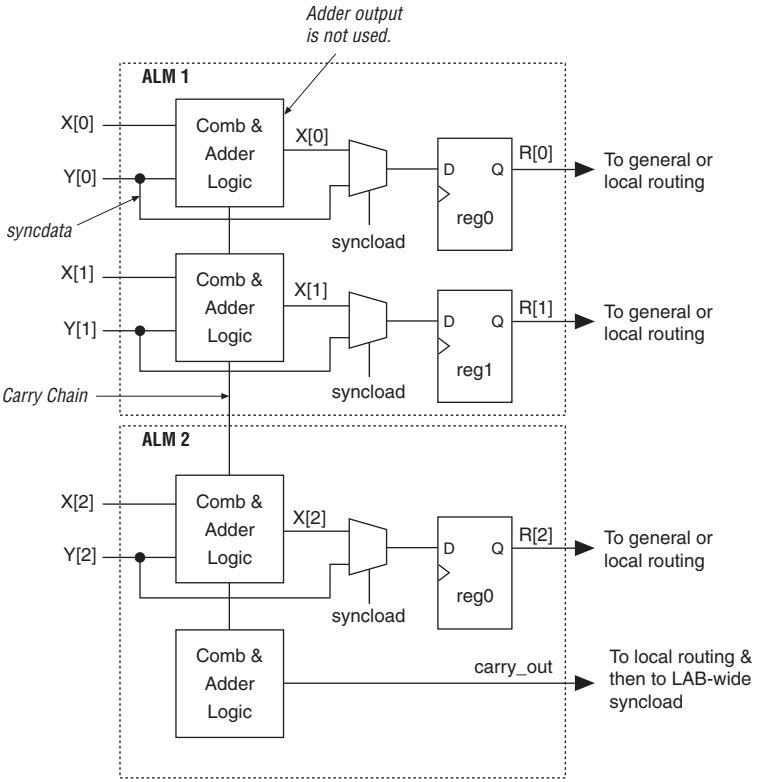
The four LUTs share the `dataa` and `datab` inputs. As shown in Figure 2–11, the carry-in signal feeds to `adder0`, and the carry-out from `adder0` feeds to carry-in of `adder1`. The carry-out from `adder1` drives to `adder0` of the next ALM in the LAB. ALMs in arithmetic mode can drive out registered and / or unregistered versions of the adder outputs.

Figure 2–11. ALM in Arithmetic Mode



While operating in arithmetic mode, the ALM can support simultaneous use of the adder's carry output along with combinational logic outputs. In this operation, the adder output is ignored. This usage of the adder with the combinational logic output provides resource savings of up to 50% for functions that can use this ability. An example of such functionality is a conditional operation, such as the one shown in Figure 2–12.

Figure 2–12. Conditional Operation Example



The equation for this example is:

$R = (X < Y)\ ?\ Y : X$

To implement this function, the adder is used to subtract *Y* from *X*. If *X* is less than *Y*, the `carry_out` signal is 1. The `carry_out` signal is fed to an adder where it drives out to the LAB local interconnect. It then feeds to the LAB-wide `syncload` signal. When asserted, `syncload` selects the `syncdata` input. In this case, the data *Y* drives the syncdata inputs to the registers. If *X* is greater than or equal to *Y*, the `syncload` signal is de-asserted and *X* drives the data port of the registers.

The arithmetic mode also offers clock enable, counter enable, synchronous up / down control, add / subtract control, synchronous clear, and synchronous load. The LAB local interconnect data inputs generate the clock enable, counter enable, synchronous up / down, and

add / subtract control signals. These control signals are good candidates for the inputs that are shared between the four LUTs in the ALM. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. These signals can also be individually disabled or enabled per register. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

Carry Chain

The carry chain provides a fast carry function between the dedicated adders in arithmetic or shared arithmetic mode. The two-bit carry select feature in Stratix III devices halves the propagation delay of carry chains within the ALM. Carry chains can begin in either the first ALM or the fifth ALM in an LAB. The final carry-out signal is routed to a ALM, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 20 (10 ALMs in arithmetic or shared arithmetic mode) by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix™ memory and DSP blocks. A carry chain can continue as far as a full column.

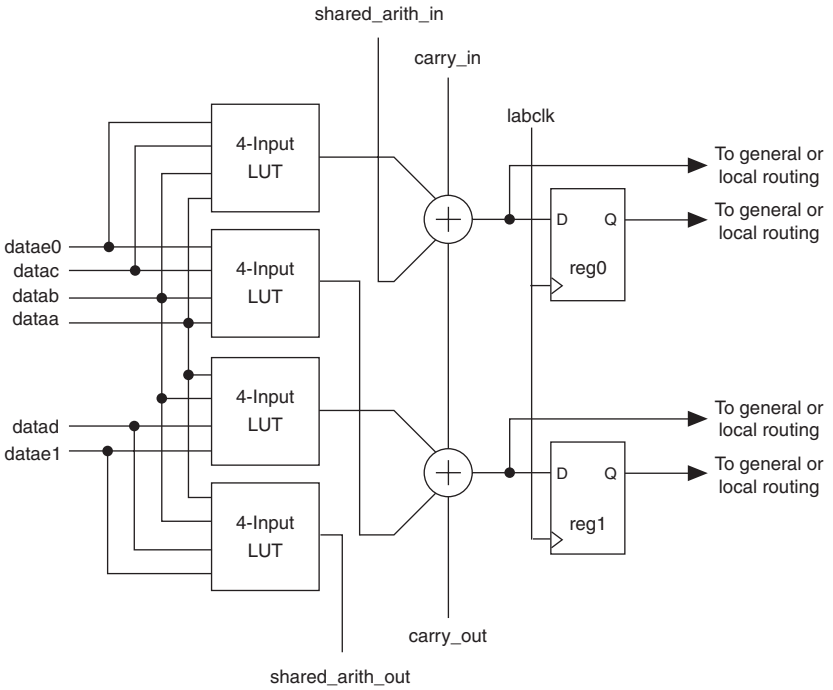
To avoid routing congestion in one small area of the device when a high fan-in arithmetic function is implemented, the LAB can support carry chains that only utilize either the top half or the bottom half of the LAB before connecting to the next LAB. This leaves the other half of the ALMs in the LAB available for implementing narrower fan-in functions in normal mode. Carry chains that use the top five ALMs in the first LAB carry into the top half of the ALMs in the next LAB within the column. Carry chains that use the bottom five ALMs in the first LAB carry into the bottom half of the ALMs in the next LAB within the column. In every alternate LAB column, the top half can be bypassed; in the other MLAB columns, the bottom half can be bypassed.

Refer to "ALM Interconnects" on page 2–22 for more information on carry chain interconnect.

Shared Arithmetic Mode

In shared arithmetic mode, the ALM can implement a three-input add within an ALM. In this mode, the ALM is configured with 4 four-input LUTs. Each LUT either computes the sum of three inputs or the carry of three inputs. The output of the carry computation is fed to the next adder (either to `adder1` in the same ALM or to `adder0` of the next ALM in the LAB) via a dedicated connection called the shared arithmetic chain. This shared arithmetic chain can significantly improve the performance of an adder tree by reducing the number of summation stages required to implement an adder tree. Figure 2–13 shows the ALM using this feature.

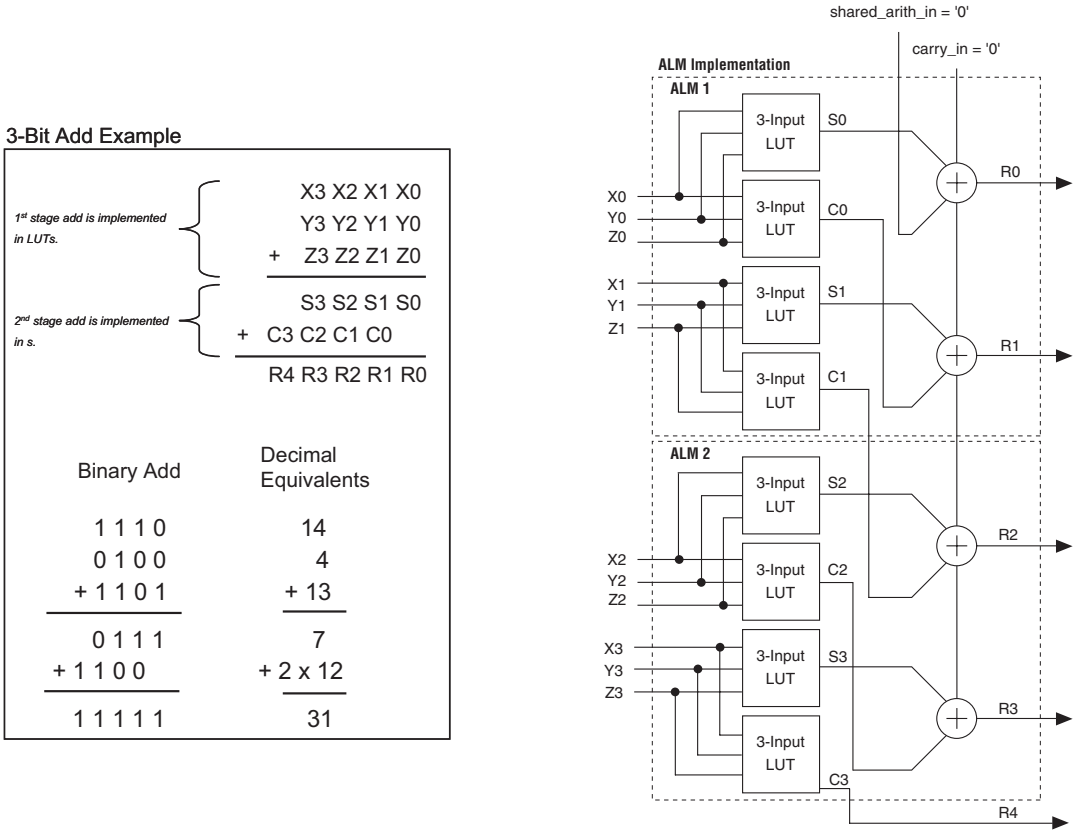
Figure 2–13. ALM in Shared Arithmetic Mode



You can find adder trees in many different applications. For example, the summation of the partial products in a logic-based multiplier can be implemented in a tree structure. Another example is a correlator function that can use a large adder tree to sum filtered data samples in a given time frame to recover or to de-spread data that was transmitted utilizing spread spectrum technology.

An example of a three-bit add operation utilizing the shared arithmetic mode is shown in Figure 2–14. The partial sum (S[3..0]) and the partial carry (C[3..0]) is obtained using the LUTs, while the result (R[3..0]) is computed using the dedicated adders.

Figure 2–14. Example of a 3-Bit Add Utilizing Shared Arithmetic Mode



Shared Arithmetic Chain

The shared arithmetic chain available in enhanced arithmetic mode allows the ALM to implement a three-input add. This significantly reduces the resources necessary to implement large adder trees or correlator functions.

The shared arithmetic chains can begin in either the first or sixth ALM in an LAB. The Quartus II Compiler creates shared arithmetic chains longer than 20 (10 ALMs in arithmetic or shared arithmetic mode) by linking

LABs together automatically. For enhanced fitting, a long shared arithmetic chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A shared arithmetic chain can continue as far as a full column.

Similar to the carry chains, the top and bottom half of shared arithmetic chains in alternate LAB columns can be bypassed. This capability allows the shared arithmetic chain to cascade through half of the ALMs in a LAB while leaving the other half available for narrower fan-in functionality. Every other LAB column is top-half bypassable, while the other LAB columns are bottom-half bypassable.

Refer to "ALM Interconnects" on page 2–22 for more information on shared arithmetic chain interconnect.

LUT-Register Mode

LUT-Register mode allows third register capability within an ALM. Two internal feedback loops allow combinational `ALUT1` to implement the master latch and combinational `ALUT0` to implement the slave latch needed for the third register. The LUT register shares its clock, clock enable, and asynchronous clear sources with the top dedicated register. Figure 2–15 shows the register constructed using two combinational blocks within the ALM. Figure 2–16 shows the ALM in LUT-Register mode.

Figure 2–15. LUT Register from Two Combinational Blocks

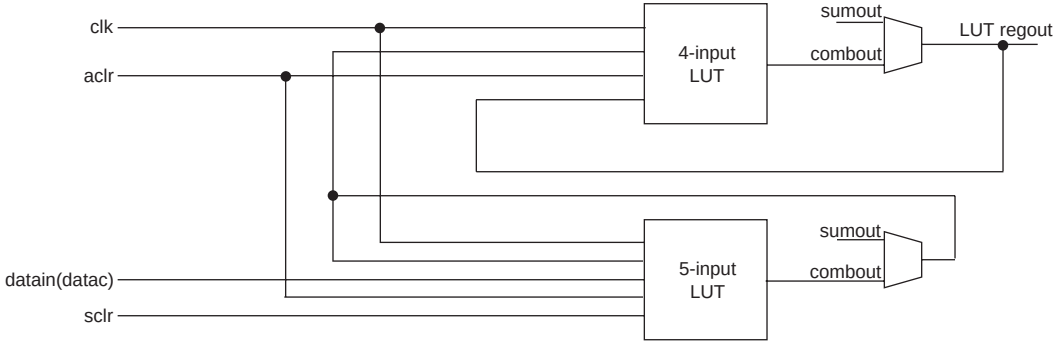
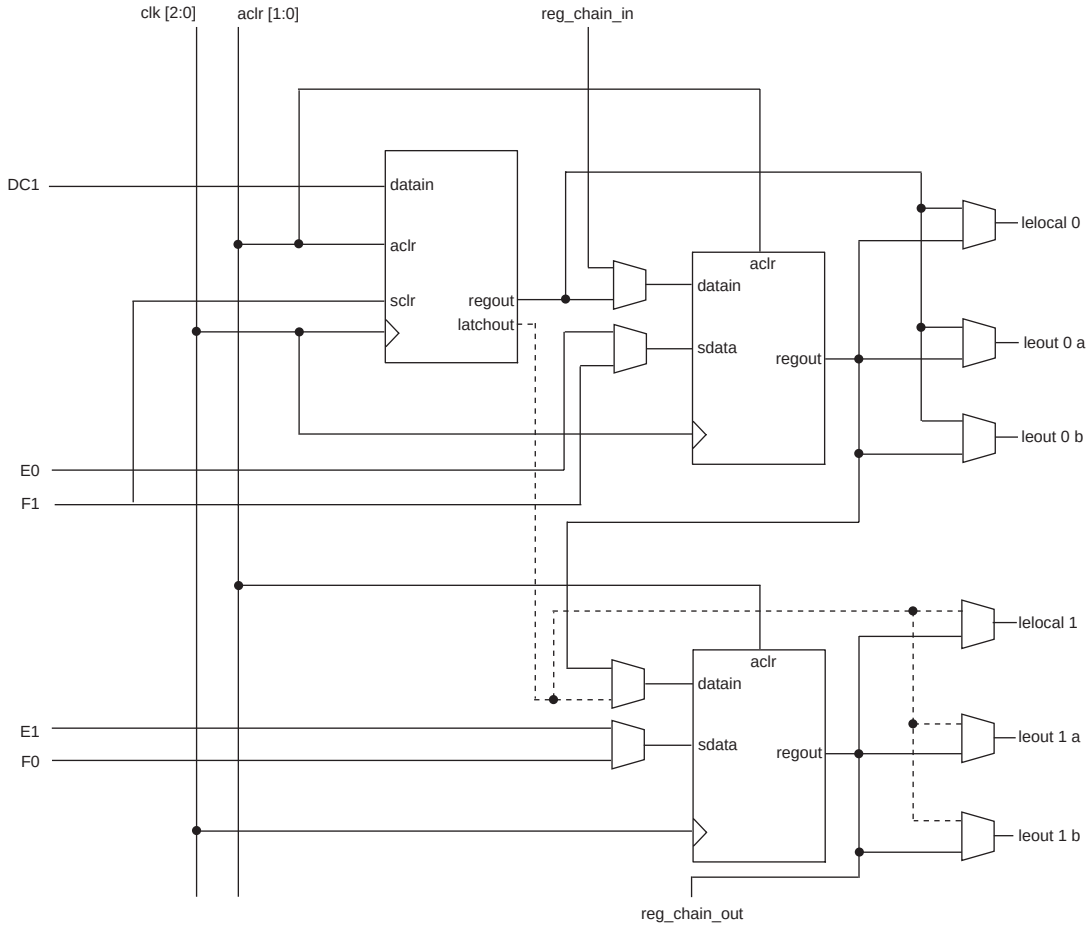


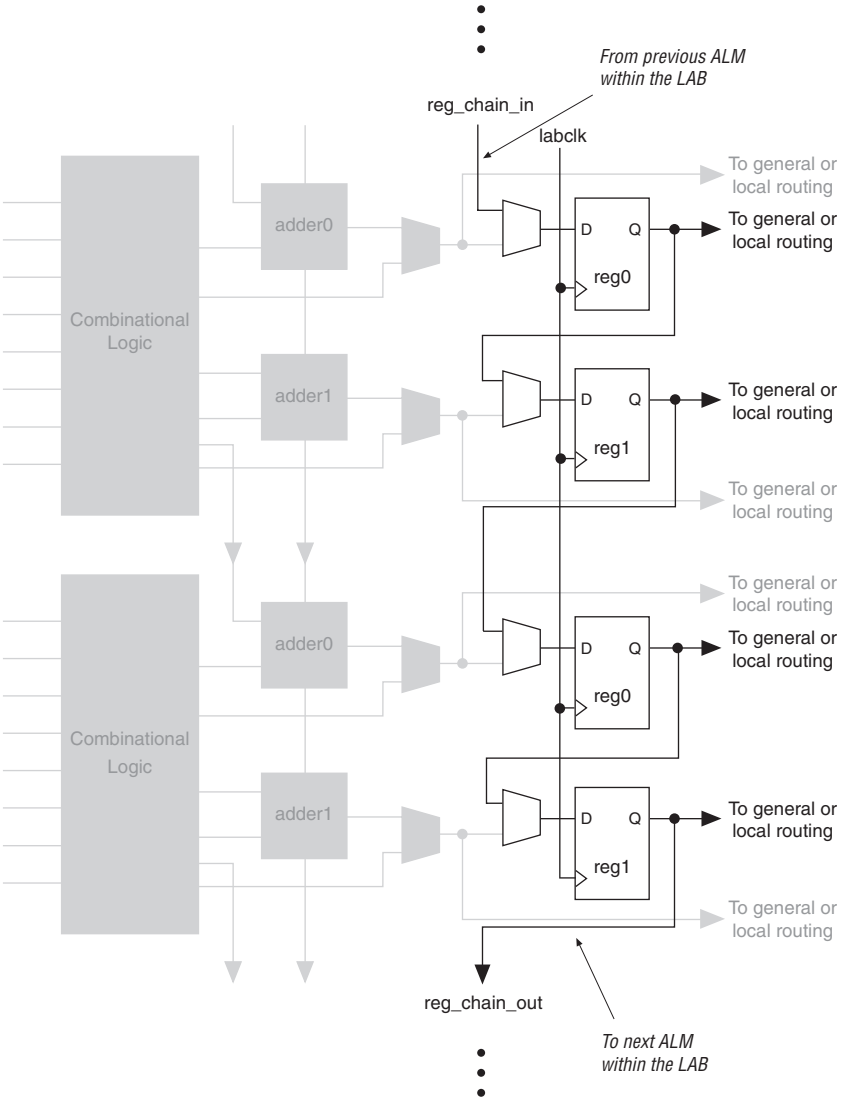
Figure 2–16. ALM in LUT-Register Mode with 3-Register Capability



Register Chain

In addition to the general routing outputs, the ALMs in an LAB have register chain outputs. The register chain routing allows registers in the same LAB to be cascaded together. The register chain interconnect allows a LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between ALMs while saving local interconnect resources (refer to Figure 2–17). The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance.

Figure 2–17. Register Chain within an LAB *Note (1)*



Note to Figure 2–17:

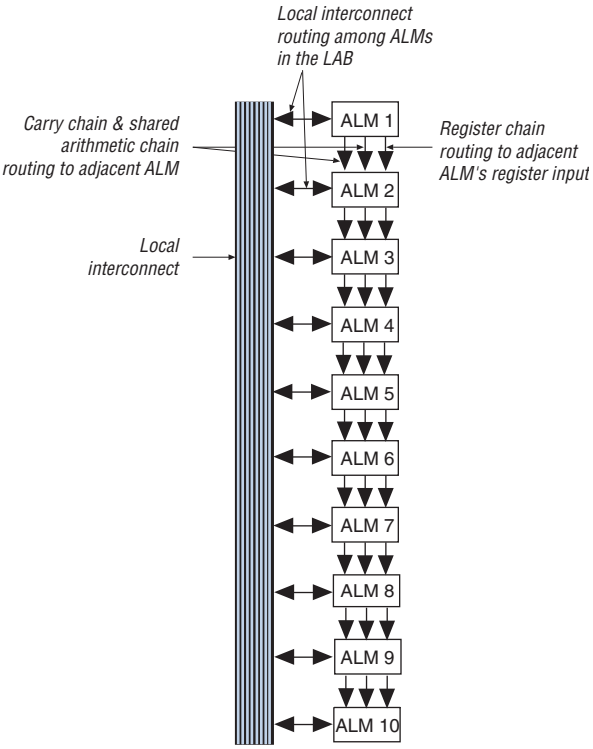
(1) You can use the combinational or adder logic to implement an unrelated, un-registered function.

Refer to "ALM Interconnects" on page 2–22 for more information on register chain interconnect.

ALM Interconnects

There are three dedicated paths between ALMs: Register Cascade, Carry-chain, and Shared Arithmetic chain. Stratix III devices include an enhanced interconnect structure in LABs for routing shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–18 shows the shared arithmetic chain, carry chain, and register chain interconnects.

Figure 2–18. Shared Arithmetic Chain, Carry Chain, and Register Chain Interconnects



Refer to the *MultiTrack Interconnect in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for information on routing between LABs.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear signal. The ALM directly supports an asynchronous clear function. You can achieve the register preset through the Quartus II software's **NOT-gate push-back logic** option. Each LAB supports up to two clears.

Stratix III devices provide a device-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This device-wide reset overrides all other control signals.

LAB Power Management Techniques

The following techniques are used to manage static and dynamic power consumption within the LAB:

- Stratix III low-voltage devices (L ordering code suffix) offer selectable core voltage to reduce both DC and AC power.
- To save AC power, Quartus II forces all adder inputs low when ALM adders are not in use.
- Stratix III LABs operate in high-performance mode or low-power mode. The Quartus II software automatically chooses the appropriate mode for an LAB based on the design to optimize speed vs. leakage trade-offs.
- Clocks represent a significant portion of dynamic power consumption due to their high switching activity and long paths. The LAB clock that distributes a clock signal to registers within a LAB is a significant contributor to overall clock power consumption. Each LAB's clock and clock enable signal are linked. For example, a combinational ALUT or register in a particular LAB using the `labclk1` signal also uses the `labclkena1` signal. To disable LAB-wide clock power consumption without disabling the entire clock tree, use the LAB-wide clock enable to gate the LAB-wide clock. The Quartus II software automatically promotes register-level clock enable signals to the LAB-level. All registers within an LAB that share a common clock and clock enable are controlled by a shared gated clock. To take advantage of these clock enables, use a clock enable construct in your HDL code for the registered logic.

Refer to the *Power Optimization* section of the *Quartus II Handbook* for details on implementation.

Refer to the *Programmable Power and Temperature Sensing Diode in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for detailed information on Stratix III programmable power capabilities.

Conclusion

Logic array block and adaptive logic modules are the basic building blocks of the Stratix III device. You can use these to configure logic functions, arithmetic functions, and register functions. The ALM provides advanced features with efficient logic utilization and is completely backward-compatible.

Document Revision History

Table 2–1 shows the revision history for this document.

Table 2–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Minor formatting changes, updated Figure 2–6 to include a missing connection.	—
November 2006 v1.0	Initial Release	—

3. MultiTrack Interconnect in Stratix III Devices

SIII51003-1.0

Introduction

Stratix® III devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures, digital signal processing (DSP) blocks, and input/output elements (IOE). These blocks communicate with themselves and to one another through a fabric of routing wires. This chapter provides details on the Stratix III core routing structure. It also describes how Stratix III block types interface to this fabric.

In the Stratix III architecture, connections between adaptive logic modules (ALMs), TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus® II Compiler automatically routes critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

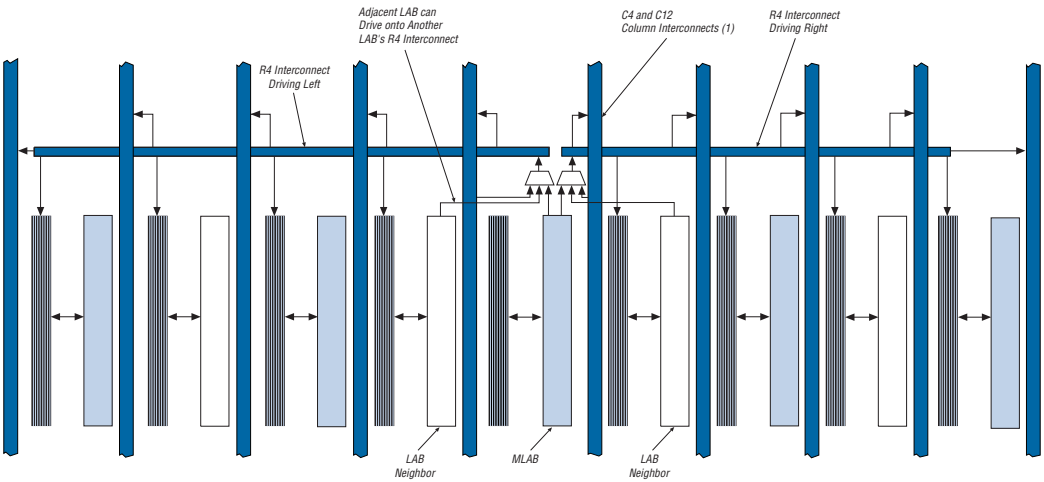
Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory blocks in the same row. These row interconnect resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R20 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors. This capability provides fast communication between adjacent LABs and blocks without using row interconnect resources. The direct link interconnect is the fastest way to communicate between two adjacent blocks.

The R4 interconnects span a combination of four LABs, memory logic array blocks (MLAB), DSP blocks, M9K blocks, and M144K blocks. Use these resources for fast row connections in a four-LAB region. Figure 3–1 shows R4 interconnect connections from a LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they drive. R4 interconnects can also drive C4 and C12 (column interconnects) for connections from one row to another. Additionally, R4 interconnects can drive R20 interconnects.

Figure 3–1. R4 Interconnect Connections *Notes (1), (2)*



Notes to Figure 3–1

(1) C4 and C12 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

R20 row interconnects span 20 LABs and provide the fastest resource for row connections between distant LABs, TriMatrix memory, DSP blocks, and row IOEs. R20 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R20 interconnects can drive R20, R4, C12, and C4 interconnects.

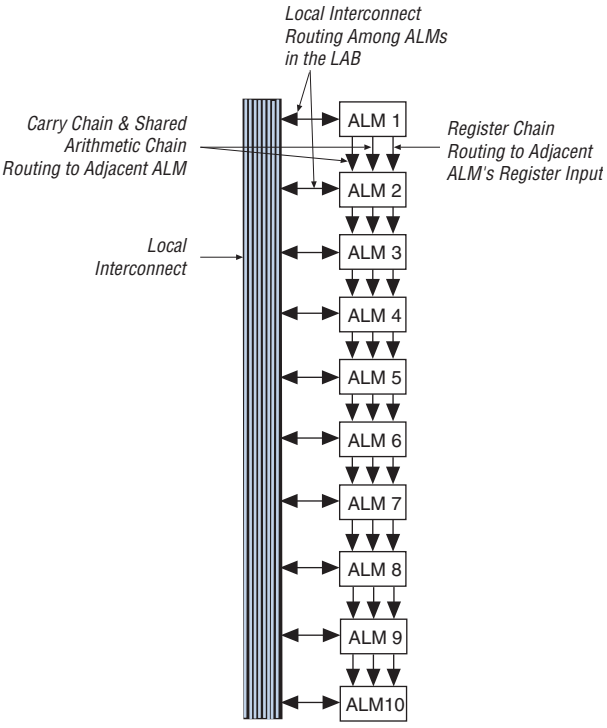
Column Interconnects

The column interconnect operates similarly to the row interconnect. It vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column interconnect resources include:

- Shared arithmetic chain interconnects in a LAB and from LAB to LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in the same device column
- C12 column interconnects for high-speed vertical routing through the device

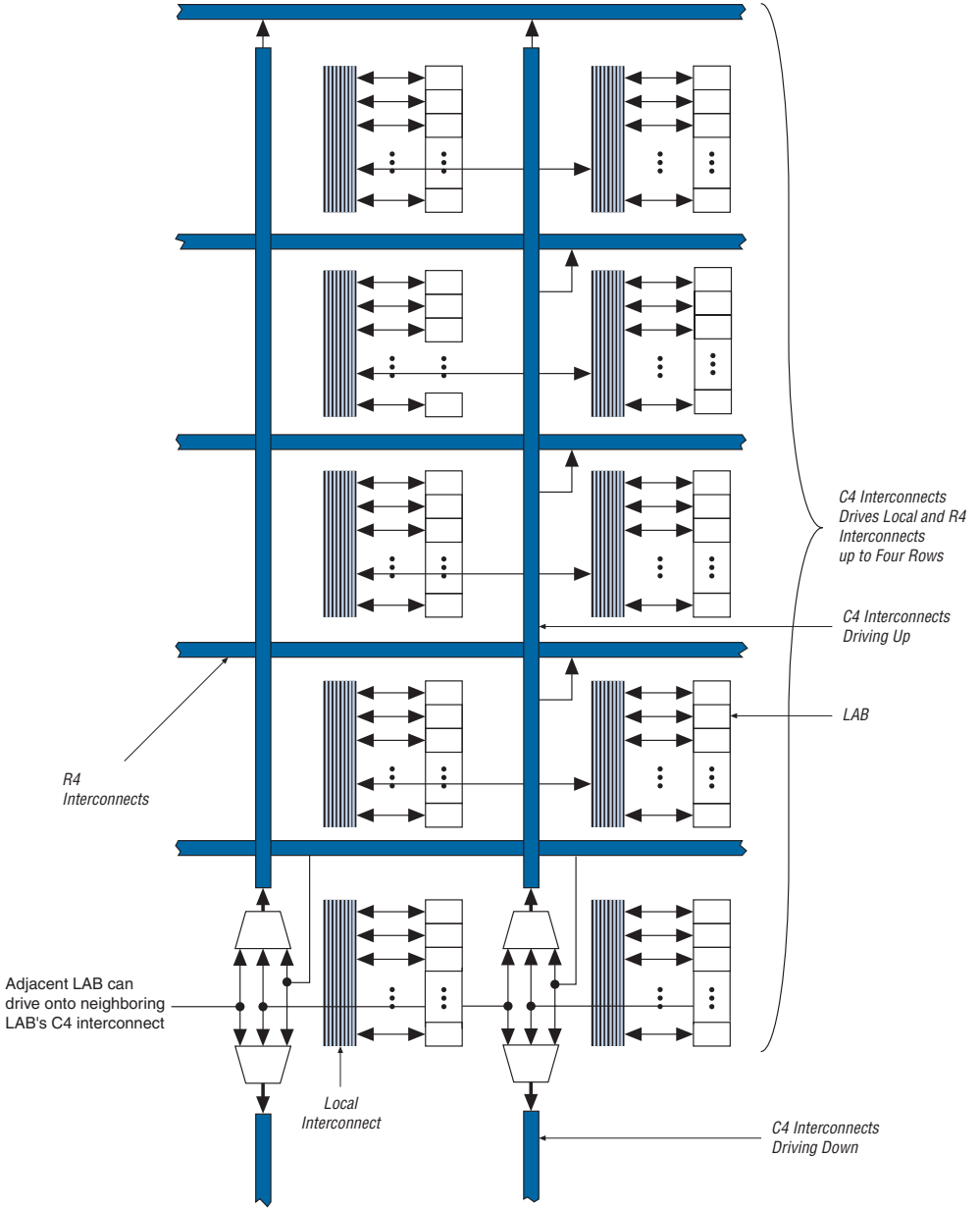
Stratix III devices include an enhanced interconnect structure in LABs for routing-shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 3–2 shows the shared arithmetic chain, carry chain, and register chain interconnects.

Figure 3–2. Shared Arithmetic Chain, Carry Chain, & Register Chain Interconnects



The C4 interconnects span four adjacent interfaces in the same device column. C4 interconnects also pass by M144K and DSP blocks. A single M144K block utilizes eight adjacent interfaces in the same column. A DSP block utilizes four adjacent interfaces in the same column. Figure 3–3 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 3–3. C4 Interconnect Connections *Note (1)*



Note to Figure 3–3:

(1) Each C4 interconnect can drive either up or down four rows.

C12 column interconnects span a length of 12 LABs and provide the fastest resource for column connections between distant LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C12 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array through interconnects similar to LAB-to-LAB interfaces. Each block (for example, TriMatrix memory blocks and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 3–1 shows the Stratix III device's routing scheme.

Table 3–1. Stratix III Device Routing Scheme (Part 1 of 2)

Source	Destination															
	Shared Arith-metic Chain	Carry Chain	Regis-ter Chain	Local Inter-connect	Direct Link Inter-connect	R4 Inter-connect	R20 Inter-connect	C4 Inter-connect	C12 Inter-connect	ALM	MLAB RAM Block	M9K RAM Block	M144K Block	DSP Blocks	Col-umn IOE	Row IOE
Shared arithmetic chain										✓						
Carry chain										✓						
Register chain										✓						
Local interconnect										✓	✓	✓	✓	✓	✓	✓
Direct link interconnect				✓												
R4 interconnect				✓ *(1)*		✓	✓	✓	✓							
R20 interconnect				✓ *(2)*		✓	✓	✓	✓							
C4 interconnect				✓		✓		✓								
C12 interconnect				✓ *(3)*		✓	✓	✓	✓							
ALM	✓	✓	✓	✓	✓	✓		✓								
MLAB RAM block				✓	✓	✓		✓								
M9K RAM block					✓	✓		✓								
M144K block					✓	✓		✓								

Table 3–1. Stratix III Device Routing Scheme (Part 2 of 2)

Source	Destination															
	Shared Arith-metic Chain	Carry Chain	Regis-ter Chain	Local Inter-connect	Direct Link Inter-connect	R4 Inter-connect	R20 Inter-connect	C4 Inter-connect	C12 Inter-connect	ALM	MLAB RAM Block	M9K RAM Block	M144K Block	DSP Blocks	Col-umn IOE	Row IOE
DSP blocks					✓	✓		✓								
Column IOE								✓	✓							
Row IOE					✓	✓	✓	✓								

Notes to Table 3–1:

(1) Except column IOE local interconnects.
(2) Row IOE local interconnects.
(3) Column IOE local interconnects.

The R4 and C4 interconnects provide superior and flexible routing capabilities. Stratix III has a three-sided routing architecture which allows the interconnect wires from each LAB to reach the adjacent LABs to its right and left. A given LAB can drive 32 other LABs using one R4 or C4 interconnect, in one hop. This routing scheme improves efficiency and flexibility by placing all the critical LABs within one hop of the routing interconnects.

Table 3–2 shows how many LABs are reachable within one, two, or three hops using the R4 and C4 interconnects.

Table 3–2. Number of LABs reachable using C4 and R4 interconnects

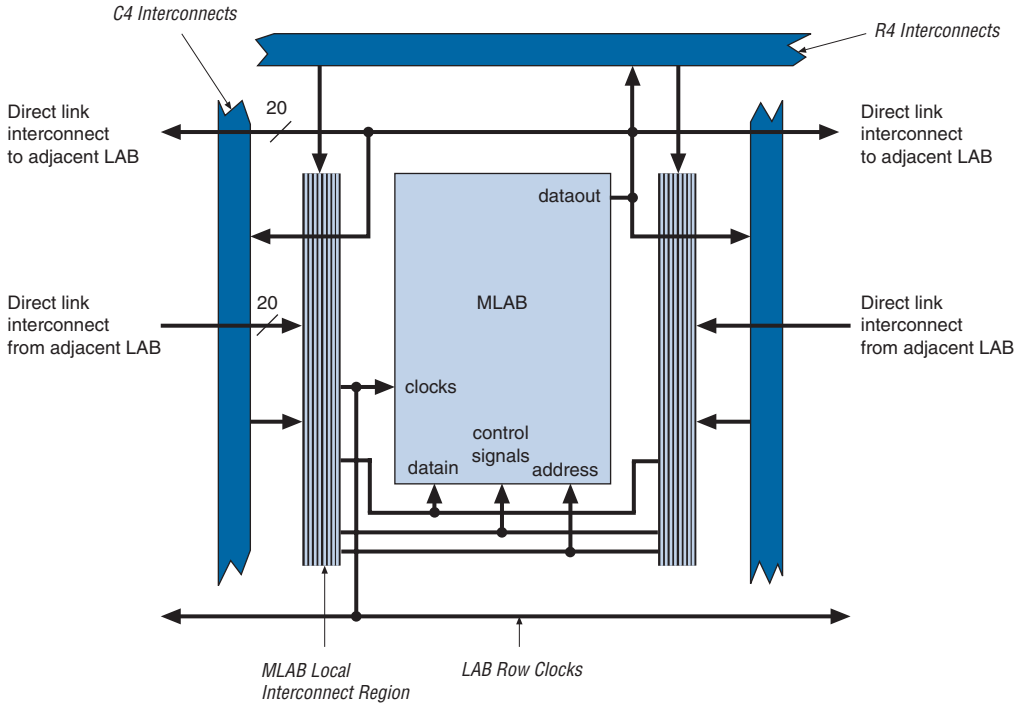
Hops	Number of LABs
1	34
2	96
3	160

Memory Block Interface

TriMatrix memory consists of three types of RAM blocks: MLAB, M9K, and M144K. This section provides a brief overview of how the different memory blocks interface to the routing structure.

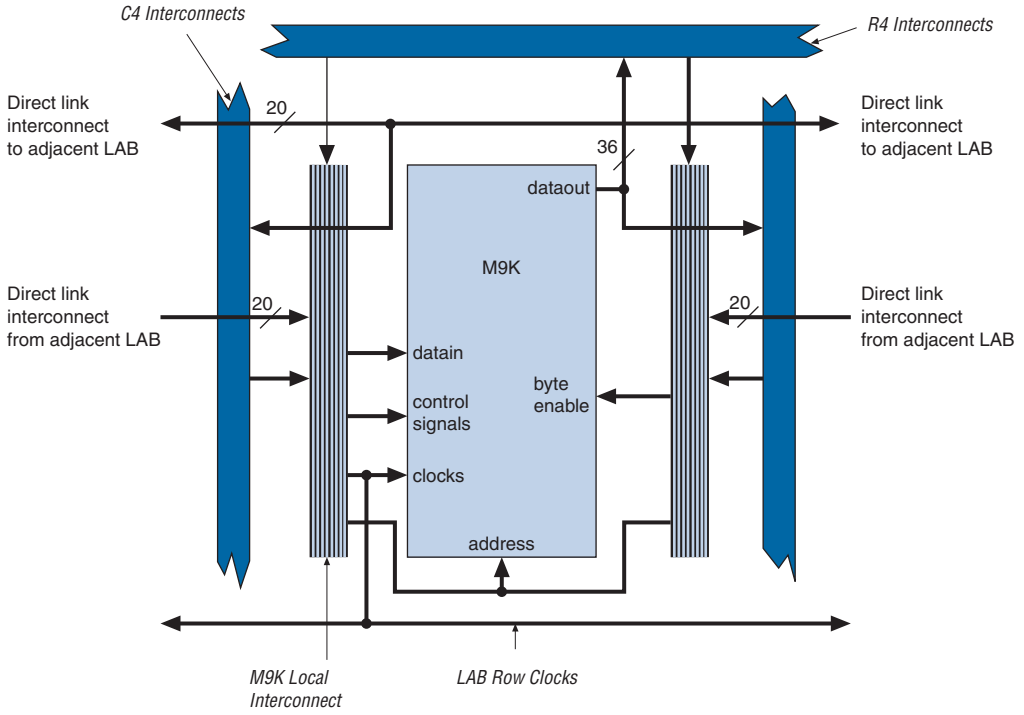
The RAM blocks in Stratix III devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The MLAB RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The MLAB RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Each MLAB RAM block has up to 20 direct link input connections from the left adjacent LAB and another 20 from the right adjacent LAB. MLAB RAM outputs can also connect to left and right LABs through a direct link interconnect. The MLAB RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 3–4 shows the MLAB RAM block to LAB row interface.

Figure 3–4. MLAB RAM Block LAB Row Interface



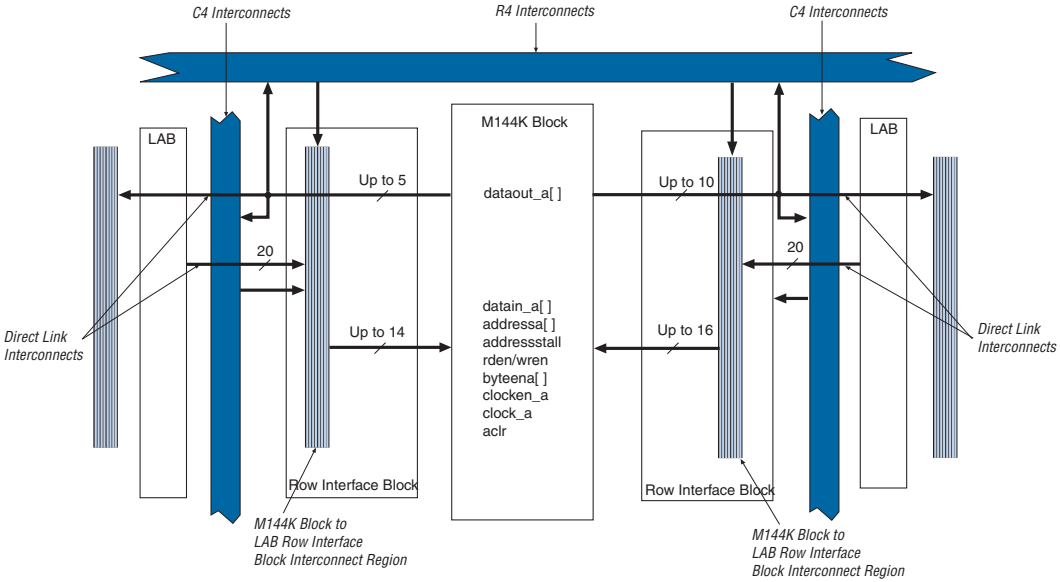
The M9K RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M9K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 20 direct link input connections to the M9K RAM Block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M9K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 3–5 shows the M9K RAM block to logic array interface.

Figure 3–5. M9K RAM Block LAB Row Interface



The M144K blocks use eight interfaces in the same device column. The M144K block local interconnects are driven by R4, C4, and direct link interconnects from adjacent LABs on either the right or left side of the MRAM block. Up to 20 direct link input connections to the M144K block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M144K block outputs can also connect to the LABs on the block's left and right sides through direct link interconnect. Figure 3–6 shows the interface between the M144K RAM block and the logic array.

Figure 3–6. M144K Row Unit Interface to Interconnect



DSP Block Interface

Stratix III device DSP block input registers can generate a shift register that cascades down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9-bit or 18-bit finite impulse response (FIR) filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36-bit blocks, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. You can consider each block unit as two 18-bit multipliers followed by an adder with 72 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like a LAB, this interconnect region can be fed with 20 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region.

These outputs work similarly to LAB outputs. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figures 3–7 and 3–8 show the DSP block interfaces to LAB rows.

Figure 3–7. High-Level View, DSP Block Interface to Interconnect

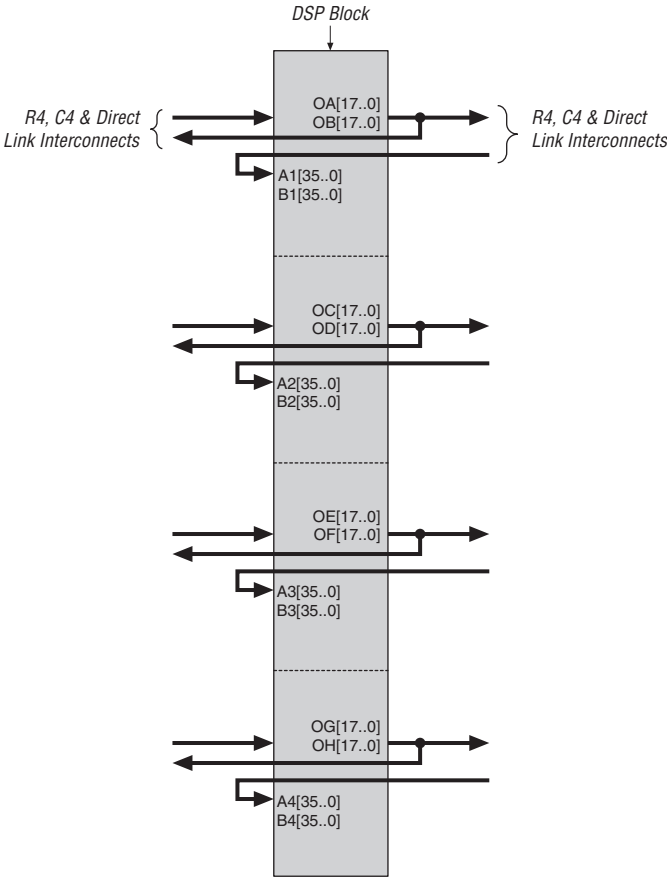
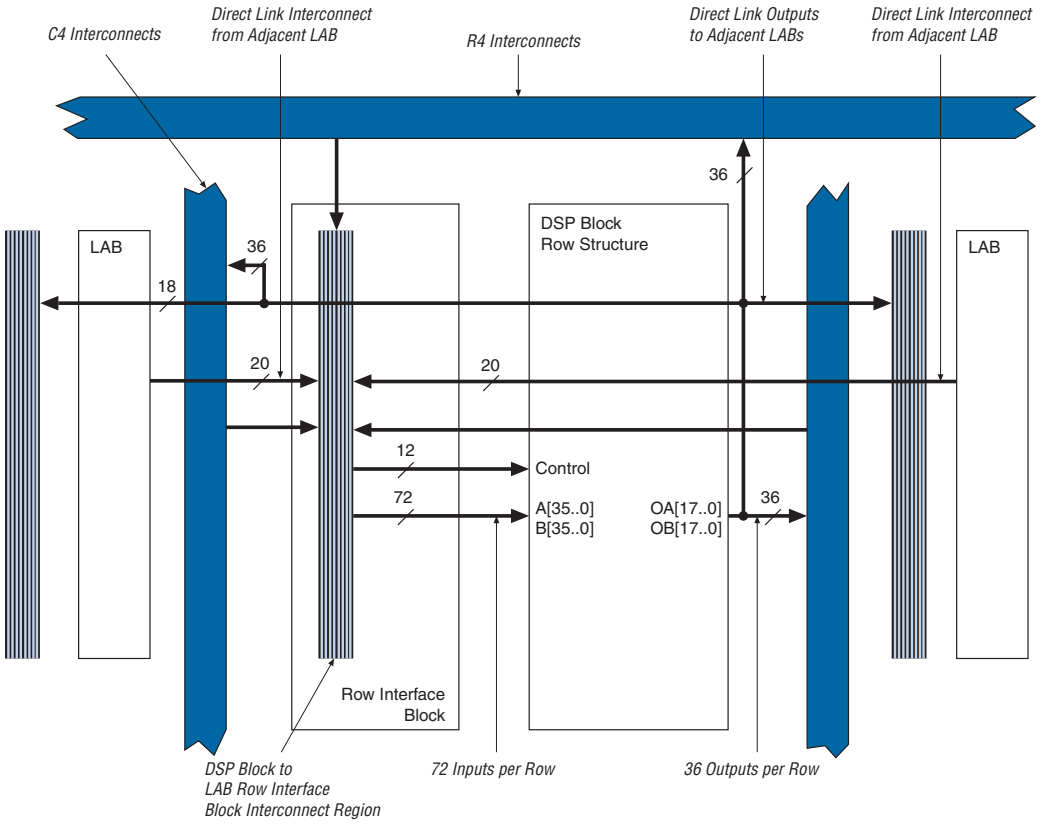


Figure 3–8. Detailed View, DSP Block Interface to Interconnect



I/O Block Connections to Interconnect

The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 3–9 shows how a row I/O block connects to the logic array. Figure 3–10 shows how a column I/O block connects to the logic array.

Figure 3–9. Row I/O Block Connection to Interconnect

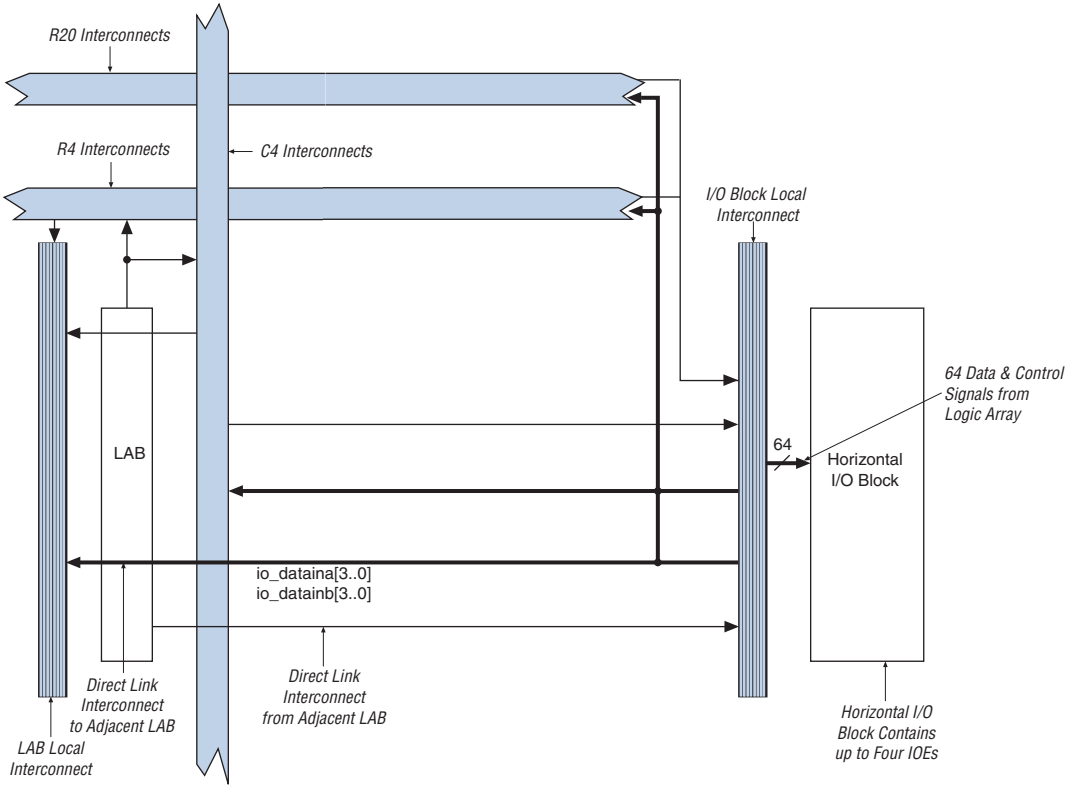
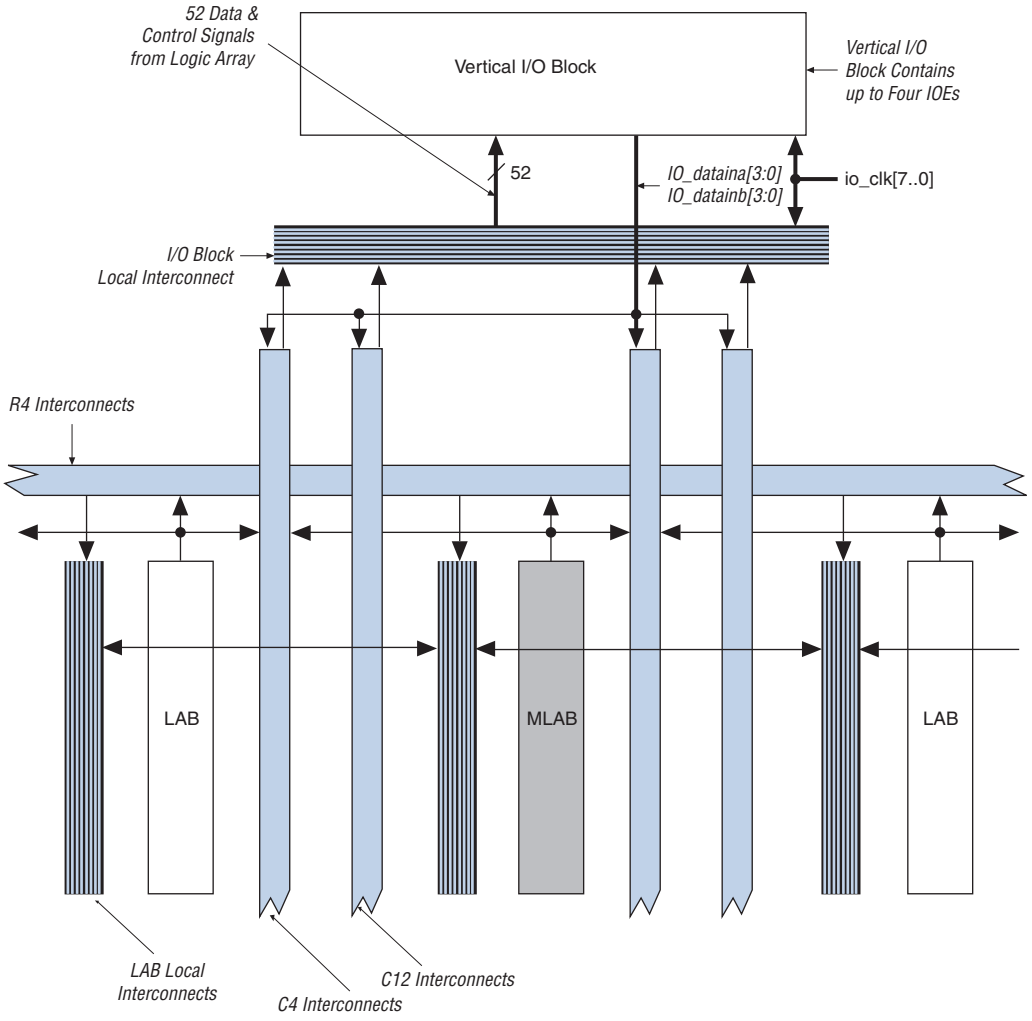


Figure 3–10. Column I/O Block Connection to Interconnect



Conclusion

Stratix III devices consist of an array of logic blocks such as LABs, TriMatrix memory, DSP blocks, and IOEs. These blocks communicate with themselves and one another through the MultiTrack interconnect structures. The Quartus II compiler automatically routes critical design paths on faster interconnects to improve design performance and optimize the device resources.

Document Revision History

Table 3–3 shows the revision history for this document.

Table 3–3. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
November 2006 v1.0	Initial Release	

4. TriMatrix Embedded Memory Blocks in Stratix III Devices

SIII51004-1.1

Introduction

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix® III FPGA designs. TriMatrix memory includes 640-bit memory logic array blocks (MLABs), 9-Kbit M9K blocks, and 144-Kbit M144K blocks. The MLABs have been optimized to implement filter delay lines, small first-in first-out (FIFO) buffers, and shift registers. You can use the M9K blocks for general purpose memory applications, and the M144K blocks are ideal for processor code storage, packet buffering, and video frame buffering.

You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register via the Quartus® II MegaWizard. You can stitch together multiple blocks of the same type to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 20,491 Kbits of embedded SRAM at up to 600 MHz operation. This chapter describes TriMatrix memory blocks, modes, features, and design considerations.

Overview

Table 4–1 summarizes the features supported by the three sizes of TriMatrix memory.

Table 4–1. Summary of TriMatrix Memory Features (Part 1 of 2)

Feature	MLABs	M9K Blocks	M144K Blocks
Maximum performance	600 MHz	600 MHz	600 MHz
Total RAM bits (including parity bits)	640	9,216	147,456
Configurations (depth × width)	64×8 64×9 64×10 32×16 32×18 32×20	8K×1 4K×2 2K×4 1K×8 1K×9 512×16 512×18 256×32 256×36	16K×8 16K×9 8K×6 8K×18 4K×32 4K×36 2K×64 2K×72
Parity bits	✓	✓	✓
Byte enable	✓	✓	✓

Table 4–1. Summary of TriMatrix Memory Features (Part 2 of 2)

Feature	MLABs	M9K Blocks	M144K Blocks
Packed mode		✓	✓
Address clock enable	✓	✓	✓
Single-port memory	✓	✓	✓
Simple dual-port memory	✓	✓	✓
True dual-port memory		✓	✓
Embedded shift register	✓	✓	✓
ROM	✓	✓	✓
FIFO buffer	✓	✓	✓
Simple dual-port mixed width support	✓ *(1)*	✓	✓
True dual-port mixed width support		✓	✓
Memory initialization file (**.mif**)	✓	✓	✓
Mixed-clock mode	✓	✓	✓
Power-up condition	Outputs cleared if registered, otherwise reads memory contents.	Outputs cleared	Outputs cleared
Register clears	Output registers	Output registers	Output registers
Write/Read operation triggering	Write: Falling clock edges Read: Rising clock edges	Write and Read: Rising clock edges	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to old or new data	Outputs set to old or new data	Outputs set to old or new data
Mixed-port read-during-write	Outputs set to old or new data	Outputs set to old data	Outputs set to old data
ECC Support	Soft IP support via Quartus II	Soft IP support via Quartus II	Built-in support in ×64 wide SDP mode or soft IP support via Quartus II

Note to Table 4–1:

(1) These features are not natively supported in the architecture, but are achieved through emulation via the Quartus II software.

Table 4–2 shows the capacity and distribution of the TriMatrix memory blocks in each Stratix III family member

Table 4–2. TriMatrix Memory Capacity and Distribution in Stratix III Devices

Device	MLABs	M9K Blocks	M144K Blocks	Total Dedicated RAM Bits (dedicated memory blocks only)	Total RAM Bits (including MLABs)
EP3SL50	950	108	6	1,836 Kb	2,430 Kb
EP3SL70	1,350	150	6	2,214 Kb	3,058 Kb
EP3SL110	2,150	275	12	4,203 Kb	5,547 Kb
EP3SL150	2,850	355	16	5,499 Kb	7,280 Kb
EP3SL200	4,000	468	24	7,668 Kb	10,168 Kb
EP3SL340	6,750	1,040	48	16,272 Kb	20,491 Kb
EP3SE50	950	400	12	5,328 Kb	5,922 Kb
EP3SE80	1,600	495	12	6,183 Kb	7,183 Kb
EP3SE110	2,150	639	16	8,055 Kb	9,399 Kb
EP3SE260	5,100	864	48	14,688 Kb	17,876 Kb

TriMatrix Memory Block Types

While the M9K and M144K memory blocks are dedicated resources, the MLABs are dual-purpose blocks. They can be configured as regular logic array blocks (LABs) or as memory logic array blocks (MLABs). Ten ALMs make up one MLAB. Each ALM in an MLAB can be configured as either a 64 × 1 or a 32 × 2 block, resulting in a 64 × 10 or 32 × 20 simple dual-port SRAM block in a single MLAB.

Parity Bit Support

All TriMatrix memory blocks have built-in parity-bit support. The ninth bit associated with each byte can store a parity bit or serve as an additional data bit. No parity function is actually performed on the ninth bit.

Byte Enable Support

All TriMatrix memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM blocks' write operations.

The default value for the byte enable signals is high (enabled), in which case writing is controlled only by the write enable signals. The byte enable registers have no clear port. When using parity bits on the M9K and M144K blocks, the byte enable controls all nine bits (eight bits of data plus one parity bit). When using parity bits on the MLAB, the byte-enable controls all 10 bits in the widest mode.

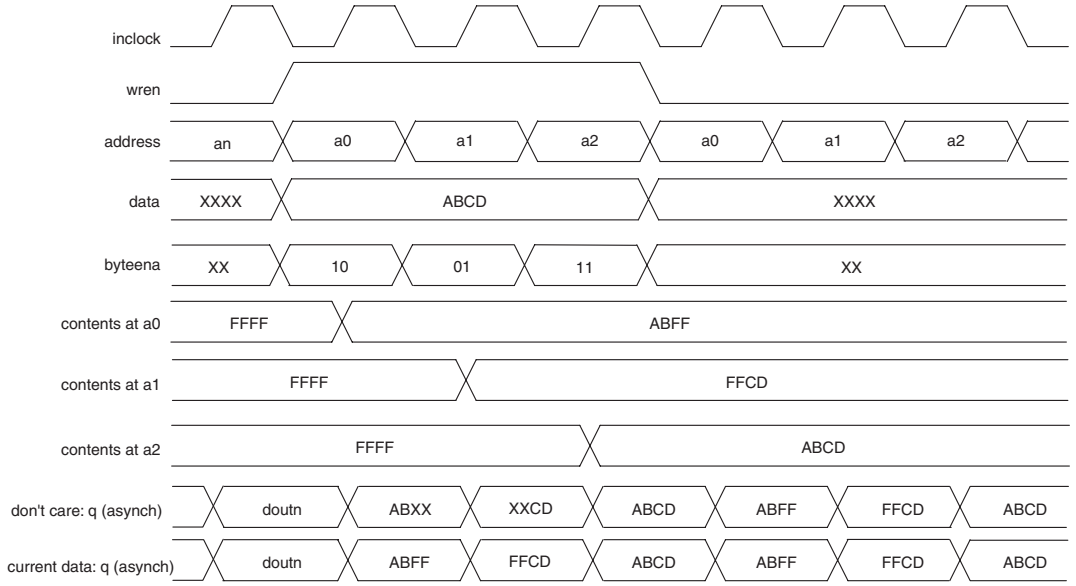
Byte enables operate in a one-hot fashion, with the least significant bit (LSB) of the `byteena` signal corresponding to the least significant byte of the data bus. For example, if using a RAM block in ×18 mode, with `byteena = 01`, `data[8..0]` is enabled and `data[17..9]` is disabled. Similarly, if `byteena = 11`, both `data[8..0]` and `data[17..9]` are enabled. Byte enables are active high.

You cannot use the byte enable feature when using the error correction coding (ECC) feature on M144K blocks.

Figure 4–1 shows how the write enable (`wren`) and byte enable (`byteena`) signals control the operations of the RAM.

When a byte-enable bit is de-asserted during a write cycle, the corresponding data byte output can appear as either a “don't care” value or the current data at that location. The output value for the masked byte is controllable via the Quartus II software. When a byte-enable bit is asserted during a write cycle, the corresponding data byte output also depends on the setting chosen in the Quartus II software.

Figure 4–1. Stratix III Byte Enable Functional Waveform



Packed Mode Support

Stratix III M9K and M144K blocks support packed mode. The packed mode feature packs two independent single-port RAMs into one memory block. The Quartus II software automatically implements packed mode where appropriate by placing the physical RAM block into true dual-port mode and using the most significant bit (MSB) of the address to distinguish between the two logical RAMs. The size of each independent single-port RAM must not exceed half of the target block size.

Address Clock Enable Support

All Stratix III memory blocks support address clock enable, which holds the previous address value for as long as the signal is enabled (`addressstall = 1`). When the memory blocks are configured in dual-port mode, each port has its own independent address clock enable. The default value for the address clock enable signals is low (disabled).

Figure 4–2 shows an address clock enable block diagram. The address clock enable is referred to by the port name `addressstall`.

Figure 4–2. Stratix III Address Clock Enable Block Diagram

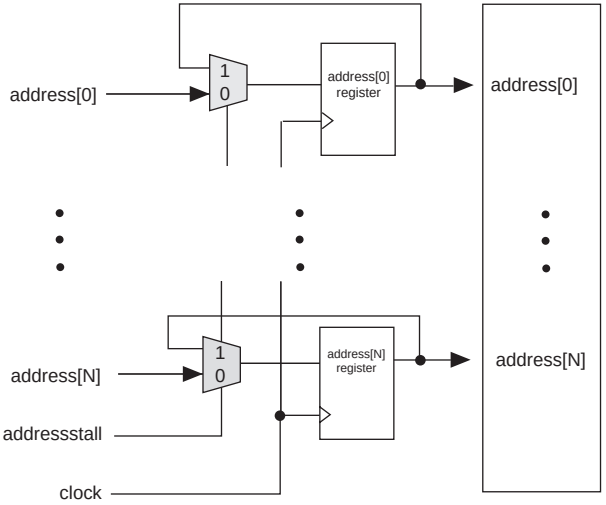


Figure 4–3 shows the address clock enable waveform during the read cycle.

Figure 4–3. Stratix III Address Clock Enable during Read Cycle Waveform

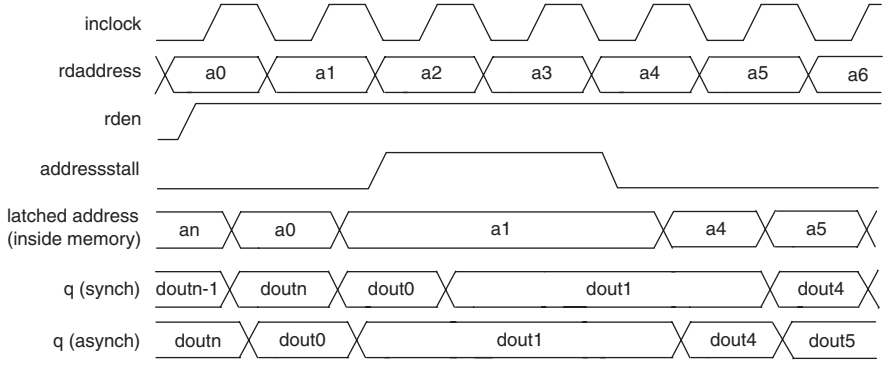
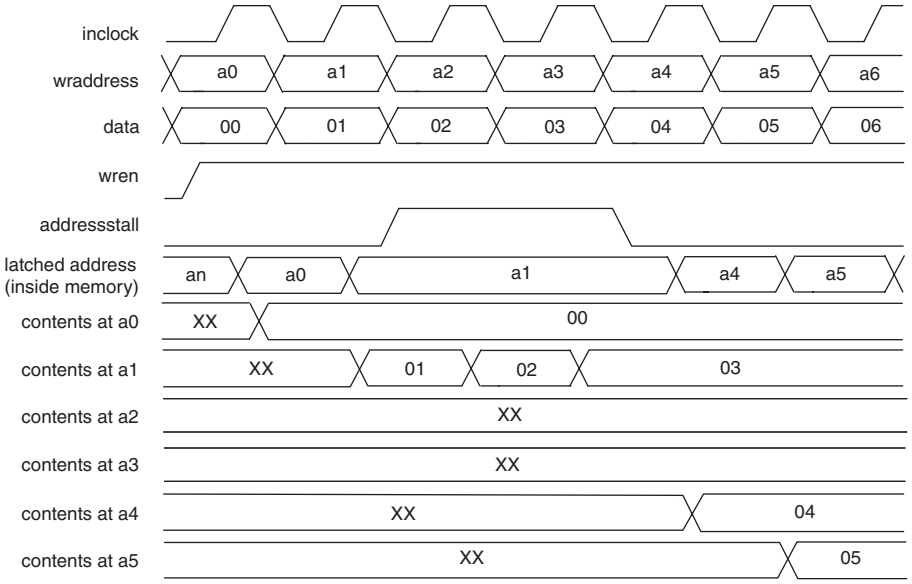


Figure 4–4 shows the address clock enable waveform during write cycle.

Figure 4–4. Stratix III Address Clock Enable during Write Cycle Waveform



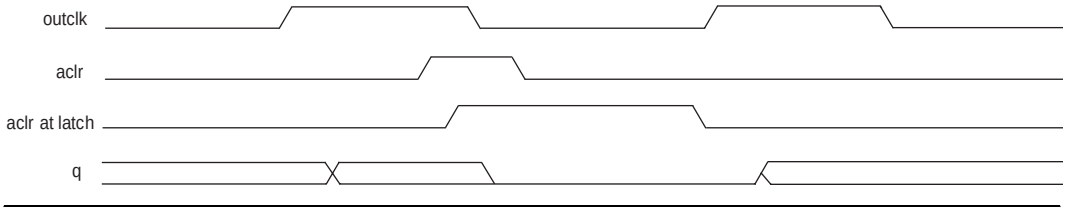
Mixed Width Support

M9K and M144K memory blocks support mixed data widths inherently. MLABs can support mixed data widths through emulation via the Quartus II software. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to a memory block. See *"Memory Modes" on page 4–9* for details on the different widths supported per memory mode.

Asynchronous Clear

Stratix III TriMatrix memory blocks support asynchronous clears on the output latches and output registers. Therefore, if your RAM is not using the output registers, you can still clear the RAM outputs via the output latch asynchronous clear. A functional waveform showing this functionality is shown in Figure 4–5.

Figure 4–5. Output Latch Asynchronous Clear Waveform



You can selectively enable asynchronous clears per logical memory via the Quartus II RAM MegaWizard.

For more information, refer to the *RAM Megafunction User Guide*.

Error Correction Code (ECC) Support

Stratix III M144K blocks have built-in support for error correction code (ECC) when in ×64-wide simple dual-port mode. ECC allows you to detect and correct data errors in the memory array. The M144K blocks have a single-error-correction double-error-detection (SECDED) implementation. SECDED can detect and fix a single bit error in a 64-bit word or detect two bit errors in a 64-bit word. It cannot detect three or more errors.

The M144K ECC status is communicated via a three-bit status flag `eccstatus[2..0]`. The status flag can be either registered or unregistered. When registered, it uses the same clock and asynchronous clear signals as the output registers. When not registered, it cannot be asynchronously cleared.

Table 4–3 shows the truth table for the ECC status flags.

Table 4–3. Truth Table for ECC Status Flags

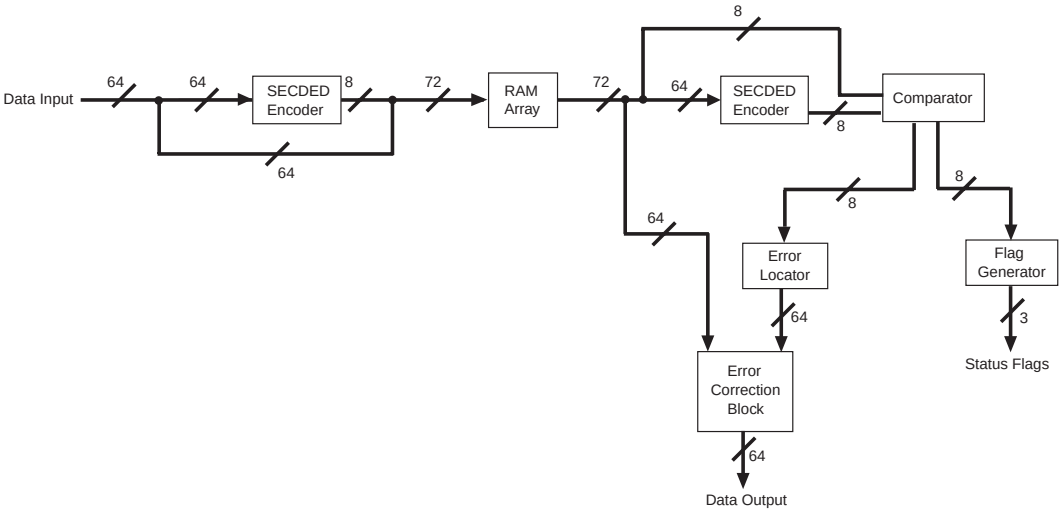
Status	eccstatus[2]	eccstatus[1]	eccstatus[0]
No error	0	0	0
Single error and fixed	0	1	1
Double error and no fix	1	0	1
Illegal	0	0	1
Illegal	0	1	0
Illegal	1	0	0
Illegal	1	1	X

You cannot use the byte enable feature when ECC is engaged.

Read during write "old data" mode is not supported when ECC is engaged.

Figure 4–6 shows a block diagram of the ECC block of the M144K.

Figure 4–6. ECC Block Diagram of the M144K



Memory Modes

Stratix III TriMatrix memory blocks allow you to implement fully synchronous SRAM memory in multiple modes of operation. M9K and M144K blocks do not support asynchronous memory (unregistered inputs). MLABs support asynchronous (flow-through) read operations.

Depending on which TriMatrix memory block you target, the following modes may be used:

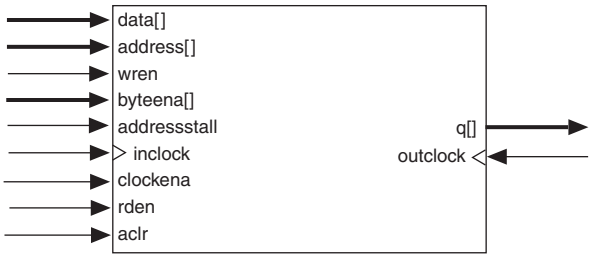
- Single-port
- Simple dual-port
- True dual-port
- Shift-register
- ROM
- FIFO

When using the memory blocks in ROM, single-port, simple dual-port, or true dual-port mode, you can corrupt the memory contents if you violate the setup or hold-time on any of the memory block input registers. This applies to both read and write operations.

Single Port RAM

All TriMatrix memory blocks support single-port mode. Single-port mode allows you to do either one-read or one-write operation at a time. Simultaneous reads and writes are not supported in single-port mode. Figure 4–7 shows the single-port RAM configuration.

Figure 4–7. Single-Port Memory *Note (1)*



Note to Figure 4–7:

(1) You can implement two single-port memory blocks in a single M9K or M144K block. See "Packed Mode Support" on page 4–5 for more details.

During a write operation, behavior of the RAM outputs is configurable. If you use the read-enable signal and perform a write operation with the read enable deactivated, the RAM outputs retain the values they held during the most recent active read enable. If you activate read enable during a write operation, or if you are not using the read-enable signal at all, the RAM outputs either show the new data being written, the old data at that address, or a don't care value. To choose the desired behavior, set the read-during-write behavior to either new data, old data, or don't care in the RAM MegaWizard® in the Quartus II software. See "Read During Write" on page 4–21 for more details on this behavior.

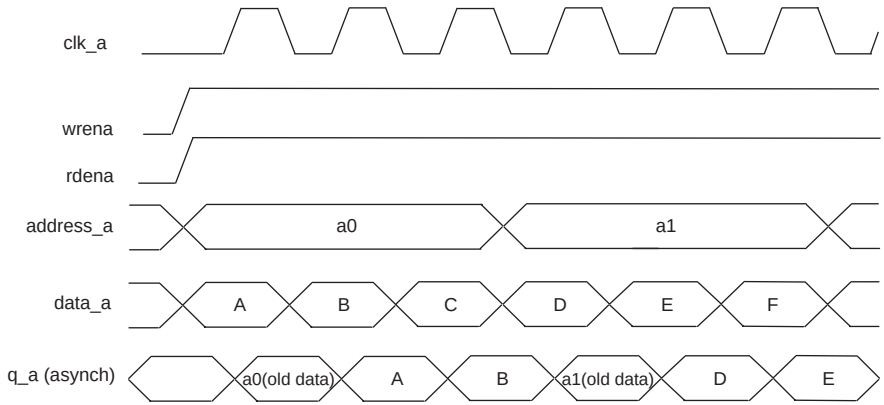
Table 4–4 shows the possible port width configurations for TriMatrix memory blocks in single-port mode.

Table 4–4. Stratix III Port Width Configurations for MLABs, M9K Blocks, and M144K Blocks (Single-Port Mode)

	MLABs	M9K Blocks	M144K Blocks
Port Width Configurations	64×8 64×9 64×10 32×16 32×18 32×20	8K×1 4K×2 2K×4 1K×8 1K×9 512×16 512×18 256×32 256×36	16K×8 16K×9 8K×16 8K×18 4K×32 4K×36 2K×64 2K×72

Figure 4–8 shows timing waveforms for read and write operations in single-port mode with unregistered outputs. Registering the RAM's outputs would simply delay the q output by one clock cycle.

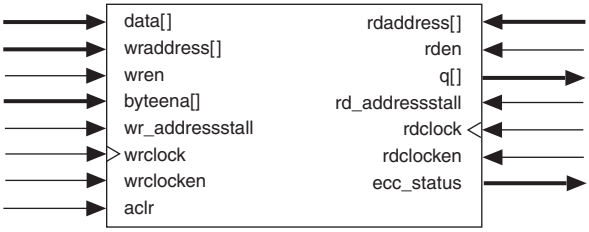
Figure 4–8. Timing Waveform for Read-Write Operations (Single-Port Mode)



Simple Dual-Port Mode

All TriMatrix memory blocks support simple dual-port mode. Simple dual-port mode allows you to perform one-read and one-write operation to different locations at the same time. Figure 4–9 shows the simple dual-port configuration.

Figure 4–9. Stratix III Simple Dual-Port Memory *Note (1)*



Note to Figure 4–9:

(1) Simple dual-port RAM supports input / output clock mode in addition to the read / write clock mode shown.

Simple dual-port mode supports different read and write data widths (mixed width support). Table 4–5 shows the mixed width configurations for the M9K blocks in simple dual-port mode. MLABs do not have native support for mixed width operation. The Quartus II software can implement mixed width memories in MLABs by using more than one MLAB.

Table 4–5. Stratix III M9K Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	8K×1	4K×2	2K×4	1K×8	512×16	256×32	1K×9	512×18	256×36
8K×1	✓	✓	✓	✓	✓	✓	—	—	—
4K×2	✓	✓	✓	✓	✓	✓	—	—	—
2K×4	✓	✓	✓	✓	✓	✓	—	—	—
1K×8	✓	✓	✓	✓	✓	✓	—	—	—
512×16	✓	✓	✓	✓	✓	✓	—	—	—
256×32	✓	✓	✓	✓	✓	✓	—	—	—
1K×9	—	—	—	—	—	—	✓	✓	✓
512×18	—	—	—	—	—	—	✓	✓	✓
256×36	—	—	—	—	—	—	✓	✓	✓

Table 4–6 shows the mixed width configurations for the M144K blocks in simple dual-port mode.

Table 4–6. Stratix III M144K Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port							
	16K×8	8K×16	4K×32	2K×64	16K×9	8K×18	4K×36	2K×72
16K×8	✓	✓	✓	✓	—	—	—	—
8K×16	✓	✓	✓	✓	—	—	—	—
4K×32	✓	✓	✓	✓	—	—	—	—
2K×64	✓	✓	✓	✓	—	—	—	—
16K×9	—	—	—	—	✓	✓	✓	✓
8K×18	—	—	—	—	✓	✓	✓	✓
4K×36	—	—	—	—	✓	✓	✓	✓
2K×72	—	—	—	—	✓	✓	✓	✓

In simple dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output a don't care value or old data. To choose the desired behavior, set the read-during-write behavior to either don't care or old data in the RAM MegaWizard in the Quartus II software. See "Read During Write" on page 4–21 for more details on this behavior.

MLABs only support a write-enable signal. Read-during-write behavior for the MLABs can be either don't care, new data, or old data. The available choices depend on the configuration of the MLAB.

Figure 4–10 shows timing waveforms for read and write operations in simple dual-port mode with unregistered outputs. Registering the RAM's outputs would simply delay the `q` output by one clock cycle.

Figure 4–10. Stratix III Simple Dual-Port Timing Waveforms

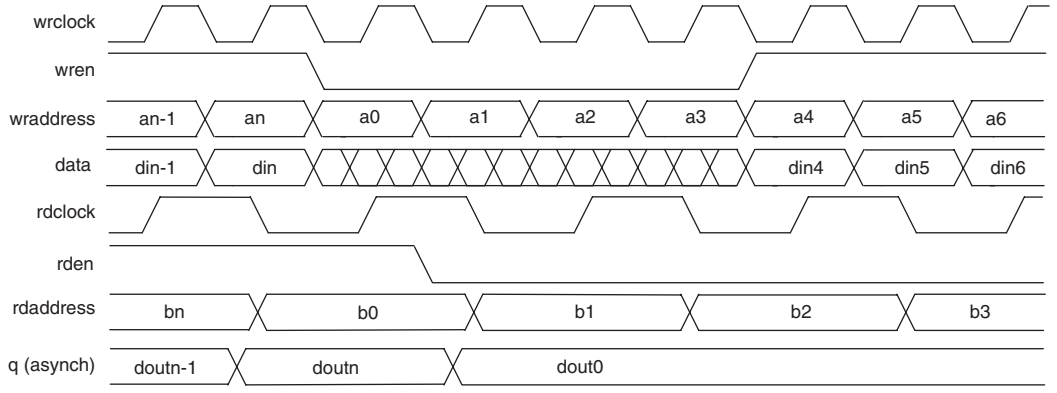
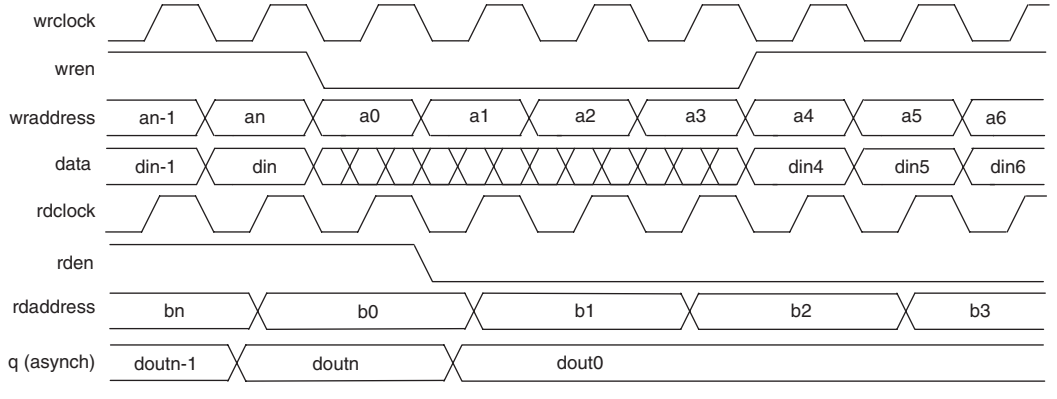


Figure 4–11 shows timing waveforms for read and write operations in mixed-port mode with unregistered outputs.

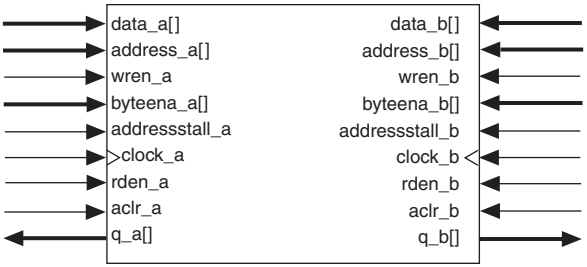
Figure 4–11. Stratix III Mixed-Port Read-During-Write Timing Waveforms



True Dual-Port Mode

Stratix III M9K and M144K blocks support true dual-port mode. Sometimes called bi-directional dual-port, this mode allows you to perform any combination of two port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 4–12 shows the true dual-port RAM configuration.

Figure 4–12. Stratix III True Dual-Port Memory *Note (1)*



Note to Figure 4–12:

(1) True dual-port memory supports input/output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M9K and M144K blocks in true dual-port mode is as follows:

- 512 × 16-bit (×18-bit with parity) (M9K)
- 4K × 32-bit (×36-bit with parity) (M144K)

Wider configurations are unavailable because the number of output drivers is equivalent to the maximum bit width of the respective memory block. Because true dual-port RAM has outputs on two ports, its maximum width equals half of the total number of output drivers. Table 4–7 lists the possible M9K block mixed-port width configurations in true dual-port mode.

Table 4–7. Stratix III M9K Block Mixed-Width Configuration (True Dual-Port Mode) (Part 1 of 2)

Read Port	Write Port						
	8K×1	4K×2	2K×4	1K×8	512×16	1K×9	512×18
8K×1	✓	✓	✓	✓	✓	—	—
4K×2	✓	✓	✓	✓	✓	—	—
2K×4	✓	✓	✓	✓	✓	—	—
1K×8	✓	✓	✓	✓	✓	—	—

Table 4–7. Stratix III M9K Block Mixed-Width Configuration (True Dual-Port Mode) (Part 2 of 2)

Read Port	Write Port						
	8K×1	4K×2	2K×4	1K×8	512×16	1K×9	512×18
512×16	✓	✓	✓	✓	✓	—	—
1K×9	—	—	—	—	—	✓	✓
512×18	—	—	—	—	—	✓	✓

Table 4–8 lists the possible M144K block mixed-port width configurations in true dual-port mode.

Table 4–8. Stratix III M144K Block Mixed-Width Configurations (True Dual-Port Mode)

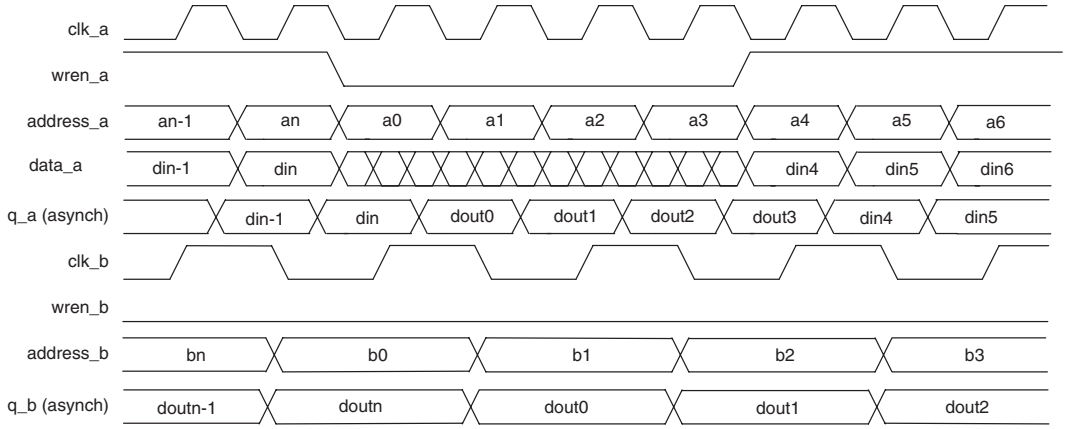
Read Port	Write Port					
	16K×8	8K×16	4K×32	16K×9	8K×18	4K×36
16K×8	✓	✓	✓	—	—	—
8K×16	✓	✓	✓	—	—	—
4K×32	✓	✓	✓	—	—	—
16K×9	—	—	—	✓	✓	✓
8K×18	—	—	—	✓	✓	✓
4K×36	—	—	—	✓	✓	✓

In true dual-port mode, M9K and M144K blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output new data at that location or old data. To choose the desired behavior, set the read-during-write behavior to either new data or old data in the RAM MegaWizard in the Quartus II software. See "Read During Write" on page 4–21 for more details on this behavior.

In true dual-port mode you can access any memory location at any time from either port. When accessing the same memory location from both ports, you must avoid possible write conflicts. A write conflict happens when you attempt to write to the same address location from both ports at the same time. This results in unknown data being stored to that address location. No conflict resolution circuitry is built into the Stratix III TriMatrix memory blocks. You must handle address conflicts external to the RAM block.

Figure 4–13 shows true dual-port timing waveforms for the write operation at port A and read operation at port B with the Read-During-Write behavior set to new data. Registering the RAM's outputs would simply delay the q outputs by one clock cycle.

Figure 4–13. Stratix III True Dual-Port Timing Waveform



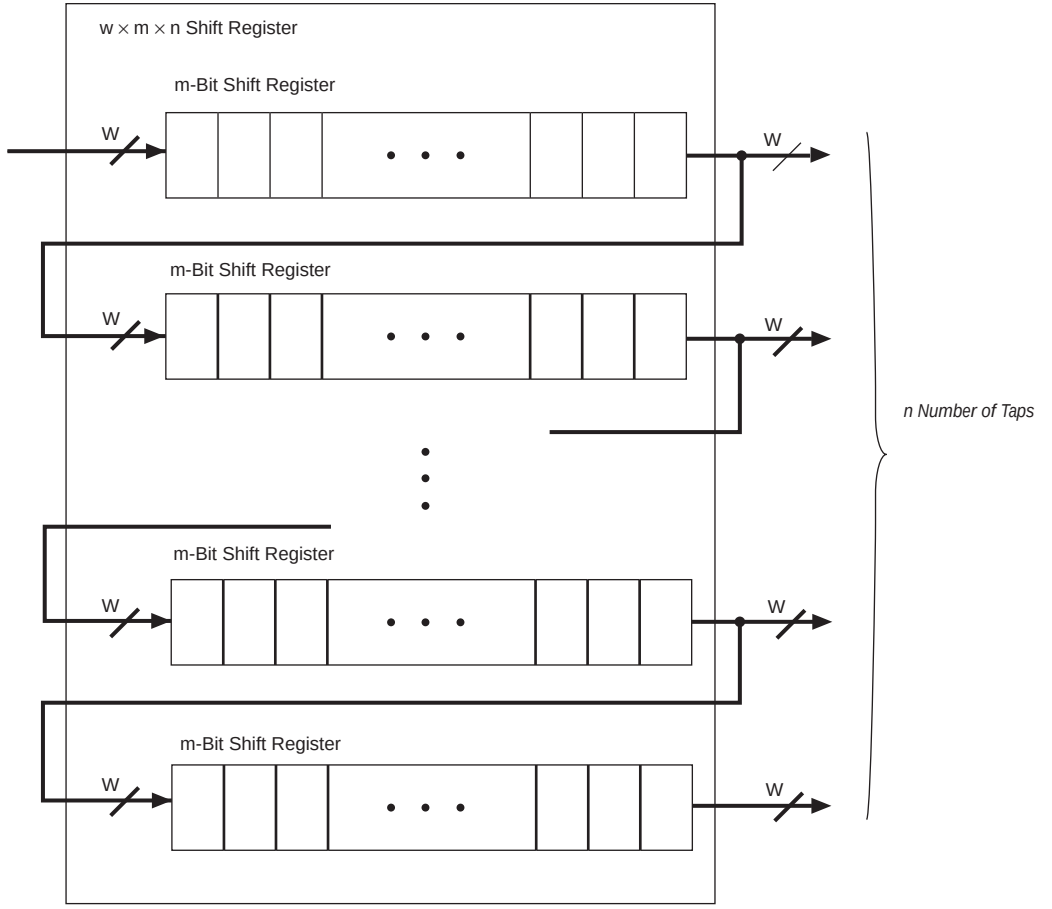
Shift-Register Mode

All Stratix III memory blocks support shift register mode. Embedded memory block configurations can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto- and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift-register block, which saves logic cell and routing resources.

The size of a shift register (w × m × n) is determined by the input data width (w), the length of the taps (m), and the number of taps (n). You can cascade memory blocks to implement larger shift registers.

Figure 4–14 shows the TriMatrix memory block in shift-register mode.

Figure 4–14. Stratix III Shift-Register Memory Configuration



ROM Mode

All Stratix III TriMatrix memory blocks support ROM mode. A memory initialization file (**.mif**) initializes the ROM contents of these blocks. The address lines of the ROM are registered on M9K and M144K blocks, but can be unregistered on MLABs. The outputs can be registered or unregistered. Output registers can be asynchronously cleared. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Mode

All TriMatrix memory blocks support FIFO mode. MLABs are ideal for designs with many small, shallow FIFO buffers. To implement FIFO buffers in your design, use the Quartus II software FIFO MegaWizard. Both single and dual-clock (asynchronous) FIFOs are supported.

Refer to the *Single- and Dual-Clock FIFO Megafunctions User Guide* for more information on implementing FIFO buffers.

Clocking Modes

Stratix III TriMatrix memory blocks support the following clocking modes:

- Independent
- Input / output
- Read / write
- Single clock

Violating the setup or hold time on the memory block address registers could corrupt the memory contents. This applies to both read and write operations.

Table 4–9 shows the clocking mode versus memory mode support matrix.

Table 4–9. Stratix III TriMatrix Memory Clock Modes

Clocking Mode	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode	ROM Mode	FIFO Mode
Independent	✓	—	—	✓	—
Input/output	✓	✓	✓	✓	—
Read/write	—	✓	—	—	✓
Single clock	✓	✓	✓	✓	✓

Independent Clock Mode

Stratix III TriMatrix memory blocks can implement independent clock mode for true dual-port memories. In this mode, a separate clock is available for each port (A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port also supports independent clock enables for port A and port B registers. Asynchronous clears are supported only for output latches and output registers on both ports.

Input/Output Clock Mode

Stratix III TriMatrix memory blocks can implement input / output clock mode for true and simple dual-port memories. In this mode, an input clock controls all registers related to the data input to the memory block including data, address, byte enables, read enables, and write enables. An output clock controls the data output registers. Asynchronous clears are available on output latches and output registers only.

Read/Write Clock Mode

Stratix III TriMatrix memory blocks can implement read / write clock mode for simple dual-port memories. In this mode, a write clock controls the data-input, write-address, and write-enable registers. Similarly, a read clock controls the data-output, read-address, and read-enable registers. The memory blocks support independent clock enables for both the read and write clocks. Asynchronous clears are available on data output latches and registers only.

Single Clock Mode

Stratix III TriMatrix memory blocks can implement single-clock mode for true dual-port, simple dual-port, and single-port memories. In this mode, a single clock, together with a clock enable, is used to control all registers of the memory block. Asynchronous clears are available on output latches and output registers only.

Design Considerations

This section describes guidelines for designing with TriMatrix memory blocks.

Selecting TriMatrix Memory Blocks

The Quartus II software automatically partitions user-defined memory into embedded memory blocks by taking into account both speed and size constraints placed on your design. For example, the Quartus II software may spread out a memory across multiple memory blocks when resources are available in order to increase the performance of the design. You can manually assign the memory to a specific block size via the RAM MegaWizard.

MLABs can implement single-port SRAM through emulation via the Quartus II software. Emulation results in minimal additional logic resources being used. Because of the dual-purpose architecture of the MLAB, it only has data input registers and output registers in the block. MLABs gain input address registers and additional optional data output registers from adjacent ALMs by using register packing.

For more information on register packing, see the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

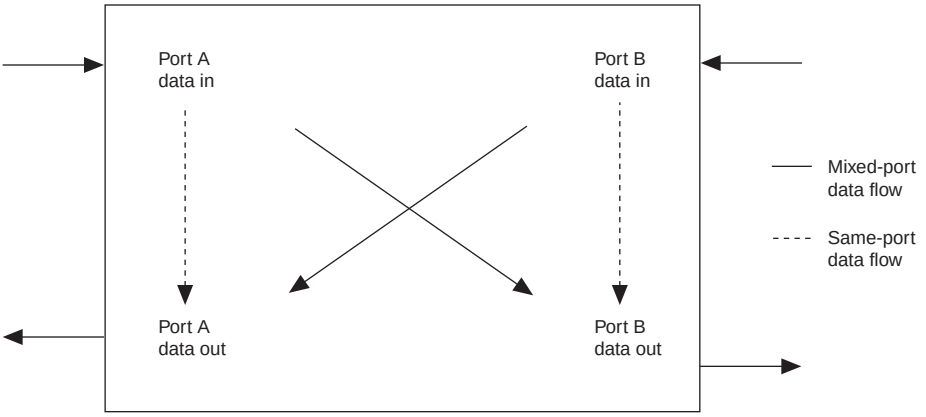
Conflict Resolution

When using the memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Since no conflict resolution circuitry is built into the memory blocks, this results in unknown data being written to that location. Therefore, you must implement conflict resolution logic external to the memory block to avoid address conflicts.

Read During Write

You can customize the read-during-write behavior of the Stratix III TriMatrix memory blocks to suit your design needs. Two types of read-during-write operations are available: same port and mixed port. Figure 4–15 shows the difference between the two types.

Figure 4–15. Stratix III Read-During-Write Data Flow



Same-Port Read-During-Write Mode

This mode applies to either a single-port RAM or the same port of a true dual-port RAM. In same-port read-during-write mode, three output choices are available: new data mode (or flow-through), old data mode, or don't care mode. In new data mode, the new data is available on the rising edge of the same clock cycle on which it was written. In old data

mode, the RAM outputs reflect the old data at that address before the write operation proceeds. In don't care mode, the RAM outputs don't care values for a read-during-write operation.

Figure 4–16 shows sample functional waveforms of same-port read-during-write behavior with new data.

Figure 4–16. Same Port Read-During Write: New Data Mode

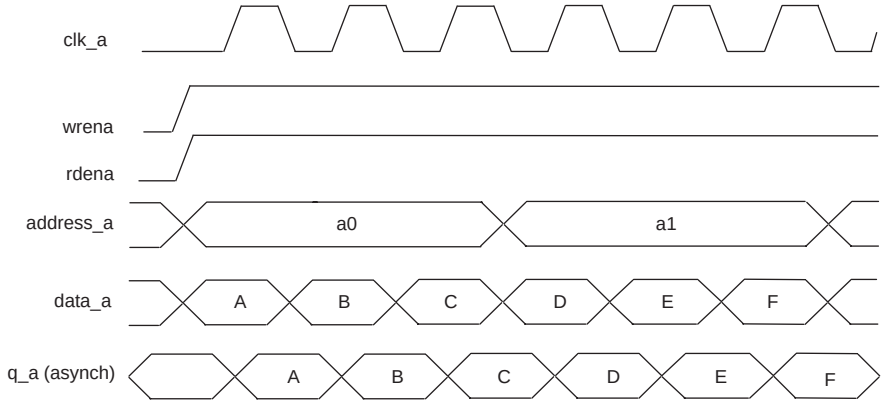
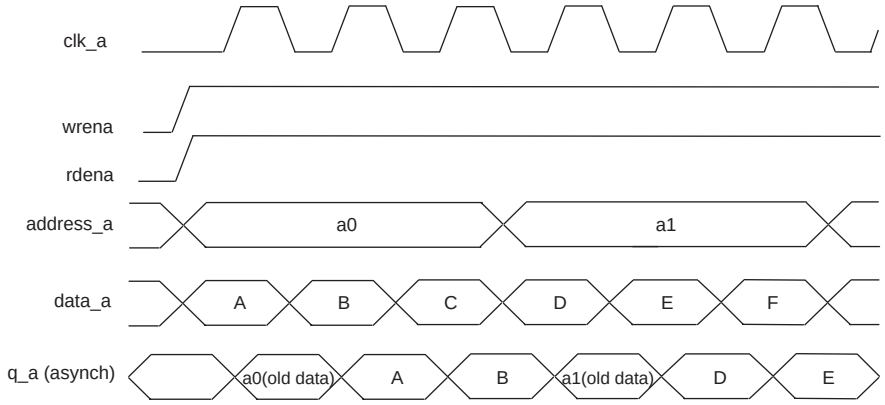


Figure 4–17 shows sample functional waveforms of same-port read-during-write behavior with old data mode.

Figure 4–17. Same Port Read-During-Write: Old Data Mode



Mixed-Port Read-During-Write Mode

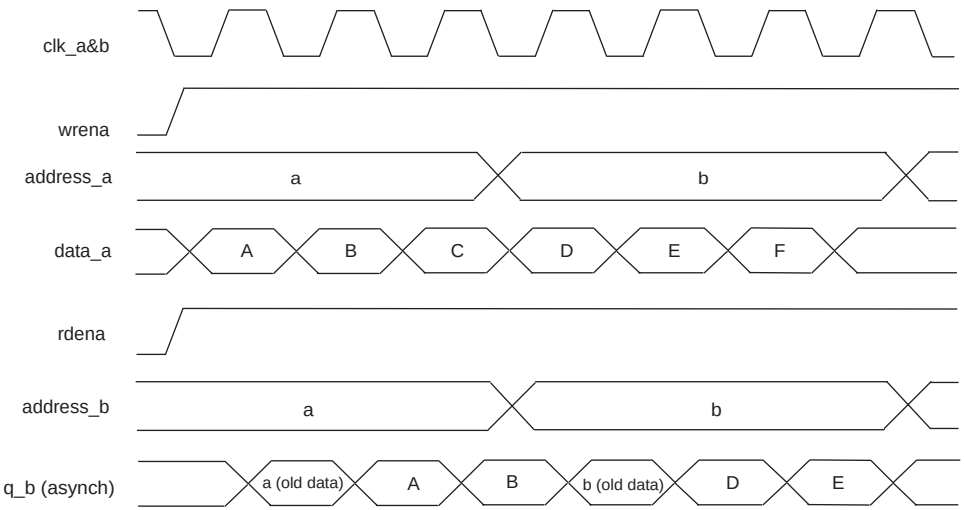
This mode applies to a RAM in simple or true dual-port mode which has one port reading and the other port writing to the same address location with the same clock.

In this mode you also have two output choices: old data or don't care. In old data mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In don't care mode, the same operation results in a "don't care" or "unknown" value on the RAM outputs.

Read-during-write behavior is controlled via the RAM MegaWizard. Refer to the *RAM Megafunction User Guide* for more details on how to implement the desired behavior.

Figure 4–18 shows a sample functional waveform of mixed-port read-during-write behavior for the old data mode. In don't care mode, the old data shown in the figure is simply replaced with "don't cares".

Figure 4–18. Mixed Port Read During Write: Old Data Mode



Mixed-port read-during-write is not supported when two different clocks are used in a dual-port RAM. The output value is unknown during a dual-clock mixed-port read-during-write operation.

Power-Up Conditions and Memory Initialization

M9K and M144K memory block outputs power up to zero (cleared), regardless of whether the output registers are used or bypassed. MLABs power up to zero if output registers are used and power up reading the memory contents if output registers are not used. However, the actual RAM cells power up to an unknown state. Therefore, after power-up, if an address is read before being written, the output from the read operation is undefined because the contents are not initialized.

All memory blocks support initialization via an MIF file (**.mif**). You can create MIF files in the Quartus II software and specify their use with the RAM MegaWizard when instantiating a memory in your design. Even if a memory is pre-initialized (for example, via a **.mif** file), it still powers up with its outputs cleared.

For more information on MIF files, refer to the *RAM Megafunction User Guide* as well as the *Quartus II Handbook*.

Power Management

Stratix III memory block clock-enables allow you to control clocking of each memory block to reduce AC power consumption. Use the read-enable signal to ensure that read operations only occur when you need them to. If your design does not require read-during-write, you can reduce your power consumption by de-asserting the read-enable signal during write operations, or any period when no memory operations occur.

The Quartus II software automatically places any unused memory blocks in low power mode to reduce static power.

Conclusion

The Stratix III TriMatrix embedded memory structure provides three different on-chip RAM block sizes to address your design needs. All memory blocks are fully customizable and can be cascaded to implement wider or deeper memories with minimal speed penalty.

You can independently configure each embedded memory block to be a single- or dual-port RAM, FIFO, ROM, or shift register via the Quartus II MegaWizard software.

Document Revision History

Table 4–10 shows the revision history for this document.

Table 4–10. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Updated Table 4–2, Table 4–9.	—
November 2006 v1.0	Initial Release	—

5. DSP Blocks in Stratix III Devices

SIII51005-1.1

Introduction

The Stratix® III family of devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications. These DSP blocks of the Altera® Stratix device family are the third generation of hardwired, fixed function silicon blocks dedicated to maximizing signal processing capability, ease of use, and lowest silicon cost.

Many complex systems such as WiMAX, 3GPP WCDMA, high-performance computing (HPC), voice over Internet protocol (VoIP), H.264 video compression, medical imaging, and HDTV use sophisticated digital signal processing techniques, and this typically requires a large number of mathematical computations. Stratix III devices are ideally suited as the DSP blocks consist of a combination of dedicated elements that perform multiplication, addition, subtraction, accumulation, summation, and dynamic shift operations. Along with the high-performance Stratix III soft logic fabric and TriMatrix™ memory structures, you can configure these blocks to build sophisticated fixed-point and floating-point arithmetic functions. These can be manipulated easily to implement common larger computationally intensive subsystems such as finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

DSP Block Overview

Each Stratix III device has two to seven columns of DSP blocks that implement multiplication, multiply-add, multiply-accumulate (MAC), and dynamic shift functions efficiently. The logical functionality of the Stratix III DSP block is a superset of the previous generation of the DSP block found in Stratix and Stratix II devices.

Architectural highlights of the Stratix III DSP block include:

- High-performance, power-optimized, fully registered and pipelined multiplication operations
- Natively supported 9-bit, 12-bit, 18-bit, 36-bit wordlengths
- Natively supported 18-bit complex multiplications
- Efficiently supported floating-point arithmetic formats (24-bit for single precision and 53-bit for double precision)
- Signed and unsigned input support

- Built-in addition, subtraction and accumulation units to combine multiplication results efficiently
- Cascading 18-bit input bus to form tap-delay line for filtering applications
- Cascading 44-bit output bus to propagate output results from one block to the next block without external logic support
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

The number of DSP blocks for the Stratix III device family is shown in Table 5–1.

Table 5–1. Number of DSP Blocks in Stratix III Devices

	Device	DSP Blocks	Independent Input and Output Multiplication Operators					Four Multiplier Adder Mode
			9 × 9 Multipliers	12 × 12 Multipliers	18 × 18 Multipliers	18 × 18 Complex	36 × 36 Multipliers	18 × 18
Stratix III Logic	EP3SL50	27	216	162	108	54	54	216
	EP3SL70	36	288	216	144	72	72	288
	EP3SL110	36	288	216	144	72	72	288
	EP3SL150	48	384	288	192	96	96	384
	EP3SL200	72	576	432	288	144	144	576
	EP3SE260	96	768	576	384	192	192	768
	EP3SL340	72	576	432	288	144	144	576
Stratix III Enhanced	EP3SE50	48	384	288	192	96	96	384
	EP3SE80	84	672	504	336	168	168	672
	EP3SE110	112	896	672	448	224	224	896
	EP3SE260 *(1)*	96	768	576	384	192	192	768

Note to Table 5–1:

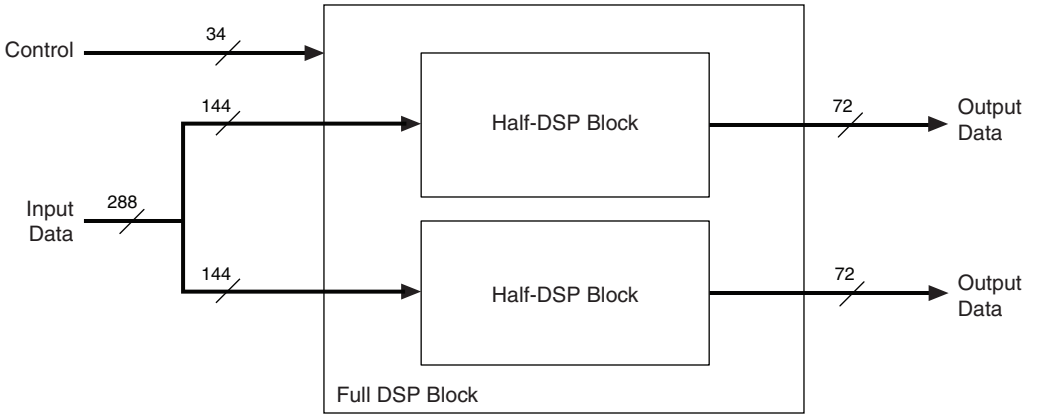
(1) The EP3SE260 device is rich in LE, memory, and multiplier resources. Hence, it aligns with both logic (*L*) and enhanced (*E*) variants.

Table 5–1 shows that the largest Stratix III DSP centric device (EP3SE110) provides up to 896 18 × 18 multiplier functionality in the 36 × 36, complex 18 × 18, and summation modes.

Each DSP block occupies four LAB blocks in height and can be divided further into two half-blocks that share some common clock signals, but are for all common purposes identical in functionality. The layout of each block is shown in Figure 5–1.

The Stratix III DSP block input data lines of 288 bits is double that of Stratix and Stratix II, but the number of output data lines remains at 144 bits.

Figure 5–1. Overview of DSP Block Signals



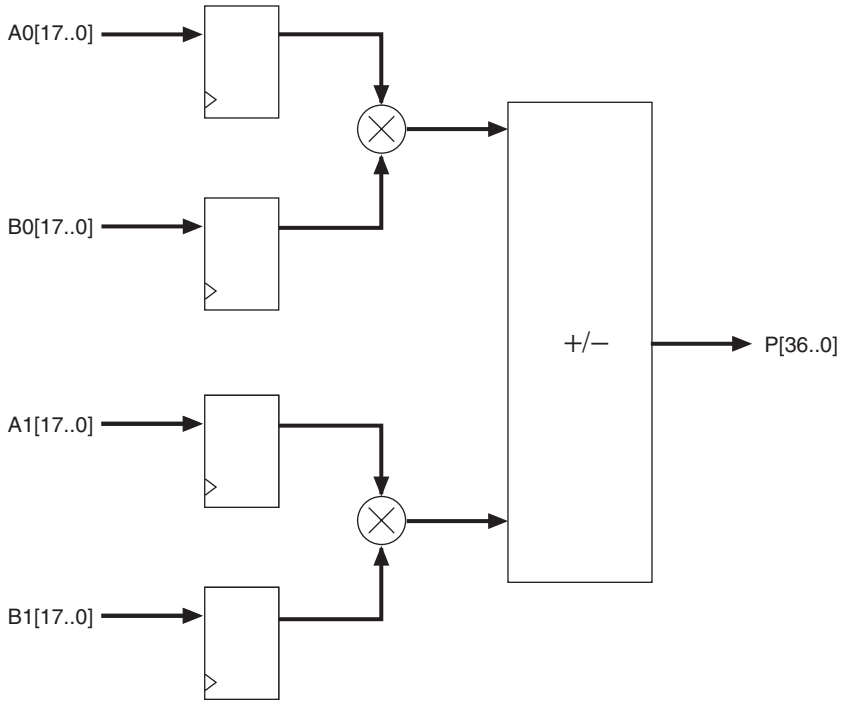
Simplified DSP Operation

In Stratix and Stratix II devices, the fundamental building block consists of an 18-bit × 18-bit multiplier that can also function as two 9-bit × 9-bit multipliers. For Stratix III, the fundamental building block is a pair of 18-bit × 18-bit multipliers followed by a first-stage 37-bit addition/subtraction unit, as shown in Equation 5–1 and Figure 5–2. Note that for all signed numbers, input and output data is represented in 2's complement format only.

Equation 5–1. Multiplier Equation

$$P[36..0] = A_0[17..0] \times B_0[17..0] \pm A_1[17..0] \times B_1[17..0]$$

Figure 5–2. Basic Two-Multiplier Adder Building Block



The structure shown in Figure 5–2 is very useful for building more complex structures, such as complex multipliers and 36 × 36 multipliers, as described in later sections.

Each Stratix III DSP block contains four Two-Multiplier Adder units (two Two-Multiplier Adder units per half-block). Therefore, there are eight 18 × 18 multiplier functionalities per DSP block.

Following the Two-Multiplier Adder units are the pipeline registers, the second-stage adders, and an output register stage. You can configure the second-stage adders to provide the following alternative functions per Half-Block:

Equation 5–2. Four-Multiplier Adder Equation

$$Z[37..0] = P_0[36..0] + P_1[36..0]$$

Equation 5–3. Four-Multiplier Adder Equation (44-Bit Accumulation)

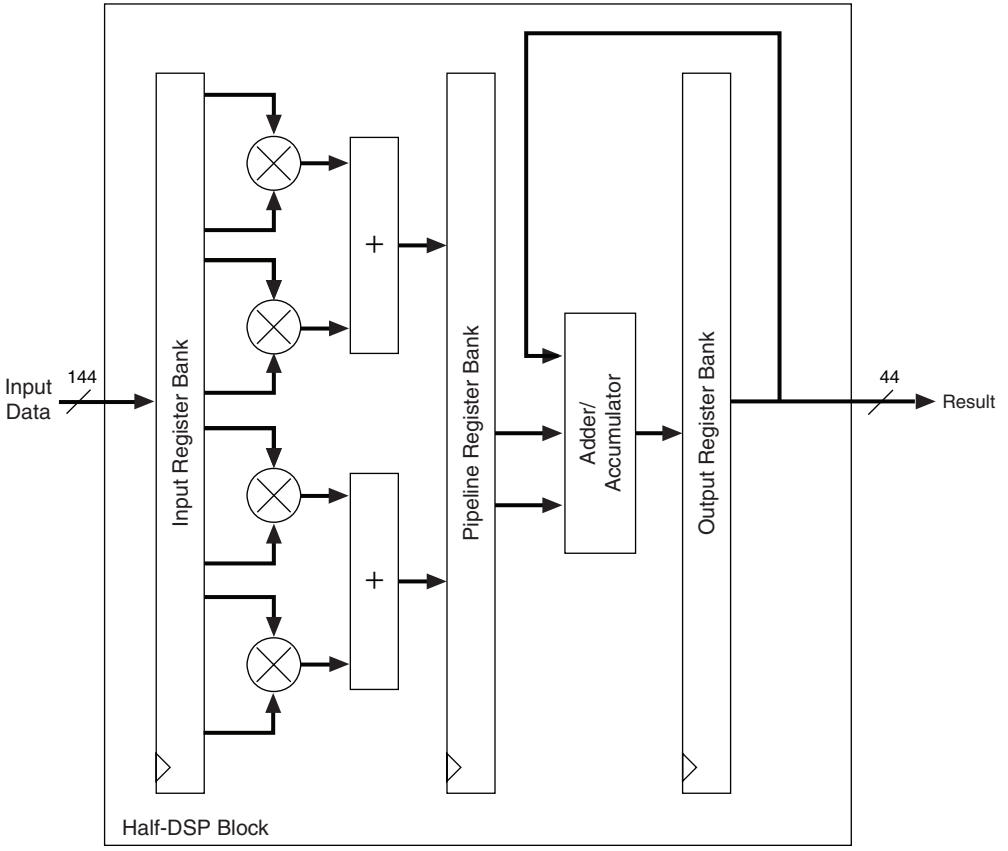
$$W_n[43..0] = W_{n-1}[43..0] \pm Z_n[37..0]$$

In these equations, *n* denotes sample time, and P[36..0] are the results from the Two-Multiplier Adder units.

Equation 5–2 provides a sum of four 18-bit × 18-bit multiplication operations (Four-Multiplier Adder), and Equation 5–3 provides a four 18-bit × 18-bit multiplication operation but with maximum of a 44-bit accumulation capability by feeding the output of the unit back to itself. This is shown in Figure 5–3.

You can bypass all register stages depending on which mode you select.

Figure 5–3. Four-Multiplier Adder and Accumulation Capability

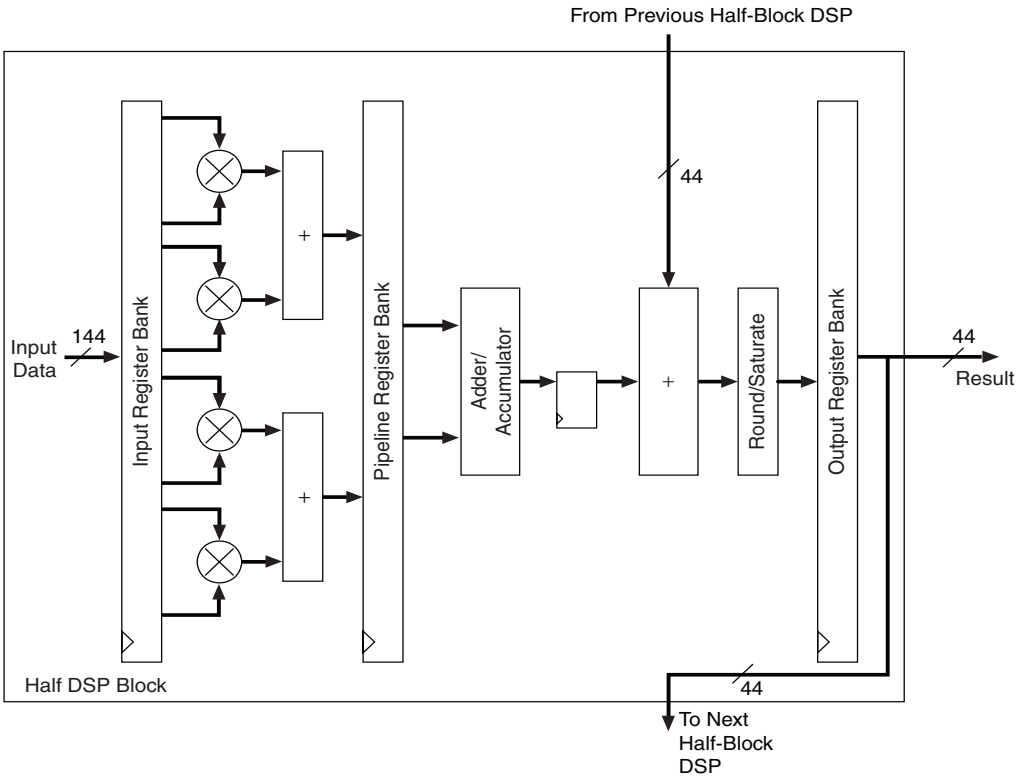


To support commonly found FIR-like structures efficiently, a major addition to the DSP block in Stratix III is the ability to propagate the result of one Half-Block to the next Half-Block completely within the DSP block without additional soft logic overhead. This is achieved by the inclusion of a dedicated addition unit and routing that adds the 44-bit result of a previous Half-Block with the 44-bit result of the current block. The 44-bit result is either fed to the next Half-Block or out of the DSP block via the output register stage. This is shown in Figure 5–4. Detailed examples are described in later sections.

The combination of a fast, low-latency Four-Multiplier Adder unit and the "chained cascade" capability of the output chaining adder provides an optimal FIR and vector multiplication capability.

To support single-channel type FIR filters efficiently, you can configure one of the multiplier input's registers to form a tap delay line input, saving resources and providing higher system performance.

Figure 5–4. Output Cascading Feature for FIR Structures

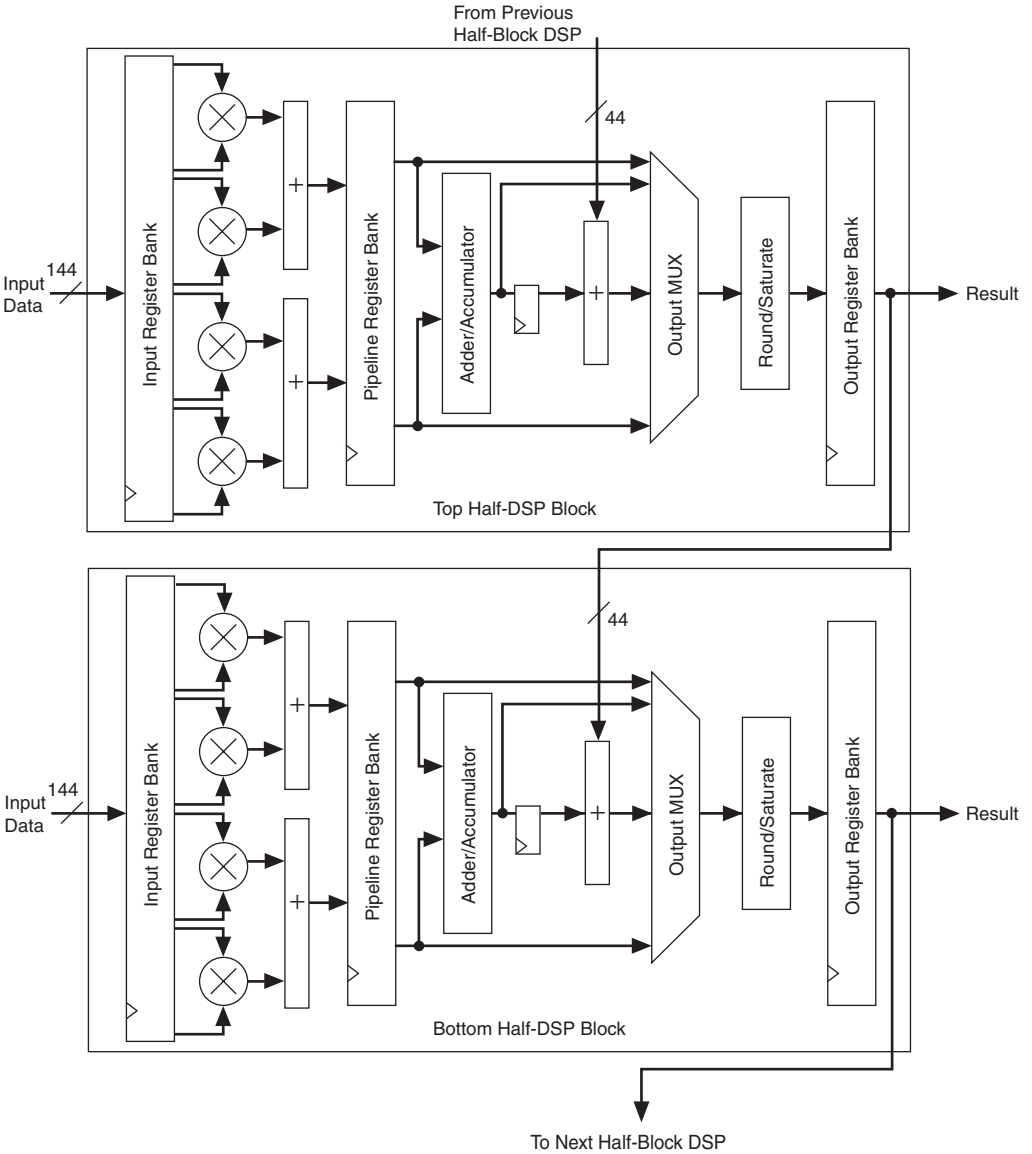


Also shown in Figure 5–4 is the optional Rounding and Saturation Unit (RSU). This unit provides a rich set of commonly found arithmetic round and saturation functions used in signal processing.

In addition to the independent multipliers and sum modes, you can use the DSP blocks to perform shift operations. The DSP block can dynamically switch between logical shift left / right, arithmetic shift left / right, and rotation operation in one clock cycle.

A top-level view of the Stratix III DSP block is shown in Figure 5–5. A more detailed diagram is shown in Figure 5–6.

Figure 5–5. Stratix III Full DSP Block Summary



Operational Modes Overview

Each Stratix III DSP block can be used in one of five basic operational modes. Table 5–2 shows the five basic operational modes and the number of multipliers that can be implemented within a single DSP block, depending on the mode.

Table 5–2. Stratix III DSP Block Operation Modes

Mode	Multiplier in Width	# of Mults	# per Block	Signed or Unsigned	RND, SAT	In Shift Register	Chainout Adder	1st Stage Add/Sub	2nd Stage Add/Acc
Independent Multiplier	9-bits	1	8	Both	No	No	No	—	—
	12-bits	1	6	Both	No	No	No	—	—
	18-bits	1	4	Both	Yes	Yes	No	—	—
	36-bits	1	2	Both	No	No	No	—	—
	Double	1	2	Both	No	No	No	—	—
Two-Multiplier Adder *(1)*	18-bits	2	4	Signed *(4)*	Yes	No	No	Both	N/A
Four-Multiplier Adder	18-bits	4	2	Both	Yes	Yes	Yes	Both	Add Only
Multiply Accumulate	18-bits	4	2	Both	Yes	Yes	Yes	Both	Both
Shift *(2)*	36-bits *(3)*	1	2	Both	No	No	—	—	—

Notes to Table 5–2:

(1) This mode also supports the loopback mode. In loopback mode, the number of loopback multipliers per DSP block is two and the remaining multipliers can be used in regular Two-Multiplier Adder mode.
(2) The dynamic shift mode supports arithmetic shift left, arithmetic shift right, logical shift left, logical shift right, and rotation operation.
(3) The dynamic shift mode operates on a 32-bit input vector but the multiplier width is configured as 36-bits.
(4) Unsigned value is also supported but you must make sure that the result can be contained within 36-bits.

The DSP block consists of two identical halves (top-half and bottom-half). Each half has four 18 × 18 multipliers.

The Quartus® II software includes megafunctions used to control the mode of operation of the multipliers. After making the appropriate parameter settings using the megafunction's MegaWizard® Plug-In Manager, the Quartus II software automatically configures the DSP block.

Stratix III DSP blocks can operate in different modes simultaneously. Each Half-block is fully independent except for the sharing of the four `clock`, `ena`, and `aclr` signals. For example, you can break down a single DSP block to operate a 9 × 9 multiplier in one Half-Block and an 18 × 18 two-multiplier adder in the other Half-Block. This increases DSP block

resource efficiency and allows you to implement more multipliers within a Stratix III device. The Quartus II software automatically places multipliers that can share the same DSP block resources within the same block.

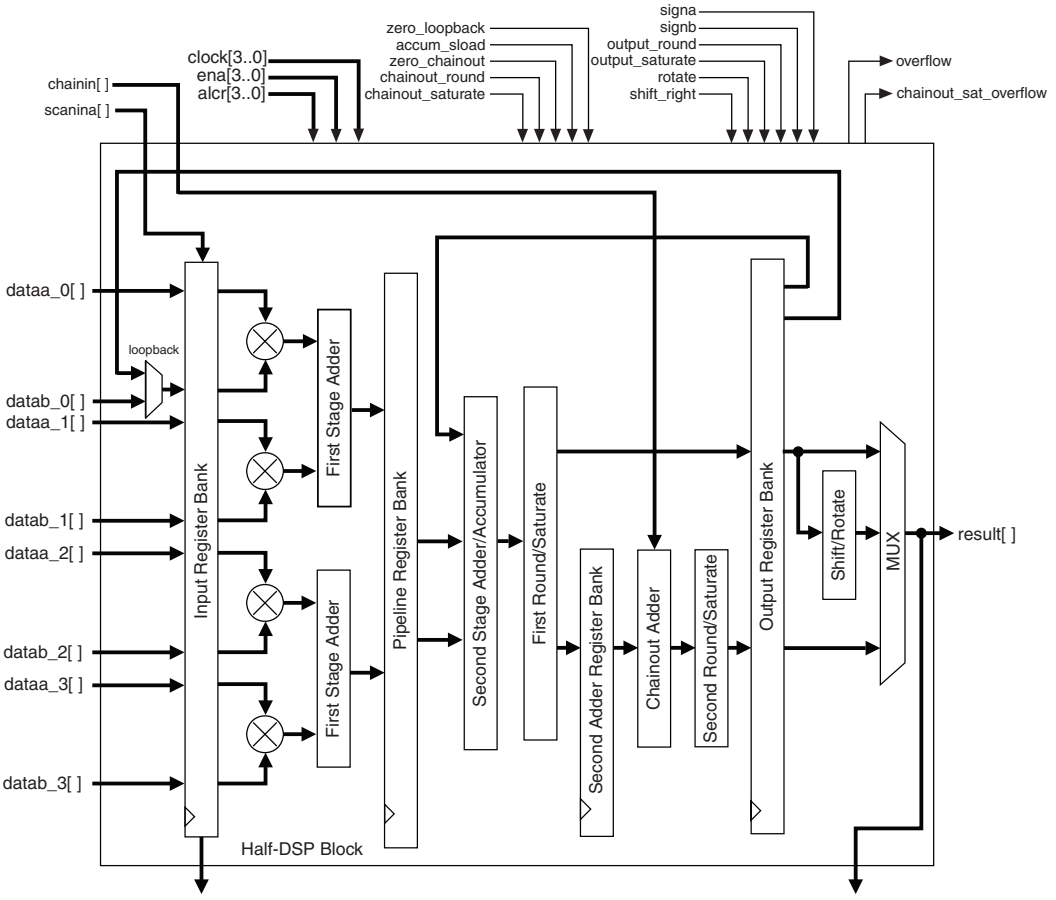
DSP Block Resource Descriptions

The DSP block consists of the following elements:

- Input register bank
- Four Two-Multiplier Adders
- Pipeline register bank
- Two second-stage adders
- Four round and saturation logic units
- Second adder register and output register bank

A detailed overall architecture of the top half of the DSP block is shown in Figure 5–6.

Figure 5–6. Half-DSP Block Architecture



Input Registers

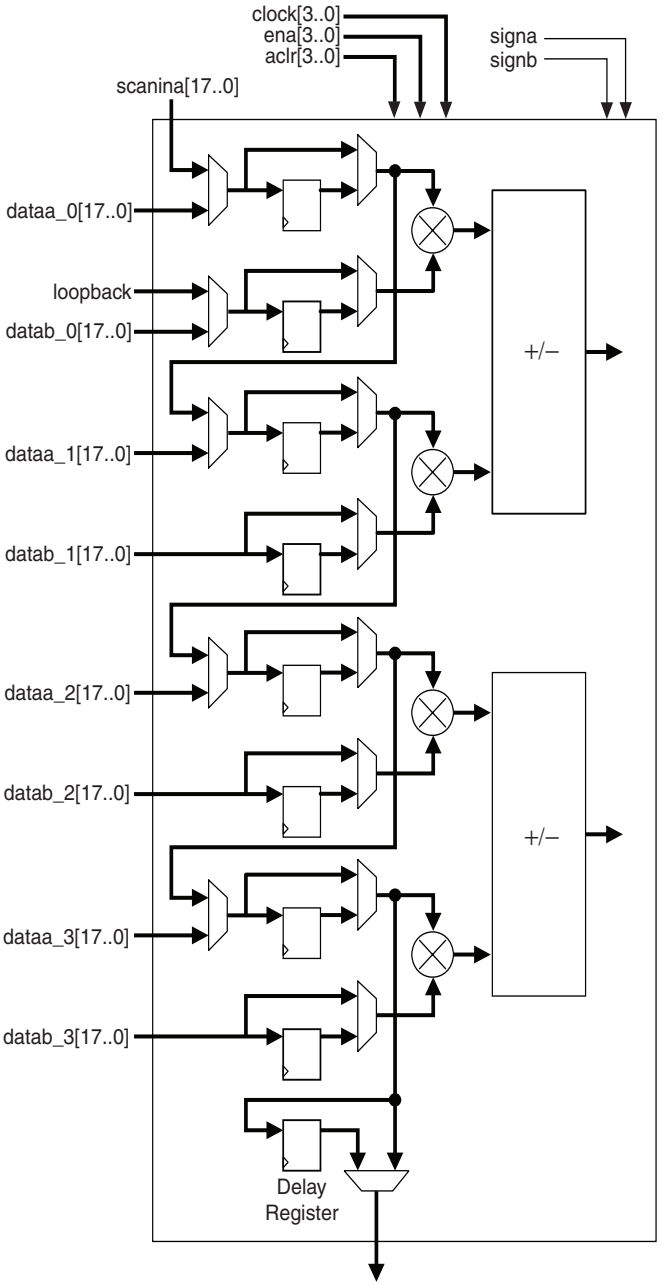
All of the DSP block registers are triggered by the positive edge of the clock signal and are cleared upon power up. Each multiplier operand can feed an input register or directly to the multiplier, bypassing the input registers. (This is configured at compile time.) The following DSP block signals control the input registers within the DSP block:

- `clock[3..0]`
- `ena[3..0]`
- `aclr[3..0]`

Every DSP block has nine 18-bit data input register banks per half DSP block. Every half DSP block has the option to use the eight data register banks as inputs to the four multipliers. The special ninth register bank is a delay register required by modes that use both the cascade and chainout features of the DSP block and is for balancing the latency requirements when using the chained cascade feature.

A feature of the input register bank is to support a tap delay line. Therefore, the top leg of the multiplier input (A) can be driven from general routing or from the cascade chain, as shown in Figure 5–7.

Figure 5–7. Input Register of Half-DSP Block



You must select whether the A-input comes from general routing or from the cascade chain at compile time. In cascade mode, the dedicated shift outputs from one multiplier block directly feeds input registers of the adjacent multiplier below it (within the same half DSP block) or the first multiplier in the next half DSP block, to form an 8-tap shift register chain per DSP Block. The DSP block can increase the length of the shift register chain by cascading to the lower DSP blocks. The dedicated shift register chain spans a single column, but you can implement longer shift register chains requiring multiple columns using the regular FPGA routing resources.

Shift registers are useful in DSP functions such as FIR filters. When implementing 18 × 18 or smaller width multipliers, you do not need external logic to create the shift register chain because the input shift registers are internal to the DSP block. This implementation significantly reduces the logical element (LE) resources required, avoids routing congestion, and results in predictable timing.

The first multiplier in every half DSP block (top- and bottom-half) in Stratix III devices has a mux for the first multiplier B-input (lower-leg input) register to select between general routing and loopback, as shown in Figure 5–6. In loopback mode, the most significant 18-bit registered outputs are connected as feedback to the multiplier input of the first top multiplier in each half DSP block. Loopback modes are used by recursive filters where the previous output is needed to compute the current output.

The loopback mode is described in detail in "Two-Multiplier Adder Sum Mode" on page 5–25.

Table 5–3 shows the summary of input register modes for the DSP block.

Table 5–3. Input Register Modes

Register Input Mode *(1)*	9 × 9	12 × 12	18 × 18	36 × 36	Double
Parallel input	✓	✓	✓	✓	✓
Shift register input *(2)*	—	—	✓	—	—
Loopback input *(3)*	—	—	✓	—	—

Notes to Table 5–3:
(1) The multiplier operand input wordlengths are statically configured at compile time.
(2) Available only on the A-operand.
(3) Only one loopback input is allowed per Half-Block. See Figure 5–15 for details.

Multiplier and First-Stage Adder

The multiplier stage natively supports 9 × 9, 12 × 12, 18 × 18, or 36 × 36 multipliers. Other wordlengths are padded up to the nearest appropriate native wordlength; for example, 16 × 16 would be padded up to use 18 × 18. Refer to "Independent Multiplier Modes" on page 5–18 for more details. Depending on the data width of the multiplier, a single DSP block can perform many multiplications in parallel.

Each multiplier operand can be a unique signed or unsigned number. Two dynamic signals, `signa` and `signb`, control the representation of each operand, respectively. A `logic 1` value on the `signa/signb` signal indicates that `data A/data B` is a signed number; a `logic 0` value indicates an unsigned number. Table 5–4 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 5–4. Multiplier Sign Representation

Data A (signa Value)	Data B (signb Value)	Result
Unsigned (logic 0)	Unsigned (logic 0)	Unsigned
Unsigned (logic 0)	Signed (logic 1)	Signed
Signed (logic 1)	Unsigned (logic 0)	Signed
Signed (logic 1)	Signed (logic 1)	Signed

Each Half Block has its own `signa` and `signb` signal. Therefore, all of the `data A` inputs feeding the same DSP Half Block must have the same sign representation. Similarly, all of the `data B` inputs feeding the same DSP Half Block must have the same sign representation. The multiplier offers full precision regardless of the sign representation in all operational modes except for full precision 18 x 18 loopback and Two-Multiplier Adder modes. Refer to "Two-Multiplier Adder Sum Mode" on page 5–25 for details.

When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

The outputs of the multipliers are the only outputs that can feed into the first-stage adder, as shown in Figure 5–6. There are four first-stage adders in a DSP block (two adders per half DSP block). The first-stage adder block has the ability to perform addition and subtraction. The control signal for addition or subtraction is static and has to be configured upon

compile time. The first-stage adders are used by the sum modes to compute the sum of two multipliers, 18 × 18-complex multipliers, and to perform the first stage of a 36 × 36 multiply and shift operation.

Depending on your specifications, the output of the first-stage adder has the option to feed into the pipeline registers, second-stage adder, round and saturation unit, or the output registers.

Pipeline Register Stage

The output from the first-stage adder can either feed or bypass the pipeline registers, as shown in Figure 5–6. Pipeline registers increase the DSP block's maximum performance (at the expense of extra cycles of latency), especially when using the subsequent DSP block stages. Pipeline registers split up the long signal path between the input-registers / multiplier / first-stage adder and the second-stage adder / round-and-saturation / output-registers, creating two shorter paths.

Second-Stage Adder

There are four individual 44-bit second-stage adders per DSP block (2 adders per half DSP block). You can configure the second-stage adders as follows:

- The final stage of a 36-bit multiplier
- A sum of four (18 × 18)
- An accumulator (44-bits maximum)
- A chained output summation (44-bits maximum)

The chained-output adder can be used at the same time as a second-level adder in chained output summation mode.

The output of the second-stage adder has the option to go into the round and saturation logic unit or the output register.

You cannot use the second-stage adder independently from the multiplier and first-stage adder.

Round and Saturation Stage

The round and saturation logic units are located at the output of the 44-bit second-stage adder (round logic unit followed by the saturation logic unit). There are two round and saturation logic units per half DSP block. The input to the round and saturation logic unit can come from one of the following stages:

- Output of the multiplier (independent multiply mode in 18 × 18)
- Output of the first-stage adder (Two-Multiplier Adder)
- Output of the pipeline registers
- Output of the second-stage adder (Four-Multiplier Adder, Multiply-Accumulate Mode in 18 × 18)

These stages are discussed in detail in "Operational Mode Descriptions" on page 5–18.

The round and saturation logic unit is controlled by the dynamic round and saturate signals, respectively. A `logic 1` value on the round and / or saturate enables the round and / or saturate logic unit, respectively.

You can use the round and saturation logic units together or independently.

Second Adder and Output Registers

The second adder register and output register banks are two banks of 44-bit registers that can also be combined to form larger 72-bit banks to support 36 × 36 output results.

The outputs of the different stages in the Stratix III devices are routed to the output registers through an output selection unit. Depending on the operational mode of the DSP block, the output selection unit selects whether the outputs of the DSP blocks comes from the outputs of the multiplier block, first-stage adder, pipeline registers, second-stage adder, or the round and saturation logic unit. The output selection unit is set automatically by the software, based on the DSP block operational mode you specified, and has the option to either drive or bypass the output registers. The exception is when the block is used in shift mode, in which case the user dynamically controls the output-select MUX directly.

When the DSP block is configured in "chained cascaded" output mode, both of the second-stage adders are used. The first one is used for performing Four-Multiplier Adder and the second is used for the chainout adder. The outputs of the Four-Multiplier Adder are routed to the second-stage adder registers before it enters the chainout adder. The output of the chainout adder goes to the regular output register bank.

Depending on the configuration, the chainout results can be routed to the input of the next half-block's chainout adder input or to the general fabric (functioning as regular output registers). Refer to "Operational Mode Descriptions" on page 5–18 for details.

The second-stage and output registers are triggered by the positive edge of the clock signal and are cleared on power up. The following DSP block signals control the output registers within the DSP block:

- clock[3..0]
- ena[3..0]
- aclr[3..0]

Operational Mode Descriptions

Independent Multiplier Modes

In independent input and output multiplier mode, the DSP block performs individual multiplication operations for general-purpose multipliers.

9-, 12- and 18-Bit Multiplier

You can configure each DSP block multiplier for 9-, 12-, or 18-bit multiplication. A single DSP block can support up to eight individual 9 × 9 multipliers, six 12 × 12 multipliers, or up to four individual 18 × 18 multipliers. For operand widths up to 9 bits, a 9 × 9 multiplier is implemented. For operand widths from 10 to 12 bits, a 12 × 12 multiplier is implemented, and for operand widths from 13 to 18 bits, an 18 × 18 multiplier is implemented. This is done by the Quartus II software by zero-padding the LSBs. Figures 5–8, 5–9, and 5–10 show the DSP block in the independent multiplier operation mode.

Figure 5–8. 18-Bit Independent Multiplier Mode Shown for Half-DSP Block

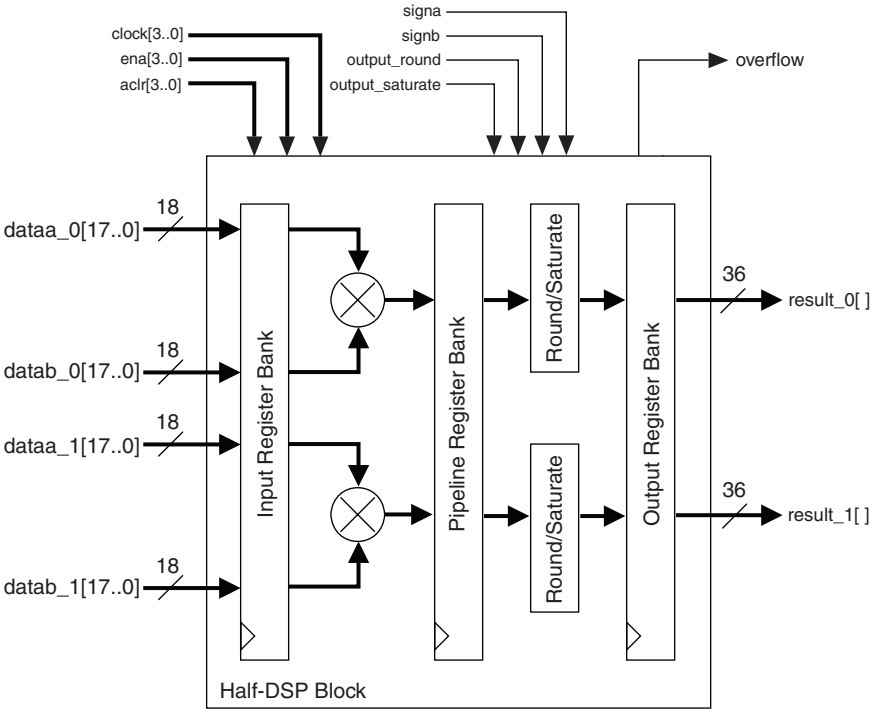


Figure 5–9. 12-Bit Independent Multiplier Mode Shown for Half-DSP Block

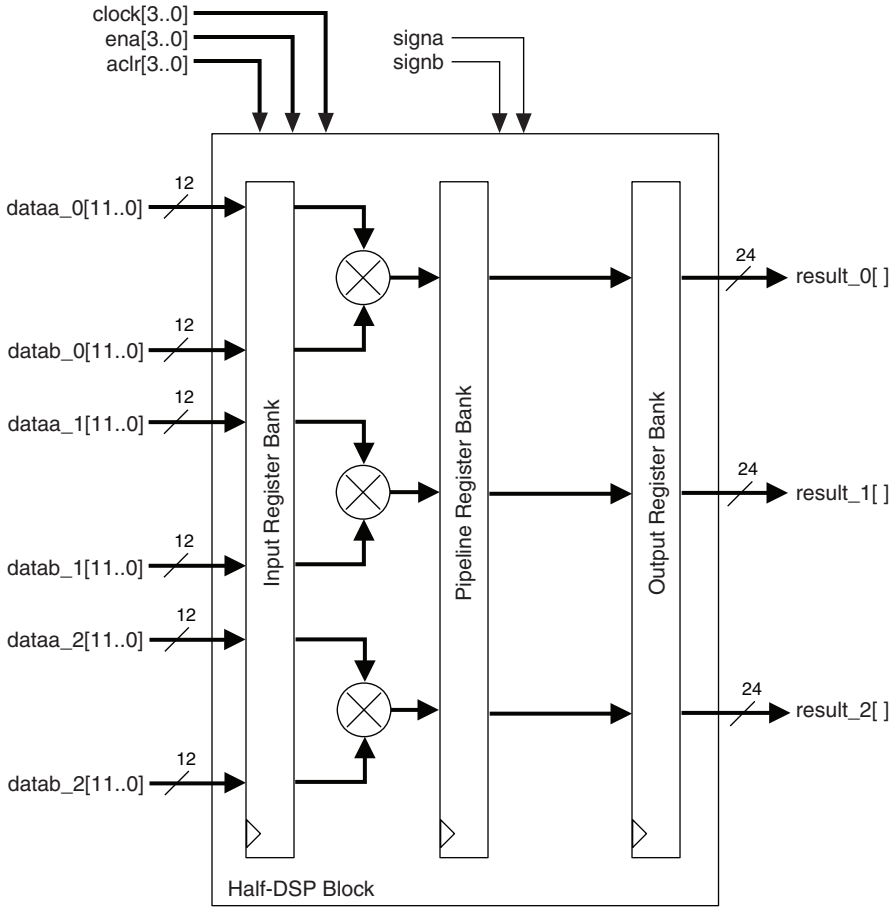
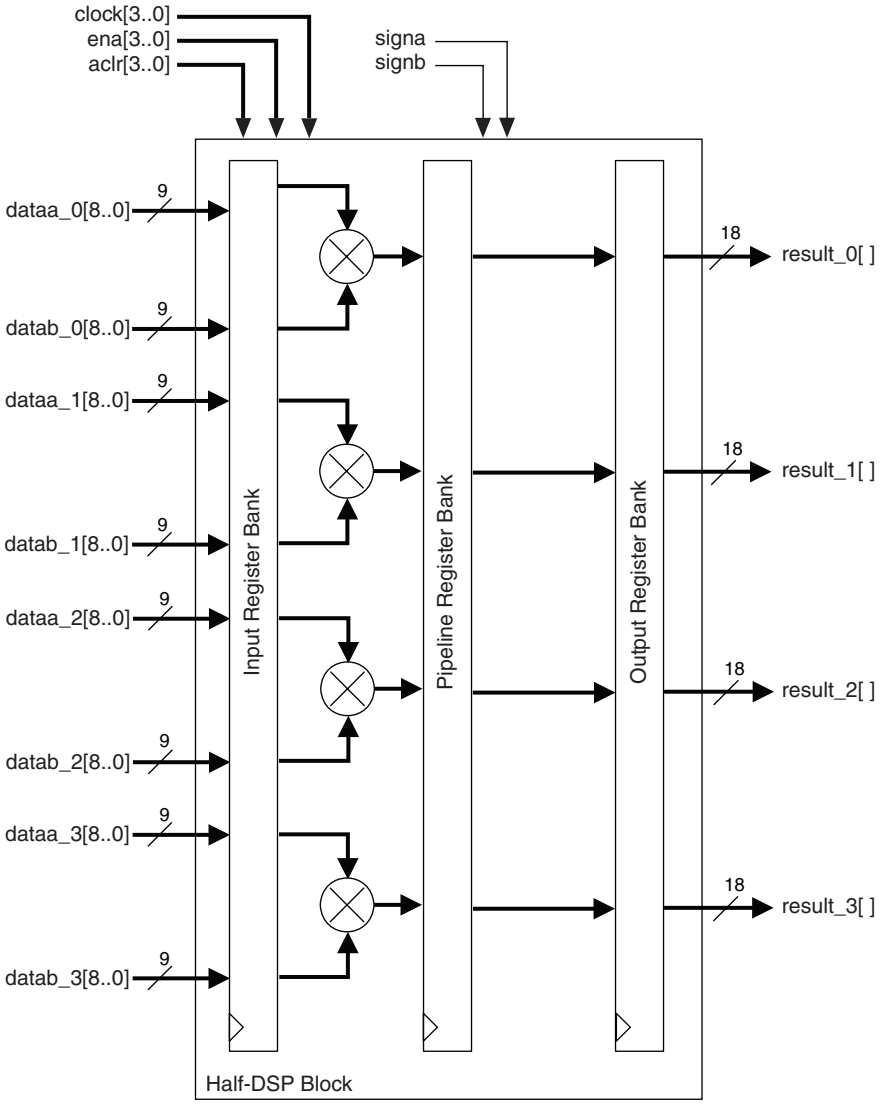


Figure 5–10. 9-Bit Independent Multiplier Mode Shown for Half-Block



The multiplier operands can accept signed integers, unsigned integers, or a combination of both. You can change the `signa` and `signb` signals dynamically and can be registered in the DSP block. Additionally, the

multiplier inputs and result can be registered independently. You can use the pipeline registers within the DSP block to pipeline the multiplier result, increasing the performance of the DSP block.

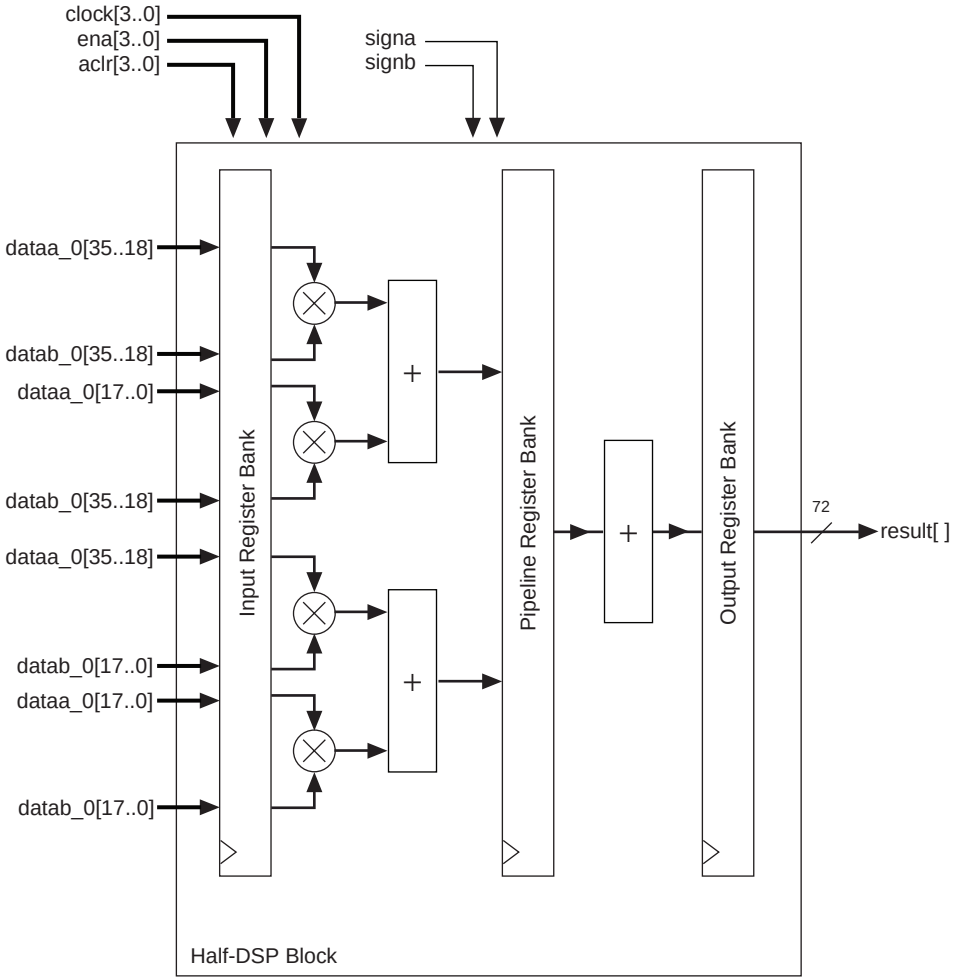
The round and saturation logic unit is supported for the 18-bit independent multiplier mode only.

36-Bit Multiplier

You can efficiently construct a 36 × 36 multiplier using four 18 × 18 multipliers. This simplification fits conveniently into one half-DSP block, and is implemented in the DSP block automatically by selecting the 36 × 36 mode. Stratix III devices can have up to two 36-bit multipliers per DSP block (one 36-bit multiplier per half DSP block). The 36-bit multiplier is also under the independent multiplier mode but uses the entire half DSP block, including the dedicated hardware logic after the pipeline registers to implement the 36 × 36 bit multiplication operation. This is shown in Figure 5–11.

The 36-bit multiplier is useful for applications requiring more than 18-bit precision; for example, for the mantissa multiplication portion of single precision and extended single precision floating-point arithmetic applications.

Figure 5–11. 36-Bit Independent Multiplier Mode Shown for Half-DSP Block



Double Multiplier

The Stratix III DSP block can be configured to efficiently support an unsigned 54 × 54 bit multiplier that is required to compute the mantissa portion of an IEEE double precision floating point multiplication. A 54 × 54 bit multiplier can be built using basic 18 × 18 multipliers, shifters and adders. In order to efficiently utilize the Stratix III DSP block's built

in shifters and adders, a special Double mode (partial 54 × 54 multiplier) is available that is a slight modification to the basic 36 × 36 Multiplier mode. This is shown in Figure 5–12 and Figure 5–13.

Figure 5–12. Double Mode Shown for Half-DSP Block

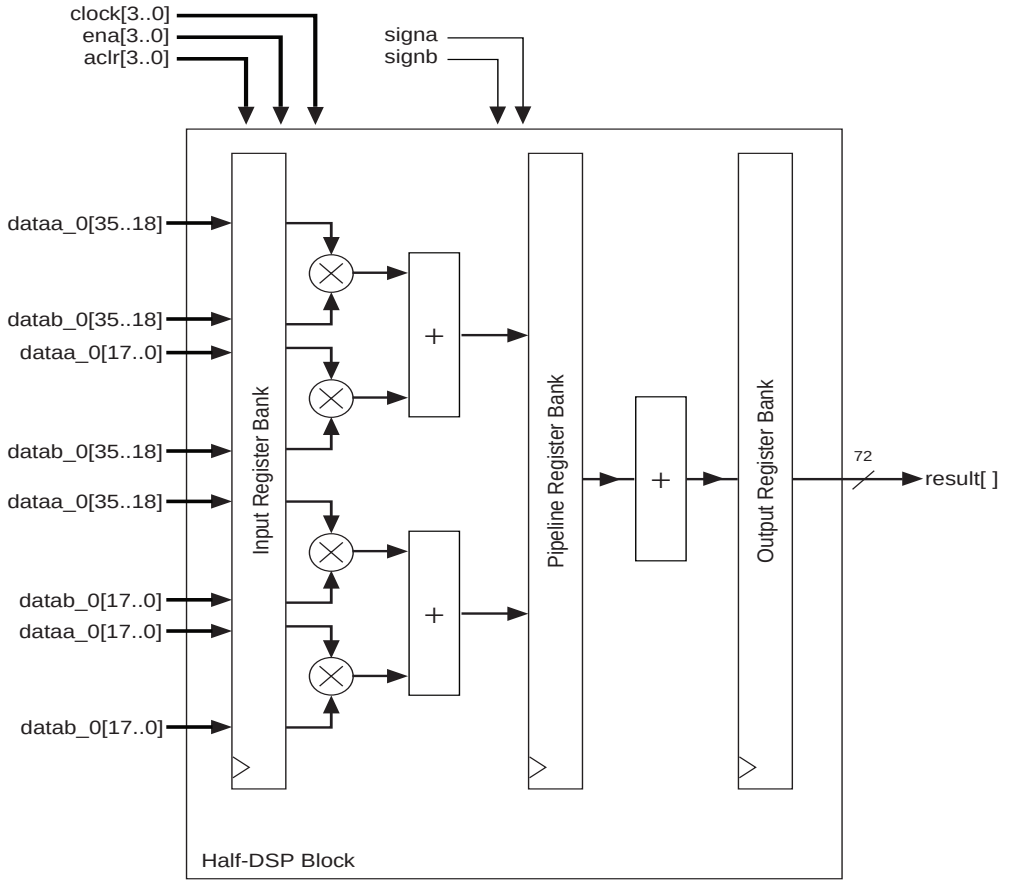
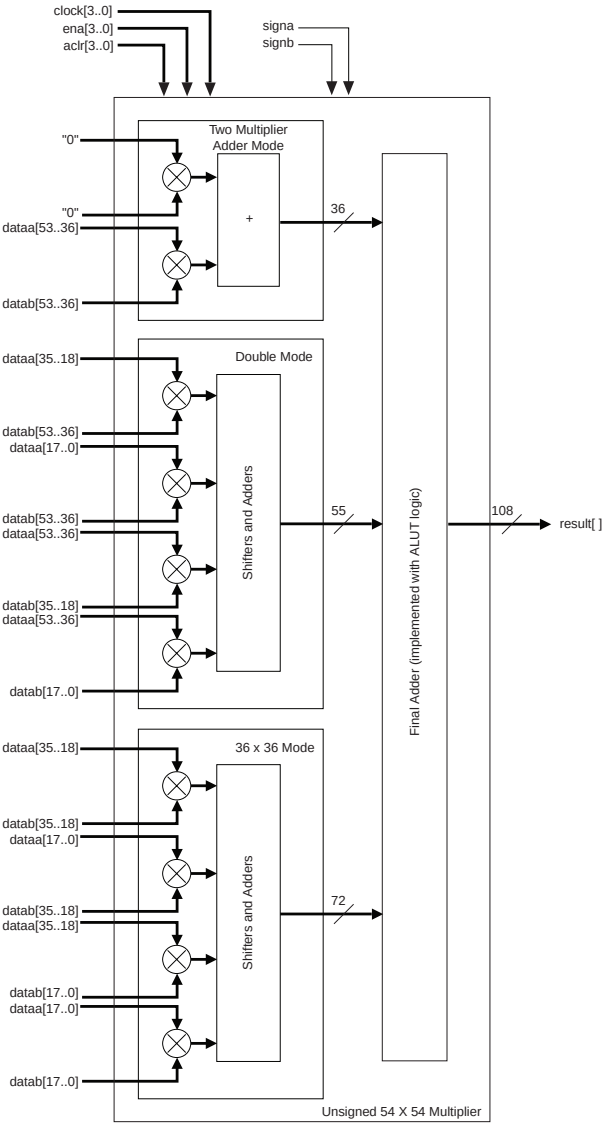


Figure 5–13. Unsigned 54 × 54 Multiplier



Two-Multiplier Adder Sum Mode

In the two-multiplier adder configuration, the DSP block can implement four 18-bit Two-Multiplier Adders (2 Two-Multiplier Adders per half DSP block). You can configure the adders to take the sum or difference of

two multiplier outputs. Summation or subtraction has to be selected at compile time. The Two-Multiplier Adder function is useful for applications such as FFTs, complex FIR, and IIR filters. Figure 5–14 shows the DSP block configured in the two-multiplier adder mode.

The loopback mode is the other sub-feature of the two-multiplier adder mode. Figure 5–15 shows the DSP block configured in the loopback mode. This mode takes the 36-bit summation result of the two multipliers and feeds back the most significant 18-bits to the input. The lower 18-bits are discarded. You have the option to disable or zero-out the loopback data by using the dynamic `zero_loopback` signal. A `logic 1` value on the `zero_loopback` signal selects the `zeroed` data or disables the looped back data, while a `logic 0` selects the looped back data.

The option to use the loopback mode or the general two-multiplier adder mode must be selected at compile time.

For the Two-Multiplier Adder mode, if all the inputs are full 18-bit and unsigned, the result will require 37 bits. As the output data width in Two-Multiplier Adder mode is limited to 36 bits, this 37-bit output requirement is not allowed. Any other combination that does not violate the 36-bit maximum result is permitted; for example, two 16 × 16 signed Two-Multiplier Adders is valid.

The two-multiplier adder mode supports the round and saturation logic unit. You can use the pipeline registers and output registers within the DSP block to pipeline the multiplier-adder result, increasing the performance of the DSP block.

Figure 5–14. Two-Multiplier Adder Mode Shown for Half-DSP Block

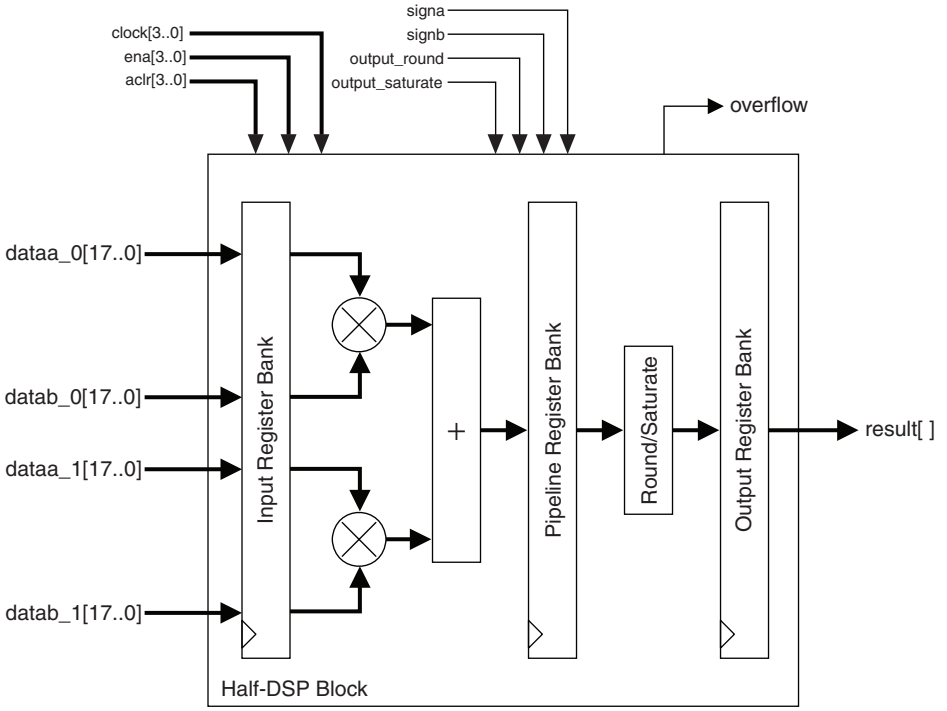
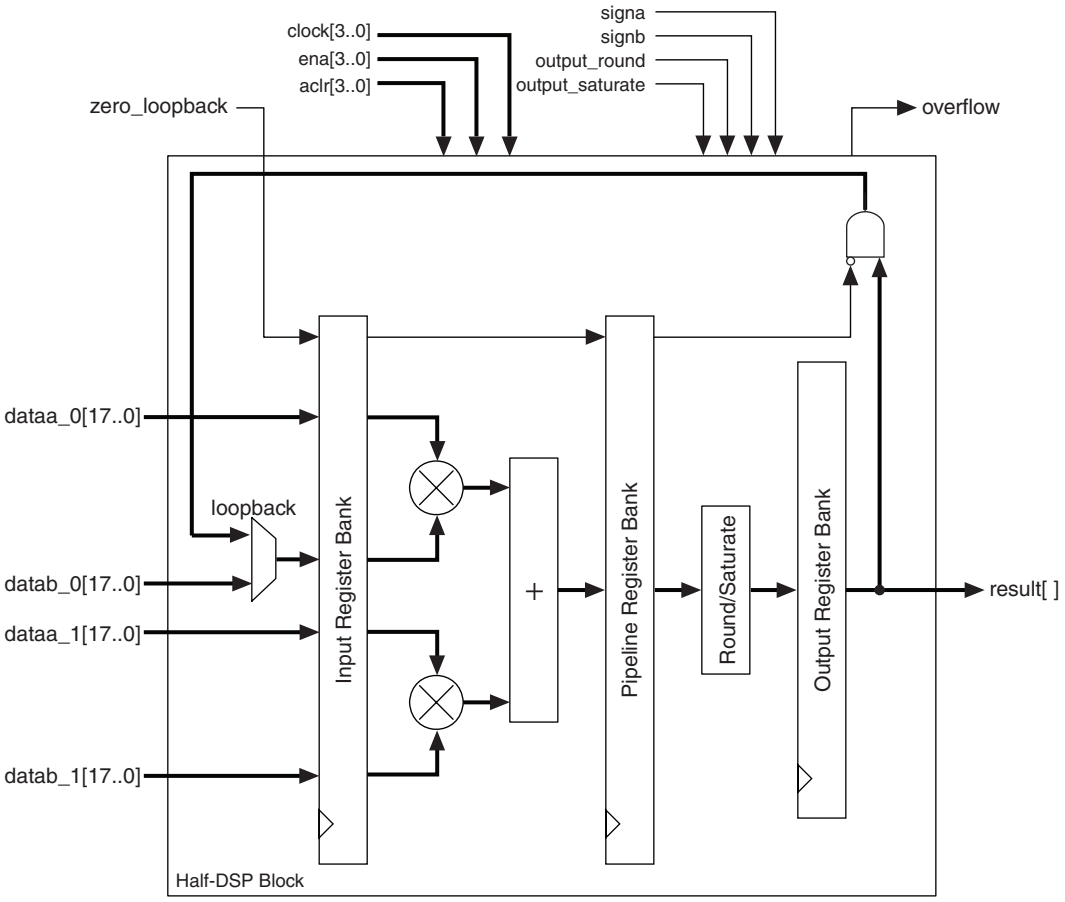


Figure 5–15. Loopback Mode for Half-DSP Block



18 × 18 Complex Multiply

You can configure the DSP block when used in Two-Multiplier Adder mode to implement complex multipliers using the two-multiplier adder mode. A single half DSP block can implement one 18-bit complex multiplier.

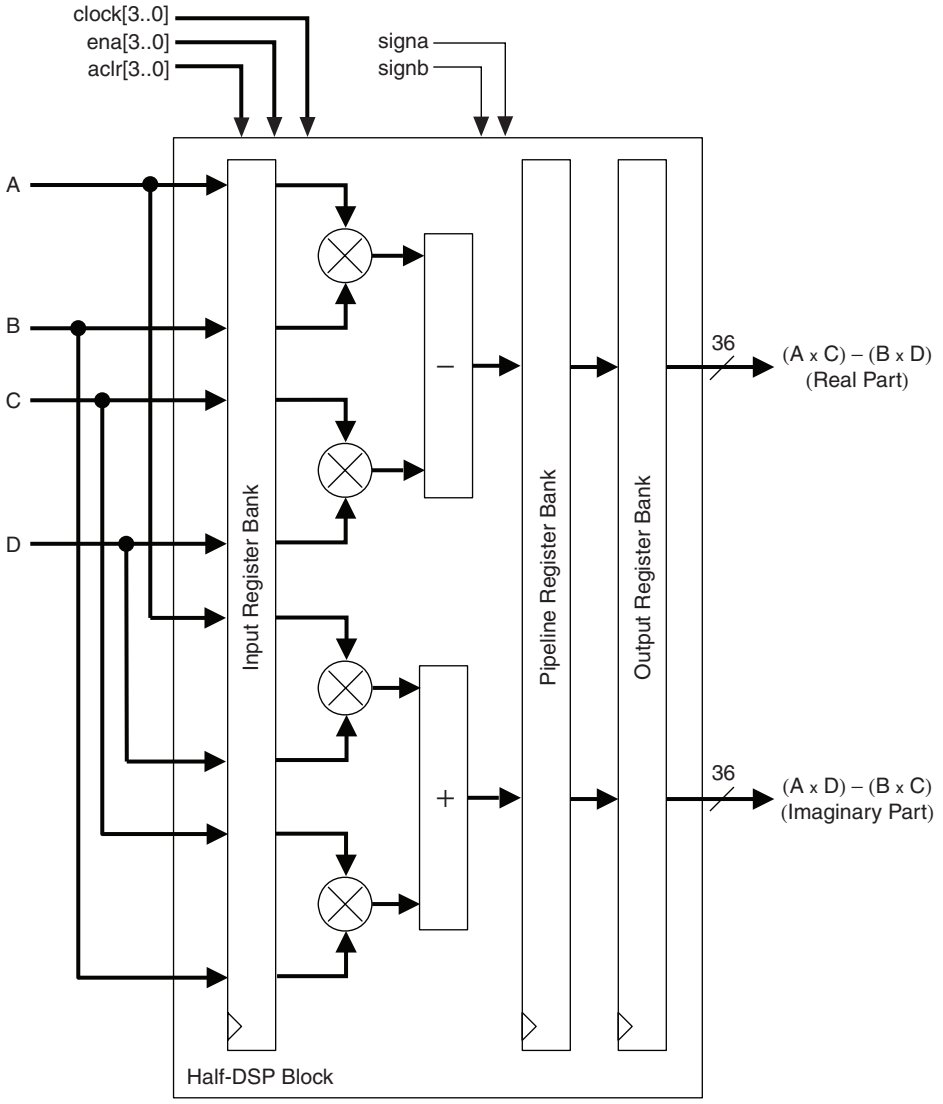
A complex multiplication can be written as shown in Equation 5–4.

Equation 5–4. Complex Multiplication Equation

$$(a + jb) \times (c + jd) = ((a \times c)) – (b \times d)) + j((a \times d) + (b \times c))$$

To implement this complex multiplication within the DSP block, the real part ((a × c) – (b × d)) is implemented using two multipliers feeding one subtractor block while the imaginary part ((a × d) + (b × c)) is implemented using another two multipliers feeding an adder block. Figure 5–16 shows an 18-bit complex multiplication. This mode automatically assumes all inputs are using signed numbers.

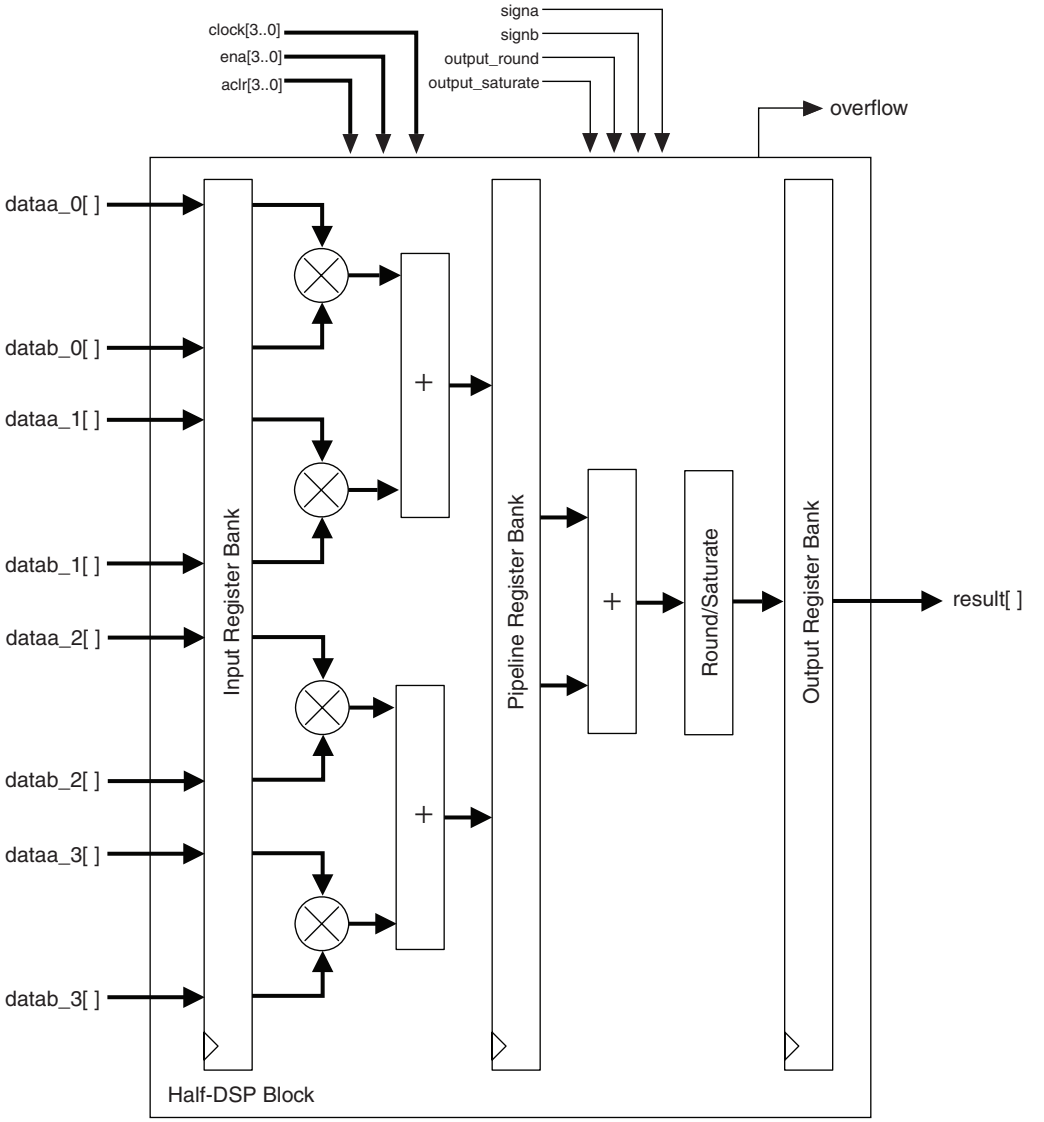
Figure 5–16. Complex Multiplier Using Two-Multiplier Adder Mode



Four-Multiplier Adder

In the four-multiplier adder configuration shown in Figure 5–17, the DSP block can implement two four-multiplier adders (one four-multiplier adder per half DSP block). These modes are useful for implementing one-dimensional and two-dimensional filtering applications. The four-multiplier adder is performed in two addition stages. The outputs of two of the four multipliers are initially summed in the two first-stage adder blocks. The results of these two adder blocks are then summed in the second-stage adder block to produce the final four-multiplier adder result, as shown by Equation 5–2 and Equation 5–3.

Figure 5–17. Four-Multiplier Adder Mode Shown for Half-DSP Block

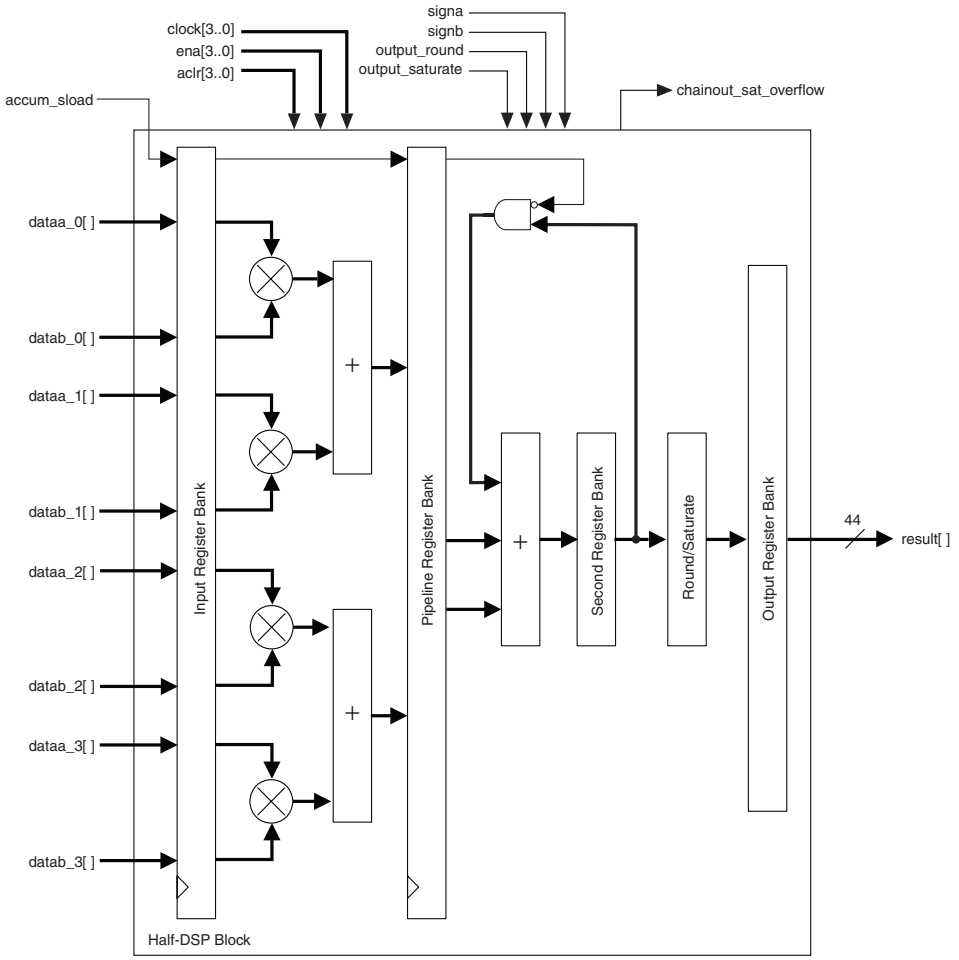


The four-multiplier adder mode supports the round and saturation logic unit. You can use the pipeline registers and output registers within the DSP block to pipeline the multiplier-adder result, increasing the performance of the DSP block.

Multiply Accumulate Mode

In multiply accumulate mode, the second-stage adder is configured as a 44-bit accumulator or subtractor. The output of the DSP block is looped back to the second-stage adder and added or subtracted with the two outputs of the first-stage adder block according to Equation 5–3. Figure 5–18 shows the DSP block configured to operate in multiply accumulate mode.

Figure 5–18. Multiply Accumulate Mode Shown for Half-DSP Block



A single DSP block can implement up to two independent 44-bit accumulators.

The dynamic accum_sload control signal is used to clear the accumulation. A logic 1 value on the accum_sload signal synchronously loads the accumulator with the multiplier result only, while a logic 0 enables accumulation by adding or subtracting the output of the DSP block (accumulator feedback) to the output of the multiplier and first-stage adder.

The control signal for the accumulator and subtractor is static and therefore has to be configured at compile time.

This mode supports the round and saturation logic unit as it is configured as an 18-bit multiplier accumulator. You can use the pipeline registers and output registers within the DSP block to increase the performance of the DSP block.

Shift Modes

Stratix III devices support the following shift modes for 32-bit input only:

- Arithmetic shift left, ASL[N]
- Arithmetic shift right, ASR[32–N]
- Logical shift left, LSL[N]
- Logical shift right, LSR[32–N]
- 32-bit rotator or Barrel shifter, ROT[N]

You can switch the shift mode between these modes using the dynamic rotate and shift control signals.

The shift mode in a Stratix III device can be easily used by the soft embedded processor such as Nios® II to perform the dynamic shift and rotate operation. Figure 5–19 shows the shift mode configuration.

The shift mode makes use of the available multipliers to logically or arithmetically shift left, right, or rotate the desired 32-bit data. The DSP block is configured like the independent 36-bit multiplier mode to perform the shift mode operations.

The arithmetic shift right requires signed input vector. During arithmetic shift right, the sign is extended to fill the MSB of the 32-bit vector. The logical shift right uses unsigned input vector. During logical shift right, zeros are padded in the most significant bits shifting the 32-bit vector to the right. The barrel shifter uses unsigned input vector and implements a rotation function on a 32-bit word length.

Two control signals `rotate` and `shift_right` together with the `signa` and `signb` signals, determining the shifting operation. Examples of shift operations are shown in Table 5–5.

Figure 5–19. Shift Operation Mode Shown for Half-DSP Block

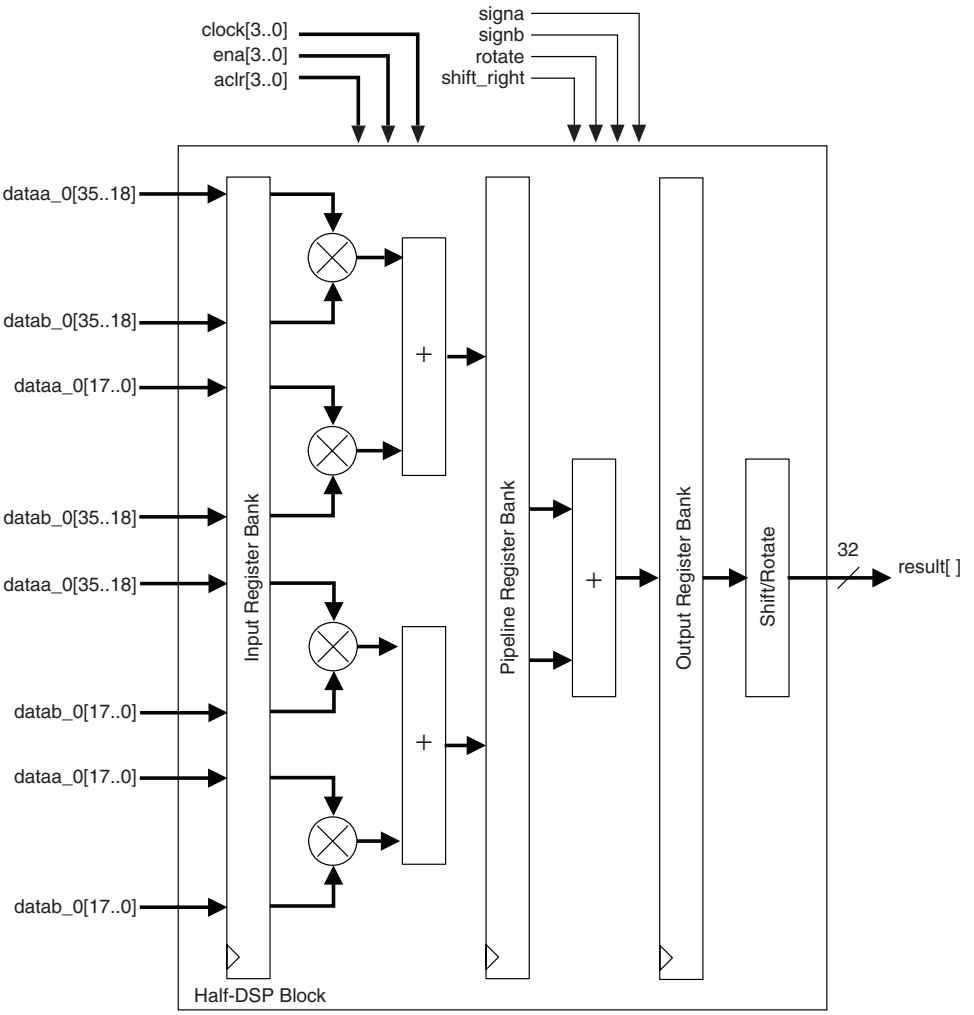


Table 5–5. Examples of Shift Operations

Example	Signa	Signb	Shift	Rotate	A-input	B-input	Result
Logical Shift Left LSL[N]	Unsigned	Unsigned	0	0	0xAABBCCDD	0x0000100	0xBBCCDD00
Logical Shift Right LSR[32-N]	Unsigned	Unsigned	1	0	0xAABBCCDD	0x0000100	0x000000AA
Arithmetic Shift Left ASL[N]	Signed	Unsigned	0	0	0xAABBCCDD	0x0000100	0xBBCCDD00
Arithmetic Shift Right ASR[32-N]	Signed	Unsigned	1	0	0xAABBCCDD	0x0000100	0xFFFFFFAA
Rotation ROT[N]	Unsigned	Unsigned	0	1	0xAABBCCDD	0x0000100	0xBBCCDDAA

Rounding and Saturation Mode

Round and saturation functions are often required in DSP arithmetic. Rounding is used to limit bit growth and its side effects and saturation is used to reduce overflow and underflow side effects.

Two rounding modes are supported in Stratix III devices:

- Round-to-nearest-integer mode
- Round-to-nearest-even mode

You must select one of the two options at compile time.

Round-to-nearest-integer provides the biased rounding support and is the simplest form of rounding commonly used in DSP arithmetic. The round-to-nearest-even method provides unbiased rounding support and is used where DC offsets are a concern. Table 5–6 shows how round-to-nearest-even works. Examples of the difference between the two modes are shown in Table 5–7. In this example, a 6-bit input is rounded to 4 bits. You can observe from Table 5–7 that the main difference between the two rounding options is when the residue bits are exactly half way between its nearest two integers and the LSB is zero (even).

Table 5–6. Example of Round-To-Nearest-Even Mode

6- to 4-bits Rounding	Odd/Even (Integer)	Fractional	Add to Integer	Result
010111	x	> 0.5 (11)	1	0110
001101	x	< 0.5 (01)	0	0011
001010	Even (0010)	= 0.5 (10)	0	0010
001110	Odd (0011)	= 0.5 (10)	1	0100
110111	x	> 0.5 (11)	1	1110
101101	x	< 0.5 (01)	0	1011
110110	Odd (1101)	= 0.5 (10)	1	1110
110010	Even (1100)	= 0.5 (10)	0	1100

Table 5–7. Comparison of Round-to-Nearest-Integer and Round-to-Nearest-Even

Round-To-Nearest-Integer	Round-To-Nearest-Even
010111 ⇒0110	010111 ⇒0110
001101 ⇒0011	001101 ⇒0011
001010 ⇒0011	001010 ⇒0010
001110 ⇒0100	001110 ⇒0100
110111 ⇒1110	110111 ⇒1110
101101 ⇒1011	101101 ⇒1011
110110 ⇒1110	110110 ⇒1110
110010 ⇒1101	110010 ⇒1100

Two saturation modes are supported in Stratix III:

- Asymmetric saturation mode
- Symmetric saturation mode

You must select one of the two options at compile time.

In 2's complement format, the maximum negative number that can be represented is $-2^{(n-1)}$ while the maximum positive number is $2^{(n-1)}-1$. Symmetrical saturation will limit the maximum negative number to $-2^{(n-1)} + 1$. For example, for 32 bits:

- Asymmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000000
- Symmetric 32-bit saturation: Max = 0x7FFFFFFF, Min = 0x80000001

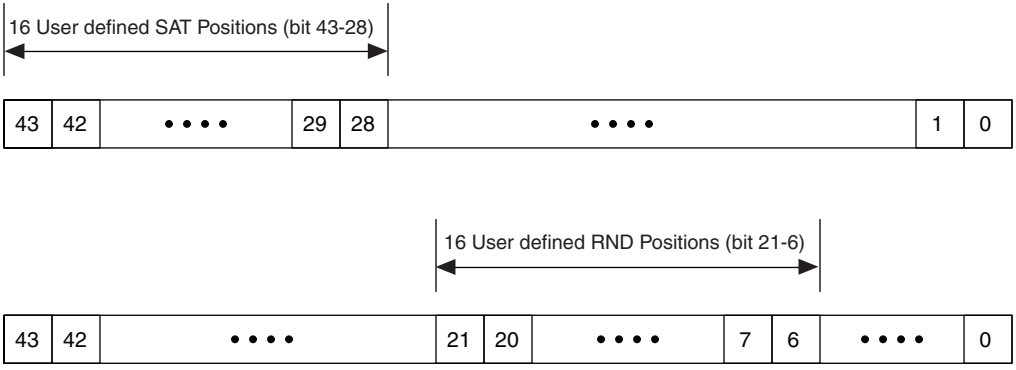
Table 5–8 shows how the saturation works. In this example, a 44-bit input is saturated to 36-bits.

Table 5–8. Examples of Saturation

44 to 36 Bits Saturation	Symmetric SAT Result	Asymmetric SAT Result
5926AC01342h	7FFFFFFFh	7FFFFFFFh
ADA38D2210h	800000001h	800000000h

Stratix III devices have up to 16 configurable bit positions out of the 44-bit bus (`[43:0]`) for the round and saturate logic unit providing higher flexibility. You must select the 16 configurable bit positions at compile time. These 16-bit positions are located at bits `[21:6]` for rounding and `[43:28]` for saturation, as shown in Figure 5–20.

Figure 5–20. Round and Saturation Locations



For symmetric saturation, the RND bit position is also used to determine where the LSP for the saturated data is located.

You can use the rounding and saturation function described above in regular supported multiplication operations as specified in Table 5–2. However, for accumulation type operations, the following convention is used.

The functionality of the round logic unit is in the format of:

Result = RND[Σ(A × B)], when used for an accumulation type of operation.

Likewise, the functionality of the saturation logic unit is in the format of:

Result = SAT[Σ(A × B)], when used for an accumulation type of operation.

If both the round and saturation logic units are used for an accumulation type of operation, the format is:

Result = SAT[RND[Σ(A × B)]]

DSP Block Control Signals

The Stratix III DSP block is configured using a set of static and dynamic signals. The DSP block dynamic signals are user configurable and can be set to toggled or not at run time. This list of dynamic signals is shown in Table 5–9 for the DSP block.

Table 5–9. DSP Block Dynamic Signals (Part 1 of 2)

Signal Name	Function	Count
• signa • signb	Signed/unsigned control for all multipliers and adders. signa for "multiplicand" input bus to dataa[17:0] each multiplier. signb for "multiplier" input bus datab[17:0] to each multiplier. signa = 1, signb = 1 for signed-signed multiplication signa = 1, signb = 0 for signed-unsigned multiplication signa = 0, signb = 1 for unsigned-signed multiplication signa = 0, signb = 0 for unsigned-unsigned multiplication	2
output_round	Round control for first stage round/saturation block. output_round = 1 for rounding on multiply output output_round = 0 for normal multiply output	1

Table 5–9. DSP Block Dynamic Signals (Part 2 of 2)

Signal Name	Function	Count
chainout_round	Round control for second stage round/saturation block. chainout_round = 1 for rounding on multiply output chainout_round = 0 for normal multiply output	1
output_saturate	Saturation control for first stage round/saturation block for Q-format multiply. If both rounding and saturation is enabled, saturation is done on the rounded result. output_saturate = 1 for saturation support output_saturate = 0 for no saturation support	1
chainout_saturate	Saturation control for second stage round/saturation block for Q-format multiply. If both rounding and saturation's enabled, saturation is done on the rounded result. chainout_saturate = 1 for saturation support chainout_saturate = 0 for no saturation support	1
accum_sload	Dynamically specifies whether the accumulator value is zero. accum_sload = 0, accumulation input is from the output registers accum_sload = 1, accumulation input is set to be zero	1
zero_chainout	Dynamically specifies whether the chainout value is zero.	1
zero_loopback	Dynamically specifies whether the loopback value is zero.	1
rotate	rotation = 1, rotation feature is enabled	1
shift_right	shift_right = 1, shift right feature is enabled	1
	Total Signals per Half-block	**11**
clock0 clock1 clock2 clock3	DSP-block-wide clock signals	4
ena0 ena1 ena2 ena3	Input and Pipeline Register enable signals	4
aclr0 aclr1 aclr2 aclr3	DSP block-wide asynchronous clear signals (active low).	4
	Total Count per Full Block	**34**

Application Examples

FIR Example

A finite impulse response filter is a common function used in many systems to perform spectral manipulations. The basic form is shown in Equation 5–5.

Equation 5–5. Finite Impulse Response FIter Equation

$$y(n) = \sum_{k=0}^{N-1} x(n-k) \times c(k)$$

In this equation, $x(n)$ is the input samples to the filter, $c(k)$ are the filter coefficients, and $y(n)$ are the filtered output samples. Typically, the coefficients do not change in time in most applications such as Digital Down Converters (DDC). FIR filters can be implemented in many forms, the most simple being the tap-delay line approach.

Stratix III DSP block can implement various types of FIR filters very efficiently. To form the tap-delay line, the input register stage of the DSP block has the ability to cascade the input in a chained fashion in 18-bit wide format. Unlike the Stratix II DSP block, which has two built-in parallel input register scan paths, Stratix III supports only one built-in 18-bit parallel input register scan path for 288 data input.

For a pair of 18-bit input buses, the A input for the first 18-bit bus is fed back to be registered again at the input of the second (lower) pair of inputs. Refer to Figure 5–21 for details.

The B input of the multiplier feeds from the general routing. You can scan in the data in 18-bit parallel form and multiply it by the 18-bit input bus from general routing in each cycle.

Normally in a FIR filter, the fixed data input (from general routing and not from cascade) is the constant that needs to be multiplied by the cascaded input. In 18-bit mode, the DSP block has enough input registers to register the general routing signals and the cascaded signal buses before multiplying them. This makes having eight taps for an 18-bit cascade mode possible. Each tap can be considered a single multiplier. If all eight multiplier inputs for the full DSP block are cascaded in a parallel scan chain, an eight-tap FIR filter is created, as shown in Figure 5–21.

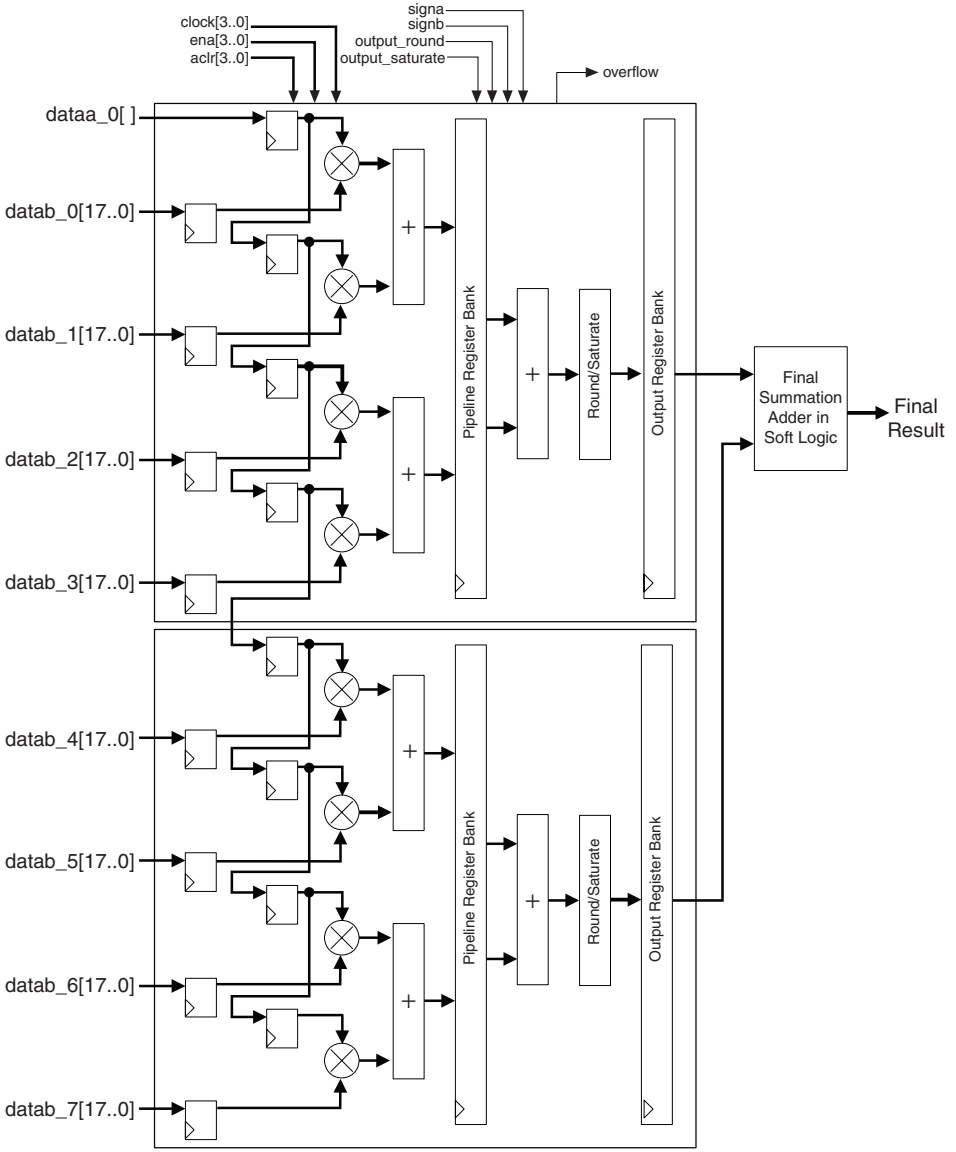
The DSP block can be concatenated to have more than eight taps by enabling the option to output the parallel scan chain to the next (lower) DSP block. Likewise, the output of previous (above) cascade chain is used as an input to the current block. The first (top) multiplier in each half

block will have the option to select the 18-bit cascade chain input from the regular routing or from the previous (above) cascade chain. Also, the last cascaded chain in each half DSP block can exit the DSP block by routing the cascade chain after the last (fourth from top) input register to the output routing channel, bypassing both the pipeline and output registers. This concatenation allows the user to easily construct their desired filter length.

You can use the Four-Multiplier Adder mode with one of the inputs to each multiplier being in a form of chained cascaded input from the previous (above) register. This is very similar to the regular Four-Multiplier Adder with the difference being that not all the inputs are from general routing.

For a complete FIR, the results per individual Four-Multiplier Adder can be combined in either a tree or chained cascade manner. Using external logic and adders, you can very easily implement a tree summation, as shown in Figure 5–21.

Figure 5–21. FIR Filter Using Tap-Delay Line Input and Tree Summation of Final Result

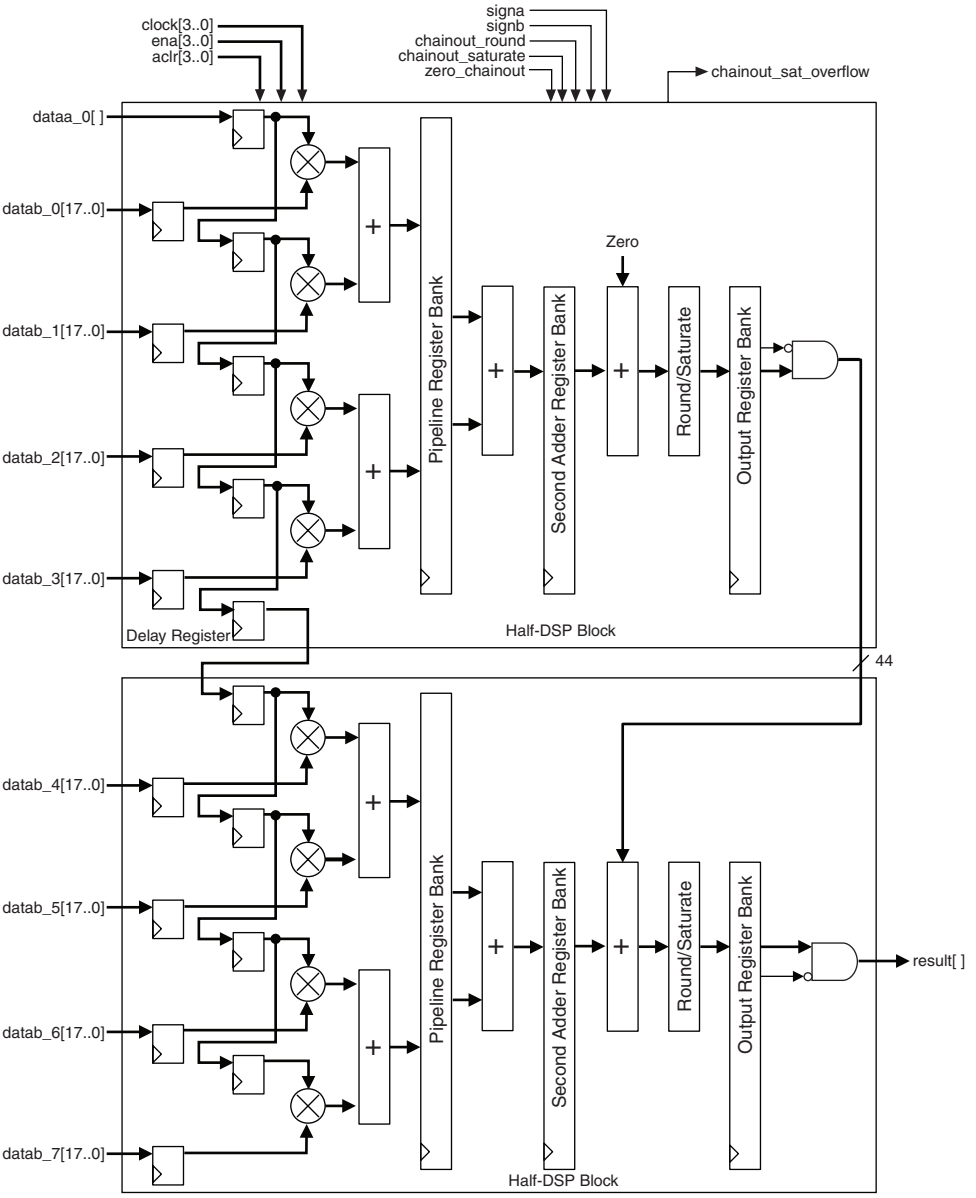


For faster and more efficient chained cascade summation, the DSP block can implement the chainout function in the cascade mode. This mode uses the second-stage 44-bit adder to add the current Four-Multiplier Adder of the half DSP block to the adjacent half DSP block of the Four-Multiplier Adder as shown in Figure 5–22.

This scheme is possible because each half DSP block has two second-stage adders. One of the two second-stage adders is used to add the current Four-Multiplier Adder. The second second-stage adder takes the output of the first second-stage adder and add it to the adjacent half DSP block of the Four-Multiplier Adder result.

In Figure 5–22, the adder that adds the adjacent half DSP block to the current Four-Multiplier Adder is shown as the chainout adder for clarity. This scheme is used to chain and add multiple DSP blocks together. The output of the chainout adder can be registered. The registered chainout output can feed the lower adjacent DSP block for a chainout summation or it can feed general FPGA routing. The chainout result can be zeroed out by applying `logic 1` on the dynamic `zerochainout` signal. The `zerochainout` signal can also be registered.

Figure 5–22. FIR Filter using Tap-Delay Line Input and Chained Cascade Summation of Final Result

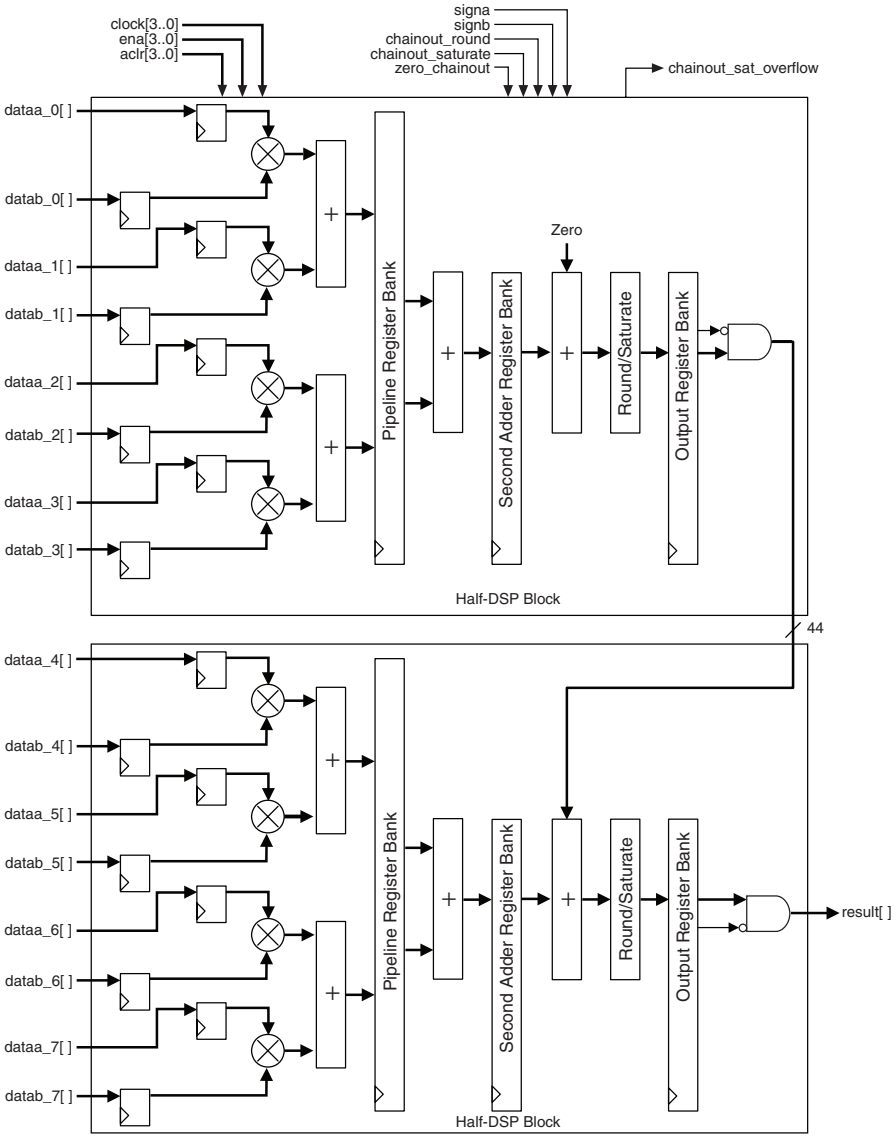


When you use **both** the input cascade and chainout features, the DSP block uses an 18-bit delay register in the boundary of each half-DSP block or from block-to-block to synchronize the input scan chain data with the chainout data. The top half computes the sum of product and chains the output to the next block after the output register. The output register uses the delay register to delay the cascade input by one clock cycle to compensate the latency for the bottom half.

For applications in which the system clock is slower than the speed of the DSP block, the multipliers can be time-multiplexed to improve efficiency. This makes multi-channel and semi-parallel FIR structures possible. The structure to achieve this is similar to Figures 5–21 and 5–22. The main difference is that the input cascade chain is no longer used and each half-DSP block is used in Four-Multiplier Mode with independent inputs. Figure 5–23 shows an example for chained cascaded summation.

In most cases, only the final stage FIR tap with the rounding and saturation unit is deployed.

Figure 5–23. Semi-Parallel FIR Structure Using Chained Cascaded Summation

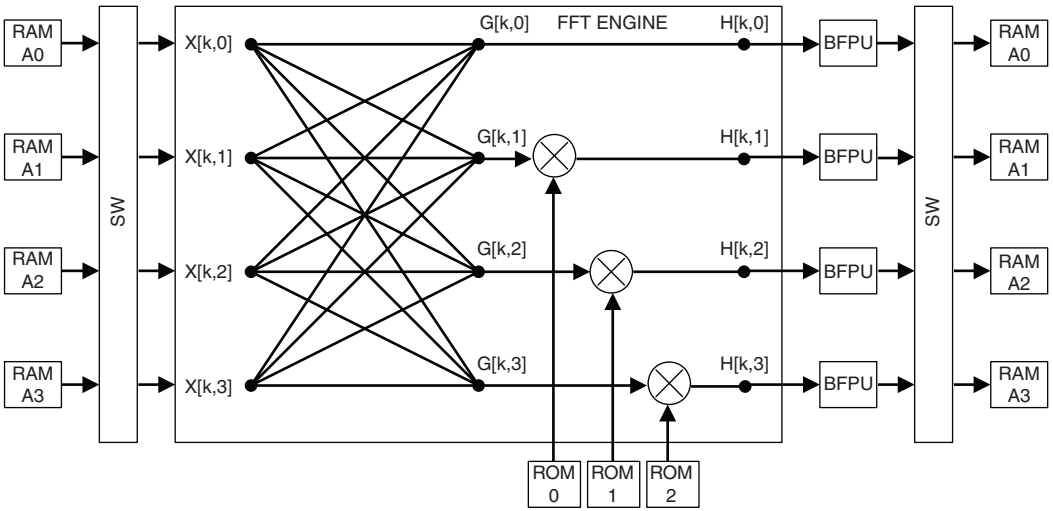


FFT Example

The Fast Fourier Transform (FFT) is a very common DSP function used to convert samples in the time domain to and from the frequency domain. A fundamental building block of the FFT is the FFT butterfly. FFTs are most efficient when operating on complex samples. You can use the Stratix III DSP block to form the core of a complex FFT butterfly very efficiently.

In Figure 5–24, a radix-4 butterfly is shown. Each butterfly requires three complex multipliers. This can be implemented in Stratix III using three half-DSP blocks assuming that the data and twiddle wordlengths are 18 bits or fewer.

Figure 5–24. Radix-4 Butterfly



Software Support

Altera provides two distinct methods for implementing various modes of the DSP block in a design: instantiation and inference. Both methods use the following Quartus II megafunctions:

- `lpm_mult`
- `altmult_add`
- `altmult_accum`
- `altfp_mult`

You can instantiate the megafunctions in the Quartus II software to use the DSP block. Alternatively, with inference, you can create an HDL design and synthesize it using a third-party synthesis tool (such as LeonardoSpectrum, Synplify, or Quartus II Native Synthesis) that infers the appropriate megafunction by recognizing multipliers, multiplier adders, multiplier accumulators, and shift functions. Using either method, the Quartus II software maps the functionality to the DSP blocks during compilation.

Refer to the *Quartus II Software Help* for instructions about using the megafunctions and the *MegaWizard Plug-In Manager*.

For more information, refer to the *Synthesis* section in volume 1 of the *Quartus II Development Software Handbook*.

Conclusion

The Stratix III device DSP blocks are optimized to support DSP applications requiring high data throughput, such as FIR filters, IIR filters, FFT functions, and encoders. These DSP blocks are flexible and can be configured to implement one of several operational modes to suit a particular application. The built-in shift register chain, multipliers, and adders/subtractors minimize the amount of external logic required to implement these functions, resulting in efficient resource utilization and improved performance and data throughput for DSP applications. The Quartus II software, used with the LeonardoSpectrum and Synplify software, provide a complete and easy-to-use flow for implementing these multiplier functions in the DSP blocks.

Document Revision History

Table 5–10 shows the revision history for this document.

Table 5–10. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Updated signal names for Figures 1 to 21. Added two new figures, Figure 5–12 and Figure 5–13. Updated Figure 5–18. Updated Table 5–5 and Table 5–9. Deleted Table 5-10. Added "Double Multiplier" on page 5–23. Clarification added for "Shift Modes" on page 5–34.	—
November 2006 v1.0	Initial Release	—

6. Clock Networks and PLLs in Stratix III Devices

SIII51006-1.1

Introduction

Stratix® III devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources, in combination with the clock synthesis precision provided by the PLLs, provides a complete clock management solution. Stratix III devices provide dedicated global clock networks (GCLKs), regional clock networks (RCLKs), and periphery clock networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 220 unique clock domains (16 GCLK + 88 RCLK + 116 PCLK) within the Stratix III device and allows up to 67 unique GCLK, RCLK, and PCLK clock sources (16 GCLK + 22 RCLK + 29 PCLK) per device quadrant. The Altera® Quartus® II software compiler automatically turns off clock networks not used in the design, thereby reducing the overall power consumption of the device.

Stratix III devices deliver abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. You can independently program every output, creating a unique, customizable clock frequency with no fixed relation to any other input or output clock. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase shift reconfiguration provide the high performance precision required in today's high-speed applications. Stratix III device PLLs are feature rich, supporting advanced capabilities such as clock switchover, dynamic phase shifting, PLL reconfiguration, and reconfigurable bandwidth. Stratix III PLLs also support external feedback mode, spread-spectrum tracking, and post-scale counter cascading features.

The Quartus II software enables the PLLs and their features without requiring any external devices. The following sections describe the Stratix III clock networks and PLLs in detail.

Clock Networks in Stratix III Devices

The GCLKs, RCLKs, and PCLKs available in Stratix III devices are organized into hierarchical clock structures that provide up to 220 unique clock domains (16 GCLK + 88 RCLK + 116 PCLK) within the Stratix III device and allows up to 67 unique GCLK, RCLK, and PCLK clock sources (16 GCLK + 22 RCLK + 29 PCLK) per device quadrant. Table 6–1 shows the clock resources available in Stratix III devices.

Table 6–1. Clock Resources in Stratix III Devices		
Clock Resource	**# of Resources Available**	**Source of Clock Resource**
Clock input pins	32 Single-ended (16 Differential)	CLK[0..15]p and CLK[0..15]n pins
Global clock networks	16	CLK[0..15]p/n pins, PLL clock outputs, and logic array
Regional clock networks	64/88 *(1)*	CLK[0..15]p/n pins, PLL clock outputs, and logic array
Peripheral clock networks	116 (29 per device quadrant) *(2)*	DPA clock outputs, horizontal I/O pins, and logic array
GCLKs/RCLKs per quadrant	32/38 *(3)*	16 GCLKs + 16 RCLKs/ 16 GCLKs + 22 RCLKs
GCLKs/RCLKs per device	80/104 *(4)*	16 GCLKs + 64 RCLKs / 16 GCLKs + 88 RCLKs

Notes to Table 6–1:

(1) There are 64 RCLKs in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices. There are 88 RCLKs in EP3SL200, EP3SE260, and EP3SL340 devices.

(2) There are a total of 56 PCLKs in EP3SL50, EP3SL70, and EP3SE50 devices. There are 88 PCLKs in EP3SL110, EP3SL150, EP3SL200, EP3SE80, and EP3SE110 devices. There are 112 PCLKs in EP3SE260 and 116 PCLKs in the EP3SL340 device.

(3) There are 32 GCLKs/RCLKs per quadrant in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices. There are 38 GCLKs/RCLKs per quadrant in EP3SL200, EP3SE260, and EP3SL340 devices.

(4) There are 80 GCLKs/RCLKs per entire device in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices. There are 104 GCLKs/RCLKS per entire device in EP3SL200, EP3SE260, and EP3SL340 devices.

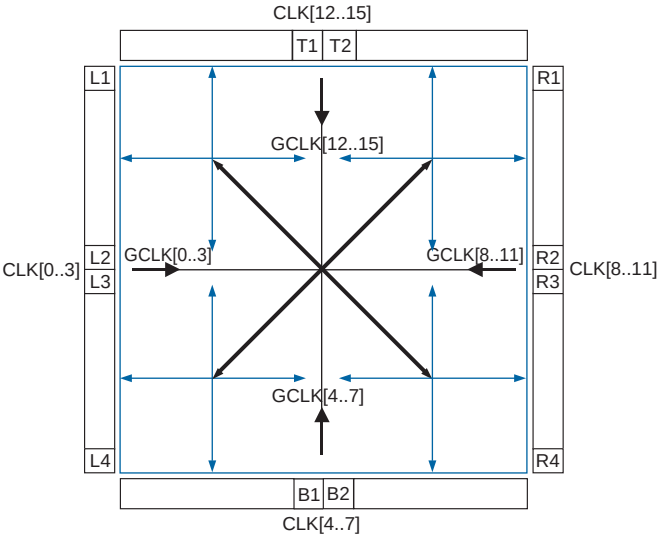
Stratix III devices have up to 32 dedicated single-ended clock pins or 16 dedicated differential clock pins (CLK[0:15]p and CLK[0:15]n) that can drive either the GCLK or RCLK networks. These clock pins are arranged on the four sides of the Stratix III device, as shown in Figures 6–1 to 6–4.

Global Clock Networks

Stratix III devices provide up to 16 GCLKs that can drive throughout the entire device, serving as low-skew clock sources for functional blocks like adaptive logic modules (ALMs), digital signal processing (DSP) blocks, TriMatrix memory blocks, and PLLs. Stratix III device I/O elements

(IOEs) and internal logic can also drive GCLKs to create internally generated global clocks and other high fan-out control signals; for example, synchronous or asynchronous clears and clock enables. Figure 6–1 shows CLK pins and PLLs that can drive GCLK networks in Stratix III devices.

Figure 6–1. Global Clock Networks



Regional Clock Networks

The regional clock (RCLK) networks only pertain to the quadrant they drive into. The RCLK networks provide the lowest clock delay and skew for logic contained within a single device quadrant. Stratix III device I/O elements and internal logic within a given quadrant can also drive RCLKs to create internally generated regional clocks and other high fan-out control signals; for example, synchronous or asynchronous clears and clock enables. Figures 6–2 to 6–4 show CLK pins and PLLs that can drive RCLK networks in Stratix III devices. The EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SE50, EP3SE80, and EP3SE110 devices contain 64 RCLKs; the EP3SL200, EP3SE260, and EP3SL340 devices contain 88 RCLKs.

Figure 6–2. Regional Clock Networks (EP3SL50, EP3SL70, and EP3SE50 Devices)

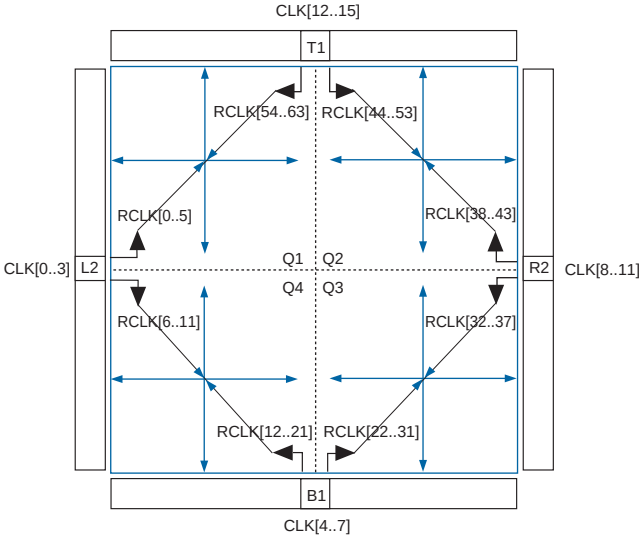


Figure 6–3. Regional Clock Networks (EP3SL110, EP3SL150, EP3SE80, and EP3SE110 Devices)

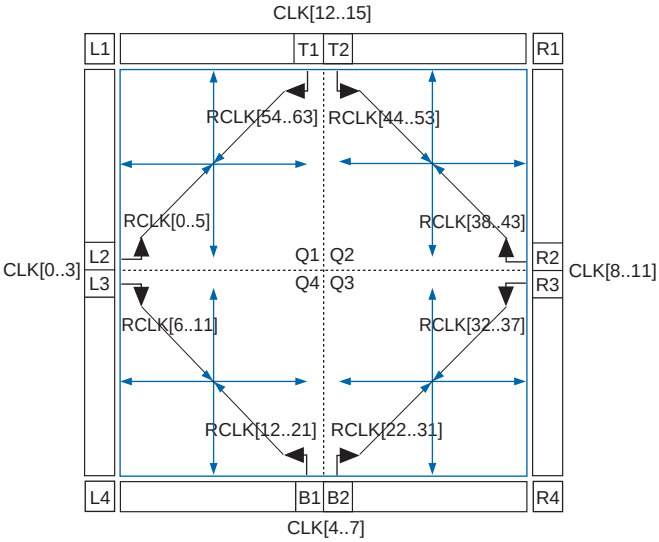
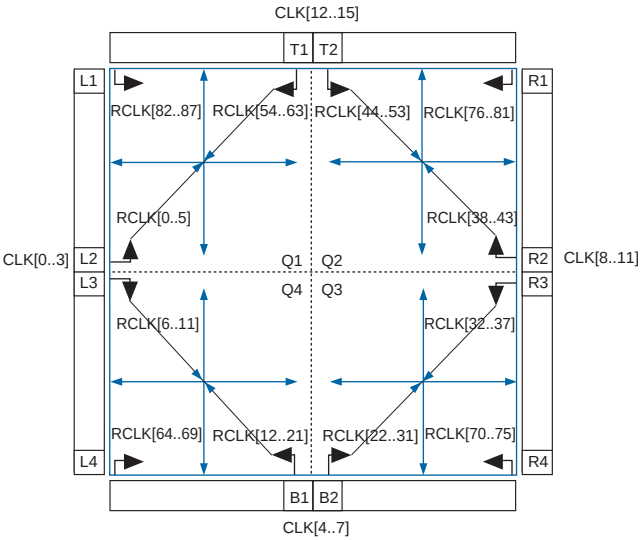


Figure 6–4. Regional Clock Networks (EP3SL200, EP3SE260, and EP3SL340 Devices) *Note (1)*



Notes to Figure 6–4:

(1) The corner RCLKs [64..87] can only be fed by their respective corner PLL outputs. See Table 6–9 for connectivity.

Periphery Clock Networks

Periphery clock (PCLK) networks are a collection of individual clock networks driven from the periphery of the Stratix III device. Clock outputs from the DPA block, horizontal I/O pins, and internal logic can drive the PCLK networks. The EP3SL50, EP3SL70, and EP3SE50 devices contain 56 PCLKs; the EP3SL110, EP3SL150, EP3SL200, EP3SE80, and EP3SE110 devices contain 88 PCLKs; the EP3SE260 device contains 112 PCLKs, and the EP3SL340 device contains 116 PCLKs. These PCLKs have higher skew compared to GCLK and RCLK networks and can be used instead of general purpose routing to drive signals into and out of the Stratix III device.

Clocking Regions

Stratix III devices provide up to 104 distinct clock domains (16 GCLKs + 88 RCLKs) in the entire device. You can utilize these clock resources to form the following four different types of clock region:

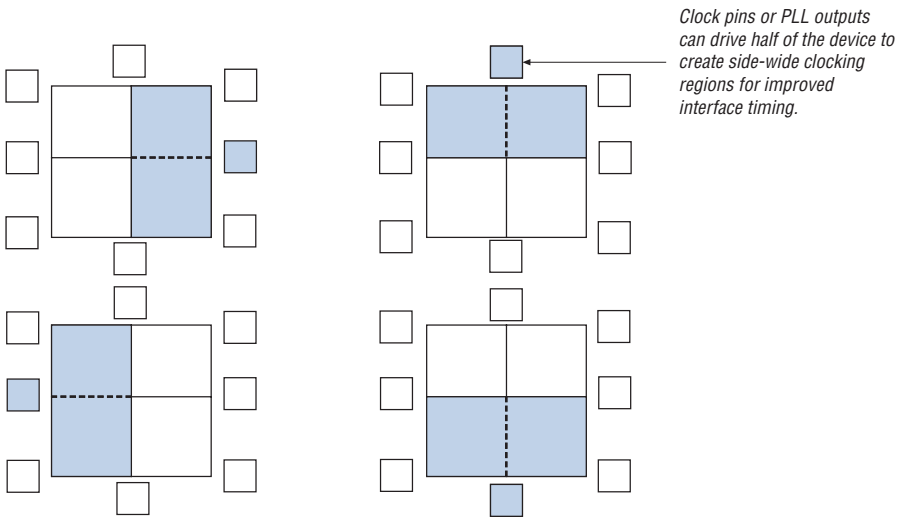
- Entire device clock region
- Regional clock region
- Dual-regional clock region
- Sub-regional clock region

In order to form the entire device clock region, a source (not necessarily a clock signal) drives a global clock network that can be routed through the entire device. This clock region has the maximum delay compared to other clock regions but allows the signal to reach every destination within the device. This is a good option for routing global reset / clear signals or routing clocks throughout the device.

In order to form a regional clock region, a source drives a single-quadrant of the device. This clock region provides the lowest skew within a quadrant and is a good option if all destinations are within a single device quadrant.

To form a dual-regional clock region, a single source (a clock pin or PLL output) generates a dual-regional clock by driving two regional clock networks (one from each quadrant). This technique allows destinations across two device quadrants to utilize the same low-skew clock. The routing of this signal on an entire side has approximately the same delay as in a regional clock region. Internal logic can also drive a dual-regional clock network. Corner PLL outputs only span one quadrant and hence cannot generate a dual-regional clock network. Figure 6–5 shows the dual-regional clock region.

Figure 6–5. Stratix III Dual-Regional Clock Region



The sub-regional clock scheme allows the formation of independent sub-regional clock regions for optimal and efficient use of global and regional clock resources. You can partition the device into a maximum of 16 sub-regional clock regions. Each region is driven by a global or regional clock or by an adjacent ALM. This technique allows the formation of optimally sized synchronous clock regions for the best utilization of clock network resources. Figures 6–6, 6–7, and 6–8 show that you can divide the device into 16, 8, or 12 independent sub-regions.

Figure 6–6. Sixteen Independent Sub-Regional Clock Regions

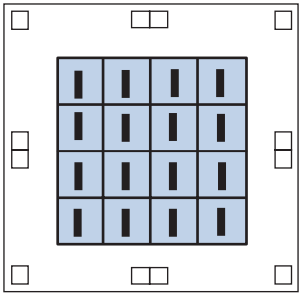


Figure 6–7. Eight Independent Sub-Regional + One Dual-Regional Clock Region

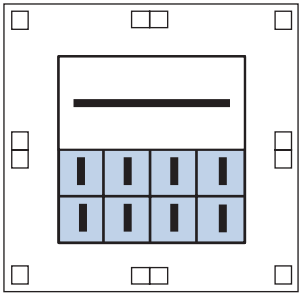
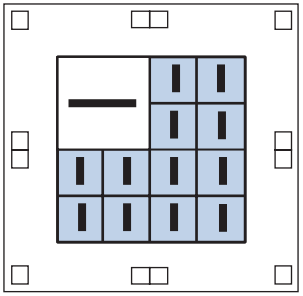


Figure 6–8. Twelve Independent Sub-Regional + One Regional Clock Region



Clock Network Sources

In Stratix III devices, clock input pins, PLL outputs, and internal logic can drive the global and regional clock networks. See Tables 6–2 to 6–6 for the connectivity between dedicated CLK[0..15] pins and the global and regional clock networks.

Dedicated Clock Inputs Pins

The CLK pins can either be differential clocks or single-ended clocks. Stratix III devices supports 16 differential clock inputs or 32 single-ended clock inputs. You can also use the dedicated clock input pins CLK[15..0] for high fan-out control signals such as asynchronous clears, presets, and clock enables for protocol signals such as TRDY and IRDY for PCI through global or regional clock networks.

Logic Array Blocks (LABs)

You can also drive each global and regional clock network via LAB-routing to enable internal logic to drive a high fan-out, low-skew signal.

Stratix III device PLLs cannot be driven by internally generated GCLKs or RCLKs. The input clock to the PLL has to come from dedicated clock input pins or pin / PLL-fed GCLKs or RCLKs only.

PLL Clock Outputs

Stratix III PLLs can drive both GCLK and RCLK networks, as shown in Tables 6–8 and 6–9.

Table 6–2 shows the connection between the dedicated clock input pins and GCLKs.

Table 6–2. Clock Input Pin Connectivity to Global Clock Networks

Clock Resources	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GCLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
GCLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
GCLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
GCLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
GCLK4	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK5	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK6	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK7	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK8	—	—	—	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—
GCLK9	—	—	—	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—
GCLK10	—	—	—	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—
GCLK11	—	—	—	—	—	—	—	—	✓	✓	✓	✓	—	—	—	—
GCLK12	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓
GCLK13	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓
GCLK14	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓
GCLK15	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓

Table 6–3 shows the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 1. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–3. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 1) (Part 1 of 2)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK0	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK1	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK2	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK3	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
RCLK4	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 6–3. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 1) (Part 2 of 2)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK5	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK54	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK55	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK57	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK58	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK59	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK60	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK61	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK62	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK63	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—

Table 6–4 shows the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 2. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–4. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 2) (Part 1 of 2)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK38	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
RCLK39	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
RCLK40	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—
RCLK41	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
RCLK42	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
RCLK43	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
RCLK44	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK45	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK46	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
RCLK47	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK48	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK49	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—

Table 6–4. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 2) (Part 2 of 2)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK51	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓
RCLK52	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
RCLK53	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—

Table 6–5 shows the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 3. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–5. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 3)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK22	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK23	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK24	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK25	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK26	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK27	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK28	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK29	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK30	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK31	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK32	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
RCLK33	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
RCLK34	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—
RCLK35	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
RCLK36	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
RCLK37	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—

Table 6–6 shows the connectivity between the dedicated clock input pins and RCLKs in device Quadrant 4. A given clock input pin can drive two adjacent regional clock networks to create a dual-regional clock network.

Table 6–6. Clock Input Pin Connectivity to Regional Clock Networks (Quadrant 4)

Clock Resource	CLK (p/n Pins)															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
RCLK6	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK7	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK8	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK9	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
RCLK10	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK11	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RCLK12	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK13	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK14	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK15	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK16	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK17	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—
RCLK18	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
RCLK19	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK20	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
RCLK21	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—

Clock Input Connections to PLLs

Dedicated clock input pin connectivity to Stratix III device PLLs is shown in Table 6–7.

Table 6–7. Stratix III Device PLLs and PLL Clock Pin Drivers (Part 1 of 2)

Dedicated Clock Input Pin	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
CLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—

Table 6–7. Stratix III Device PLLs and PLL Clock Pin Drivers (Part 2 of 2)

Dedicated Clock Input Pin	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
CLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—
CLK4	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK5	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK6	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK7	—	—	—	—	✓	✓	—	—	—	—	—	—
CLK8	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK9	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK10	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK11	—	—	—	—	—	—	✓	✓	✓	✓	—	—
CLK12	—	—	—	—	—	—	—	—	—	—	✓	✓
CLK13	—	—	—	—	—	—	—	—	—	—	✓	✓
CLK14	—	—	—	—	—	—	—	—	—	—	✓	✓
CLK15	—	—	—	—	—	—	—	—	—	—	✓	✓

Clock Output Connections

PLLs in Stratix III devices can drive up to 20 regional clock networks and 4 global clock networks. Refer to Table 6–8 for Stratix III PLL connectivity to GCLK networks. The Quartus II software automatically assigns PLL clock outputs to regional or global clock networks.

Table 6–8 shows how the PLL clock outputs connect to GCLK networks.

Table 6–8. Stratix III PLL Connectivity to GCLKs (Part 1 of 2)

Clock Network	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
GCLK0	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK1	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK2	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK3	✓	✓	✓	✓	—	—	—	—	—	—	—	—
GCLK4	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK5	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK6	—	—	—	—	✓	✓	—	—	—	—	—	—

Table 6–8. Stratix III PLL Connectivity to GCLKs (Part 2 of 2)

Clock Network	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
GCLK7	—	—	—	—	✓	✓	—	—	—	—	—	—
GCLK8	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK9	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK10	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK11	—	—	—	—	—	—	✓	✓	✓	✓	—	—
GCLK12	—	—	—	—	—	—	—	—	—	—	✓	✓
GCLK13	—	—	—	—	—	—	—	—	—	—	✓	✓
GCLK14	—	—	—	—	—	—	—	—	—	—	✓	✓
GCLK15	—	—	—	—	—	—	—	—	—	—	✓	✓

Table 6–9 shows how the PLL clock outputs connect to RCLK networks.

Table 6–9. Stratix III Regional clock Outputs From PLLs

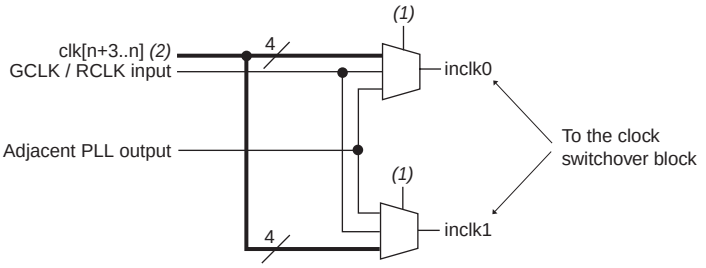
Clock Resource	PLL Number											
	L1	L2	L3	L4	B1	B2	R1	R2	R3	R4	T1	T2
RCLK[0..11]	—	✓	✓	—	—	—	—	—	—	—	—	—
RCLK[12..31]	—	—	—	—	✓	✓	—	—	—	—	—	—
RCLK[32..43]	—	—	—	—	—	—	—	✓	✓	—	—	—
RCLK[44..63]	—	—	—	—	—	—	—	—	—	—	✓	✓
RCLK[64..69]	—	—	—	✓	—	—	—	—	—	—	—	—
RCLK[70..75]	—	—	—	—	—	—	—	—	—	✓	—	—
RCLK[76..81]	—	—	—	—	—	—	✓	—	—	—	—	—
RCLK[82..87]	✓	—	—	—	—	—	—	—	—	—	—	—

Clock Source Control for PLLs

The clock input to Stratix III PLLs comes from clock input multiplexers. The clock multiplexer inputs come from dedicated clock input pins, PLLs through the GCLK and RCLK networks, or from dedicated connections between adjacent Top / Bottom and Left / Right PLLs. The clock input sources to Top / Bottom and Left / Right PLLs (L2, L3, T1, T2, B1, B2, R2, and R3) are shown in Figure 6–9; the corresponding clock input sources to Left / Right PLLs (L1, L4, R1, and R4) are shown in Figure 6–10.

The multiplexer select lines are set in the configuration file (SRAM object file [**.SOF**] or programmer object file [**.POF**]) only. Once programmed, this block cannot be changed without loading a new configuration file (**.SOF** or **.POF**). The Quartus II software automatically sets the multiplexer select signals depending on the clock sources selected in the design.

Figure 6–9. Clock Input Multiplexer Logic for L2, L3, T1, T2, B1, B2, R2, and R3 PLLs

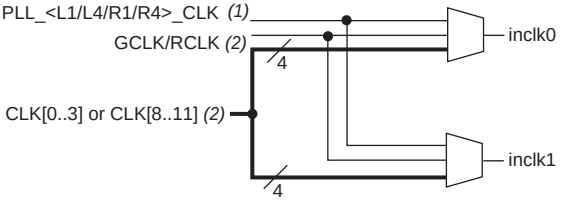


Notes to Figure 6–9:

(1) The input clock multiplexing is controlled through a configuration file (**.SOF** or **.POF**) only and cannot be dynamically controlled in user mode operation.

(2) n=0 for L2 and L3 PLLs; n=4 for B1 and B2 PLLs; n=8 for R2 and R3 PLLs, and n=12 for T1 and T2 PLLs.

Figure 6–10. Clock Input Multiplexer Logic for L1, L4, R1, and R4 PLLs



Notes to Figure 6–10:

(1) Dedicated clock input pins to PLLs - L1, L4, R1 and R4, respectively. For example, `PLL_L1_CLK` is the dedicated clock input for `PLL_L1`.

(2) GCLK / RCLK networks fed by PLL outputs or dedicated `CLK` input pins.

(3) The center clock pins can feed the corner PLLs on the same side directly, through a dedicated path. However, these paths may not be fully compensated.

Clock Control Block

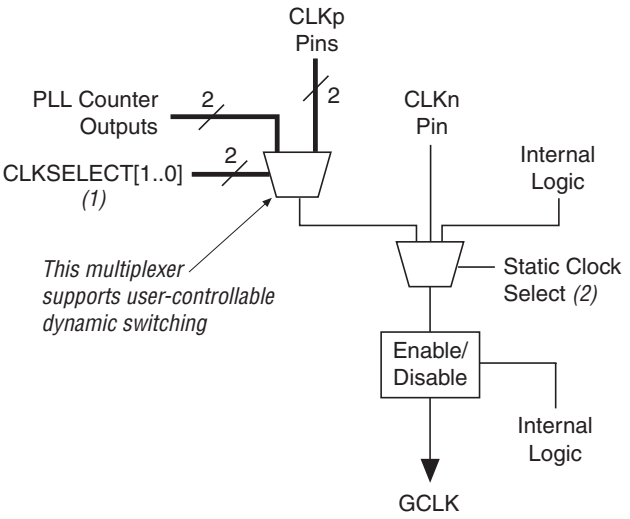
Every global and regional clock network has its own clock control block. The control block provides the following features:

- Clock source selection (dynamic selection for global clocks)
- Global clock multiplexing
- Clock power down (static or dynamic clock enable or disable)

Figures 6–11 and 6–12 show the global clock and regional clock select blocks, respectively.

You can select the clock source for the global clock select block either statically or dynamically. You can either statically select the clock source using a setting in the Quartus II software, or you can dynamically select the clock source using internal logic to drive the multiplexer select inputs. When selecting the clock source dynamically, you can either select two PLL outputs (such as `CLK0` or `CLK1`), or a combination of clock pins or PLL outputs.

Figure 6–11. Stratix III Global Clock Control Block

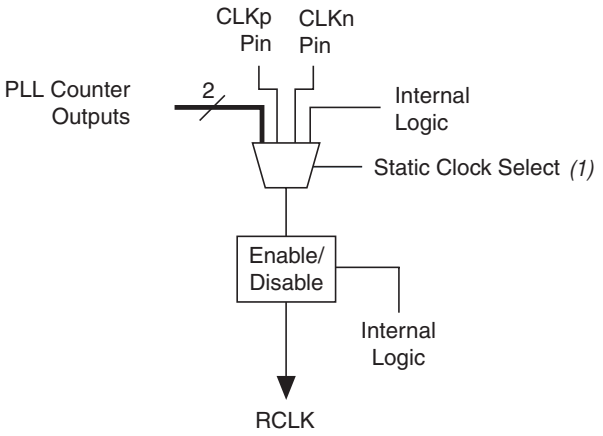


Notes to Figure 6–11:

(1) These clock select signals can only be dynamically controlled through internal logic when the device is operating in user mode.

(2) These clock select signals can only be set through a configuration file (**.SOF** or **.POF**) and cannot be dynamically controlled during user mode operation.

Figure 6–12. Regional Clock Control Block



Note to Figure 6–12:

(1) This clock select signal can only be dynamically controlled through a configuration file (**.SOF** or **.POF**) and cannot be dynamically controlled during user mode operation.

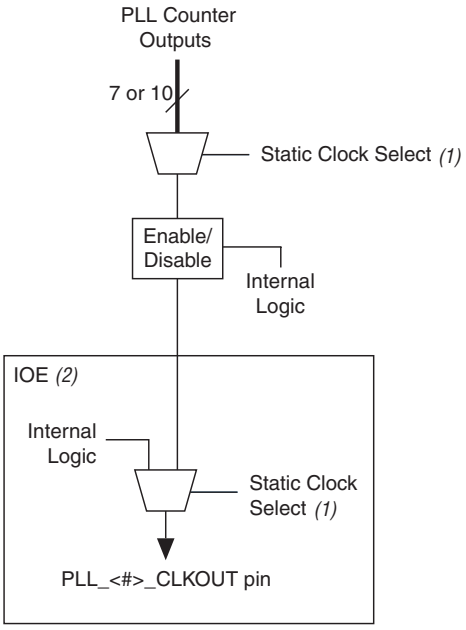
The clock source selection for the regional clock select block can only be controlled statically using configuration bit settings in the configuration file (**.sof** or **.pof**) generated by the Quartus II software.

The Stratix III clock networks can be powered down by both static and dynamic approaches. When a clock net is powered down, all the logic fed by the clock net is in an off-state, thereby reducing the overall power consumption of the device. The unused global and regional clock networks are automatically powered down through configuration bit settings in the configuration file (**.sof** or **.pof**) generated by the Quartus II software. The dynamic clock enable or disable feature allows the internal logic to control power-up or power-down synchronously on GCLK and RCLK networks, including dual-regional clock regions. This function is independent of the PLL and is applied directly on the clock network, as shown in Figures 6–11 and 6–12.

You can set the input clock sources and the `clkena` signals for the global and regional clock network multiplexers through the Quartus II software using the altclkctrl megafunction. You can also enable or disable the dedicated external clock output pins using the altclkctrl megafunction. Figure 6–13 shows the external PLL output clock control block.

When using the altclkctrl megafunction to implement clock source selection (dynamic), the inputs from the clock pins feed the `inclock[0..1]` ports of the multiplexer, while the PLL outputs feed the `inclock[2..3]` ports. You can choose from among these inputs using the `CLKSELECT[1..0]` signal.

Figure 6–13. Stratix III External PLL Output Clock Control Block



Notes to Figure 6–13:

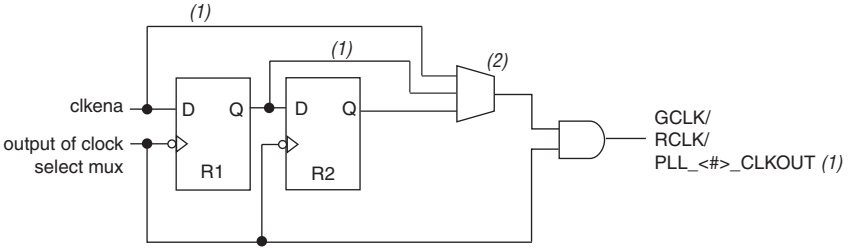
(1) This clock select signal can only be set through a configuration file (**.SOF** or **.POF**) and cannot be dynamically controlled during user mode operation.

(2) The clock control block feeds to a multiplexer within the `PLL_<#>_CLKOUT` pin's IOE. The `PLL_<#>_CLKOUT` pin is a dual-purpose pin. Therefore, this multiplexer selects either an internal signal or the output of the clock control block.

Clock Enable Signals

Figure 6–14 shows how the clock enable / disable circuit of the clock control block is implemented in Stratix III devices.

Figure 6–14. clkena Implementation



Notes to Figure 6–14:

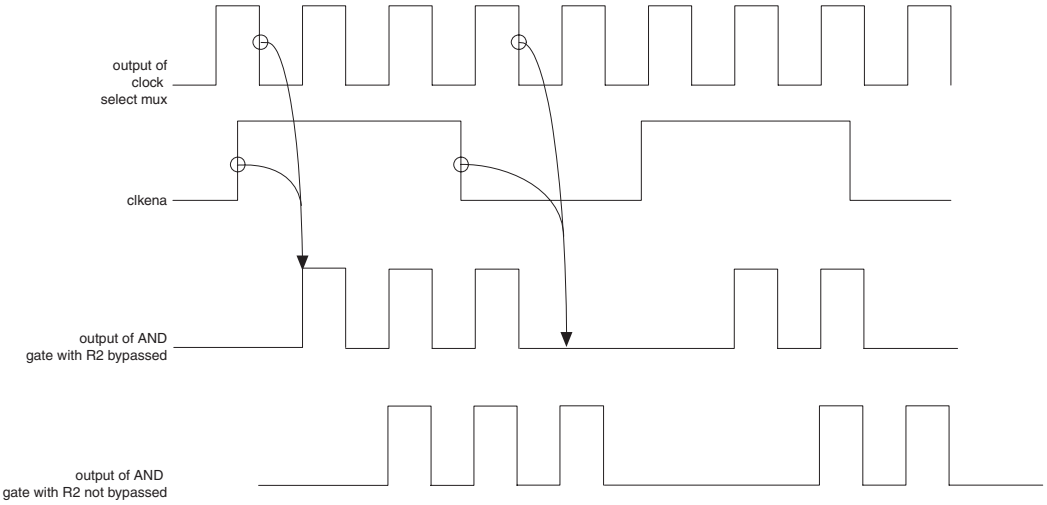
(1) The R1 and R2 bypass paths are not available for PLL external clock outputs.

(2) The select line is statically controlled by a bit setting in the configuration file (**.SOF** or **.POF**).

In Stratix III devices, the `clkena` signals are supported at the clock network level instead of at the PLL output counter level. This allows you to gate off the clock even when a PLL is not being used. You can also use the `clkena` signals to control the dedicated external clocks from the PLLs. Figure 6–15 shows the waveform example for a clock output enable. `clkena` is synchronous to the falling edge of the clock output.

Stratix III devices also have an additional metastability register that aids in asynchronous enable / disable of the GCLK / RCLK networks. This register can be optionally bypassed in the Quartus II software.

Figure 6–15. clkena Signals



Note to Figure 6–15:

(1) You can use the `clkena` signals to enable or disable the global and regional networks or the `PLL_<#>_CLKOUT` pins.

The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. The `clkena` signal can also disable clock outputs if the system is not tolerant of frequency over-shoot during resynchronization.

PLLs in Stratix III Devices

Stratix III devices offer up to 12 PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces. The nomenclature for the PLLs follows their geographical location in the device floor plan. The PLLs that reside on the top and bottom sides of the device are named PLL_T1, PLL_T2, PLL_B1 and PLL_B2; the PLLs that reside on the left and right sides of the device are named PLL_L1, PLL_L2, PLL_L3, PLL_L4, PLL_R1, PLL_R2, PLL_R3, and PLL_R4, respectively.

Table 6–10 shows the number of PLLs available in the Stratix III device family.

Table 6–10. Stratix III Device PLL Availability

Device	L1	L2	L3	L4	T1	T2	B1	B2	R1	R2	R3	R4
EP3SL50	—	✓	—	—	✓	—	✓	—	—	✓	—	—
EP3SL70	—	✓	—	—	✓	—	✓	—	—	✓	—	—
EP3SL110 *(1)*	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
EP3SL150 *(1)*	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
EP3SL200 *(2)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP3SL340	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP3SE50	—	✓	—	—	✓	—	✓	—	—	✓	—	—
EP3SE80 *(1)*	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
EP3SE110 *(1)*	—	✓	✓	—	✓	✓	✓	✓	—	✓	✓	—
EP3SE260 *(2)*	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 6–10:
(1) PLLs T2, B2, L3, and R3 are not available in the F780 package.
(2) PLLs L1, L4, R1, and R4 are not available in the F1152 package.

All Stratix III PLLs have the same core analog structure with only minor differences in features that are supported. Table 6–11 highlights the features of Top/Bottom and Left/Right PLLs in Stratix III devices.

Table 6–11. Stratix III PLL Features (Part 1 of 2)

Feature	Stratix III Top/Bottom PLLs	Stratix III Left/Right PLLs
C (output) counters	10	7
M, N, C counter sizes	1 to 512	1 to 512
Dedicated clock outputs	6 single-ended or 4 single-ended and 1 differential pair	2 single-ended or 1 differential pair

Table 6–11. Stratix III PLL Features (Part 2 of 2)

Feature	Stratix III Top/Bottom PLLs	Stratix III Left/Right PLLs
Clock input pins	8 single-ended or 4 differential pin pairs	8 single-ended or 4 differential pin pairs
External feedback input pin	Single-ended or differential	Single-ended only
Spread-spectrum input clock tracking	Yes *(1)*	Yes *(1)*
PLL cascading	Through GCLK and RCLK and dedicated path between adjacent PLLs	Through GCLK and RCLK and dedicated path between adjacent PLLs *(2)*
Compensation modes	All except LVDS clock network compensation	All except external feedback mode when using differential I/Os
PLL drives `LVDSCLK` and `LOADEN`	No	Yes
VCO output drives DPA clock	No	Yes
Phase shift resolution	Down to 96.125 ps *(3)*	Down to 96.125 ps *(3)*
Programmable duty cycle	Yes	Yes
Output counter cascading	Yes	Yes
Input clock switchover	Yes	Yes

Notes to Table 6–11:

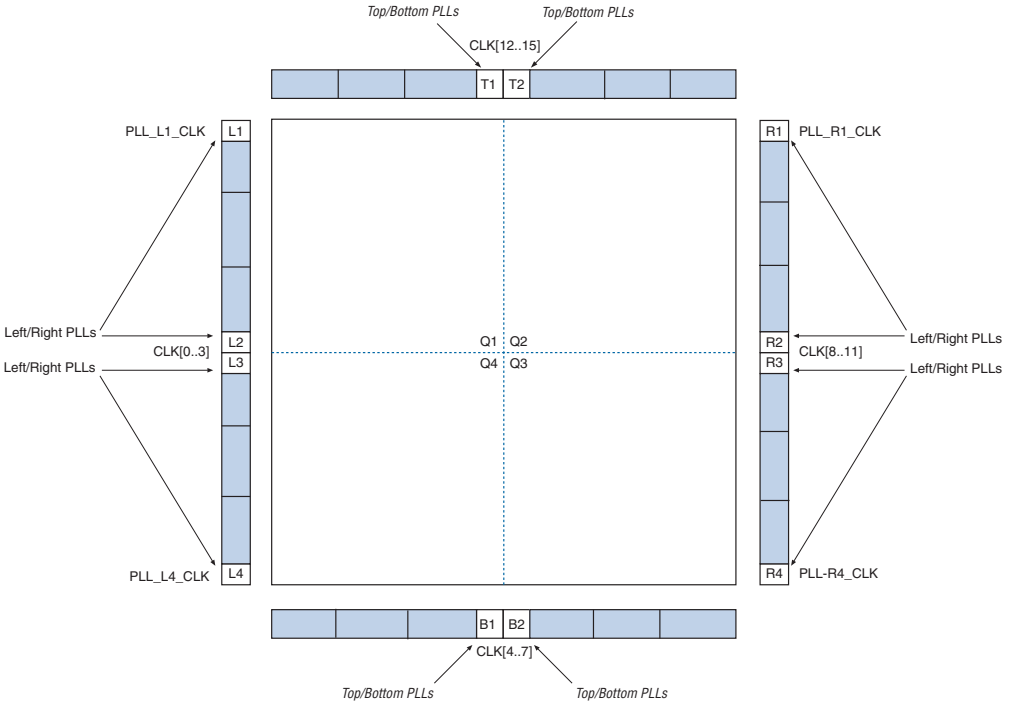
(1) Provided input clock jitter is within input jitter tolerance specifications.

(2) The dedicated path between adjacent PLLs is not available on L1, L4, R1, and R4 PLLs.

(3) The smallest phase shift is determined by the voltage-controlled oscillator (VCO) period divided by eight. For degree increments, the Stratix III device can shift all output frequencies in increments of at least 45 degrees. Smaller degree increments are possible depending on the frequency and divide parameters.

Figure 6–16 shows the location of PLLs in Stratix III devices.

Figure 6–16. Stratix III PLL Locations



Stratix III PLL Hardware Overview

Stratix III devices contain up to 12 PLLs with advanced clock management features. The main goal of a PLL is to synchronize the phase and frequency of an internal or external clock to an input reference clock. There are a number of components that comprise a PLL to achieve this phase alignment.

Stratix III PLLs align the rising edge of the input reference clock to a feedback clock using the phase-frequency detector (PFD). The falling edges are determined by the duty-cycle specifications. The PFD produces an up or down signal that determines whether the voltage-controlled oscillator (VCO) needs to operate at a higher or lower frequency. The output of the PFD feeds the charge pump and loop filter, which produces a control voltage for setting the VCO frequency. If the PFD produces an up signal, then the VCO frequency increases. A down signal decreases the VCO frequency. The PFD outputs these up and down signals to a charge

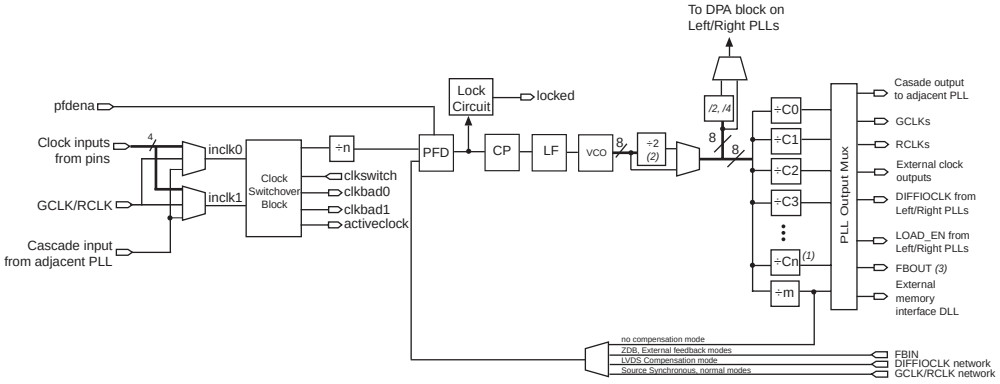
pump. If the charge pump receives an up signal, current is driven into the loop filter. Conversely, if the charge pump receives a down signal, current is drawn from the loop filter.

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. The loop filter also removes glitches from the charge pump and prevents voltage over-shoot, which filters the jitter on the VCO. The voltage from the loop filter determines how fast the VCO operates. A divide counter (m) is inserted in the feedback loop to increase the VCO frequency above the input reference frequency. VCO frequency (f_{VCO}) is equal to (m) times the input reference clock (f_{REF}). The input reference clock (f_{REF}) to the PFD is equal to the input clock (f_{IN}) divided by the pre-scale counter (N). Therefore, the feedback clock (f_{FB}) applied to one input of the PFD is locked to the f_{REF} that is applied to the other input of the PFD.

The VCO output from Left/Right PLLs can feed seven post-scale counters (C[0..6]), while the corresponding VCO output from Top/Bottom PLLs can feed ten post-scale counters (C[0..9]). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

Figure 6–17 shows a simplified block diagram of the major components of the Stratix III PLL.

Figure 6–17. Stratix III PLL Block Diagram



Notes to Figure 6–17:

(1) The number of post scale counters is 7 for Left/Right PLLs and 10 for Top/Bottom PLLs.

(2) This is the VCO post-scale counter K.

(3) The FBOUT port is fed by the M counter in Stratix III PLLs.

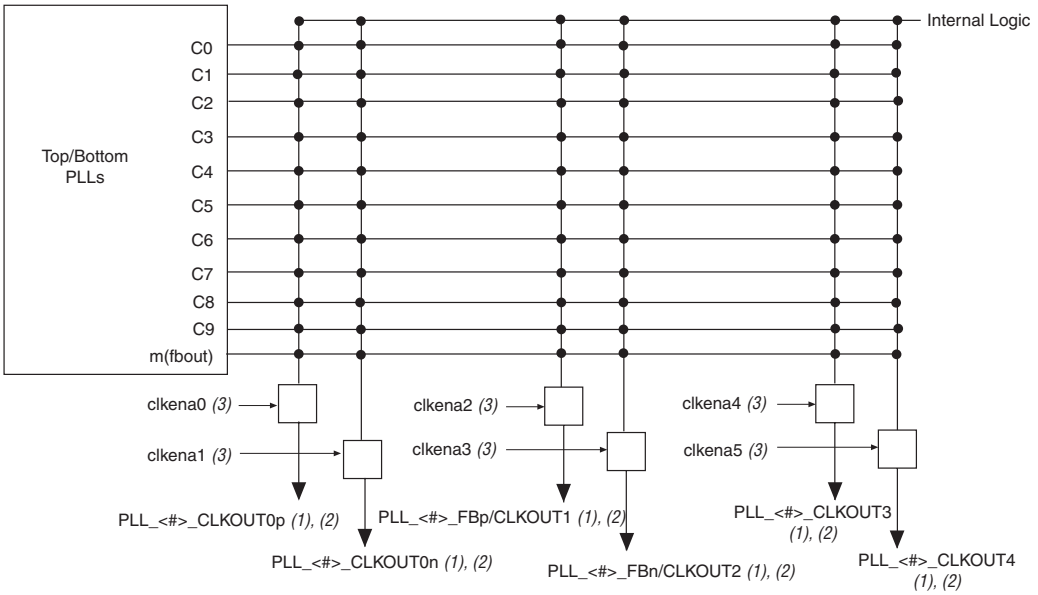
PLL Clock I/O Pins

Each Top / Bottom PLL supports six clock I / O pins, organized as three pairs of pins:

- 1st pair: 2 single-ended I / O or 1 differential I / O
- 2nd pair: 2 single-ended I / O or 1 differential external feedback input (FBp / FBn)
- 3rd pair: 2 single-ended I / O or 1 differential input

Figure 6–18 shows the clock I / O pins associated with Top / Bottom PLLs.

Figure 6–18. External Clock Outputs for Top/Bottom PLLs



Notes to Figure 6–18:

(1) These clock output pins can be fed by any one of the `C[9..0]`, m counters.

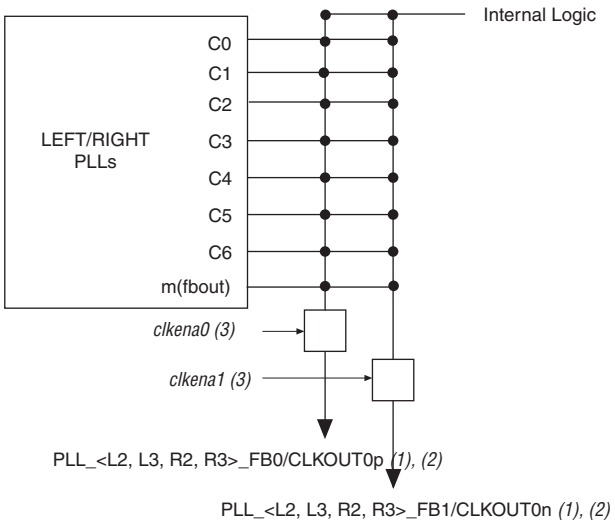
(2) The `CLKOUT0p` and `CLKOUT0n` pins can be either single-ended or differential clock outputs. `CLKOUT1` and `CLKOUT2` pins are dual-purpose I / O pins that can be used as two single-ended outputs or one differential external feedback input pin. `CLKOUT3` and `CLKOUT4` pins are two single-ended output pins.

(3) These external clock enable signals are available only when using the `altclkctrl` megafunction.

Any of the output counters (`C[9..0]` on Top / Bottom PLLs and `C[6..0]` on Left / Right PLLs) or the `M` counter can feed the dedicated external clock outputs, as shown in Figures 6–18 and 6–19. Therefore, one counter or frequency can drive all output pins available from a given PLL.

Each Left/Right PLL supports two clock I/O pins, configured as either two single-ended I/Os or one differential I/O pair. When using both pins as single-ended I/Os, one of them can be the clock output while the other pin is the external feedback input (FB) pin. Hence, Left/Right PLLs only support external feedback mode for single-ended I/O standards only.

Figure 6–19. External Clock Outputs for Left/Right PLLs



Notes to Figure 6–19:

(1) These clock output pins can be fed by any one of the `C[6..0]`, m counters.

(2) The `CLKOUT0p` and `CLKOUT0n` pins are dual-purpose I/O pins that can be used as two single-ended outputs or one single-ended output and one external feedback input pin.

(3) These external clock enable signals are available only when using the `altclkctrl` megafunction.

Each pin of a single-ended output pair can either be in-phase or 180-degrees out-of-phase. The Quartus II software places the NOT gate in the design into the IOE to implement 180 phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, differential HSTL, and differential SSTL.

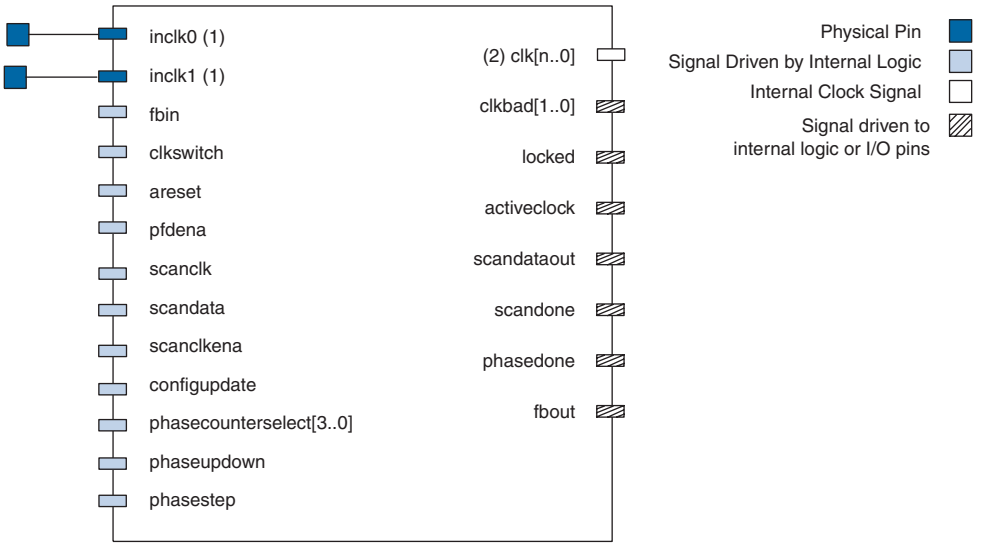
Refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook* to determine which I/O standards are supported by the PLL clock input and output pins.

Stratix III PLLs can also drive out to any regular I/O pin through the global or regional clock network. You can also use the external clock output pins as user I/O pins if external PLL clocking is not needed.

Stratix III PLL Software Overview

Stratix III PLLs are enabled in the Quartus II software by using the altpll megafunction. Figure 6–20 shows the Stratix III PLL ports as they are named in the altpll megafunction of the Quartus II software.

Figure 6–20. Stratix III PLL Ports



Notes to Figure 6–20:

(1) You can feed the `inclk0` or `inclk1` clock input from any one of four dedicated clock pins located on the same side of the device as the PLL.

(2) You can drive to global or regional clock networks or dedicated external clock output pins. n = 6 for Left / Right PLLs and n = 9 for Top / Bottom PLLs.

Table 6–12 shows the PLL input signals for Stratix III devices.

Table 6–12. PLL Input Signals (Part 1 of 2)

Port	Description	Source	Destination
`inclk0`	Input clock to the PLL	Dedicated pin, adjacent PLL, GCLK, or RCLK network	`N` counter
`inclk1`	Input clock to the PLL	Dedicated pin, adjacent PLL, GCLK, or RCLK network	`N` counter
`fbin`	Compensation feedback input to the PLL	Pin or GCLK, RCLK, LVSDCLK	PFD

Table 6–12. PLL Input Signals (Part 2 of 2)

Port	Description	Source	Destination
clkswitch	Switchover signal used to initiate clock switchover asynchronously. When used in manual switchover, clkswitch is used as a select signal between inclk0 and inclk1. If clkswitch = 0, inclk0 is selected and vice versa.	Logic array or I/O pin	Clock switchover circuit
areset	Signal used to reset the PLL which resynchronizes all the counter outputs. Active high	Logic array	General PLL control signal
pfdena	Enables the outputs from the phase frequency detector. Active high	Logic array	PFD
scanclk	Serial clock signal for the real-time PLL reconfiguration feature.	Logic array	Reconfiguration circuit
scandata	Serial input data stream for the real-time PLL reconfiguration feature.	Logic array	Reconfiguration circuit
scanclkena	Enables scanclk and allows the scandata to be loaded in the scan chain. Active high	Logic array or I/O pin	PLL reconfiguration circuit
configupdate	Writes the data in the scan chain to the PLL. Active high	Logic array or I/O pins	PLL reconfiguration circuit
phasecounterselect[3:0]	Selects corresponding PLL counter for dynamic phase shift	Logic array or I/O pins	PLL reconfiguration circuit
phaseupdown	Selects dynamic phase shift direction; 1 = UP; 0 = DOWN	Logic array or I/O pin	PLL reconfiguration circuit
phasestep	Logic high enables dynamic phase shifting	Logic array or I/O pin	PLL reconfiguration circuit

Table 6–13 shows the PLL output signals for Stratix III devices.

Table 6–13. PLL Output Signals

Port	Description	Source	Destination
clk[9..0] for Top/Bottom PLLs clk[6..0] for Left/Right PLLs	PLL output counters driving regional, global, or external clocks.	PLL counter	Internal or external clock
clkbad[1..0]	Signals indicating which reference clock is no longer toggling. clkbad1 indicates inclk1 status, clkbad0 indicates inclk0 status. 1= good; 0 = bad	PLL switchover circuit	Logic array
locked	Lock or gated lock output from lock detect circuit. Active high	PLL lock detect	Logic array
activeclock	Signal to indicate which clock (0 = inclk0 or 1 = inclk1) is driving the PLL. If this signal is low, inclk0 drives the PLL. If this signal is high, inclk1 drives the PLL.	PLL clock multiplexer	Logic array
scandataout	Output of the last shift register in the scan chain.	PLL scan chain	Logic array
scandone	Signal indicating when the PLL has completed reconfiguration. One-to-0 transition indicates that the PLL has been reconfigured.	PLL scan chain	Logic array
phasedone	When asserted it indicates that the phase reconfiguration is complete and the PLL is ready to act on a possible second reconfiguration. Asserts based on internal PLL timing. De-asserts on rising edge of SCANCLK.	PLL scan chain	Logic array
fbout	Output of m counter. Used for clock delay compensation.	M counter	Logic array

Clock Feedback Modes

Stratix III PLLs support up to six different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle. Table 6–14 shows the clock feedback modes supported by Stratix III device PLLs.

Table 6–14. Clock Feedback Mode Availability

Clock Feedback Mode	Availability	
	Top/Bottom PLLs	Left/Right PLLs
Source-synchronous mode	Yes	Yes
No-compensation mode	Yes	Yes
Normal mode	Yes	Yes
Zero-delay buffer (ZDB) mode	Yes	Yes
External-feedback mode	Yes	Yes *(1)*
LVDS compensation	No	Yes

Note to Table 6–14:

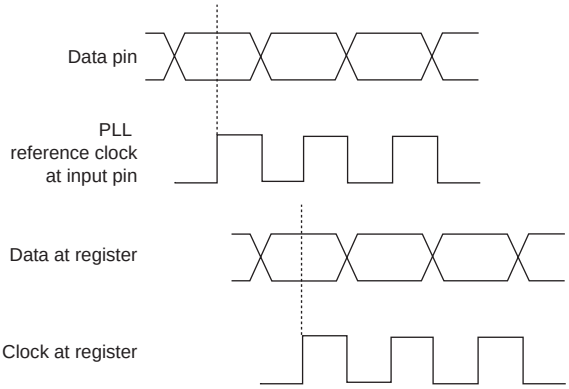
(1) External feedback mode supported for single-ended inputs and outputs only on Left / Right PLLs.

The input and output delays are fully compensated by a PLL only when using the dedicated clock input pins associated with a given PLL as the clock sources. For example, when using `PLL_T1` in normal mode, the clock delays from the input pin to the PLL clock output-to-destination register are fully compensated provided the clock input pin is one of the following four pins: `CLK12`, `CLK13`, `CLK14`, or `CLK15`. When an RCLK or GCLK network drives the PLL, the input and output delays may not be fully compensated in the Quartus II software.

Source Synchronous Mode

If data and clock arrive at the same time on the input pins, the same phase relationship is maintained at the clock and data ports of any IOE input register. Figure 6–21 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfers. Data and clock signals at the IOE experience similar buffer delays as long as you use the same I/O standard.

Figure 6–21. Phase Relationship Between Clock and Data in Source-Synchronous and LVDS Modes



The source-synchronous mode compensates for the delay of the clock network used plus any difference in the delay between these two paths:

- Data pin to IOE register input
- Clock input pin to the PLL PFD input

Set the input pin to register delay chain within the IOE to **zero** in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins need to use the **PLL COMPENSATED** logic option in the Quartus II software.

Source-Synchronous Mode for LVDS Compensation

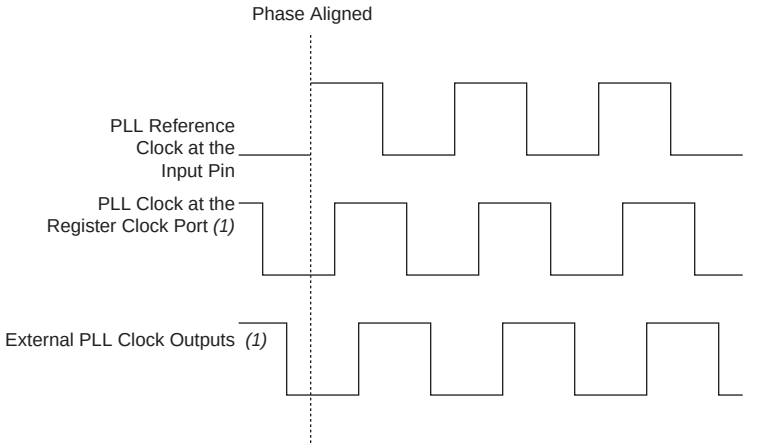
The goal of this mode is to maintain the same data and clock timing relationship seen at the pins at the internal SERDES capture register, except that the clock is inverted (180-degree phase shift). Thus, this mode ideally compensates for the delay of the LVDS clock network plus any difference in delay between these two paths:

- Data pin-to-SERDES capture register
- Clock input pin-to-SERDES capture register. In addition, the output counter needs to provide the 180-degree phase shift.

No-Compensation Mode

In the no-compensation mode, the PLL does not compensate for any clock networks. This mode provides better jitter performance because the clock feedback into the PFD passes through less circuitry. Both the PLL internal- and external-clock outputs are phase-shifted with respect to the PLL clock input. Figure 6–22 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 6–22. Phase Relationship Between PLL Clocks in No Compensation Mode

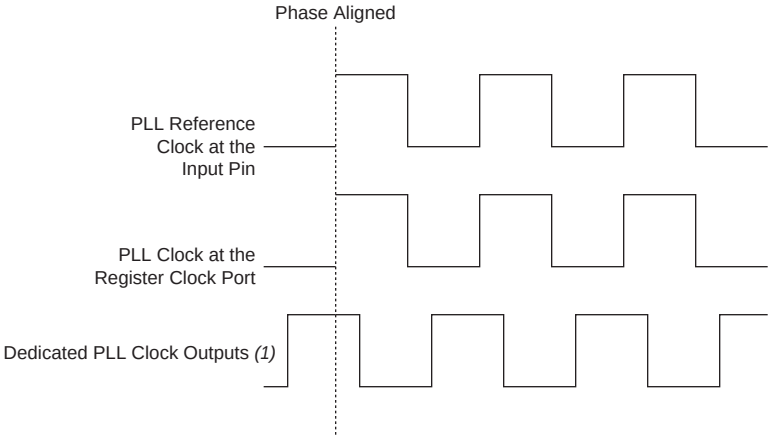


Note to Figure 6–22:
(1) The PLL clock outputs will lag the PLL input clocks depending on routine delays.

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock-output pin has a phase delay relative to the clock input pin if connected in this mode. The Quartus II software timing analyzer reports any phase difference between the two. In normal mode, the delay introduced by the GCLK or RCLK network is fully compensated. Figure 6–23 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 6–23. Phase Relationship Between PLL Clocks in Normal Mode



Note to Figure 6–23:
(1) The external clock output can lead or lag the PLL internal clock signals.

Zero-Delay Buffer Mode

In zero-delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, you must use the same I/O standard on the input clocks and output clocks in order to guarantee clock alignment at the input and output pins. This mode is supported on all Stratix III PLLs.

When using Stratix III PLLs in ZDB mode, along with single-ended I/O standards, to ensure phase alignment between the clock input pin (CLK) and the external clock output (CLKOUT) pin, you are required to instantiate a bi-directional I/O pin in the design to serve as the feedback path connecting the FBOUT and FBIN ports of the PLL. The PLL uses this bi-directional I/O pin to mimic, and hence compensate for, the output delay from the clock output port of the PLL to the external clock output pin. Figure 6–24 shows ZDB mode implementation in Stratix III PLLs. You cannot use differential I/O standards on the PLL clock input or output pins when using ZDB mode.

The bi-directional I/O pin that you instantiate in your design should always be assigned a single-ended I/O standard.

Figure 6–24. Zero-Delay Buffer Mode in Stratix III PLLs

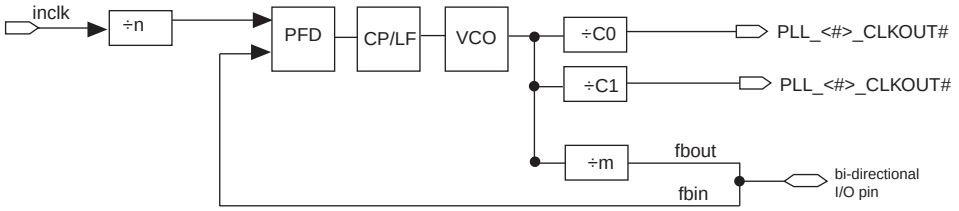
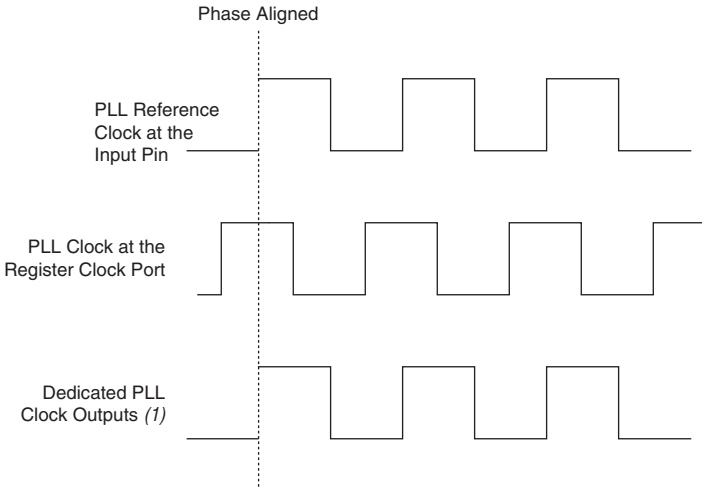


Figure 6–25 shows an example waveform of the PLL clocks' phase relationship in ZDB mode.

Figure 6–25. Phase Relationship Between PLL Clocks in Zero Delay Buffer Mode



Note to Figure 6–25:
(1) The internal PLL clock output can lead or lag the external PLL clock outputs.

External Feedback Mode

In external-feedback (EFB) mode, the external-feedback input pin (`fbin`) is phase-aligned with the clock input pin, as shown in Figure 6–27. Aligning these clocks allows you to remove clock delay and skew between devices. This mode is supported on all Stratix III PLLs.

In this mode, the output of the M counter (FBOUT) feeds back to the PLL fbin input (using a trace on the board) becoming part of the feedback loop. Also, you use one of the dual-purpose external clock outputs as the fbin input pin in EFB mode.

When using this mode, you must use the same I/O standard on the input clock, feedback input, and output clocks. Left/Right PLLs support EFB mode when using single-ended I/O standards only. Figure 6–26 shows EFB mode implementation in Stratix III devices.

Figure 6–26. External Feedback Mode in Stratix III Devices

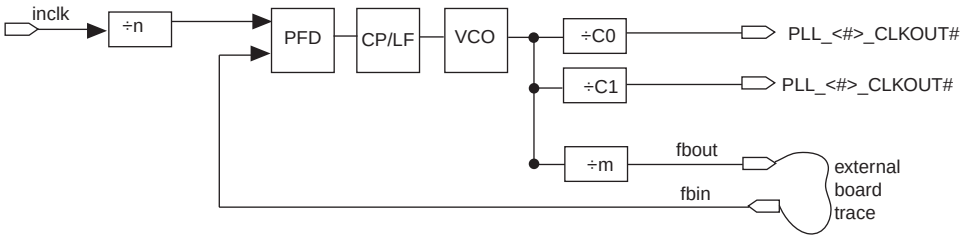
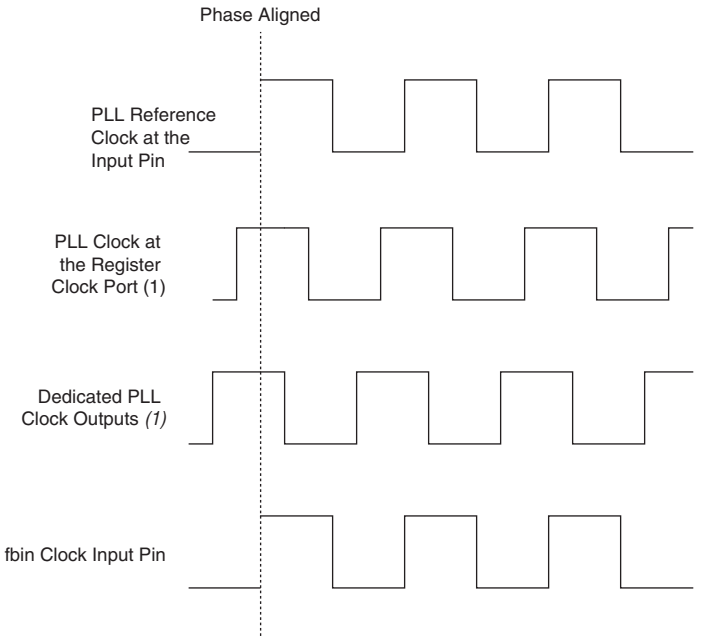


Figure 6–27 shows an example waveform of the phase relationship between PLL clocks in EFB mode.

Figure 6–27. Phase Relationship Between PLL Clocks in External-Feedback Mode



Note to Figure 6–27:
(1) The PLL clock outputs can lead or lag the fbin clock input.

Clock Multiplication and Division

Each Stratix III PLL provides clock synthesis for PLL output ports using m / (n* post-scale counter) scaling factors. The input clock is divided by a pre-scale factor, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match f_{in} (m / n). Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz within the VCO range). Then the post-scale counters scale down the VCO frequency for each output port.

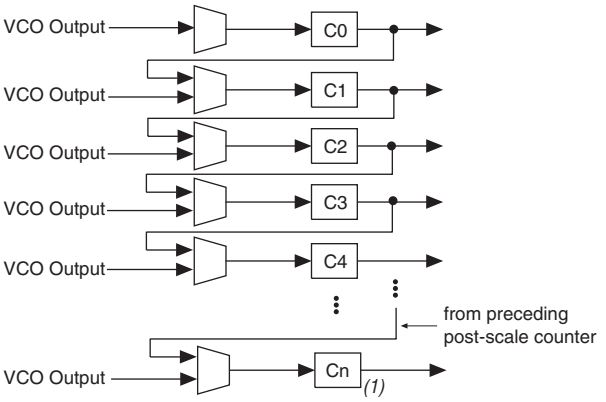
Each PLL has one pre-scale counter, n, and one multiply counter, m, with a range of 1 to 512 for both m and n. The n counter does not use duty-cycle control because the only purpose of this counter is to calculate frequency division. There are seven generic post-scale counters per Left / Right PLL and ten post-scale counters per Top / Bottom PLL that can feed GCLKs, RCLKs, or external clock outputs. These post-scale counters range from 1 to 512 with a 50% duty cycle setting. The high- and low-count values for each counter range from 1 to 256. The sum of the high- and low-count values chosen for a design selects the divide value for a given counter.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the altpll megafunction.

Post-Scale Counter Cascading

The Stratix III PLLs support post-scale counter cascading to create counters larger than 512. This is automatically implemented in the Quartus II software by feeding the output of one C counter into the input of the next C counter as shown in Figure 6–28.

Figure 6–28. Counter Cascading



Note to Figure 6–28:
(1) n = 6 or n = 9

When cascading post-scale counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter settings. For example, if C0 = 40 and C1 = 20, then the cascaded value is C0*C1 = 800.

Post-scale counter cascading is set in the configuration file. It cannot be done using PLL reconfiguration.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on the PLL post-scale counters. The duty-cycle setting is achieved by a low and high time-count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The post-scale counter value determines the precision of the duty cycle. The precision is defined by 50% divided by the post-scale counter value. For example, if the `C0` counter is 10, then steps of 5% are possible for duty-cycle choices between 5% to 90%.

If the PLL is in external feedback mode, you must set the duty cycle for the counter driving the `fbin` pin to 50%. Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

PLL Control Signals

You can use the following three signals to observe and control the PLL operation and resynchronization.

pfdena

Use the `pfdena` signal to maintain the most recent locked frequency so your system has time to store its current settings before shutting down. The `pfdena` signal controls the PFD output with a programmable gate. If you disable PFD, the VCO operates at its most recent set value of control voltage and frequency with some long-term drift to a lower frequency. The PLL continues running even if it goes out-of-lock or the input clock is disabled. You can use either your own control signal or the control signals available from the clock switchover circuit (`activeclock`, `clkbad[0]`, or `clkbad[1])` to control `pfdena`.

areset

The areset signal is the reset or resynchronization input for each PLL. The device input pins or internal logic can drive these input signals. When areset is driven high, the PLL counters reset, clearing the PLL output and placing the PLL out-of-lock. The VCO is then set back to its nominal setting. When areset is driven low again, the PLL will resynchronize to its input as it re-locks.

You should assert the areset signal every time the PLL loses lock to guarantee the correct phase relationship between the PLL input clock and output clocks. You can set up the PLL to automatically reset (self reset) upon a loss-of-lock condition using the Quartus II MegaWizard. You should include the areset signal in designs if any of the following conditions are true:

- PLL reconfiguration or clock switchover is enabled in the design.
- Phase relationships between the PLL input and output clocks need to be maintained after a loss-of-lock condition.

If the input clock to the PLL is not toggling or is unstable upon power up, assert the areset signal after the input clock is stable and within specifications.

locked

The locked output of the PLL indicates that the PLL has locked onto the reference clock and the PLL clock outputs are operating at the desired phase and frequency set in the Quartus II software MegaWizard. Without any additional circuitry, the lock signal may toggle as the PLL begins the locking process. The lock detection circuit provides a signal to the core logic that gives an indication if the feedback clock has locked onto the reference clock both in phase and frequency.

Altera recommends that you use the areset and locked signals in your designs to control and observe the status of your PLL.

Clock Switchover

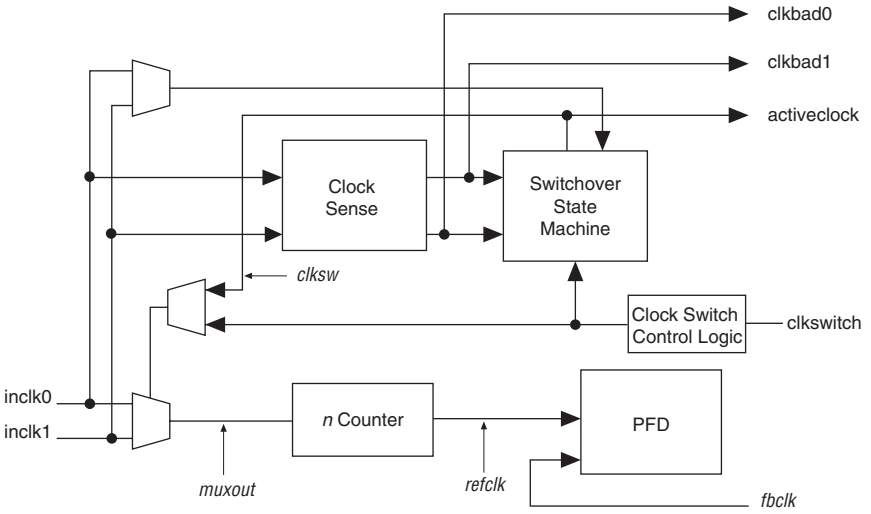
The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual-clock domain application such as in a system that turns on the redundant clock if the previous clock stops running. The design can perform clock switchover automatically, when the clock is no longer toggling or based on a user control signal, clkswitch.

The following clock switchover modes are supported in Stratix III PLLs:

- Automatic switchover: The clock sense circuit monitors the current reference clock and if it stops toggling, automatically switches to the other clock `inclk0` or `inclk1`.
- Manual clock switchover: Clock switchover is controlled via the `clkswitch` signal in this mode. When the `clkswitch` signal goes from logic low to logic high, and stays high for at least three clock cycles, the reference clock to the PLL is switched from `inclk0` to `inclk1`, or vice-versa.
- Automatic switchover with manual override: This mode combines Modes 1 and 2. When the `clkswitch` signal goes high, it overrides automatic clock switchover mode.

Stratix III device PLLs support a fully configurable clock switchover capability. Figure 6–29 shows the block diagram of the switchover circuit built into the PLL. When the current reference clock is not present, the clock sense block automatically switches to the backup clock for PLL reference. The clock switchover circuit also sends out three status signals—`clkbad[0]`, `clkbad[1]`, and `activeclock`—from the PLL to implement a custom switchover circuit in the logic array. You can select a clock source as the backup clock by connecting it to the `inclk1` port of the PLL in your design.

Figure 6–29. Automatic Clock Switchover Circuit Block Diagram



Automatic Clock Switchover

Use the switchover circuitry to automatically switch between inclk0/inclk1 when the current reference clock to the PLL stops toggling. For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal (clksw) that controls the multiplexer select input as shown in Figure 6–29. In this case, inclk1 becomes the reference clock for the PLL. When using the automatic switchover mode, you can switch back and forth between inclk0 and inclk1 clocks any number of times, when one of the two clocks fails and the other clock is available.

When using the automatic clock switchover mode, the following requirements need to be satisfied:

- Both clock inputs need to be running.
- The period of the two clock inputs can differ by no more than 100% (2×).

If the current clock input stops toggling while the other clock is also not toggling, switchover will not be initiated and the clkbad[0:1] signals will not be valid. Also, if both clock inputs are not the same frequency, but their period difference is within 100%, the clock sense block will detect when a clock stops toggling, but the PLL may lose lock after the switchover is completed and need time to relock.

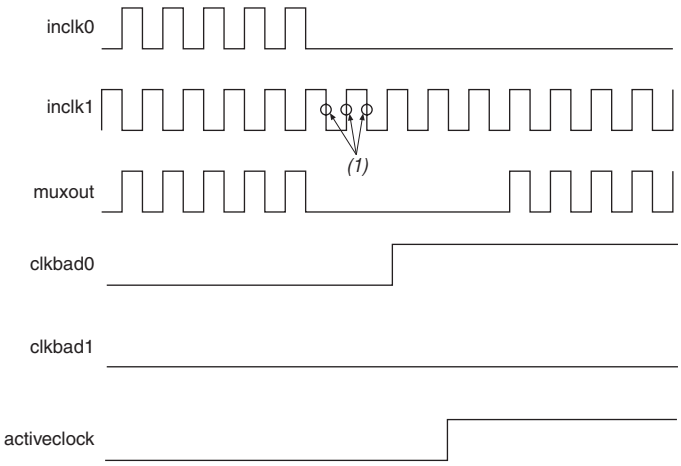
Altera recommends resetting the PLL using the areset signal to maintain the phase relationships between the PLL input and output clocks when using clock switchover.

When using automatic switchover mode, the clkbad[0] and clkbad[1] signals indicate the status of the two clock inputs. When they are asserted, the clock sense block has detected that the corresponding clock input has stopped toggling. These two signals are not valid if the frequency difference between inclk0 and inclk1 is greater than 20%.

The activeclock signal indicates which of the two clock inputs (inclk0 or inclk1) is being selected as the reference clock to the PLL. When the frequency difference between the two clock inputs is more than 20%, the activeclock signal is the only valid status signal.

Figure 6–30 shows an example waveform of the switchover feature when using the automatic switchover mode. In this example, the inclk0 signal is stuck low. After the inclk0 signal is stuck at low for approximately two clock cycles, the clock sense circuitry drives the clkbad[0] signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the clksw signal to switch to the backup clock, inclk1.

Figure 6–30. Automatic Switchover Upon Loss of Clock Detection



Note to Figure 6–30:

(1) Switchover is enabled on the falling edge of `inclk0` or `inclk1`, depending on which clock is available. In this figure, switchover is enabled on the falling edge of `inclk1`.

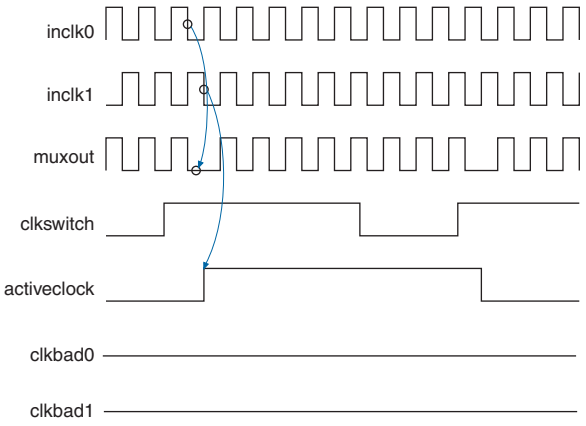
Manual Override

In the automatic switchover with manual override mode, you can use the `clkswitch` input for user- or system-controlled switch conditions. You can use this mode for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 200 MHz, you must control the switchover using `clkswitch` because the automatic clock-sense circuitry cannot monitor clock input (`inclk0`, `inclk1`) frequencies with a frequency difference of more than 100% (2×). This feature is useful when the clock sources originate from multiple cards on the backplane, requiring a system-controlled switchover between the frequencies of operation. You should choose the backup clock frequency and set the `m`, `n`, `c`, and `k` counters accordingly so the VCO operates within the recommended operating frequency range of 600 to 1,300 MHz. The altpll Megawizard Plug-in Manager notifies users if a given combination of `inclk0` and `inclk1` frequencies cannot meet this requirement.

Figure 6–31 shows an example of a waveform illustrating the switchover feature when controlled by `clkswitch`. In this case, both clock sources are functional and `inclk0` is selected as the reference clock. `clkswitch` goes high, which starts the switchover sequence. On the falling edge of `inclk0`, the counter's reference clock, `muxout`, is gated off to prevent any clock glitching. On the falling edge of `inclk1`, the reference clock

multiplexer switches from inclk0 to inclk1 as the PLL reference, and the activeclock signal changes to indicate which clock is currently feeding the PLL.

Figure 6–31. Clock Switchover Using the clkswitch (Manual) Control

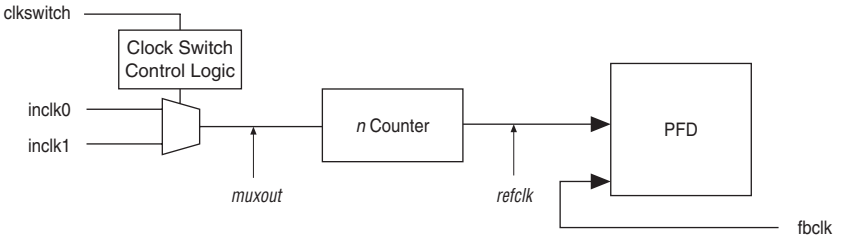


In this mode, the activeclock signal mirrors the clkswitch signal. As both clocks are still functional during the manual switch, neither clkbad signal goes high. Since the switchover circuit is positive-edge sensitive, the falling edge of the clkswitch signal does not cause the circuit to switch back from inclk1 to inclk0. When the clkswitch signal goes high again, the process repeats. clkswitch and automatic switch only work if the clock being switched to is available. If the clock is not available, the state machine waits until the clock is available.

Manual Clock Switchover

In manual clock switchover mode, the clkswitch signal controls whether inclk0 or inclk1 is selected as the input clock to the PLL. By default, inclk0 is selected. A low-to-high transition on clkswitch and clkswitch being held high for at least three inclk cycles initiates a clock switchover event. You must bring clkswitch back low again in order to perform another switchover event in the future. If you do not require another switchover event in the future you can leave clkswitch in a logic high state after the initial switch. Pulsing clkswitch high for at least three inclk cycles performs another switchover event. If inclk0 and inclk1 are different frequencies and are always running, the clkswitch minimum high time must be greater than or equal to three of the slower frequency inclk0/inclk1 cycles. Figure 6–32 shows the block diagram of the manual switchover circuit.

Figure 6–32. Manual Clock Switchover Circuitry in Stratix III PLLs



For more information on PLL software support in the Quartus II software, refer to the *altpll Megafunction User Guide*.

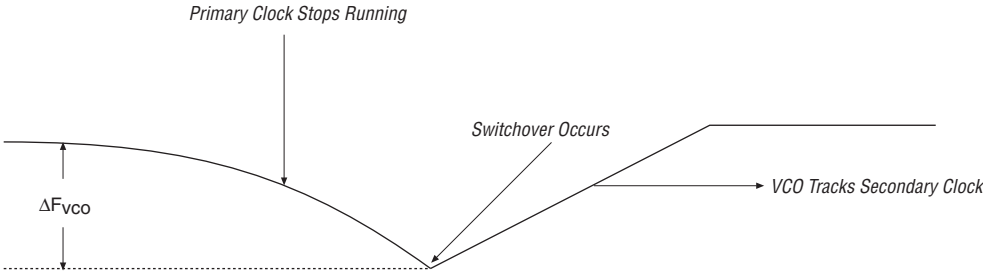
Guidelines

Use the following guidelines when implementing clock switchover in Stratix III PLLs.

- Automatic clock switchover requires that the `inclk0` and `inclk1` frequencies be within 100% (2×) of each other. Failing to meet this requirement causes the `clkbad[0]` and `clkbad[1]` signals to not function properly.
- When using manual clock switchover, the difference between `inclk0` and `inclk1` can be more than 100% (2×). However, differences in frequency and / or phase of the two clock sources will likely cause the PLL to lose lock. Resetting the PLL ensures that the correct phase relationships are maintained between input and output clocks.
- Applications that require a clock switchover feature and a small frequency drift should use a low-bandwidth PLL. The low bandwidth PLL reacts more slowly than a high-bandwidth PLL to reference input clock changes. When the switchover happens, a low bandwidth PLL propagates the stopping of the clock to the output more slowly than a high-bandwidth PLL. However, be aware that the low-bandwidth PLL also increases lock time.
- After a switchover occurs, there may be a finite resynchronization period for the PLL to lock onto a new clock. The exact amount of time it takes for the PLL to re-lock depends on the PLL configuration.
- The phase relationship between the input clock to the PLL and the output clock from the PLL is important in your design. Assert `areset` for at least 10 ns after performing a clock switchover. Wait for the locked signal to go high and be stable before re-enabling the output clocks from the PLL.

- Figure 6–33 shows how the VCO frequency gradually decreases when the current clock is lost and then increases as the VCO locks on to the backup clock.

Figure 6–33. VCO Switchover Operating Frequency



- Disable the system during clock switchover if it is not tolerant of frequency variations during the PLL resynchronization period. You can use the `clkbad[0]` and `clkbad[1]` status signals to turn off the PFD (`PFDENA = 0`) so the VCO maintains its most recent frequency. You can also use the state machine to switch over to the secondary clock. When the PFD is re-enabled, output clock-enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clock(s).

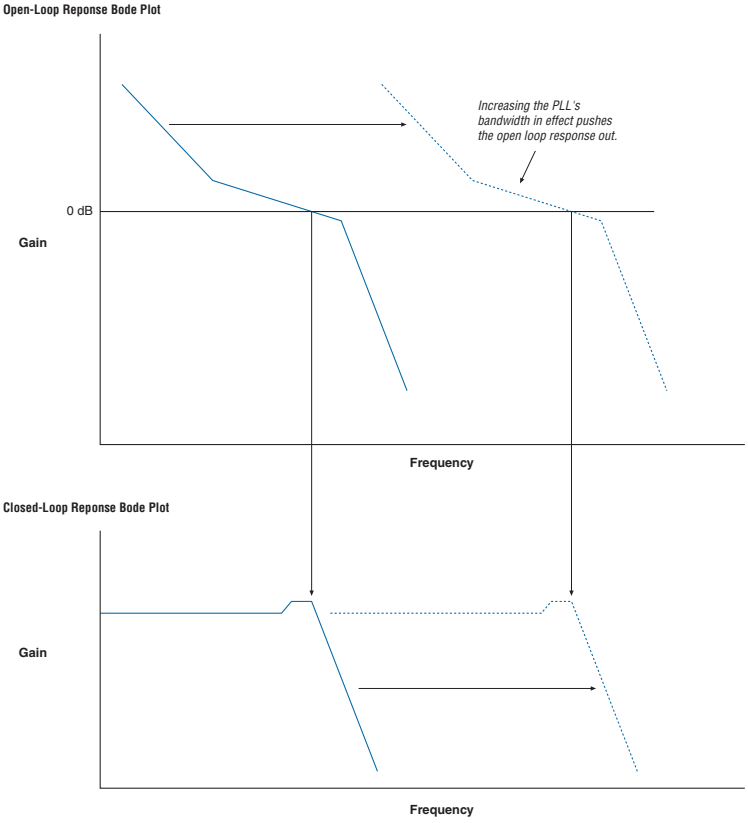
Programmable Bandwidth

Stratix III PLLs provide advanced control of the PLL bandwidth using the PLL loop's programmable characteristics, including loop filter and charge pump.

Background

PLL bandwidth is the measure of the PLL's ability to track the input clock and its associated jitter. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open loop PLL response. As Figure 6–34 shows, these points correspond to approximately the same frequency. Stratix III PLLs provide three bandwidth settings—low, medium (default), and high.

Figure 6–34. Open- and Closed-Loop Response Bode Plots



A high-bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low-bandwidth PLL filters out reference clock jitter but increases lock time. Stratix III PLLs allow you to control the bandwidth over a finite range to customize the PLL characteristics for a particular application. The programmable bandwidth feature in Stratix III PLLs benefits applications requiring clock switchover.

A high-bandwidth PLL can benefit a system that needs to accept a spread-spectrum clock signal. Stratix III PLLs can track a spread-spectrum clock by using a high-bandwidth setting. Using a low-bandwidth in this case could cause the PLL to filter out the jitter on the input clock.

A low-bandwidth PLL can benefit a system using clock switchover. When the clock switchover happens, the PLL input temporarily stops. A low-bandwidth PLL reacts more slowly to changes on its input clock and takes longer to drift to a lower frequency (caused by the input stopping) than a high-bandwidth PLL.

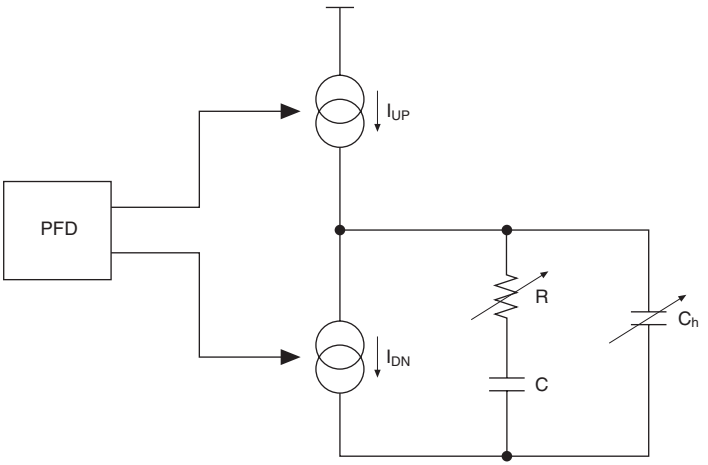
Implementation

Traditionally, external components such as the VCO or loop filter control a PLL's bandwidth. Most loop filters consist of passive components such as resistors and capacitors that take up unnecessary board space and increase cost. With Stratix III PLLs, all the components are contained within the device to increase performance and decrease cost.

When you specify the bandwidth setting (low, medium, or high) in the altpll Megawizard Plug-in Manager, the Quartus II software automatically sets the corresponding charge pump and loop filter (`Icp`, `R`, `C`) values to achieve the desired bandwidth range.

Figure 6–35 shows the loop filter and the components that you can set using the Quartus II software. The components are the loop filter resistor, `R`, the high frequency capacitor, C_H, and the charge pump current, I_{UP} or I_{DN}.

Figure 6–35. Loop Filter Programmable Components



Phase-Shift Implementation

Phase shift is used to implement a robust solution for clock delays in Stratix III devices. Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase output and counter starting time is the most accurate method of inserting delays, since it is purely based on counter settings, which are independent of process, voltage, and temperature.

You can phase-shift the output clocks from the Stratix III PLLs in either of these two resolutions:

- Fine resolution using VCO phase taps
- Coarse resolution using counter starting time

Fine-resolution phase shifts are implemented by allowing any of the output counters (`C[n..0]`) or the `m` counter to use any of the eight phases of the VCO as the reference clock. This allows you to adjust the delay time with a fine resolution. The minimum delay time that you can insert using this method is defined by:

$$\Phi_{fine} = \frac{1}{8} T_{VCO} = \frac{1}{8 f_{VCO}} = \frac{N}{8 M f_{REF}}$$

where f_{REF} is the input reference clock frequency.

For example, if f_{REF} is 100 MHz, *n* is 1, and *m* is 8, then f_{VCO} is 800 MHz and Φfine equals 156.25 ps. This phase shift is defined by the PLL operating frequency, which is governed by the reference clock frequency and the counter settings.

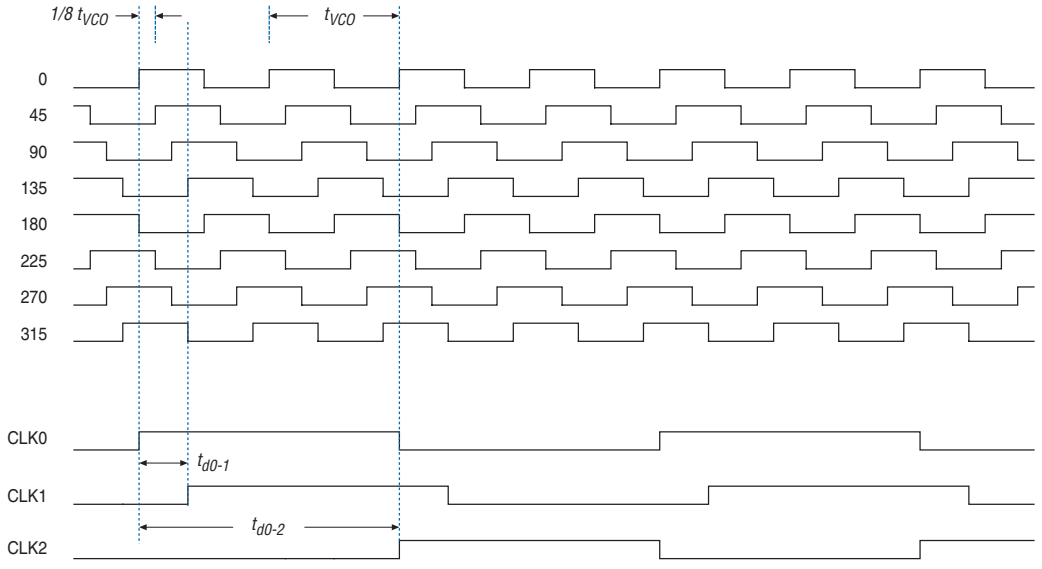
Coarse-resolution phase shifts are implemented by delaying the start of the counters for a predetermined number of counter clocks. You can express coarse phase shift as:

$$\Phi_{coarse} = \frac{C-1}{f_{VCO}} = \frac{(C-1)N}{M f_{REF}}$$

where *C* is the count value set for the counter delay time, (this is the initial setting in the PLL usage section of the compilation report in the Quartus II software). If the initial value is 1, C – 1 = 0° phase shift.

Figure 6–36 shows an example of phase-shift insertion with the fine resolution using the VCO phase taps method. The eight phases from the VCO are shown and labeled for reference. For this example, CLK0 is based off the 0phase from the VCO and has the *C* value for the counter set to one. The CLK1 signal is divided by four, two VCO clocks for high time and two VCO clocks for low time. CLK1 is based off the 135° phase tap from the VCO and also has the *C* value for the counter set to one. The CLK1 signal is also divided by 4. In this case, the two clocks are offset by 3 Φ_{FINE}. CLK2 is based off the 0phase from the VCO but has the *C* value for the counter set to three. This arrangement creates a delay of 2 Φ_{COARSE} (two complete VCO periods).

Figure 6–36. Delay Insertion Using VCO Phase Output and Counter Delay Time



You can use the coarse- and fine-phase shifts to implement clock delays in Stratix III devices.

Stratix III devices support dynamic phase-shifting of VCO phase taps only. The phase shift is reconfigurable any number of times, and each phase shift takes about one SCANCLK cycle, allowing you to implement large phase shifts quickly.

PLL Reconfiguration

Phase-locked loops (PLLs) use several divide counters and different voltage-controlled oscillator (VCO) phase taps to perform frequency synthesis and phase shifts. In Stratix III PLLs, you can reconfigure both the counter settings and phase-shift the PLL output clock in real time. You can also change the charge pump and loop-filter components, which dynamically affects the PLL bandwidth. You can use these PLL components to update the output-clock frequency and the PLL bandwidth and to phase-shift in real time, without reconfiguring the entire Stratix III device.

The ability to reconfigure the PLL in real time is useful in applications that operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output-clock phase dynamically. For instance, a system generating test patterns is required to generate and transmit patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring the PLL components in real time allows you to switch between two such output frequencies within a few microseconds. You can also use this feature to adjust clock-to-out (t_{CO}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

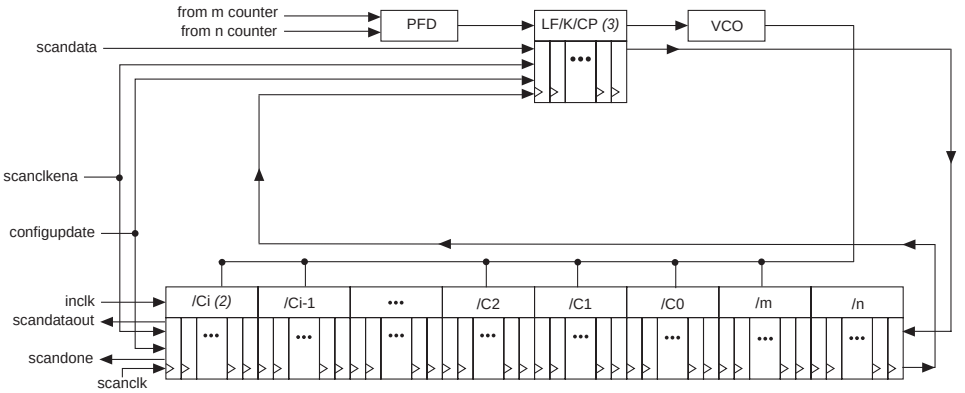
PLL Reconfiguration Hardware Implementation

The following PLL components are reconfigurable in real time:

- Pre-scale counter (n)
- Feedback counter (m)
- Post-scale output counters (C0 – C9)
- Post VCO Divider (K)
- Dynamically adjust the charge-pump current (Icp) and loop-filter components (R, C) to facilitate reconfiguration of the PLL bandwidth

Figure 6–37 shows how PLL counter settings can be dynamically adjusted by shifting their new settings into a serial shift-register chain or scan chain. Serial data is input to the scan chain via the scandataport and shift registers are clocked by scanclk. The maximum scanclk frequency is 100 MHz. Serial data is shifted through the scan chain as long as the scanclkena signal stays asserted. After the last bit of data is clocked, asserting the configupdate signal for at least one scanclk clock cycle causes the PLL configuration bits to be synchronously updated with the data in the scan registers.

Figure 6–37. PLL Reconfiguration Scan Chain



Notes to Figure 6–37:

(1) The Stratix III Left/Right PLLs support C0 – C6 counters.

(2) i = 6 or i = 9.

(3) This figure shows the corresponding scan register for the K counter in between the scan registers for the charge pump and loop filter. The K counter is physically located after the VCO.

The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, all counters are not updated simultaneously.

Table 6–15 shows how these signals can be driven by the programmable logic device (PLD) logic array or I/O pins.

Table 6–15. Real-Time PLL Reconfiguration Ports (Part 1 of 2)

PLL Port Name	Description	Source	Destination
scandata	Serial input data stream to scan chain.	Logic array or I/O pin	PLL reconfiguration circuit
scanclk	Serial clock input signal. This clock can be free running.	GCLK/RCLK or I/O pins	PLL reconfiguration circuit
scanclkena	Enables scanclk and allows the scandata to be loaded in the scan chain. Active high	Logic array or I/O pin	PLL reconfiguration circuit
configupdate	Writes the data in the scan chain to the PLL. Active high	Logic array or I/O pin	PLL reconfiguration circuit

Table 6–15. Real-Time PLL Reconfiguration Ports (Part 2 of 2)

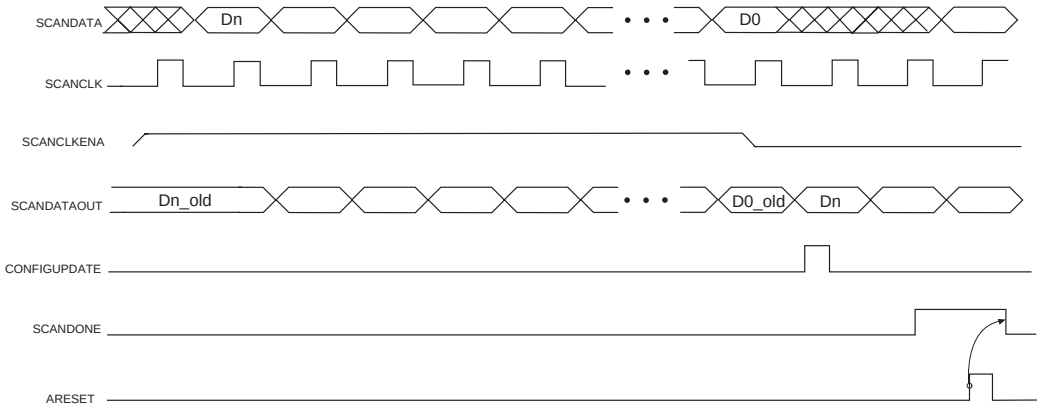
PLL Port Name	Description	Source	Destination
scandone	Indicates when the PLL has finished reprogramming. A rising edge indicates the PLL has begun reprogramming. A falling edge indicated the PLL has finished reprogramming.	PLL reconfiguration circuit	Logic array or I/O pins
scandataout	Used to output the contents of the scan chain.	PLL reconfiguration circuit	Logic array or I/O pins

The procedure to reconfigure the PLL counters is shown below:

1. The scanclkena signal is asserted at least one scanclk cycle prior to shifting in the first bit of scandata (Dn).
2. Serial data (scandata) is shifted into the scan chain on the 2nd rising edge of scanclk.
3. After all 234 bits (Top / Bottom PLLs) or 180 bits (Left / Right PLLs) have been scanned into the scan chain, the scanclkena signal is de-asserted to prevent inadvertent shifting of bits in the scan chain.
4. The configupdate signal is asserted for one scanclk cycle to update the PLL counters with the contents of the scan chain.
5. The scandone signal goes high indicating the PLL is being reconfigured. A falling edge indicates the PLL counters have been updated with new settings.
6. Reset the PLL using the areset signal if you make any changes to the M or N counters or the Icp, R, or C settings.
7. Steps 1-5 can be repeated to reconfigure the PLL any number of times.

Figure 6–38 shows a functional simulation of the PLL reconfiguration feature.

Figure 6–38. PLL Reconfiguration Waveform



When you reconfigure the counter clock frequency, you cannot reconfigure the corresponding counter phase shift settings using the same interface. Instead, reconfigure the phase shifts in real time using the dynamic phase shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase shift setting (for example, 90 degrees) on the clock output, you must reconfigure the phase shift immediately after reconfiguring the counter clock frequency.

Post-Scale Counters (C0 to C9)

The multiply or divide values and duty cycle of post-scale counters can be reconfigured in real time. Each counter has an 8-bit high-time setting and an 8-bit low-time setting. The duty cycle is the ratio of output high- or low-time to the total cycle time, which is the sum of the two. Additionally, these counters have two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

When the `rbypass` bit is set to 1, it bypasses the counter, resulting in a divide by 1. When this bit is set to 0, the high- and low-time counters are added to compute the effective division of the VCO output frequency. For example, if the post-scale divide factor is 10, the high- and low-count values could be set to 5 and 5, respectively, to achieve a 50-50% duty cycle. The PLL implements this duty cycle by transitioning the output clock

from high to low on the rising edge of the VCO output clock. However, a 4 and 6 setting for the high- and low-count values, respectively, would produce an output clock with 40-60% duty cycle.

The `rselodd` bit indicates an odd divide factor for the VCO output frequency along with a 50% duty cycle. For example, if the post-scale divide factor is 3, the high- and low-time count values could be set to 2 and 1, respectively, to achieve this division. This implies a 67%-33% duty cycle. If you need a 50%-50% duty cycle, you can set the `rselodd` control bit to 1 to achieve this duty cycle despite an odd division factor. The PLL implements this duty cycle by transitioning the output clock from high to low on a falling edge of the VCO output clock. When you set `rselodd` = 1, you subtract 0.5 cycles from the high time and you add 0.5 cycles to the low time. For example:

- High-time count = 2 cycles
- Low-time count = 1 cycle
- `rselodd` = 1 effectively equals:
  - High-time count = 1.5 cycles
  - Low-time count = 1.5 cycles
  - Duty cycle = (1.5 / 3) % high-time count and (1.5 / 3) % low-time count

Scan Chain Description

The length of the scan chain varies for different Stratix III PLLs. The Top / Bottom PLLs have 10 post-scale counters and a 234-bit scan chain, while the Left / Right PLLs have 7 post-scale counters and a 180-bit scan chain. Table 6–16 shows the number of bits for each component of a Stratix III PLL.

Table 6–16. Top/Bottom PLL Reprogramming Bits (Part 1 of 2)

Block Name	Number of Bits		Total
	Counter	Other *(1)*	
C9 *(2)*	16	2	18
C8	16	2	18
C7	16	2	18
C6 *(3)*	16	2	18
C5	16	2	18
C4	16	2	18
C3	16	2	18
C2	16	2	18

Table 6–16. Top/Bottom PLL Reprogramming Bits (Part 2 of 2)

Block Name	Number of Bits		Total
	Counter	Other *(1)*	
C1	16	2	18
C0	16	2	18
M	16	2	18
N	16	2	18
Charge Pump	0	9	9
VCO Post-Scale divider (K)	1	0	1
Loop Filter *(4)*	0	9	9
Total number of bits	—	—	234

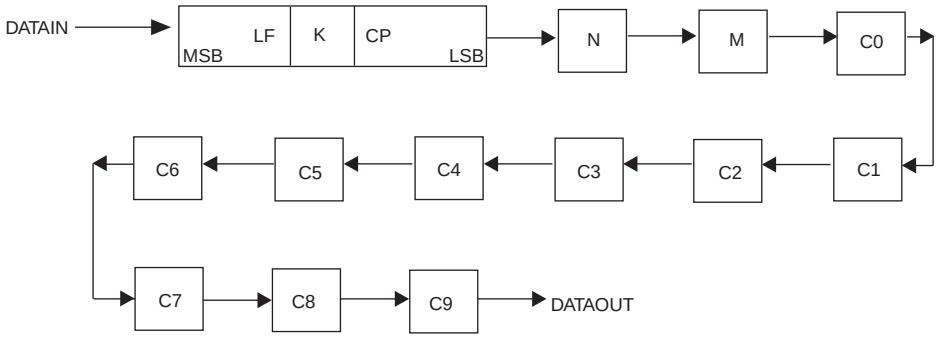
Notes to Table 6–16:

(1) Includes two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.
(2) LSB bit for C9 low-count value is the first bit shifted into the scan chain for Top / Bottom PLLs.
(3) LSB bit for C6 low-count value is the first bit shifted into the scan chain for Left / Right PLLs.
(4) MSB bit for loop filter is the last bit shifted into the scan chain.

Table 6–16 shows the scan chain order of PLL components for Top / Bottom PLLs which have 10 post-scale counters. The order of bits is the same for the Left / Right PLLs, but the reconfiguration bits start with the C6 post-scale counter.

Figure 6–39 shows the scan-chain order of PLL components for the Top / Bottom PLLs.

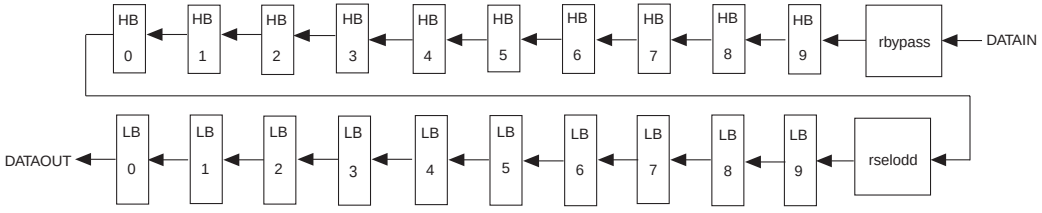
Figure 6–39. Scan-Chain Order of PLL Components for Top/Bottom PLLs *Note (1)*



Note to Figure 6–39:
(1) Left / Right PLLs have the same scan-chain order. The post-scale counters end at C6.

Figure 6–40 shows the scan-chain bit-order sequence for post-scale counters in all Stratix III PLLs.

Figure 6–40. Scan-Chain Bit-Order Sequence for Post-Scale Counters in Stratix III PLLs



Charge Pump and Loop Filter

You can reconfigure the charge-pump and loop-filter settings to update the PLL bandwidth in real time. Tables 6–17, 6–18, and 6–19 show the possible settings for charge pump current (I_{cp}), loop-filter resistor (R), and capacitor (C) values for Stratix III PLLs.

Table 6–17. charge_pump_current Bit Settings

CP[2]	CP[1]	CP[0]	Decimal Value for Setting
0	0	0	0
0	0	1	1
0	1	1	3
1	1	1	7

Table 6–18. loop_filter_r Bit Settings

LFR[4]	LFR[3]	LFR[2]	LFR[1]	LFR[0]	Decimal Value for Setting
0	0	0	0	0	0
0	0	0	1	1	3
0	0	1	0	0	4
0	1	0	0	0	8
1	0	0	0	0	16
1	0	0	1	1	19
1	0	1	0	0	20
1	1	0	0	0	24
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	1	0	30

Table 6–19. loop_filter_c Bit Settings		
LFC[1]	**LFC[0]**	**Decimal Value for Setting**
0	0	0
0	1	1
1	1	3

Bypassing PLL

Bypassing a PLL counter results in a multiply (m counter) or a divide (n and C0 to C9 counters) factor of one.

Table 6–20 shows the settings for bypassing the counters in Stratix III PLLs.

Table 6–20. PLL Counter Settings											
PLL Scan Chain Bits [0..10] Settings											
LSB *(2)*										**MSB** *(1)*	**Description**
0	X	X	X	X	X	X	X	X	X	1 *(3)*	PLL counter bypassed
X	X	X	X	X	X	X	X	X	X	0 *(3)*	PLL counter not bypassed because bit 10 (MSB) is set to 0

Notes to Table 6–20:
(1) Most significant bit (MSB)
(2) Least significant bit (LSB).
(3) Counter-bypass bit.

To bypass any of the PLL counters, set the bypass bit to **1**. The values on the other bits is ignored. To bypass the VCO post-scale counter (K), set the corresponding bit to **0**.

Dynamic Phase-Shifting

The dynamic phase-shifting feature allows the output phases of individual PLL outputs to be dynamically adjusted relative to each other and to the reference clock without the need to send serial data through the scan chain of the corresponding PLL. This feature simplifies the interface and allows you to quickly adjust clock-to-out (t_{CO}) delays by changing

the output clock phase-shift in real time. This adjustment is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 of the VCO frequency at a time. The output clocks are active during this phase-reconfiguration process.

Table 6–21 shows the control signals that are used for dynamic phase-shifting.

Table 6–21. Dynamic Phase-Shifting Control Signals

Signal Name	Description	Source	Destination
PHASECOUNTERSELECT[3:0]	Counter select. Four bits decoded to select either the M or one of the C counters for phase adjustment. One address maps to select all C counters. This signal is registered in the PLL on the rising edge of SCANCLK.	Logic array or I/O pins	PLL reconfiguration circuit
PHASEUPDOWN	Selects dynamic phase shift direction; 1= UP; 0= DOWN. Signal is registered in the PLL on the rising edge of SCANCLK.	Logic array or I/O pin	PLL reconfiguration circuit
PHASESTEP	Logic high enables dynamic phase shifting.	Logic array or I/O pin	PLL reconfiguration circuit
SCANCLK	Free running clock from core used in combination with PHASESTEP to enable/disable dynamic phase shifting. Shared with SCANCLK for dynamic reconfiguration.	GCLK/RCLK or I/O pin	PLL reconfiguration circuit
PHASEDONE	When asserted it indicates to core-logic that the phase adjustment is complete and PLL is ready to act on a possible second adjustment pulse. Asserts based on internal PLL timing. De-asserts on rising edge of SCANCLK.	PLL reconfiguration circuit	Logic array or I/O pins

Table 6–22 shows the PLL counter selection based on the corresponding PHASECOUNTERSELECT setting.

Table 6–22. Phase Counter Select Mapping

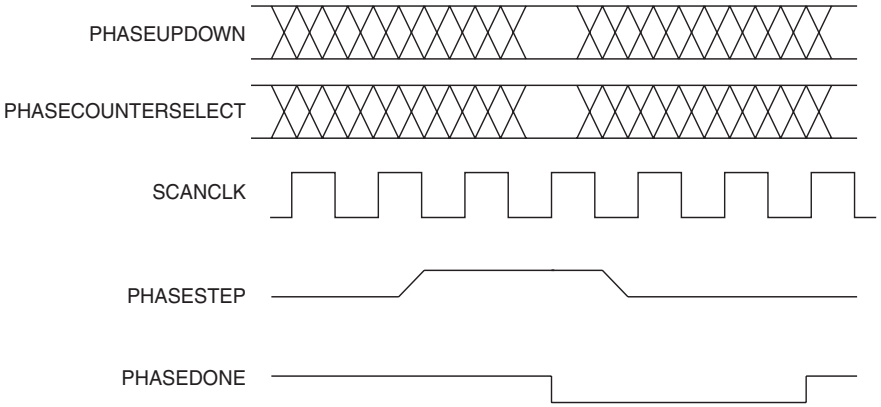
PHASECOUNTERSELECT[3]	[2]	[1]	[0]	Selects
0	0	0	0	All Output Counters
0	0	0	1	M Counter
0	0	1	0	C0 Counter
0	0	1	1	C1 Counter
0	1	0	0	C2 Counter
0	1	0	1	C3 Counter
0	1	1	0	C4 Counter
0	1	1	1	C5 Counter
1	0	0	0	C6 Counter
1	0	0	1	C7 Counter
1	0	1	0	C8 Counter
1	0	1	1	C9 Counter

The procedure to perform one dynamic phase-shift step is as follows:

1. Set phaseupdown and phasecounterselect as required.
2. Assert phasestep. Each phasestep pulse enables one phase shift. The phasestep pulses must be at least one scanclk cycle apart.
3. Wait for phasedone to go low.
4. Deassert phasestep.
5. Wait for phasedone to go high.
6. Repeat steps 1-5 as many times as required to perform multiple phase-shifts.

All signals are synchronous to scanclk. They are latched on scanclk edges and must meet t_{su} / t_h requirements with respect to scanclk edges.

Figure 6–41. Dynamic Phase Shifting Waveform



Dynamic phase-shifting can be repeated indefinitely. All signals are synchronous to `scanclk` and must meet t_{su} / t_h requirements with respect to `scanclk` edges.

The `phasestep` signal is latched on the negative edge of `scanclk`. In Figure 6–41, this is shown by the second `scanclk` falling edge. `phasestep` must stay high for at least two `scanclk` cycles. On the second `scanclk` rising edge after `phasestep` is latched (the fourth `scanclk` rising edge in Figure 6–41), the values of `phaseupdown` and `phasecounterselect` are latched and the PLL starts dynamic phase-shifting for the specified counter(s) and in the indicated direction. On the fourth `scanclk` rising edge, `phasedone` goes high to low and remains low until the PLL finishes dynamic phase-shifting. You can perform another dynamic phase-shift after the `phasedone` signal goes from low to high.

Depending on the VCO and `scanclk` frequencies, `phasedone` low time may be greater than or less than one `scanclk` cycle. The maximum time for reconfiguring phase shift dynamically is to be determined (TBD) based on device characterization.

After `phasedone` goes from low to high, you can perform another dynamic phase shift.

For details on the altpll_reconfig Megawizard Plug-In Manager, refer to the *altpll_reconfig Megafunction Users Guide*.

Spread-Spectrum Tracking

Stratix III devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of PLL. Stratix III PLLs can track a spread-spectrum input clock as long as it is within the input-jitter tolerance specifications. Stratix III devices cannot internally generate spread-spectrum clocks.

PLL Specifications

Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook* for information on PLL timing specifications.

Conclusion

Stratix III device PLLs provide you with complete control of device clocks and system timing. The ability to reconfigure the PLL counter clock frequency and phase shift in real time can be especially useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output-clock phase-shift dynamically. These PLLs are also capable of offering flexible system-level clock management that was previously only available in discrete PLL devices. Stratix III PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.

Document Revision History

Table 6–23 shows the revision history for this document.

Table 6–23. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Changed frequency difference between inclk0 and inclk1 to more than 20% instead of 100% on page 42. Updated Table 6–16, note to Figure 6–17, and Figure 6–19.	—
November 2006 v1.0	Initial Release	—

Section II. I/O Interfaces

This section provides information on Stratix® III device I/O features, external memory interfaces, and high-speed differential interfaces with DPA. This section includes the following chapters:

- Chapter 7, Stratix III Device I/O Features
- Chapter 8, External Memory Interfaces in Stratix III Devices
- Chapter 9, High-Speed Differential I/O Interfaces and DPA in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

7. Stratix III Device I/O Features

SIII51007-1.1

Introduction

Stratix® III I/Os are specifically designed for ease of use and rapid system integration while simultaneously providing the high bandwidth required to maximize internal logic capabilities and produce system-level performance. Independent modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic termination and output control provide best-in-class signal integrity. Numerous I/O features assist in high-speed data transfer into and out of the device, including:

- Single-ended, non-voltage-referenced and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), reduced swing differential signal (RSDS), mini-LVDS, high-speed transceiver logic (HSTL), and stub series terminated logic (SSTL)
- Single data rate (SDR) and half data rate (HDR - half frequency and twice data width of SDR) input and output options
- Up to 132 full duplex 1.25 Gbps true LVDS channels (132 Tx + 132 Rx) on the row I/O banks
- Hard DPA block with serializer/deserializer (SERDES)
- De-skew, read and write leveling, and clock-domain crossing functionality
- Programmable output current strength
- Programmable slew rate
- Programmable delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)
- Differential OCT

Stratix III I/O Standards Support

Stratix III devices support a wide range of industry I/O standards. Table 7–1 shows the I/O standards Stratix III devices support as well as the typical applications. Stratix III devices support a V_{CCIO} voltage level of 3.0, 2.5, 1.8, 1.5, and 1.2 V. For interface with 3.3-V I/O standard, Stratix III requires an external voltage regulator to regulate V_{CCIO} to 3.0 V.

Table 7–1. Stratix III I/O Standard Applications (Part 1 of 2)

I/O Standard	Application
3.0-V LVTTL	General purpose
3.0-V LVCMOS	General purpose
2.5-V LVTTL/LVCMOS	General purpose
1.8-V LVTTL/LVCMOS	General purpose
1.5-V LVTTL/LVCMOS	General purpose
1.2-V LVTTL/LVCMOS	General purpose
3.0-V PCI	PC and embedded system
3.0-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
SSTL-15 Class I	DDR3 SDRAM
SSTL-15 Class II	DDR3 SDRAM
HSTL-18 Class I	QDRII/RLDRAM II
HSTL-18 CLass II	QDRII/RLDRAM II
HSTL-15 Class I	QDRII/QDRII+/RLDRAM II
HSTL-15 Class II	QDRII/QDRII+/RLDRAM II
HSTL-12 Class I	Memory interface
HSTL-12 Class II	Memory interface
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM
Differential SSTL-18 Class II	DDR2 SDRAM
Differential SSTL-15 Class I	DDR3 SDRAM
Differential SSTL-15 Class II	DDR3 SDRAM
Differential HSTL-18 Class I	Clock interfaces
Differential HSTL-18 Class II	Clock interfaces
Differential HSTL-15 Class I	Clock interfaces
Differential HSTL-15 Class II	Clock interfaces
Differential HSTL-12 Class I	Clock interfaces
Differential HSTL-12 Class II	Clock interfaces

Table 7–1. Stratix III I/O Standard Applications (Part 2 of 2)	
I/O Standard	**Application**
LVDS	High-speed communications
RSDS	Flat panel display
mini-LVDS	Flat panel display
LVPECL	Video graphics and clock distribution

I/O Standards and Voltage Levels

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 7–2 shows the supported I/O standards and the typical values for input and output V_{CCIO}, V_{CCPD}, V_{REF}, and board V_{TT}.

Table 7–2. Stratix III I/O Standards and Voltage Levels *Notes (1), (2), (3)* **(Part 1 of 3)**

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Top and Bottom I/O Banks	Left and Right I/O Banks	Top and Bottom I/O Banks	Left and Right I/O Banks			
3.0-V LVTTL	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	NA	NA
3.0-V LVCMOS	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	NA	NA
2.5-V LVTTL/LVCMOS	JESD8-5	3.0/2.5	3.0/2.5	2.5	2.5	2.5	NA	NA
1.8-V LVTTL/LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	NA	NA
1.5-V LVTTL/LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	NA	NA
1.2-V LVTTL/LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	NA	NA
3.0-V PCI	PCI Rev 2.1	3.0	3.0	3.0	3.0	3.0	NA	NA
3.0-V PCI-X	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	NA	NA
SSTL-2 Class I	JESD8-9B	2.5	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	2.5	2.5	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	1.8	1.8	1.8	1.8	2.5	0.90	0.90

Table 7–2. Stratix III I/O Standards and Voltage Levels Notes (1), (2), (3) (Part 2 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Top and Bottom I/O Banks	Left and Right I/O Banks	Top and Bottom I/O Banks	Left and Right I/O Banks			
SSTL-18 Class II	JESD8-15	1.8	1.8	1.8	1.8	2.5	0.90	0.90
SSTL-15 Class I		1.5	1.5	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II		1.5	1.5	1.5	NA	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	1.8	1.8	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	1.8	1.8	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	1.5	1.5	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II	JESD8-6	1.5	1.5	1.5	NA	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	1.2	1.2	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II	JESD8-16A	1.2	1.2	1.2	NA	2.5	0.6	0.6
Differential SSTL-2 Class I	JESD8-9B	2.5	2.5	2.5	2.5	2.5	NA	1.25
Differential SSTL-2 Class II	JESD8-9B	2.5	2.5	2.5	2.5	2.5	NA	1.25
Differential SSTL-18 Class I	JESD8-15	1.8	1.8	1.8	1.8	2.5	NA	0.90
Differential SSTL-18 Class II	JESD8-15	1.8	1.8	1.8	1.8	2.5	NA	0.90
Differential SSTL-15 Class I	--	1.5	1.5	1.5	1.5	2.5	NA	0.75
Differential SSTL-15 Class II	--	1.5	1.5	1.5	NA	2.5	NA	0.75
Differential HSTL-18 Class I	JESD8-6	1.8	1.8	1.8	1.8	2.5	NA	0.90
Differential HSTL-18 Class II	JESD8-6	1.8	1.8	1.8	1.8	2.5	NA	0.90
Differential HSTL-15 Class I	JESD8-6	1.5	1.5	1.5	1.5	2.5	NA	0.75
Differential HSTL-15 Class II	JESD8-6	1.5	1.5	1.5	NA	2.5	NA	0.75
Differential HSTL-12 Class I	JESD8-16A	1.2	1.2	1.2	1.2	2.5	NA	0.60

Table 7–2. Stratix III I/O Standards and Voltage Levels Notes (1), (2), (3) (Part 3 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Top and Bottom I/O Banks	Left and Right I/O Banks	Top and Bottom I/O Banks	Left and Right I/O Banks			
Differential HSTL-12 Class II	JESD8-16A	1.2	1.2	1.2	NA	2.5	NA	0.60
LVDS	ANSI/TIA/EIA-644	2.5	2.5	2.5	2.5	2.5	NA	NA
RSDS	--	2.5	2.5	2.5	2.5	2.5	NA	NA
mini-LVDS	--	2.5	2.5	2.5	2.5		NA	NA
LVPECL	--	2.5	2.5	NA	NA	2.5	NA	NA

Notes to Table 7–2:

(1) Any input pins with PCI-clamping diode-enabled forces the V_{CCIO} to 3.0 V.

(2) V_{CCPD} is either 2.5 V or 3.0 V. For 3.0-V I/O standard, V_{CCPD} = 3.0 V. For 2.5 V and below I/O standards, V_{CCPD} = 2.5 V.

(3) Single-ended HSTL/SSTL and LVDS input buffers are powered by V_{CCPD}.

Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook* for detailed electrical characteristics of each I/O standard.

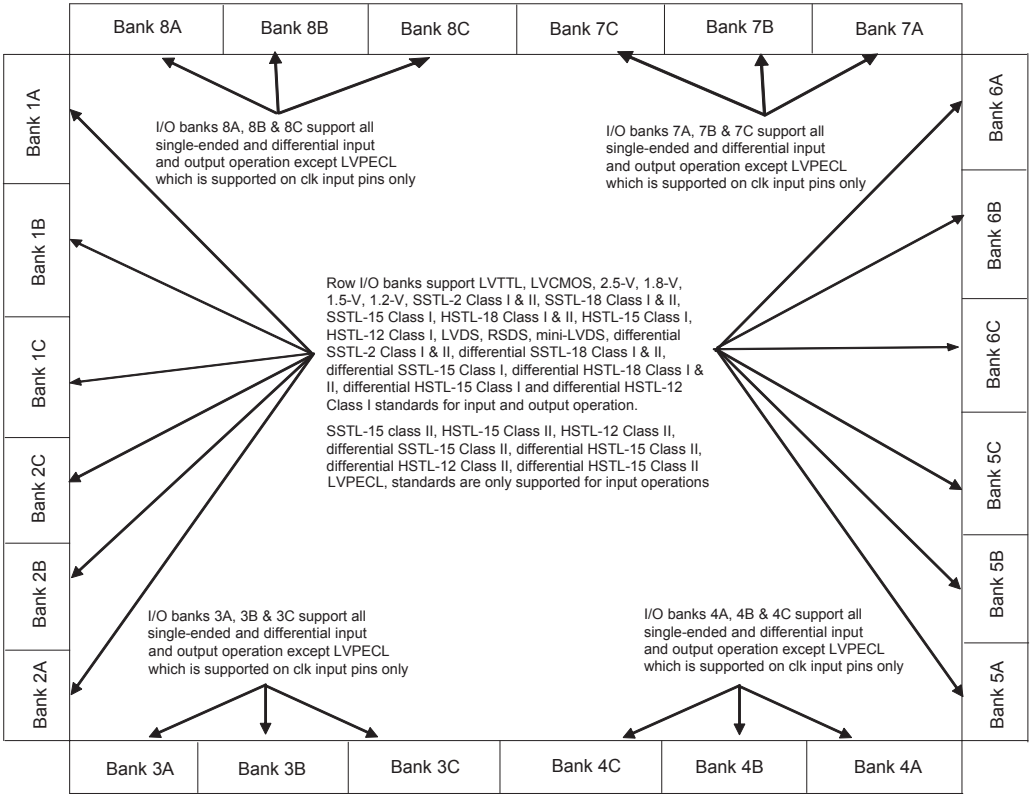
Stratix III I/O Banks

Stratix III devices contain up to 24 I/O banks, as shown in Figure 7–1. The row I/O banks contain true differential input and output buffers and dedicated circuitry to support differential standards at speeds up to 1.25 Gbps.

Every I/O bank in Stratix III devices can support high-performance external memory interfaces with dedicated circuitry. The I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support both differential input or output buffer. The only exceptions are the `clk1`, `clk3`, `clk8`, `clk10`, `PLL_L1_clk`, `PLL_L4_clk`, `PLL_R1_clk`, and `PLL_R4_clk` pins which support differential input operations only.

Refer to the *High-speed Differential I/O Interface with DPA in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for the number of channels available for the LVDS I/O standard.

Figure 7–1. Stratix III I/O banks *Notes (1), (2), (3), (4), (5), (6), (7)*



Notes to Figure 7–1:

(1) Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

(2) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without differential OCT support.

(3) Column I/O supports LVDS outputs using single-ended buffers and external resistor networks.

(4) Row I/O supports PCI / PCI-X with external clamp diode.

(5) Differential clock inputs on column I/O use $V_{CCCLKIN}$. All outputs use the corresponding Bank V_{CCIO}.

(6) Row I/O supports dedicated LVDS output buffer.

(7) Column and row I/O banks support LVPECL standards for input clock operation.

Modular I/O Banks

The I/O pins in Stratix III devices are arranged in groups called modular I/O banks. Depending on device densities, the number of I/O banks range from 16 to 24 banks. The size of each bank is 24, 32, 36, 40, or 48 I/O pins. Figures 7–4 to 7–7 show the number of I/O pins available in each I/O bank.

In Stratix III devices, the maximum number of I/O banks per side is six or four, depending on the device density. When migrating between devices with a different number of I/O banks per side, it is the middle or "B" bank which is removed or inserted. For example, when moving from a 24-bank device to a 16-bank device, the banks that are dropped are "B" banks namely: 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B. Similarly, when moving from a 16-bank device to a 24-bank device, the banks that are added are "B" banks namely: 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B.

During migration from a smaller device to a larger device, the bank size increases or remains the same but never decreases. For example, banks may increase from a size of 24 I/O to a bank of size 32, 36, 40,or 48 I/O, but will never decrease. This is shown in Figure 7–2.

Figure 7–2. Bank Migration Path with Increasing Device Size

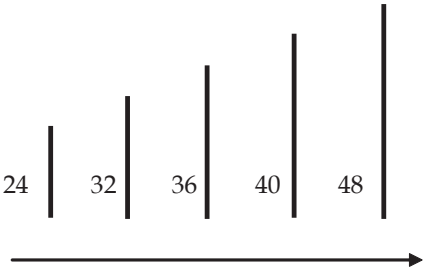
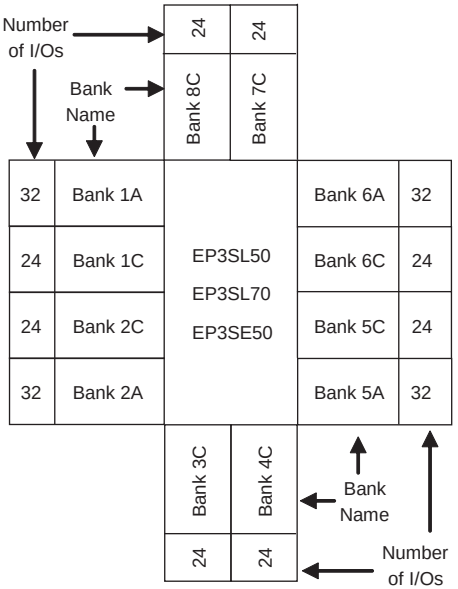


Figure 7–3 through Figure 7–7 shows the number of I/Os and packaging information for different sets of available devices.

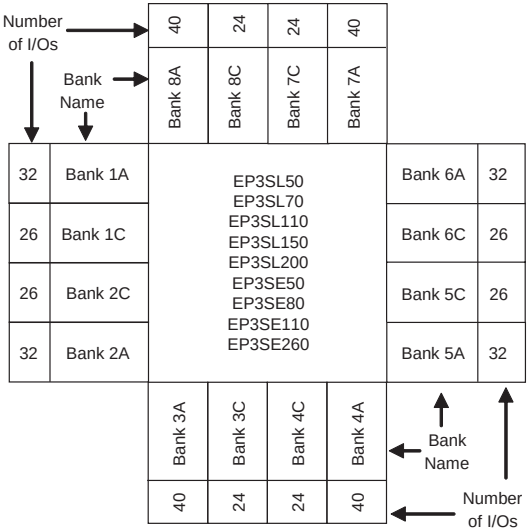
Figure 7–3. Number of I/Os in Each Bank in EP3SL50, EP3SL70, and EP3SE50 Devices in 484-pin FineLine BGA Package *Note (1)*



Note to Figure 7–3:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) that can be used for data inputs.

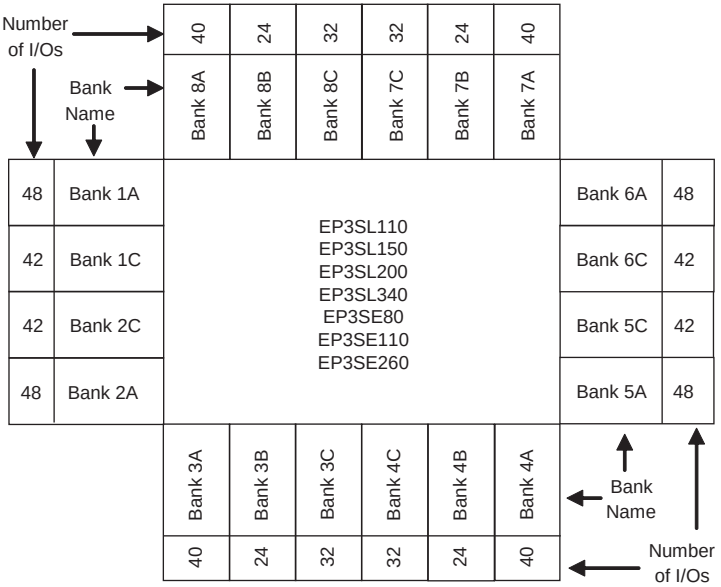
Figure 7–4. Number of I/Os in Each Bank in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SL200, EP3SE50, EP3SE80, EP3SE110, and EP3SE260 in the 780-pin FineLine BGA Package *Note (1)*



Note to Figure 7–4:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) that can be used for data inputs.

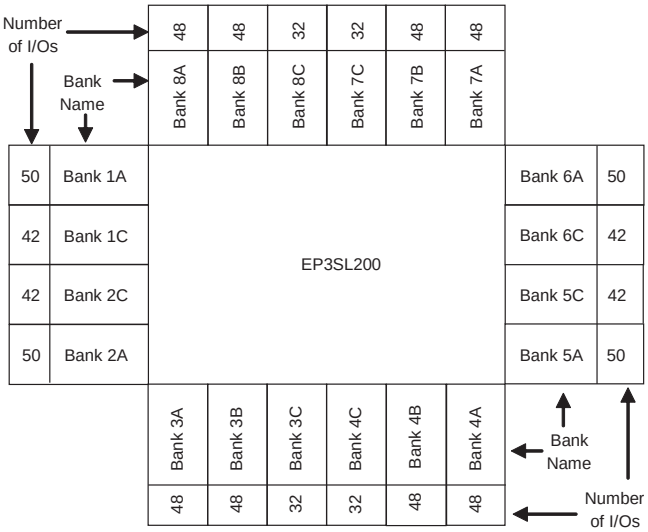
Figure 7–5. Number of I/Os in Each Bank in EP3SL110, EP3SL150, EP3SL200, EP3SL340, EP3SE80, EP3SE110, and EP3SE260 Devices in the 1152-pin FineLine BGA Package Note (1)



Notes to Figure 7–5:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) that can be used for data inputs.

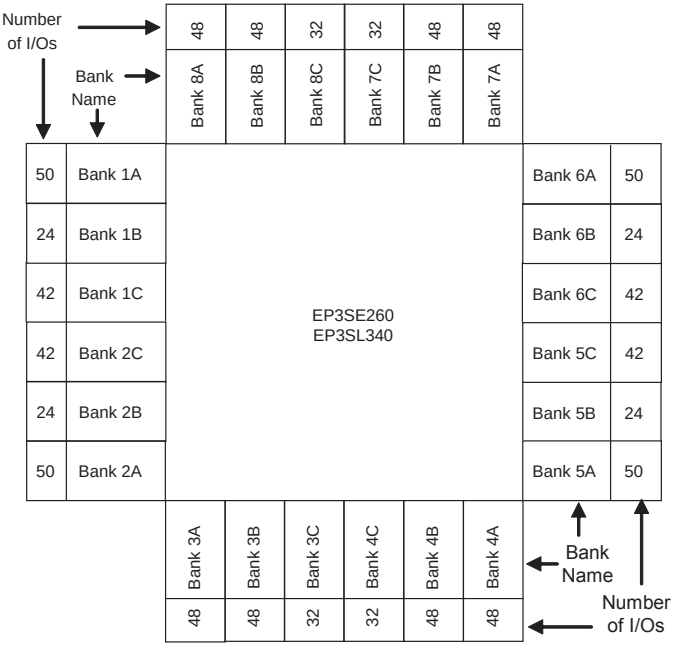
Figure 7–6. Number of I/Os in Each Bank in EP3SL200 Devices in the 1517-pin FineLine BGA Package *Note (1)*



Notes to Figure 7–6:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp` and `PLL_R1_CLKn`) that can be used for data inputs.

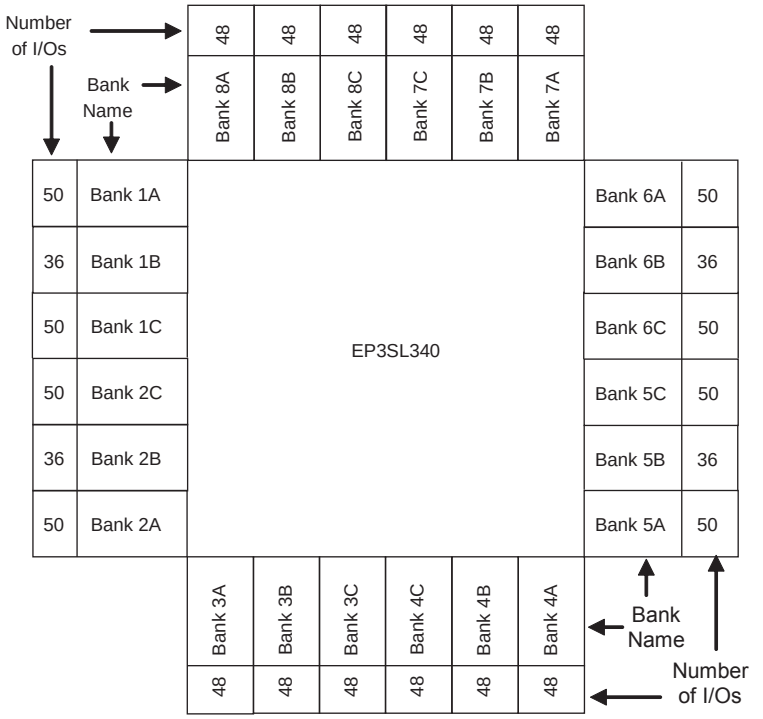
Figure 7–7. Number of I/Os in Each Bank in EP3SE260, EP3SL340 Devices in the 1517-pin FineLine BGA Package *Note (1)*



Note to Figure 7–7:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp` and `PLL_R1_CLKn`) that can be used for data inputs.

Figure 7–8. Number of I/Os in Each Bank in EP3SL340 Devices in the 1760-pin FineLine BGA Package Note (1)



Note to Figure 7–8:

(1) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp` and `PLL_R1_CLKn`) that can be used for data inputs.

Stratix III I/O Structure

The I/O element (IOE) in Stratix III devices contains a bi-directional I/O buffer and I/O registers to support a complete embedded bi-directional single data rate or DDR transfer. The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row IOEs drive row, column, or direct link interconnects. The column IOEs drive column interconnects.

The Stratix III bi-directional IOE also supports features such as:

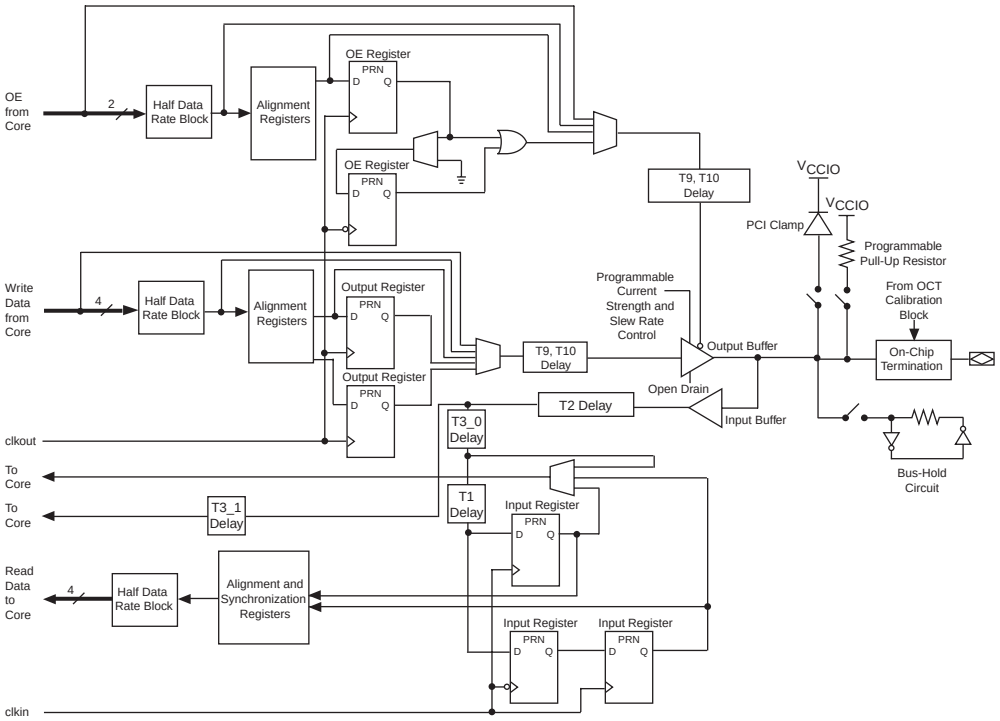
- Programmable input delay

- Programmable output-current strength
- Programmable slew rate
- Programmable output delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination with calibration
- On-chip series termination without calibration
- On-chip parallel termination with calibration
- On-chip differential termination
- PCI clamping diode

Figure 7–9 shows the Stratix III IOE structure.

The I/O registers are composed of the input path for handling data from the pin to the core, the output path for handling data from the core to the pin, and the output-enable (OE) path for handling the OE signal for the output buffer. These registers allow faster source-synchronous register-to-register transfers and resynchronization. The input path consists of the DDR input registers, alignment and synchronization registers, and HDR (half data rate blocks). You can bypass each block of the input path.

Figure 7–9. Stratix III IOE Structure *Note (1)*



Note to Figure 7–9:

(1) `T3_0` and `T3_1` delays have the same available settings in Quartus II.

The output and OE paths are divided into output or OE registers, alignment registers, and HDR blocks. You can bypass each block of the output and output-enable path.

For more information on I/O registers and how they are used for memory applications, refer to the *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

3.3-V I/O Interface

In order to interface with 3.3-V devices, Stratix III devices require external voltage regulators to limit the V_{CCIO} voltage to 3 V. In addition to regulating the V_{CCIO} to 3 V, Altera® recommends using programmable slew rate control, termination resistors, and clamping diodes to limit AC overshoot and undershoot on the I/O pins.

External Memory Interfaces

In addition to the I/O registers in each IOE, Stratix III devices also have dedicated registers and phase-shift circuitry on all I/O banks for interfacing with external memory interfaces. Table 7–3 lists the memory interfaces and the corresponding I/O standards supported by Stratix III devices.

Table 7–3. Memory Interface Standards Supported

Memory Interface Standard	I/O Standard
DDR SDRAM	SSTL-2
DDR2 SDRAM	SSTL-18
DDR3 SDRAM	SSTL-15
RLDRAM II	HSTL-18
QDRII SRAM	HSTL-18
QDRII+ SRAM	HSTL-15

For more information on external memory interfaces, refer to the *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

High-Speed Differential I/O with DPA Support

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSLI, RapidIO™, and NPSI. Stratix III devices support ×2, ×4, ×6, ×7, ×8, and ×10 SERDES modes for high-speed differential I/O interfaces and ×4, ×6, ×7, ×8, and ×10 SERDES modes with dedicated dynamic phase alignment (DPA) circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems.

×2 mode is supported by the DDR registers, and is not included in SERDES. In Stratix III devices, SERDES can be bypassed in the Quartus® II MegaWizard® Plug-in Manager to support DDR (×2) operation.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs)

For more information on DPA support, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Programmable Current Strength

The output buffer for each Stratix III device I/O pin has a programmable current-strength control for certain I/O standards. You can use programmable current strength to mitigate the effects of high signal attenuation due to a long transmission line or a legacy backplane. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of current strength that you can control. Information about programmable current strength appears in Table 7–4.

Table 7–4. Programmable Current Strength (Part 1 of 2) *Note (1)*

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.0-V LVTTL	16, 12, 8, 4	12, 8, 4
3.0-V LVCMOS	16, 12, 8, 4	8, 4
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVTTL/LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.2-V LVTTL/LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 10, 8	12, 8
SSTL-2 Class II	16	16
SSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
SSTL-18 Class II	16, 8	16, 8
SSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
SSTL-15 Class II	16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4

Table 7–4. Programmable Current Strength (Part 2 of 2) Note (1)		
I/O Standard	**I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins**	**I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins**
HSTL-18 Class II	16	16
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	16	—
HSTL-12 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-12 Class II	16	—

Notes to Table 7–4

(1) The default setting in the Quartus II software is 50ohm OCT Rs without calibration for all non-voltage reference and HSTL / SSTL class I I / O standards. The default setting is 25ohm OCT Rs without calibration for HSTL / SSTL class II I / O standards.

Altera recommends performing I / O buffer information specification (IBIS) or SPICE simulations to determine the right current strength setting for your specific application.

Programmable Slew Rate Control

The output buffer for each Stratix III device regular- and dual-function I / O pin has a programmable output slew-rate control that you can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slow slew rate can help reduce system noise, but adds a nominal delay to rising and falling edges. Each I / O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis.

You cannot use the programmable slew rate feature when using OCT R_S.

Quartus II allows four settings for programmable slew rate control—0, 1, 2, and 3—where 0 is slow slew rate and 3 is fast slew rate. In Quartus II, the default setting for 2.5-, 1.8-,1.5-,1.2-, 3.0-V PCI / PCI-X, and 3.0-V LVTTL / LVCMOS is 1. The default setting for SSTL-2, -18, -15 Class I and Class II and HSTL-18, -15, -12 Class I and Class II is 3.

You can use faster slew rates to improve the available timing margin in memory-interface applications or when the output pin has a high-capacitive loading. Altera recommends performing IBIS or SPICE simulations to determine the right slew rate setting for your specific application.

Programmable Delay

Programmable IOE Delay

The Stratix III device IOE includes programmable delays shown in Figure 7–9 that can be activated to ensure zero hold times, minimize setup times, or increase clock-to-output times. Each pin can have a different input delay from pin to input register or a delay from the output register to the output pin values to ensure that the bus has the same delay going into or out of the device. This feature helps read and time margins as it minimizes the uncertainties between signals in the bus.

Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter of the *Stratix III Device Handbook*, volume 2 for the programmable IOE delay specifications.

Programmable Output Buffer Delay

Stratix III devices support delay chains built inside the single-ended output buffer shown in Figure 7–9. The delay chains can independently control the rising and falling edge delays of the output buffer, providing the ability to adjust the output-buffer duty cycle, compensate channel-to-channel skew, reduce SSO noise by deliberately introducing channel-to-channel skew, and improve high-speed memory-interface timing margins. Stratix III devices support four levels of output buffer delay settings. The default setting is no delay.

Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter of the *Stratix III Device Handbook*, volume 2 for the programmable output buffer delay specifications.

Open-Drain Output

Stratix III devices provide an optional open-drain output (equivalent to an open-collector output) for each I/O pin. When configured as open-drain, the logic value of the output is either `high-Z` or `0`. Typically, an external pull-up resistor is needed to provide logic high.

Bus Hold

Each Stratix III device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls non-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent over-driving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature if the I/O pin is configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state.

See the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook* for the specific sustaining current driven through this resistor and the overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix III device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the I/O to the V_{CCIO} level.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins. If the programmable pull-up option is enabled, you cannot use the bus-hold feature.

MultiVolt I/O Interface

The Stratix III architecture supports the MultiVolt™ I/O interface feature that allows Stratix III devices in all packages to interface with systems of different supply voltages.

The VCCIO pins can be connected to a 1.2-, 1.5-, 1.8-, 2.5-, or 3.0-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply. (For example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems).

The Stratix III VCCPD power pins must be connected to a 2.5- or 3.0-V power supply. Using these power pins to supply the pre-driver power to the output buffers increases the performance of the output pins. Table 7–5 summarizes Stratix III MultiVolt I/O support. For 3.0-V LVTTL/LVCMOS:

- In column I/O banks, when V_{CCIO} = 3.0 V, Altera recommends you turn the internal diode on.
- In all I/O banks, when V_{CCIO} = 2.5 V, Altera recommends you use an external clamp diode.
- In row I/O banks, when V_{CCIO} = 3.0 V, Altera recommends you use an external clamp diode.

Table 7–5. Stratix III MultiVolt I/O Support Note (1)

V_{CCIO} (V)	Input Signal (V)					Output Signal (V)				
	1.2	1.5	1.8	2.5	3.0	1.2	1.5	1.8	2.5	3.0
1.2	✓	—	—	—	—	✓	—	—	—	—
1.5	—	✓	✓(1)	—	—	—	✓	—	—	—
1.8	—	✓(1)	✓	—	—	—	—	✓	—	—
2.5	—	—	—	✓	✓	—	—	—	✓	—
3.0	—	—	—	✓	✓	—	—	—	—	✓

Note to Table 7–5:

(1) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix III V_{IL} maximum and V_{IH} minimum voltage specifications.

OCT Support

Stratix III devices feature dynamic series and parallel on-chip termination to provide I/O impedance matching and termination capabilities. On-chip termination (OCT) maintains signal quality, saves board space, and reduces external component costs.

Stratix III devices support on-chip series (R_S) with or without calibration, parallel (R_T) with calibration, and dynamic series and parallel termination for single-ended I/O standards and on-chip differential termination (R_D) for differential LVDS I/O standards. Stratix III devices support OCT in all I/O banks by selecting one of the OCT I/O standards.

Stratix III devices support OCT R_S and R_T in the same I/O bank for different I/O standards if they use the same V_{CCIO} supply voltage. Each I/O in an I/O bank can be independently configured to support OCT R_S, programmable current strength, or OCT R_T.

You cannot configure both OCT R_S and programmable current strength for the same I/O buffer.

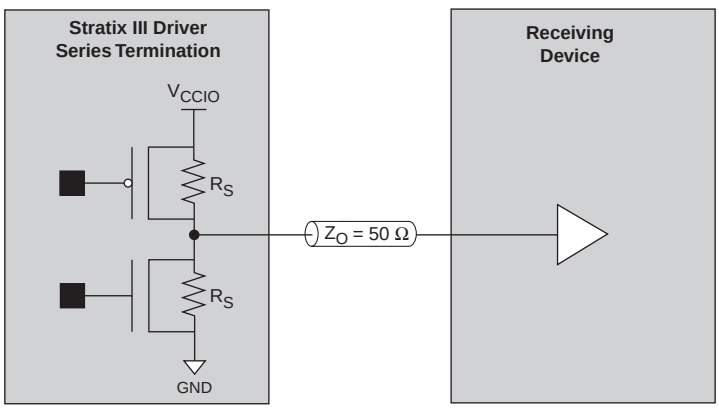
A pair of R_{UP} and R_{DN} pins are available in a given I/O bank, and are shared for series- and parallel-calibrated termination. The R_{UP} and R_{DN} pins share the same V_{CCIO} and GND, respectively, with the I/O bank where they are located. The R_{UP} and R_{DN} pins are dual-purpose I/Os, and function as regular I/Os if you do not use the calibration circuit. When used for calibration, the R_{UP} pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25-Ω or 50-Ω, respectively; the R_{DN} pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25-Ω or 50-Ω, respectively. For on-chip parallel termination, the R_{UP} pin is connected to V_{CCIO} through an external 50-Ω ±1% resistor; the R_{DN} pin is connected to GND through an external 50-Ω ±1% resistor.

On-Chip Series (R_S) Termination without Calibration

Stratix III devices support driver-impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, you can significantly reduce reflections. Stratix III devices support on-chip series termination for single-ended I/O standards (see Figure 7–10).

The R_S shown in Figure 7–10 is the intrinsic impedance of the output transistors. The typical R_S values are 25 Ω and 50 Ω. When matching impedance is selected, current strength is no longer selectable.

Figure 7–10. Stratix III On-Chip Series Termination without Calibration



To use on-chip termination for the SSTL Class I standard, you should select the 50-Ω on-chip series termination setting, hence eliminating the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, you should select the 25-Ω on-chip series termination setting (to match the 50-Ω transmission line and the near-end external 50-Ω pull-up to V_{TT}).

On-Chip Series Termination with Calibration

Stratix III devices support on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the R_{UP} and R_{DN} pins, and dynamically enables or disables the transistors until they match. The R_S shown in Figure 7–11 is the intrinsic impedance of transistors. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. Table 7–6 shows the list of I/O standards that support on-chip series termination with calibration.

Figure 7–11. Stratix III On-Chip Series Termination with Calibration

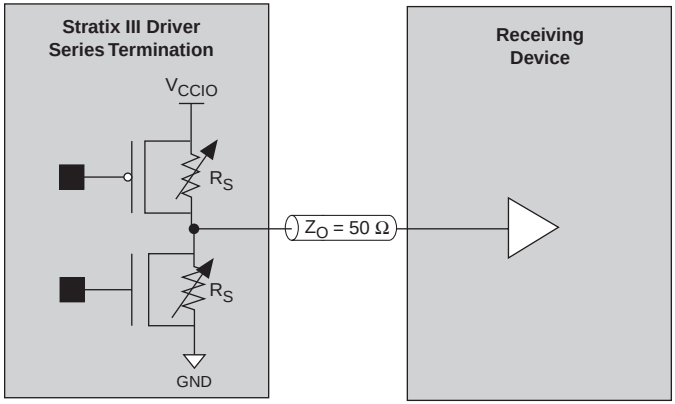


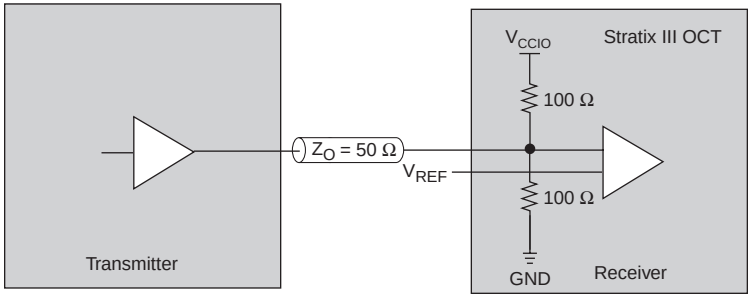
Table 7–6. Selectable I/O Standards with On-Chip Series Termination with Calibration

I/O Standard	On-chip Series Termination Setting		
	Row I/O	Column I/O	Unit
3.0-V LVTTL	50	50	Ω
	25	25	Ω
3.0-V LVCMOS	50	50	Ω
	25	25	Ω
2.5-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.8-V LVTTL/LVCMOS	50	50	Ω
	25	25	Ω
1.5-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
1.2-V LVTTL/LVCMOS	50	50	Ω
		25	Ω
SSTL-2 Class I	50	50	Ω
SSTL-2 Class II	25	25	Ω
SSTL-18 Class I	50	50	Ω
SSTL-18 Class II	25	25	Ω
SSTL-15 Class I	50	50	Ω
SSTL-15 Class II	N/A	25	Ω
HSTL-18 Class I	50	50	Ω
HSTL-18 Class II	25	25	Ω
HSTL-15 Class I	50	50	Ω
HSTL-15 Class II	N/A	25	Ω
HSTL-12 Class I	50	50	Ω
HSTL-12 Class II	N/A	25	Ω

On-Chip Parallel Termination with Calibration

Stratix III devices support on-chip parallel termination with calibration in all banks. On-chip parallel termination with calibration is only supported for input or bidirectional pin configurations. Output pin configurations do not support on-chip parallel termination with calibration. Figure 7–12 shows on-chip parallel termination with calibration.

Figure 7–12. Stratix III On-Chip Parallel Termination with Calibration



The on-chip parallel termination calibration circuit compares the total impedance of the I/O buffer to the external 50-Ω ±1% resistors connected to the R_{UP} and R_{DN} pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of the device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. Table 7–7 shows the list of I/O standards that support on-chip parallel termination with calibration.

Table 7–7. Selectable I/O Standards with On-Chip Parallel Termination with Calibration (Part 1 of 2)

I/O Standard	On-Chip Parallel Termination Setting (Column I/O)	On-Chip Parallel Termination Setting (Row I/O)	Unit
SSTL-2 Class I, II	50	50	Ω
SSTL-18 Class I, II	50	50	Ω
SSTL-15 Class I, II	50	50	Ω
HSTL-18 Class I, II	50	50	Ω
HSTL-15 Class I, II	50	50	Ω
HSTL-12 Class I, II	50	50	Ω
Differential SSTL-2 Class I, II	50	50	Ω
Differential SSTL-18 Class I, II	50	50	Ω
Differential SSTL-15 Class I, II	50	50	Ω
Differential HSTL-18 Class I, II	50	50	Ω

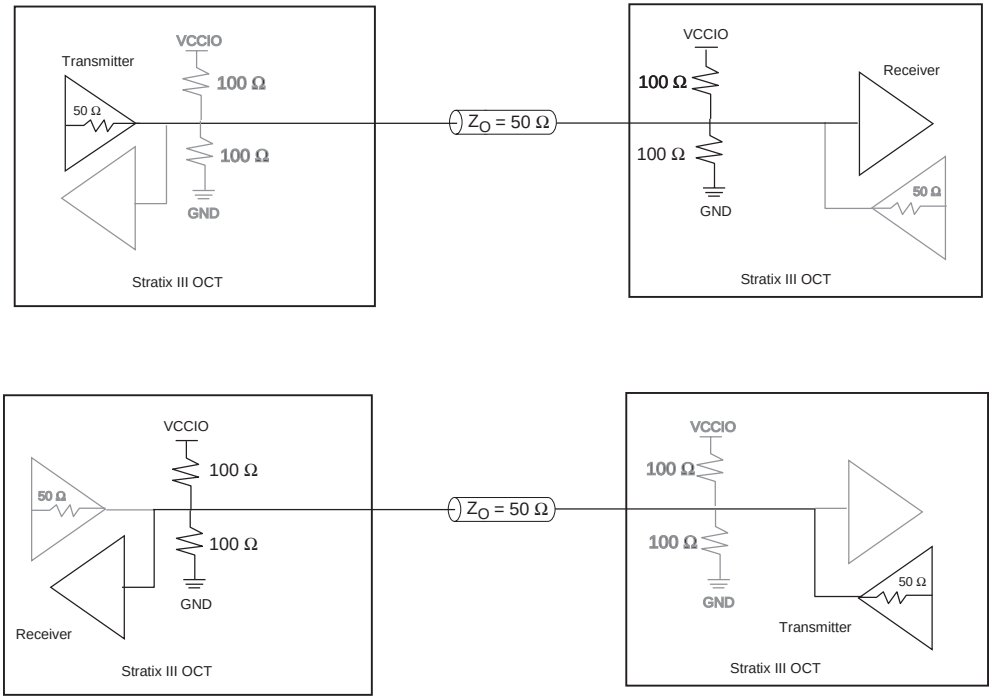
Table 7–7. Selectable I/O Standards with On-Chip Parallel Termination with Calibration (Part 2 of 2)

I/O Standard	On-Chip Parallel Termination Setting (Column I/O)	On-Chip Parallel Termination Setting (Row I/O)	Unit
Differential HSTL-15 Class I, II	50	50	Ω
Differential HSTL-12 Class I, II	50	50	Ω

Dynamic On-Chip Termination

Stratix III devices support on-off dynamic series and parallel termination for a bi-directional I/O in all I/O banks. Figure 7–13 shows the termination schemes supported in the Stratix III device. Dynamic parallel termination is enabled only when the bi-directional I/O acts as a receiver and is disabled when it acts as a driver. Similarly dynamic series termination is enabled only when the bi-directional I/O acts as a driver and is disabled when it acts as a receiver. This feature is useful for terminating any high-performance bidirectional path because the signal integrity is optimized depending on the direction of the data.

Figure 7–13. Dynamic Parallel OCT in Stratix III Devices

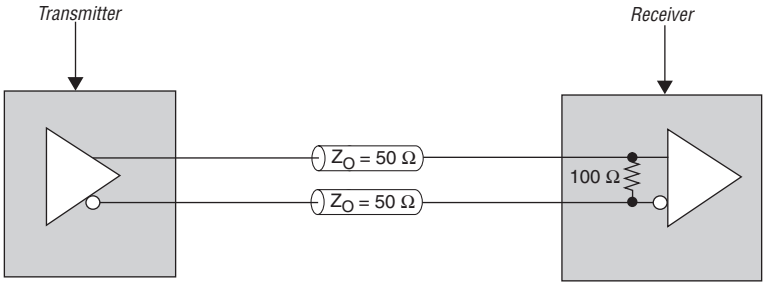


For more information on tolerance specifications for on-chip termination with calibration, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

LVDS Input On-Chip Termination (R_D)

Stratix III devices support on-chip termination for differential LVDS input buffers with a nominal resistance value of 100 Ω, as shown in Figure 7–14. Differential on-chip termination R_D is only available in row I/O banks; column I/O banks do not support OCT R_D. The dedicated clock input pairs `CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n` on the row I/O banks of the Stratix III devices do not support R_D termination.

Figure 7–14. Differential Input On-Chip Termination



For more information on differential on-chip termination, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

OCT Calibration

Stratix III devices support calibrated on-chip series termination (R_S) and calibrated on-chip parallel termination (R_T) on all I/O pins. You can calibrate the Stratix III I/O bank with any of eight OCT calibration blocks in EP3SL50, EP3SL70, EP3SL110, EP3SL150, EP3SL200, EP3SE50, EP3SE80, and EP3SE110 devices and ten OCT calibration blocks in EP3SE260 and EP3SL340 devices.

OCT Calibration Block Location

Figures 7–15, 7–16, and 7–17 show the location of OCT calibration blocks in Stratix III devices.

Figure 7–15. OCT Calibration Block (CB) Location in EP3SL50, EP3SL70, and EP3SE50 Devices

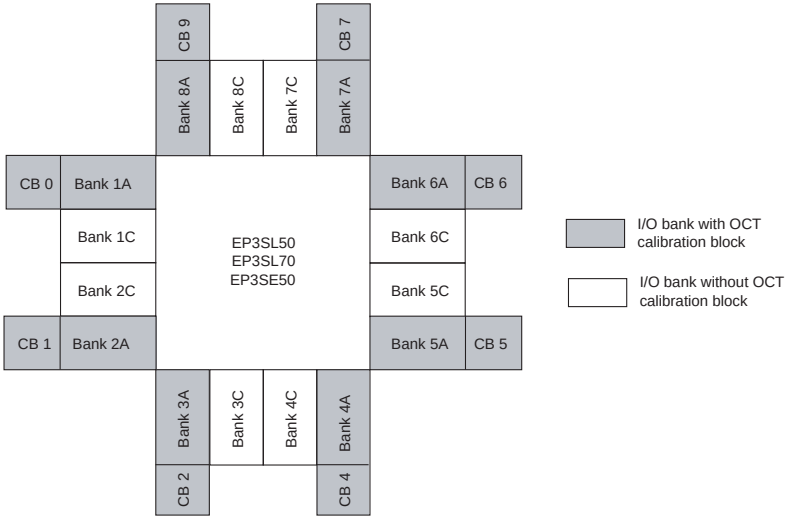


Figure 7–16. OCT Calibration Block (CB) Location in EP3SL110, EP3SL150, EP3SL200, EP3SE80, and EP3SE110 Devices

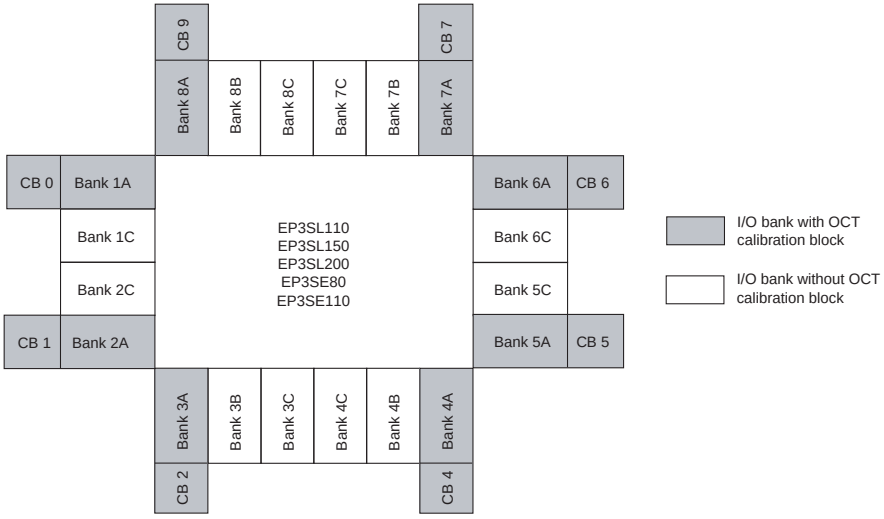
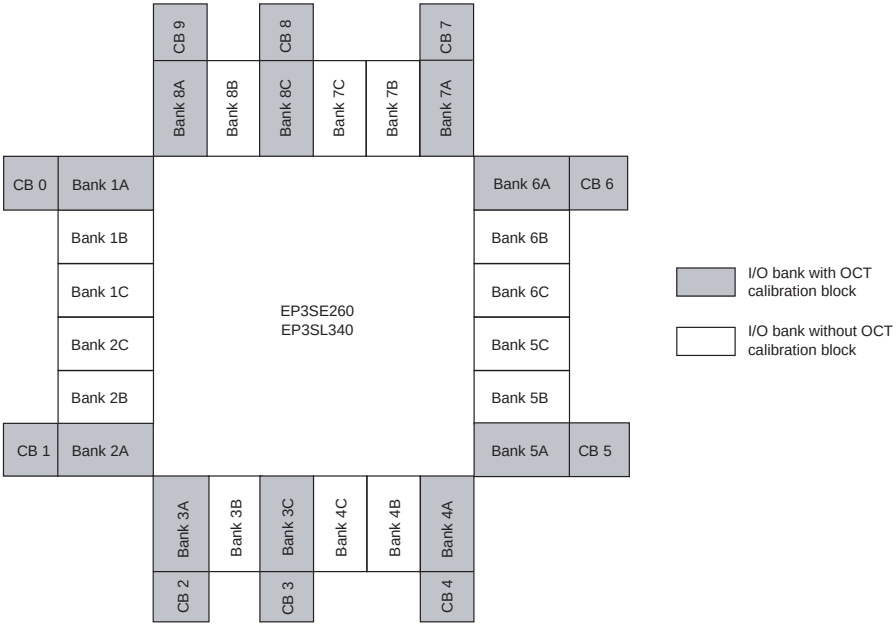


Figure 7–17. OCT Calibration Block (CB) Location in EP3SE260 and EP3SL340

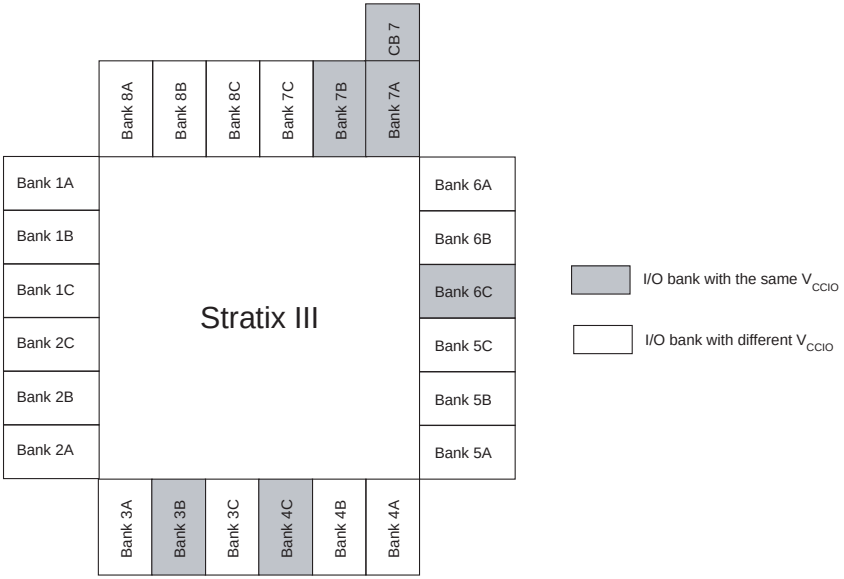


Sharing OCT Calibration Block in Multiple I/O Banks

An OCT calibration block has the same V_{CCIO} as the I/O bank that contains the block. OCT R_S calibration is supported on all I/O banks with different V_{CCIO} voltage standards, up to the number of available OCT calibration blocks. You can configure I/O banks to receive calibrated codes from any OCT calibration block with the same V_{CCIO}. All I/O banks with the same V_{CCIO} can share one OCT calibration block, even if that particular I/O bank has a dedicated OCT calibration block.

For example, Figure 7–18 shows a group of I/O banks that have the same V_{CCIO} voltage. If a group of I/O banks have the same V_{CCIO} voltage, you can use one OCT calibration block to calibrate the group of I/O banks placed around the periphery. Since 3B, 4C, 6C, and 7B have the same V_{CCIO} as bank 7A, you can calibrate all four I/O banks (3B, 4C, 6C, and 7B) with the OCT calibration block located in bank 7A. You can enable this by serially shifting out OCT R_S calibration codes from the OCT calibration block located in bank 7A to the I/O banks located around the periphery.

Figure 7–18. Example of Sharing Multiple I/O Banks with One OCT Calibration Block



OCT Calibration Block Ports

Table 7–8 shows the calibration block port names and their descriptions.

Table 7–8. OCT Calibration Block Ports and Description

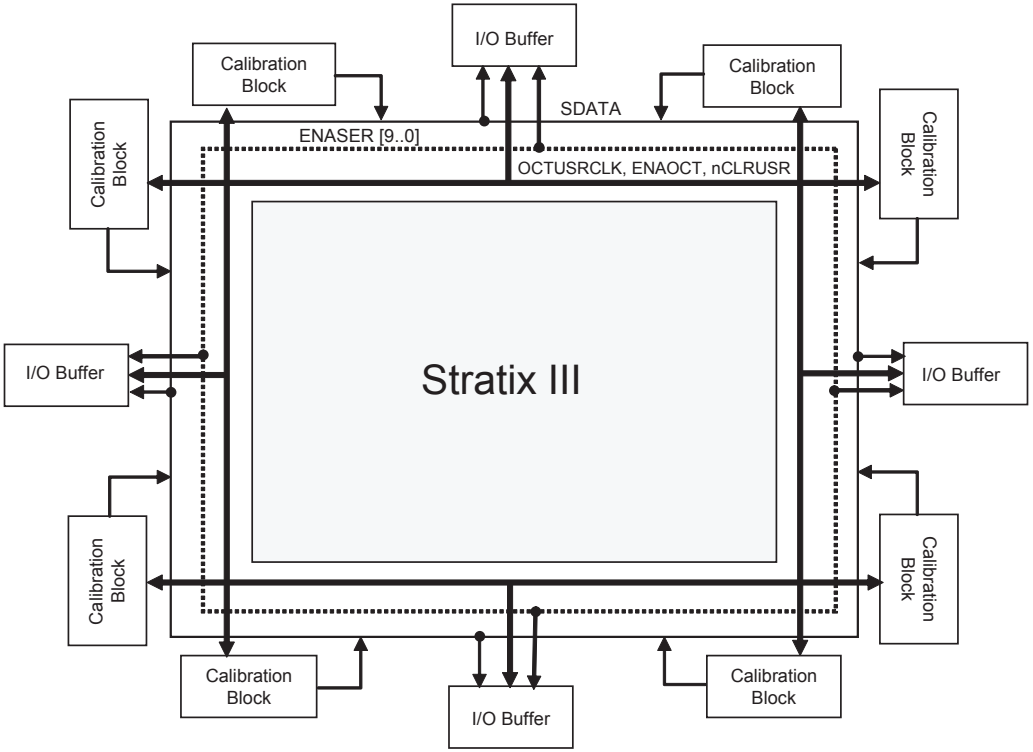
Signal Name	Description
OCTUSRCLK	User-provided clock for OCT block
ENAOCT	Enable OCT Termination (Generated by user IP)
ENASER[9..0]	Enable OCT Serializer
SDATA	OCT Serial Data Stream Generated internally in each OCT block
S2PENA	Serial-to-parallel load enable
nCLRUSR	Clear user

OCT Calibration Block Code Data Transfer

SDATA, OCTUSRCLK, and ENASER signals are used to serially transfer calibrated codes from each OCT calibration block to any I/O. Figure 7–19 shows signals that are used to complete OCT calibration and to shift out codes from OCT calibration blocks to I/O buffers. When the OCT R_S and OCT R_T calibrations complete, ENASER signals are asserted in a sequence to send out codes from an OCT calibration block to I/O buffers in one or more I/O banks that are configured to receive the codes.

All OCT calibration blocks share one OCT SDATA line. The SDATA line is used to serially shift out the calibration codes. Only one OCT calibration block can drive the OCT data line at any time. When the ENASER signal for a corresponding OCT calibration block is asserted, its calibration code is sent out on the SDATA line to I/O buffers in selected I/O banks. Use the OCTUSRCLK signal to serially shift the calibrated codes from the OCT calibration blocks to the I/O buffer.

Figure 7–19. Signals for Shift-Out Codes from the OCT Calibration Block to I/O Buffers

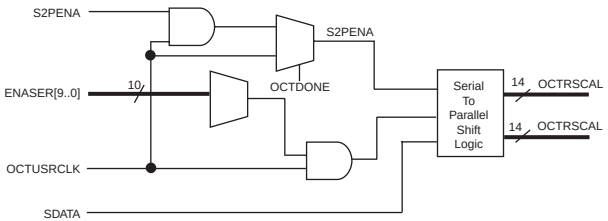


OCT Calibration Block Architecture

Figure 7–20 shows the logic blocks in the OCT calibration block. One of eight ENASER signals (ten ENASER signals for EP3SE260 and EP3SL340 devices) are selected by configuration bits. For example, if ENASER4 is selected by configuration bits, the I/O buffer communicates to OCT calibration block 4.

It requires 28 clock cycles using OCTUSRCLK to serially shift the 14-bit OCT R_S calibration code and the 14-bit OCT R_T calibration code into registers in I/O buffer. During these 28 clock cycles, the corresponding ENASER signal is asserted. Asserting the next ENASER signal should happen after one or more clock cycles after the current ENASER signal is de-asserted to avoid driving the OCT data line with two tri-state drivers at the same time.

Figure 7–20. OCT Calibration Block



OCT Calibration Modes of Operation

When calibration is complete, you must serially shift out the 28-bit OCT calibration code (14-bit OCT R_S code and 14-bit OCT R_T) from each OCT calibration blocks to the corresponding I/O buffer. The codes from the OCT calibration blocks are serially shifted out to the I/O buffer. Only one OCT calibration block can send out the codes at any given time.

For Stratix III devices, you can continuously use I/Os for transmitting or receiving data while the I/Os are calibrated and the calibrated codes are serially shifted from the OCT calibration blocks to the I/Os. After calibrated codes are shifted in serially to each I/O bank, the calibrated codes must be converted from serial format to parallel format before being used in the I/O buffers. Use the S2PENA signals to complete serial-to-parallel shifting. The S2PENA signals are generated differently during power-up mode and user mode. You cannot use I/Os for transmitting or receiving data when serially shifted calibrated codes are parallel shifted in I/Os.

Power Up Mode

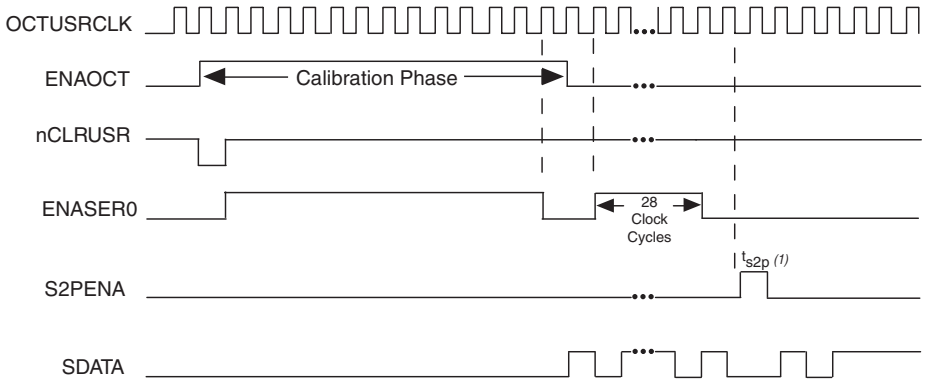
During power-up mode, an internal oscillator clock signal drives the S2PENA signal, causing parallel shifting to occur at every clock cycle during power-up mode. This parallel shifting does not create issues for the I/O buffers because I/O buffers are tri-stated during power-up mode.

User Mode

During user mode, the S2PENA signals are driven by the user IP. After the serial shifting operation, the S2PENA signals of the I/O banks can be asserted at any time to update the calibration codes in each I/O bank. All I/O banks that received the codes from the same OCT calibration block can have S2PENA asserted at the same time, or at a different time, even while another OCT calibration block is calibrating and serially shifting. The S2PENA signal is asserted for one clock cycle after ENASER is deasserted for one clock cycle and is synchronized with the user IP system clock. Do not synchronize S2PENA with OCTUSRCLK. The OCTUSRCLK clock frequency must be 20 MHz or less.

Figure 7–21 shows the user-mode signal-timing waveforms. You must generate user signals on the rising edge of OCTUSRCLK. You must assert ENAOCT one cycle before asserting ENASER[N] (N is a calibration block number). You must also assert nCLRUSR for one clock cycle and then deassert before asserting ENASER[N]. After the calibrations complete, ENAOCT can be deasserted one clock cycle after the last ENASER is deasserted.

Figure 7–21. OCT User-Mode Signal Timing Waveform



Note to Figure 7–21:
(1) t_{s2p} = one OCT clock cycle.

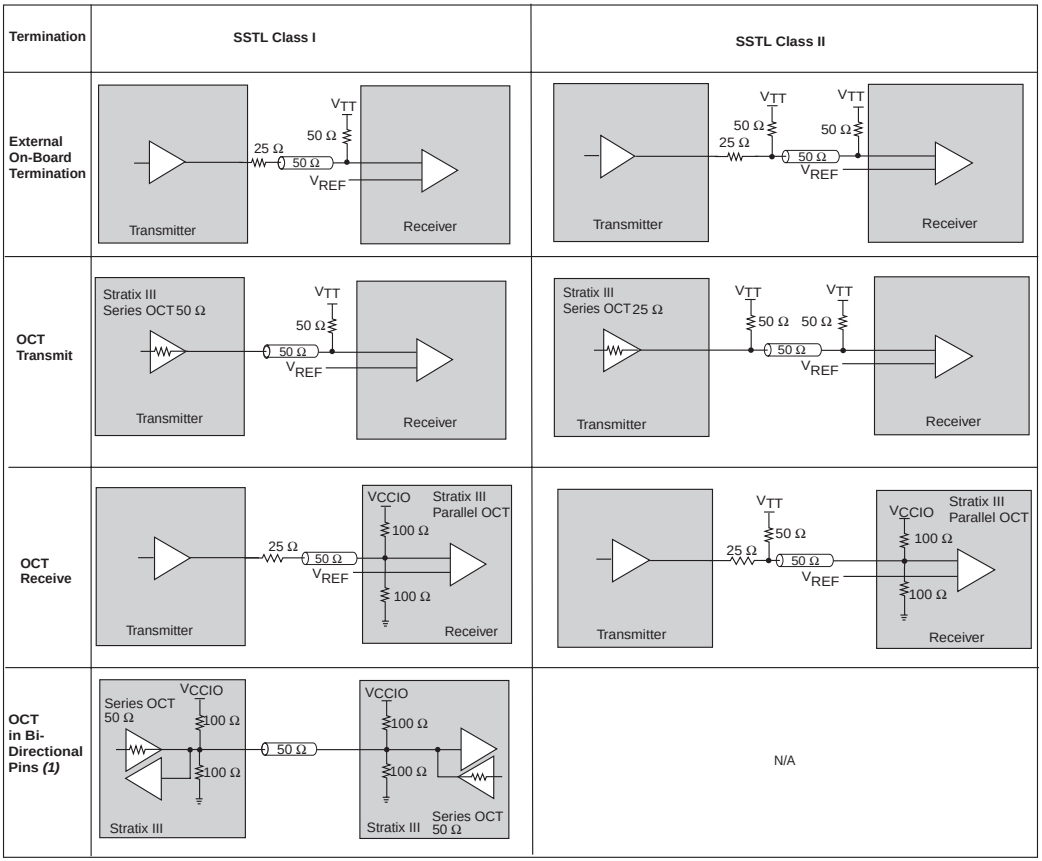
Termination Schemes for I/O Standards

The following section describes the different termination schemes for the I/O standards used in Stratix III devices.

Single-Ended I/O Standards Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device Figures 7–22 and 7–23 show the details of SSTL and HSTL I/O termination on Stratix III devices.

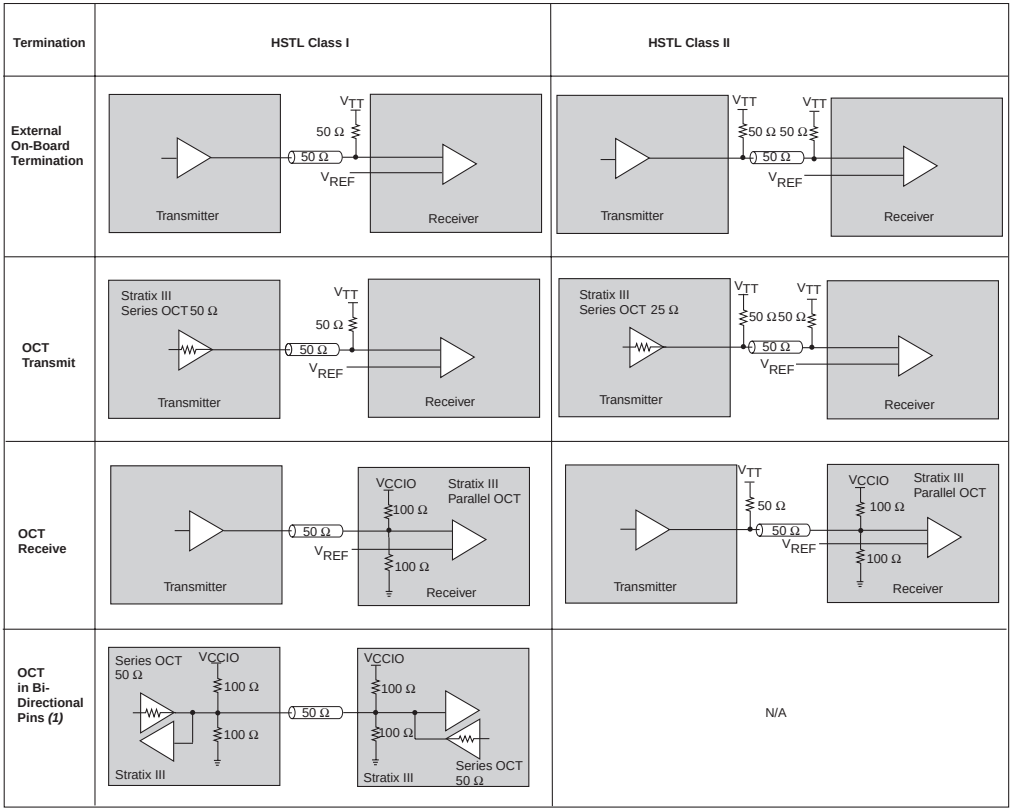
Figure 7–22. Stratix III SSTL I/O Standard Termination



Note to Figure 7–22:

(1) In Stratix III devices, series and parallel OCT cannot be used simultaneously. For more information, refer to "Dynamic On-Chip Termination" on page 7–26.

Figure 7–23. Stratix III HSTL I/O Standard Termination



Note to Figure 7–23:

(1) In Stratix III devices, series and parallel OCT cannot be used simultaneously. For more information, refer to "Dynamic On-Chip Termination" on page 7–26.

Differential I/O Standards Termination

Stratix III devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, HSTL-12, LVDS, LVPECL, RSDS, and mini-LVDS Figures 7–24 through 7–30 show the details of various differential I/O termination on Stratix III devices.

Figure 7–24. Stratix III Differential SSTL I/O Standard Termination

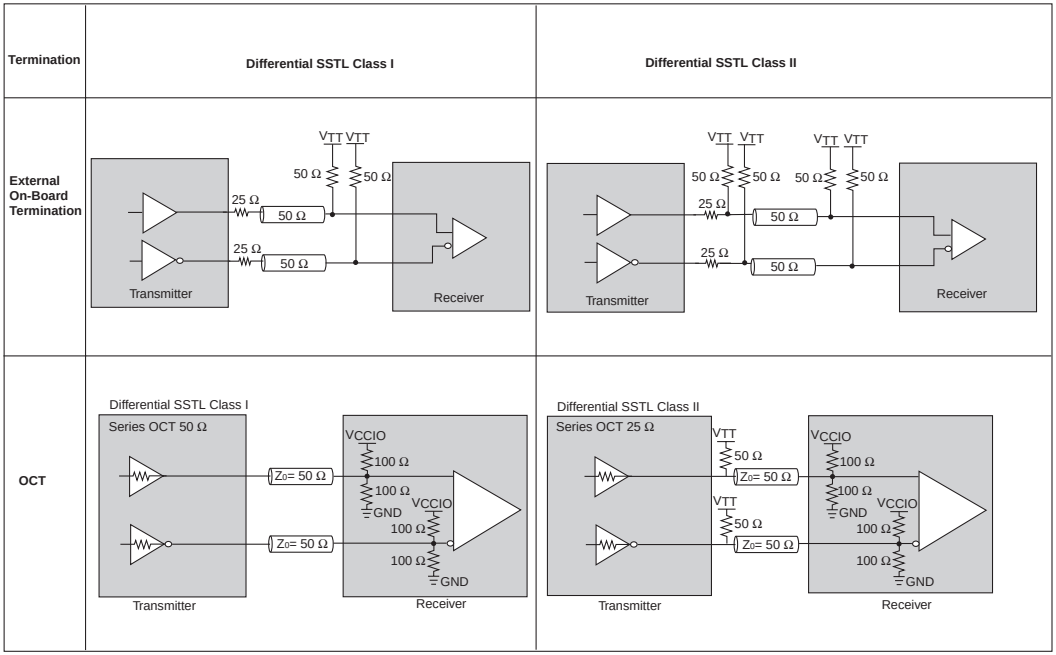
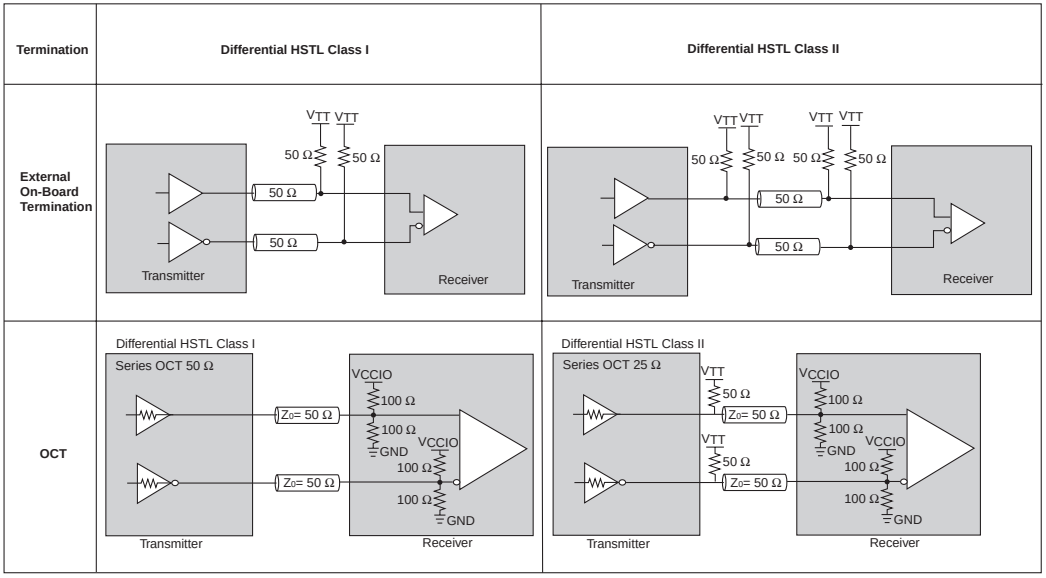


Figure 7–25. Stratix III Differential HSTL I/O Standard Termination

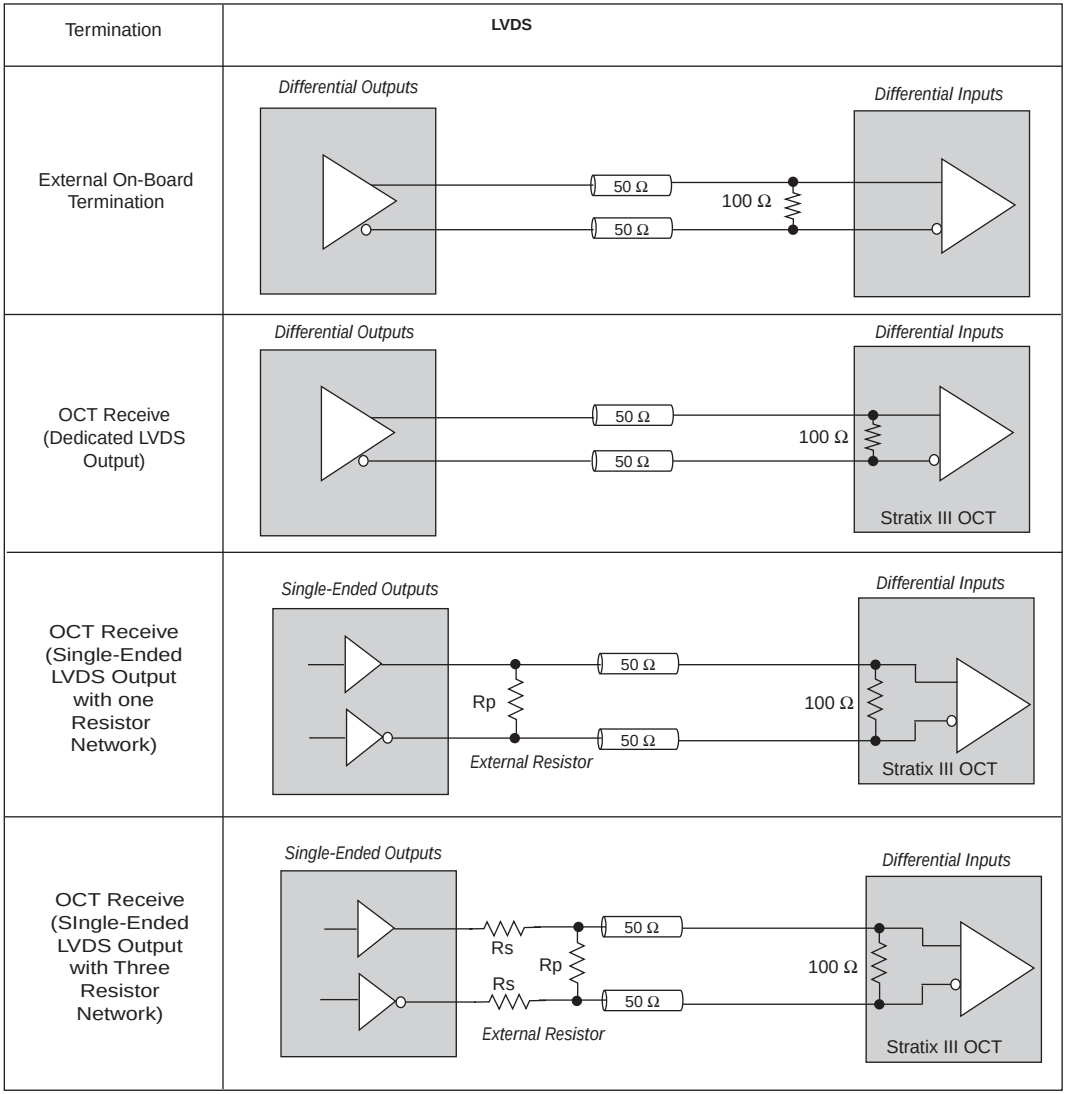


LVDS

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix III devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level. The LVDS input buffer requires 2.5-V V_{CCPD}. Use this standard in applications requiring high-bandwidth data transfer, backplane drivers, and clock distribution. LVDS requires a 100-Ω termination resistor between the two signals at the input buffer. Stratix III devices provide an optional 100-Ω differential termination resistor in the device using on-chip differential termination.

Figure 7–26 shows the details of LVDS termination. The on-chip differential resistor is only available in row I/O banks. The one-resistor topology is for a data rate of up to 200 Mbps. The three-resistor topology is for data rates of higher than 200 Mbps.

Figure 7–26. Stratix III LVDS I/O Standard Termination *Note (1)*



Note to Figure 7–26:

(1) The R_S and R_P values are pending characterization.

Differential LVPECL

In Stratix III devices, the LVPECL I/O standard is supported on input clock pins on column and row I/O banks. LVPECL output operation is not supported by Stratix III devices. LVDS input buffers are used to support LVPECL input operation. AC coupling is required when LVPECL common mode voltage of the output buffer is higher than Stratix III LVPECL input common mode voltage. Figure 7–27 shows the AC coupled termination scheme. The 50-Ω resistors used at the receiver end are external to the device.

DC-coupled LVPECL is supported if the LVPECL output common mode voltage is within the Stratix III LVPECL input buffer specification (see Figure 7–28).

Figure 7–27. LVPECL AC Coupled Termination

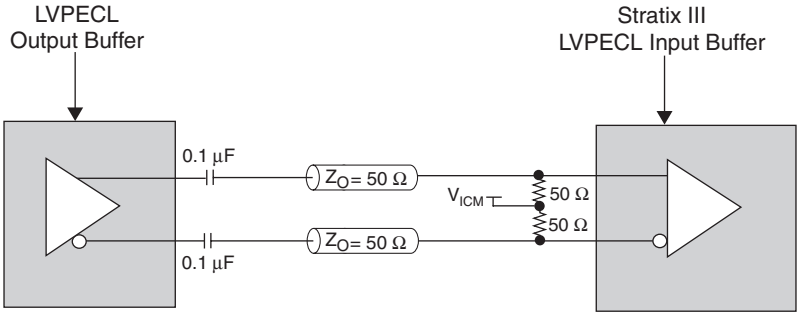
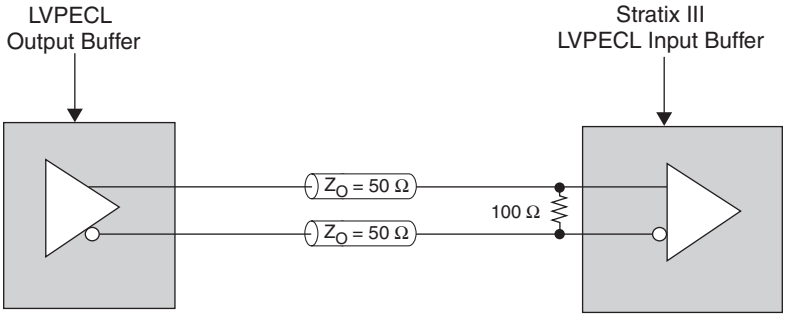


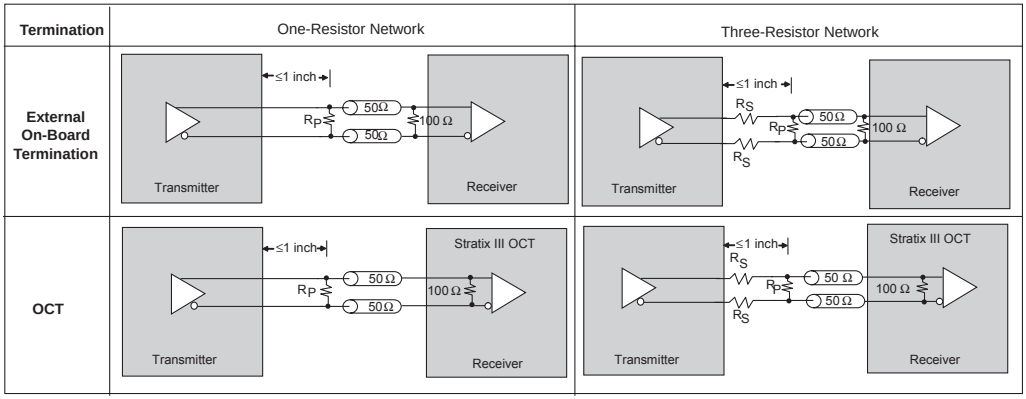
Figure 7–28. LVPECL DC Coupled Termination



RSDS

Stratix III devices support the RSDS output standard with a data rate up to 230 Mbps using LVDS output buffer types. For transmitters, use the LVDS output buffer with the external one- or three-resistor network as shown in Figure 7–29. The one-resistor topology is for a data rate of up to 200 Mbps. The three-resistor topology is for a data rate of higher than 200 Mbps.

Figure 7–29. Stratix III RSDS I/O Standard Termination *Note (1)*



Note to Figure 7–29:
(1) The R_S and R_P values are pending characterization.

A resistor network is required to attenuate the LVDS output-voltage swing to meet the RSDS specifications. You can modify the three-resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\Omega$$

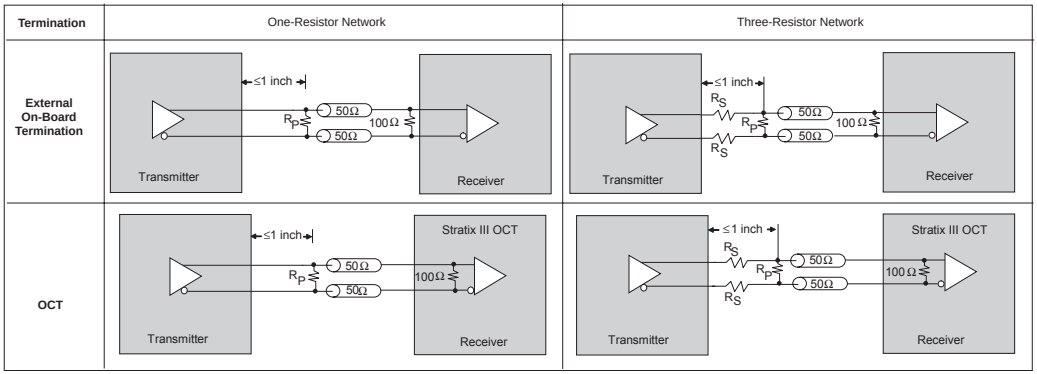
Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information on the RSDS I/O standard, refer to the *RSDS Specification* from the National Semiconductor web site at **www.national.com**.

mini-LVDS

Stratix III devices support the mini-LVDS output standard with a data rate up to 340 Mbps using LVDS output buffer types. For transmitters, use the LVDS output buffer with the external one- or three-resistor network as shown in Figure 7–30. The one-resistor topology is for a data rate of up to 200 Mbps. The three-resistor topology is for a data rate of higher than 200 Mbps.

Figure 7–30. Stratix III mini-LVDS I/O Standard Termination *Note (1)*



Note to Figure 7–30:
(1) The R_S and R_P values are pending characterization.

A resistor network is required to attenuate the LVDS output voltage swing to meet the mini-LVDS specifications. You can modify the three-resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy the following equation:

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\Omega$$

Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information on the mini-LVDS I/O standard, see the *mini-LVDS Specification* from the Texas Instruments web site at **www.ti.com**.

Design Considerations

While Stratix III devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other considerations that require attention to ensure the success of those designs.

I/O Termination

I/O termination requirements for single-ended and differential I/O standards are discussed in this section.

Single-Ended I/O Standards

Although single-ended, non-voltage-referenced I/O standards do not require termination, impedance matching is necessary to reduce reflections and improve signal integrity.

Voltage-referenced I/O standards require both an input reference voltage, $V_{REF,}$ and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device. Each voltage-referenced I/O standard requires a unique termination setup. For example, a proper resistive signal termination scheme is critical in SSTL2 standards to produce a reliable DDR memory system with superior noise margin.

Stratix III on-chip series and parallel termination provides the convenience of no external components. Alternatively, you can use external pull-up resistors to terminate the voltage-referenced I/O standards such as SSTL and HSTL.

Differential I/O Standards

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the signal line. Stratix III devices provide an optional differential on-chip resistor when using LVDS.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs*.

I/O Banks Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix III devices.

Non-Voltage-Referenced Standards

Each Stratix III device I/O bank has its own VCCIO pins and supports only one V_{CCIO}, either 1.2, 1.5, 1.8, 2.5, or 3 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments, as shown in Table 7–2.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Since an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs and 3-V LVCMOS inputs (not output or bi-directional pins).

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix III devices I/O bank supports multiple VREF pins feeding a common V_{REF} bus. The number of available VREF pins increases as device density increases. If these pins are not used as VREF pins, they cannot be used as generic I/O pins and should be tied to V_{CCIO} or GND. Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards as long as all voltage-referenced standards use the same V_{REF} setting.

For performance reasons, voltage-referenced input standards use their own V_{CCPD} level as the power source. This feature allows you to place voltage-referenced input signals in an I/O bank with any V_{CCIO} possible. For example, you can only place HSTL-15 input pins in an I/O bank with a 2.5-V V_{CCIO}.

Voltage-referenced bi-directional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both non-voltage-referenced and voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 2.5-V inputs (but not outputs), and HSTL and HSTL-15 I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

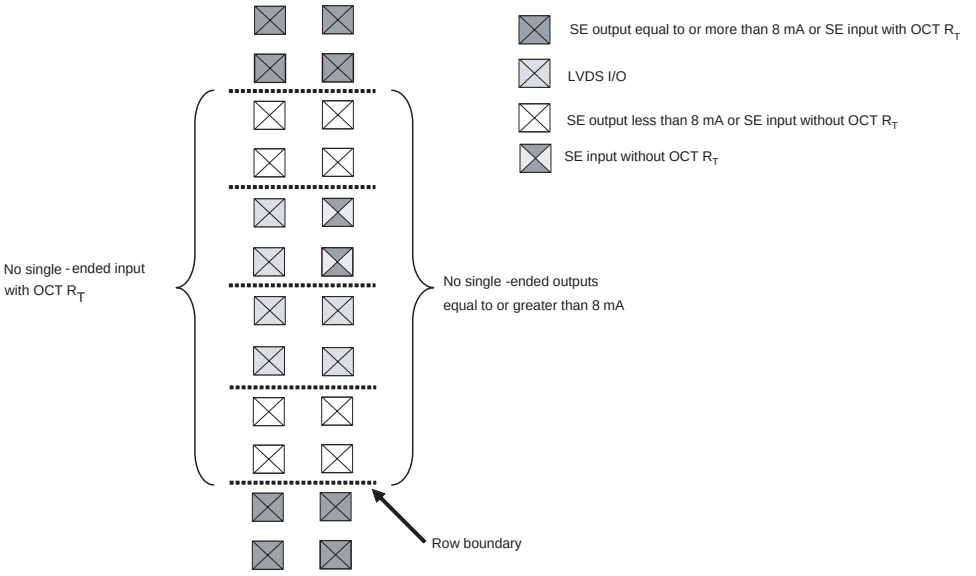
I/O Placement Guidelines

This section provides I/O placement guidelines for the programmable I/O standards supported by Stratix III devices and includes essential information for designing systems using the devices' selectable I/O capabilities.

I/O Pin Placement with Respect to LVDS I/O Pins

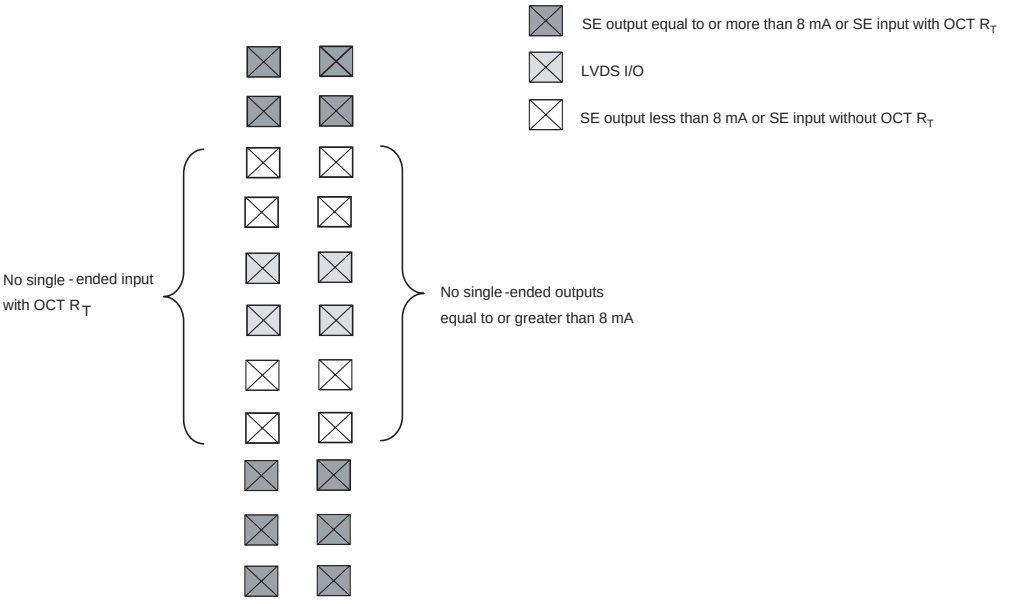
The placement of single-ended I/O pins with respect to LVDS I/O pins is restricted. As shown in Figure 7–31, you should place row I/O single-ended outputs with driving strength equal or greater than 8 mA at least one row away from the LVDS I/O. The same restriction applies to single-ended inputs with OCT R_T. You can place single-ended outputs with driving strength less than 8 mA in the rows adjacent to the LVDS I/O. The restriction does not apply when you use the LVDS input buffer for differential HSTL/SSTL input. Single-ended inputs without OCT R_T have no placement restriction. When DPA is enabled, the constraint on single-ended I/O is the same as that on regular LVDS I/O.

Figure 7–31. Single-Ended Row I/O Pin Placement with Respect to LVDS I/O Pins



The restriction on placing single-ended column I/O is similar to that on row I/O. You should place the single-ended outputs with driving strength equal or greater than 8 mA at least four I/Os away from the LVDS I/O. The same rule applies to single-ended input with OCT R_T. The restriction does not apply when the LVDS input buffer is used for differential HSTL/SSTL inputs. Single-ended outputs with a driving strength less than 8 mA and single-ended inputs without OCT R_T have no restriction. The single-ended I/O placement rules for column I/O are shown in Figure 7–32.

Figure 7–32. Single-Ended Column I/O Pin Placement with Respect to LVDS I/O Pins



Conclusion

Stratix III devices provide I/O capabilities that allow you to work in compliance with current and emerging I/O standards and requirements. With the Stratix III device features, you can reduce board design interface costs and increase development flexibility.

Document Revision History

Table 7–9 shows the revision history for this document.

Table 7–9. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Added the feature programmable input delay to "Stratix III I/O Structure" on page 7–13. Updated Table 7–4 and Table 7–7. Updated "LVDS Input On-Chip Termination (RD)" on page 7–27. Updated Figure 7–3 through Figure 7–8. Updated Figure 7–24, Figure 7–25. Minor text edits to page 14.	—
November 2006 v1.0	Initial Release	—

8. External Memory Interfaces in Stratix III Devices

SIII51008-1.1

Introduction

The Stratix® III I/O structure has been completely redesigned from the ground up to provide flexible and high-performance support for existing and emerging external memory standards. These include high-performance double data rate (DDR) memory standards such as DDR3, DDR2, DDR SDRAM; QDRII+, QDRII SRAM; and RLDRAM II at frequencies of up to 400 MHz.

Packed with features such as dynamic on-chip termination (OCT), trace mismatch compensation, read/write leveling, half data rate (HDR) blocks, and 4- to 36-bit programmable DQ group widths, Stratix III I/O elements provide easy-to-use built-in functionality required for a rapid and robust implementation.

Double data rate external memory support is found on all sides of the Stratix III FPGA. Stratix III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces with the new small modular I/O bank structure.

A self-calibrating megafunction (ALTMEMPHY) is optimized to take advantage of the Stratix III I/O structure, and along with the new Quartus® II timing analysis tool, TimeQuest, completes the picture to provide the total solution for the highest reliable frequency of operation across process, voltage, and temperature (PVT) variations.

Table 8–1 summarizes the maximum clock rate Stratix III devices can support with external memory devices.

Table 8–1. Stratix III Maximum Clock Rate Support for External Memory Interfaces Note (1)

Memory Standards	–2 Speed Grade (MHz)		–3 Speed Grade (MHz)		–4 Speed Grade (MHz)		-4L Speed Grade (MHz) (2)	
	Top/ Bottom I/O Banks	Left/ Right I/O Banks (3)	Top/ Bottom I/O Banks	Left/ Right I/O Banks (3)	Top/ Bottom I/O Banks	Left/ Right I/O Banks (3)	Top/ Bottom I/O Banks	Left/ Right I/O Banks
DDR3 SDRAM (4)	400 (5)	300	333	TBD (6)	333	TBD (6)	—	—
DDR2 SDRAM (4)	400 (5)	300	333	267	333	267	200	167
DDR SDRAM (4)	200	200	200	200	200	200	200	167
QDRII+ SRAM	350 (5)	300	300	250	300	250	—	—
QDRII SRAM (7)	350 (5)	300	300	250	300	250	167	133
RLDRAM II (7)	400 (5)	300	300	250	300	250	—	—

Notes to Table 8–1:

(1) Numbers are based on half-rate controller and are preliminary until characterization is final.
(2) Performance is based on 0.9-V core voltage. At 1.1-V core voltage, the -4L speed grade devices have the same performance as the -4 speed grade devices.
(3) Left / right I / O banks have lower maximum performance than the top / bottom I / O banks due to the left / right I / Os having higher pin capacitance to support the LVDS I / O standard.
(4) This applies for interfaces with both modules and components.
(5) Memory interfaces above 333 MHz require the use of the deskew circuitry pending characterization.
(6) Support will be evaluated after characterization.
(7) This applies to QDRII SRAM and RLDRAM II devices running at 1.5-V and 1.8-V I / O voltages.

Figure 8–1 shows a general block diagram for Stratix III external memory support, showing the phase-locked loop (PLL), delay-locked loop (DLL), and I / O banks. The number of available I / O banks depend on the device density.

Figure 8–1. Stratix III External Memory Support

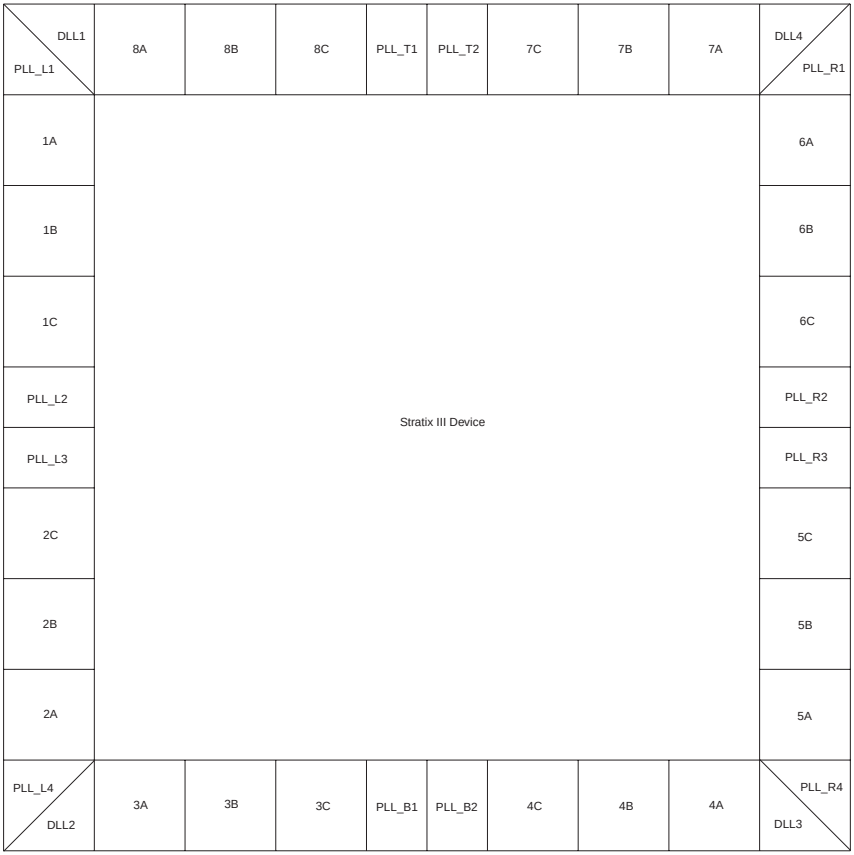
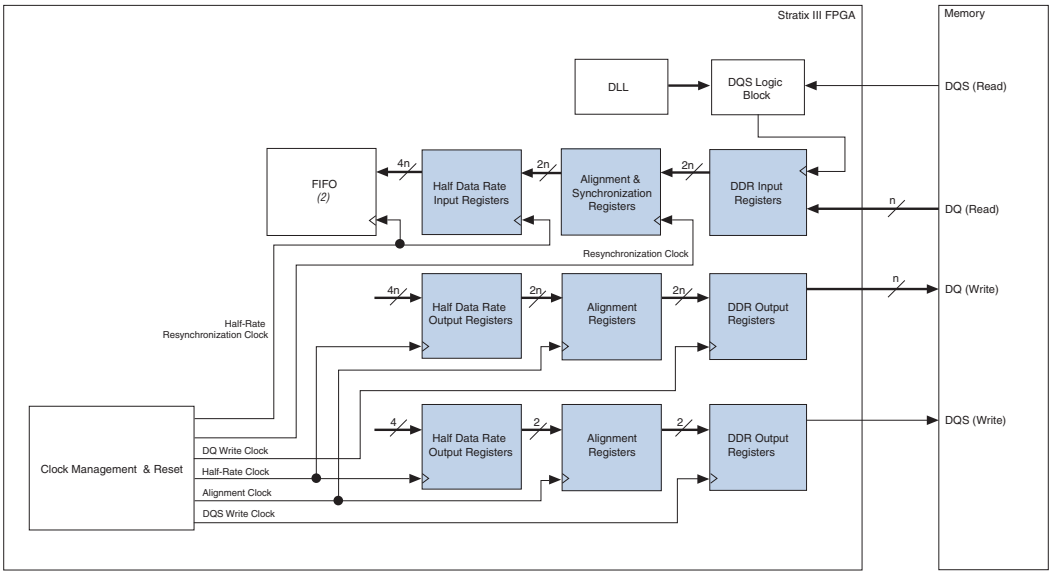


Figure 8–2 shows the overview of the memory interface data path.

Figure 8–2. External Memory Interface Data Path Overview *Note (1), (2)*



Note to Figure 8–2:

(1) Each register block can be bypassed.

(2) The blocks for each memory interface may differ slightly.

This chapter describes the hardware features in Stratix III devices that facilitate high-speed memory interfacing for each DDR memory standard. Stratix III devices feature DLLs, PLLs, dynamic OCT, read / write leveling, and deskew ciruitry.

Memory Interfaces Pin Support

A typical memory interface requires data (D, Q, or DQ), data strobe (DQS and DQSn / CQn), address, command, and clock pins. Some memory interfaces use data mask (DM) pins to enable write masking and QVLD pins to indicate that the read data is ready to be captured. This section describes how Stratix III devices support all these different pins.

Data and Data Clock/Strobe Pins

Stratix III DDR memory interface data pins are called DQ pins. The read data-strobes or clocks are called DQS pins. Depending on the memory specifications, the DQS pins can be bidirectional single-ended signals (in DDR2 and DDR SDRAM), unidirectional differential signals (in RLDRAM II), bidirectional differential signals (DDR3 and DDR2 SDRAM), or unidirectional complementary signals (QDRII+ and QDRII SRAM). Connect the unidirectional read data-strobes or clocks to Stratix III DQS pins and use any available DQ or DQS pins (in the same I / O bank or device side as the read data pins) for the unidirectional write data-strobes or clocks since trace lengths from the pins to registers are optimized on these pins.

Stratix III devices offer differential input buffers for differential read data-strobe / clock operations and provide an independent DQS logic block for each CQn pin for complementary read data-strobe / clock operations. In the Stratix III pin tables, the differential DQS pin-pairs are denoted as DQS and DQSn pins, while the complementary DQS signals are denoted as DQS and CQn pins. DQSn and CQn pins are marked separately in the pin table. Each CQn pin connects to a DQS logic block and the shifted CQn signals go to the active-low input registers in the DQ IOE registers.

In DDR2 SDRAM, you can use the optional differential DQS / DQSn feature in Stratix III devices for better signal integrity. You can also use the single-ended DQS option to reduce pin utilization.

The DQ pins can be bidirectional signals, as in DDR3, DDR2, and DDR SDRAM, and RLDRAM II common I / O (CIO) interfaces, or unidirectional signals, as in QDRII+, QDRII SRAM, and RLDRAM II separate I / O (SIO) devices. Connect the unidirectional read data signals to Stratix III DQ pins and the unidirectional write data signals to a different group of DQ pins.

Using a DQS / DQ group for the write data signals minimizes output skew, allows access to the write leveling circuitry, and allows vertical migration. These pins also have access to deskewing circuitry that can compensate for delay mismatch between signals on the bus.

Table 8–2 summarizes the pin connections between a Stratix III device and an external memory device.

Table 8–2. Stratix III Memory Interfaces Pin Utilization

Pin Description	Stratix III Pin Utilization
Read Data	DQ
Write Data	DQ *(1)*
Parity, DM, BWSn, ECC, QVLD	DQ
Read Clocks/Strobes	Differential DQS/DQSn for DDR3/DDR2 SDRAM and RLDRAM II *(2)*
	Single-ended DQS for DDR2/DDR SDRAM *(2)*
	Complementary DQS/CQn for QDRII+/QDRII SRAM
Write Clocks/Strobes	Any unused DQ or DQS pins for QDRII+/QDRII SRAM and RLDRAM II
Memory Clocks	Any unused DQ pins for DDR3 SDRAM (for write leveling access)
	Adjacent user I/Os for other memory interfaces

Notes to Table 8–2:

(1) If write data is unidirectional, connect write data to a separate DQ group other than the read DQ group.

(2) DDR2 SDRAM support either single-ended or differential DQS signaling.

The DQS and DQ pins use DQS phase-shift circuitry (described in "Stratix III External Memory Interface Features" on page 8–22) to compensate for PVT variations. The DQS and DQ pin locations are fixed in the pin table. The memory interface circuitry is available in every Stratix III I/O bank. All the memory interface pins support the I/O standards required to support DDR3, DDR2, and DDR SDRAM; QDRII+ and QDRII SRAM; and RLDRAM II devices.

DQ and DQS output signals are generated using the DDIO registers. The clock generating the DQS signals has a 90° phase offset compared to the clock generating the DQ signals.

Every I/O bank in the Stratix III device can support DQS and DQ signals with DQ bus modes of ×4, ×8/×9, ×16/×18, or ×32/×36 although not all devices support ×16/×18 or ×32/×36 (see Table 8–4). In ×4 mode, each DQS and DQSn pin-pair drives up to four DQ pins within that group. There is no support for the CQn pin in this mode. In ×8/×9 mode, each DQS and DQSn/CQn pin-pair drives up to ten DQ pins, to support one parity bit or DM, eight data bits, and an optional QVLD pin. If the parity bit, DM bit, QVLD pin, or any data bit is not used, these pins can be used as regular user I/O pins.

Similarly, with ×16/×18 and ×32/×36 modes, each DQS and DQSn/CQn pin-pair drives up to 19 and 37 DQ pins, respectively, with the optional QVLD pin in each group. There are two parity or DM bits (counted in the number of DQ pins) in the ×16/×18 mode and four parity or DM bits in the ×32/×36 mode. Table 8–3 lists the maximum number of pins per DQS/DQ bus mode, including the DQS and DQSn/CQn pin-pair.

Table 8–3. Stratix III DQS/DQ Bus Mode Pins

Mode	DQSn Support	CQn Support	Maximum Number of Pins per Group	Data	Parity (Optional)	QVLD (Optional)
×4	Yes	No	6	4	-	-
×8/×9 *(1)*	Yes	Yes	12	8	1	1
×16/×18 *(2)*	Yes	Yes	21	16	2	1
×32/×36 *(3)*	Yes	Yes	39	32	4	1

Notes to Table 8–3:

(1) Two ×4 DQ groups are stitched to make a ×8/×9 group. One pin from one of the original ×4 group becomes a user I/O pin.

(2) Four ×4 DQ groups are stitched to make a ×16/×18 group. Three pins from any of the original ×4 group become user I/O pins.

(3) Eight ×4 DQ groups are stitched to make a ×32/×36 group. Nine pins from any of the original ×4 group become user I/O pins.

Table 8–4 shows the maximum number of DQS/DQ groups per side of the Stratix III device. For a more detailed listing of the number of DQS/DQ groups available per bank in each Stratix III device, see Figures 8–3 through Figure 8–8.

Table 8–4. Number of DQS/DQ Groups in Stratix III Devices per Side (Part 1 of 3) Note (1), (2)

Device	Package	Side	×4	×8/×9	×16/×18	×32/×36
EP3SE50/ EP3SL50/ EP3SL70	484-pin FineLine BGA®	Left	12	4	0	0
		Bottom	5	2	0	0
		Right	12	4	0	0
		Top	5	2	0	0
	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0

Table 8–4. Number of DQS/DQ Groups in Stratix III Devices per Side (Part 2 of 3) *Note (1), (2)*

Device	Package	Side	×4	×8/×9	×16/×18	×32/×36
EP3SE80/ EP3SE110/ EP3SL110/ EP3SL150	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0
	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
EP3SL200	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0
	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
	1517-pin FineLine BGA	Left	26	12	4	0
		Bottom	38	18	8	4
		Right	26	12	4	0
		Top	38	18	8	4
EP3SE260	780-pin FineLine BGA	Left	14	6	2	0
		Bottom	17	8	2	0
		Right	14	6	2	0
		Top	17	8	2	0
	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
	1517-pin FineLine BGA	Left	34	16	6	0
		Bottom	38	18	8	4
		Right	34	16	6	0
		Top	38	18	8	4

Table 8–4. Number of DQS/DQ Groups in Stratix III Devices per Side (Part 3 of 3) Note (1), (2)

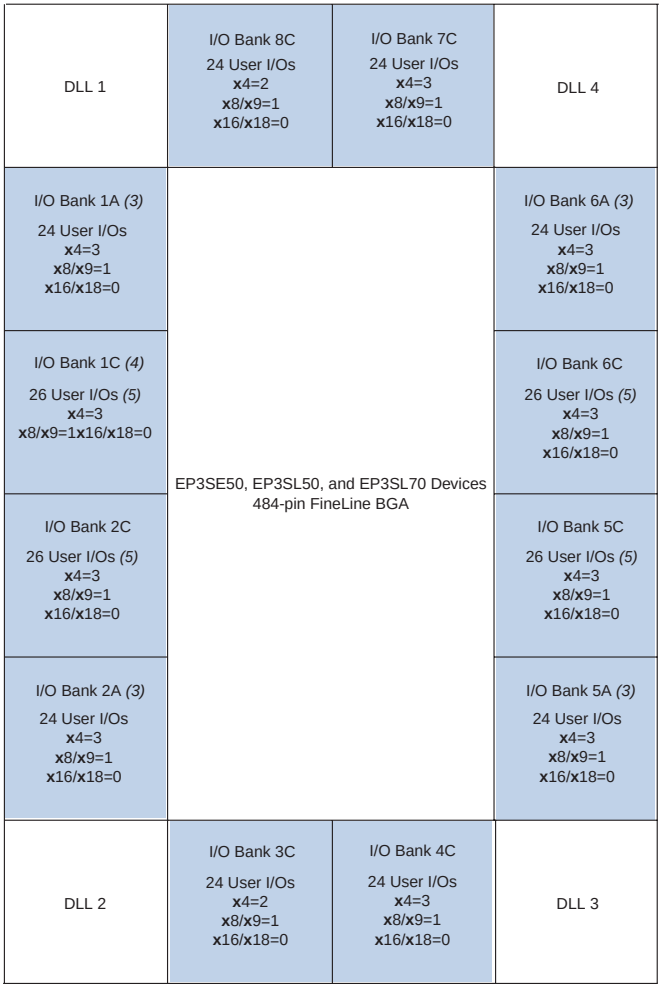
Device	Package	Side	×4	×8/×9	×16/×18	×32/×36
EP3SL340	1152-pin FineLine BGA	Left	26	12	4	0
		Bottom	26	12	4	0
		Right	26	12	4	0
		Top	26	12	4	0
	1517-pin FineLine BGA	Left	34	16	6	0
		Bottom	38	18	8	4
		Right	34	16	6	0
		Top	38	18	8	4
	1760-pin FineLine BGA	Left	40	18	6	0
		Bottom	44	22	10	4
		Right	40	18	6	0
		Top	44	22	10	4

Note to Table 8–4:

(1) Numbers are preliminary.

(2) Some of the DQS / DQ pins can also be used as R_{UP} / R_{DN} or configuration pins. Make sure that the DQS / DQ groups that you have chosen are not also used for configuration or OCT calibration.

Figure 8–3. Number of DQS/DQ Groups per Bank in EP3SE50, EP3SL50, and EP3SL70 Devices in 484-pin FineLine BGA Package *Notes (1), (2)*



Notes to Figure 8–3:

(1) Numbers are preliminary.

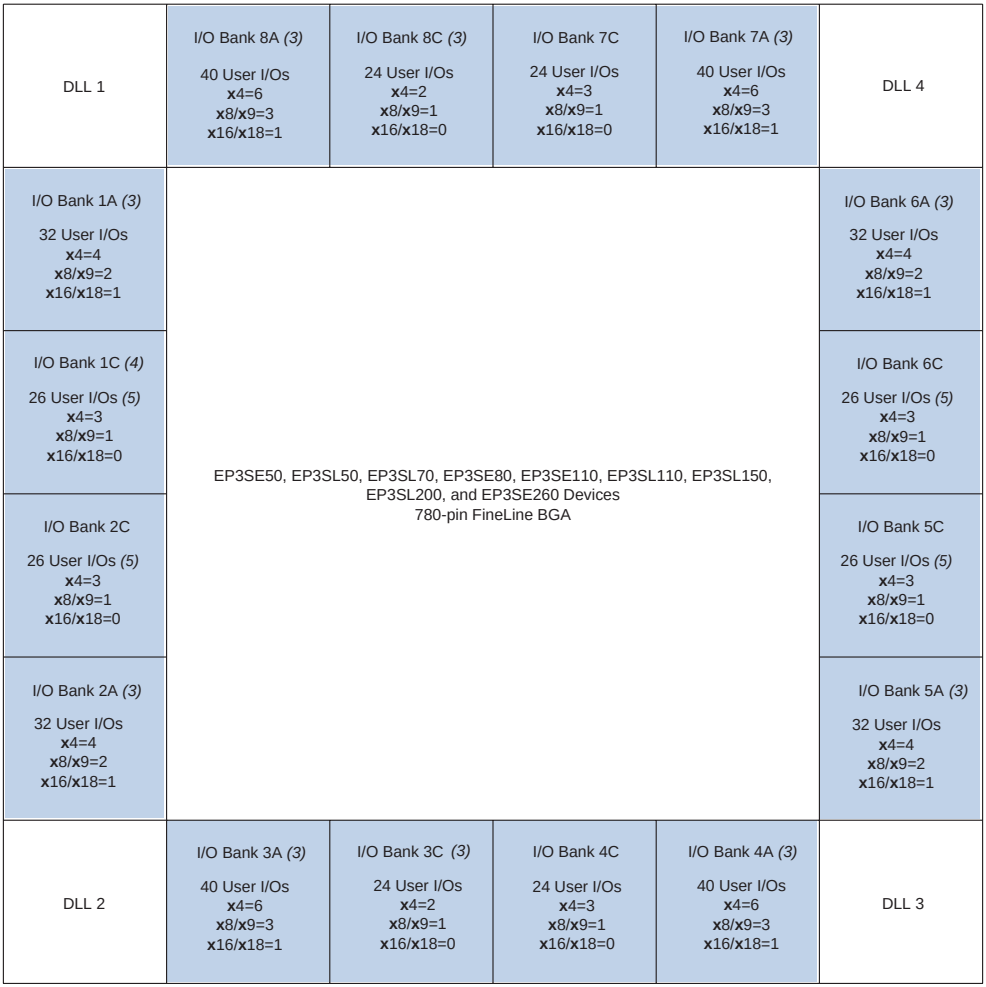
(2) This device does not support ×32/×36 mode.

(3) Some of the ×4 groups may use R_{UP}/R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration.

(4) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(5) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`)

Figure 8–4. Number of DQS/DQ Groups per Bank in EP3SE50, EP3SL50, EP3SL70, EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, and EP3SE260 Devices in 780-pin FineLine BGA Package *Notes (1), (2)*



Notes to Figure 8–4:

(1) Numbers are preliminary until devices are available.

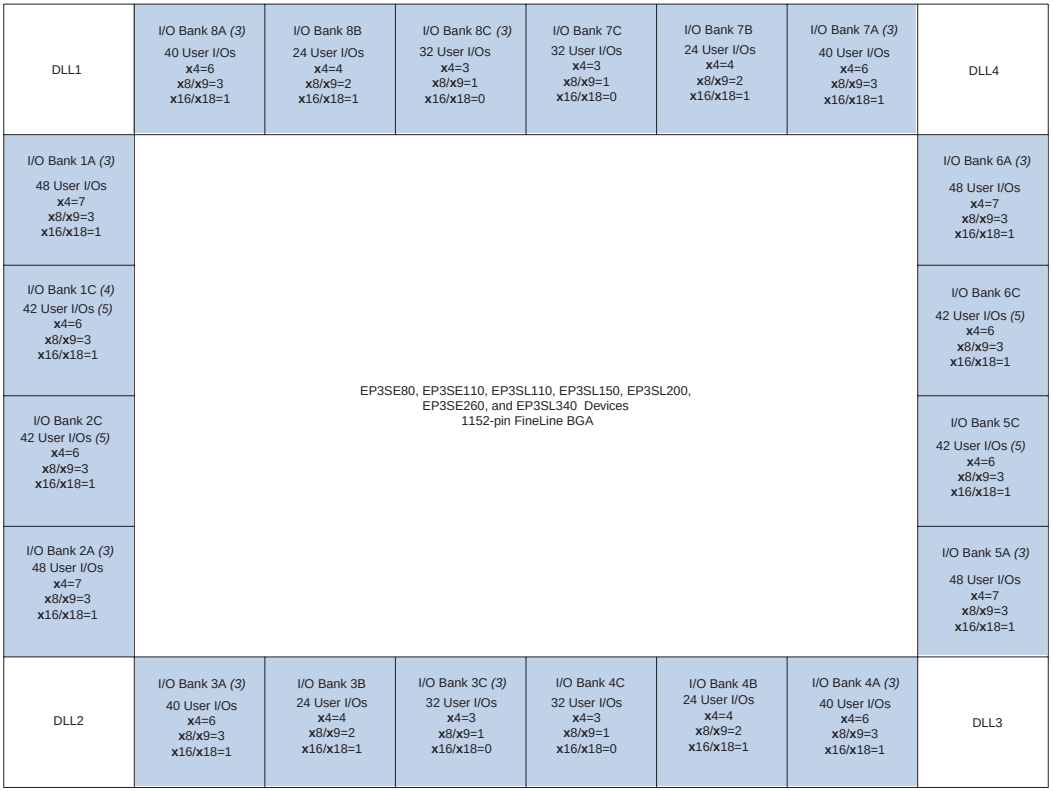
(2) This device does not support ×32/×36 mode.

(3) Some of the ×4 groups may use R_{UP}/R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration. Only EP3SE260 has OCT calibration blocks in I/O banks 3C and 8C.

(4) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(5) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`)

Figure 8–5. Number of DQS/DQ Groups in EP3SE80, EP3SE110, EP3SL110, EP3SL150, EP3SL200, EP3SE260, and EP3SL340 Devices in 1152-pin FineLine BGA Package *Notes (1), (2)*



Notes to Figure 8–5:

(1) Numbers are preliminary until devices are available.

(2) This device does not support ×32/×36 mode.

(3) Some of the ×4 groups may use R_{UP}/R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration. Only EP3SE260 and EP3SL340 has OCT calibration blocks in I/O banks 3C and 8C.

(4) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

(5) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`)

Figure 8–6. Number of DQS/DQ Groups per Bank in EP3SL200 Devices in 1517-pin FineLine BGA Package *Note (1)*

<table>
<tr><td>DLL1</td><td>I/O Bank 8A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 8B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 8C
32 User I/Os
x4=3
x8/x9=1
x16/x18=0
x32/x36=0</td><td>I/O Bank 7C
32 User I/Os
x4=3
x8/x9=1
x16//x18=0
x32/x36=0</td><td>I/O Bank 7B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 7A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>DLL4</td></tr>
<tr><td>I/O Bank 1A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td colspan="5" rowspan="4">EP3SL200 Devices
1517-pin FineLine BGA</td><td>I/O Bank 6A (2)
50 User I/Os
x4=7
x8/x9=3
x6/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 1C (4)
42 User I/Os (3)
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 6C
42 User I/Os (3)
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 2C
42 User I/Os (3)
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 5C
42 User I/Os (3)
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 2A (2)
50 User I/Os
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 5A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>DLL2</td><td>I/O Bank 3A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 3B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 3C
32 User I/Os
x4=3
x8/x9=1
x16/x18=0
x32/x36=0</td><td>I/O Bank 4C
32 User I/Os
x4=3
x8/x9=1
x16/x18=0
x32/x36=0</td><td>I/O Bank 4B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 4A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>DLL3</td></tr>
</table>

Notes to Figure 8–6:

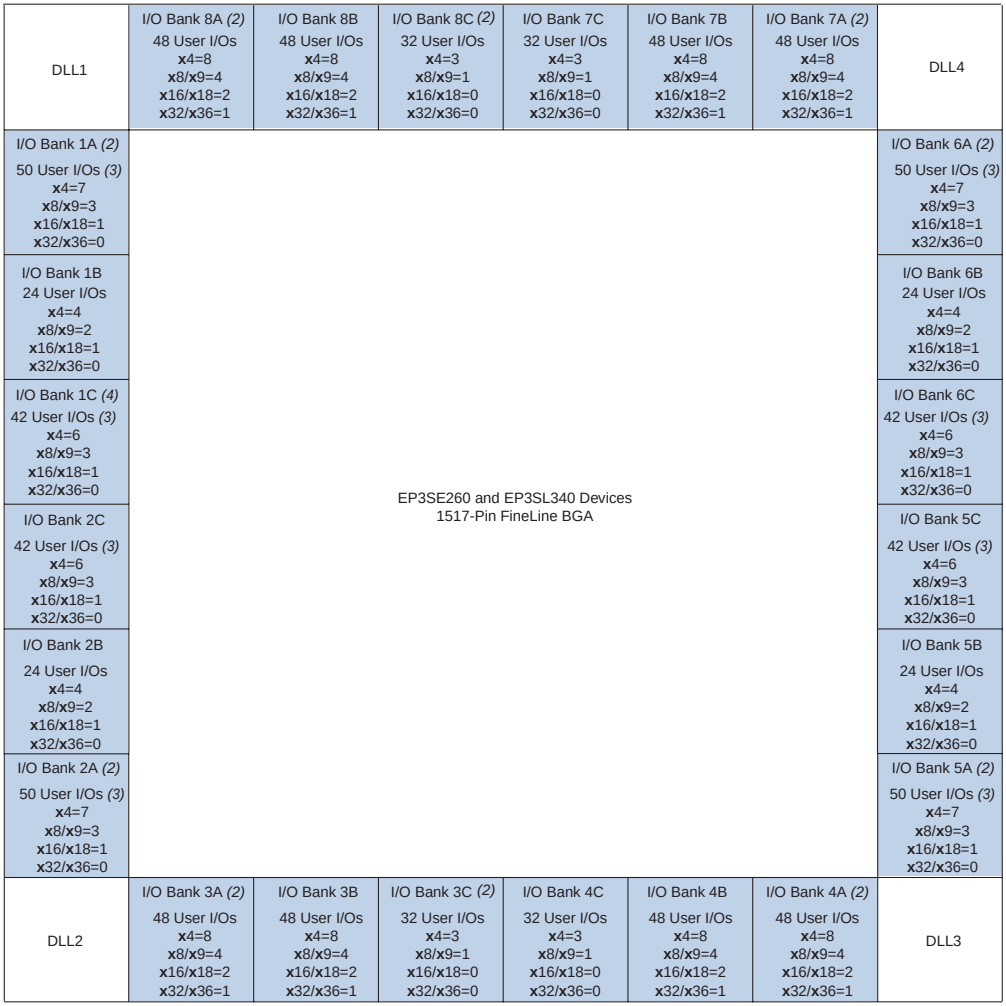
(1) Numbers are preliminary.

(2) Some of the ×4 groups may use R_{UP} / R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration.

(3) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

(4) Some of the DQS/DQ pins in this bank can also be used as configuration pins. Choose the DQS/DQ pins that are not going to be used by your configuration scheme.

Figure 8–7. Number of DQS/DQ Groups per Bank in EP3SE260 and EP3SL340 Devices in 1517-pin FineLine BGA Package *Note (1)*



Notes to Figure 8–7:

(1) Numbers are preliminary.

(2) Some of the ×4 groups may use R_{UP} / R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration.

(3) All I / O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

(4) Some of the DQS / DQ pins in this bank can also be used as configuration pins. Choose the DQS / DQ pins that are not going to be used by your configuration scheme.

Figure 8–8. DQS/DQ Bus Mode Support per Bank in EP3SL340 Devices in 1760-pin FineLine BGA Package *Note (1)*

<table>
<tr><td>DLL1</td><td>I/O Bank 8A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 8B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 8C (2)
48 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 7C
48 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 7B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 7A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>DLL4</td></tr>
<tr><td>I/O Bank 1A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td colspan="5" rowspan="8">EP3SL340 Devices
1760-pin FineLine BGA</td><td>I/O Bank 6A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 1B
36 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 6B
36 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 1C (4)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 6C
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 2C
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 5C
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 2B
36 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 5B
36 User I/Os (3)
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>I/O Bank 2A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 5A (2)
50 User I/Os (3)
x4=7
x8/x9=3
x16/x18=1
x32/x36=0</td></tr>
<tr><td>DLL2</td><td>I/O Bank 3A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 3B
48 User I/Os
x4=8
x81x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 3C (2)
48 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 4C
48 User I/Os
x4=6
x8/x9=3
x16/x18=1
x32/x36=0</td><td>I/O Bank 4B
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>I/O Bank 4A (2)
48 User I/Os
x4=8
x8/x9=4
x16/x18=2
x32/x36=1</td><td>DLL3</td></tr>
</table>

Notes to Figure 8–8:

(1) Numbers are preliminary.

(2) Some of the ×4 groups may use R_{UP} / R_{DN} pins as DQ pins. You cannot use these groups if you are using these R_{UP} and R_{DN} pins for OCT calibration.

(3) All I / O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

(4) Some of the DQS / DQ pins in this bank can also be used as configuration pins. Choose the DQS / DQ pins that are not going to be used by your configuration scheme.

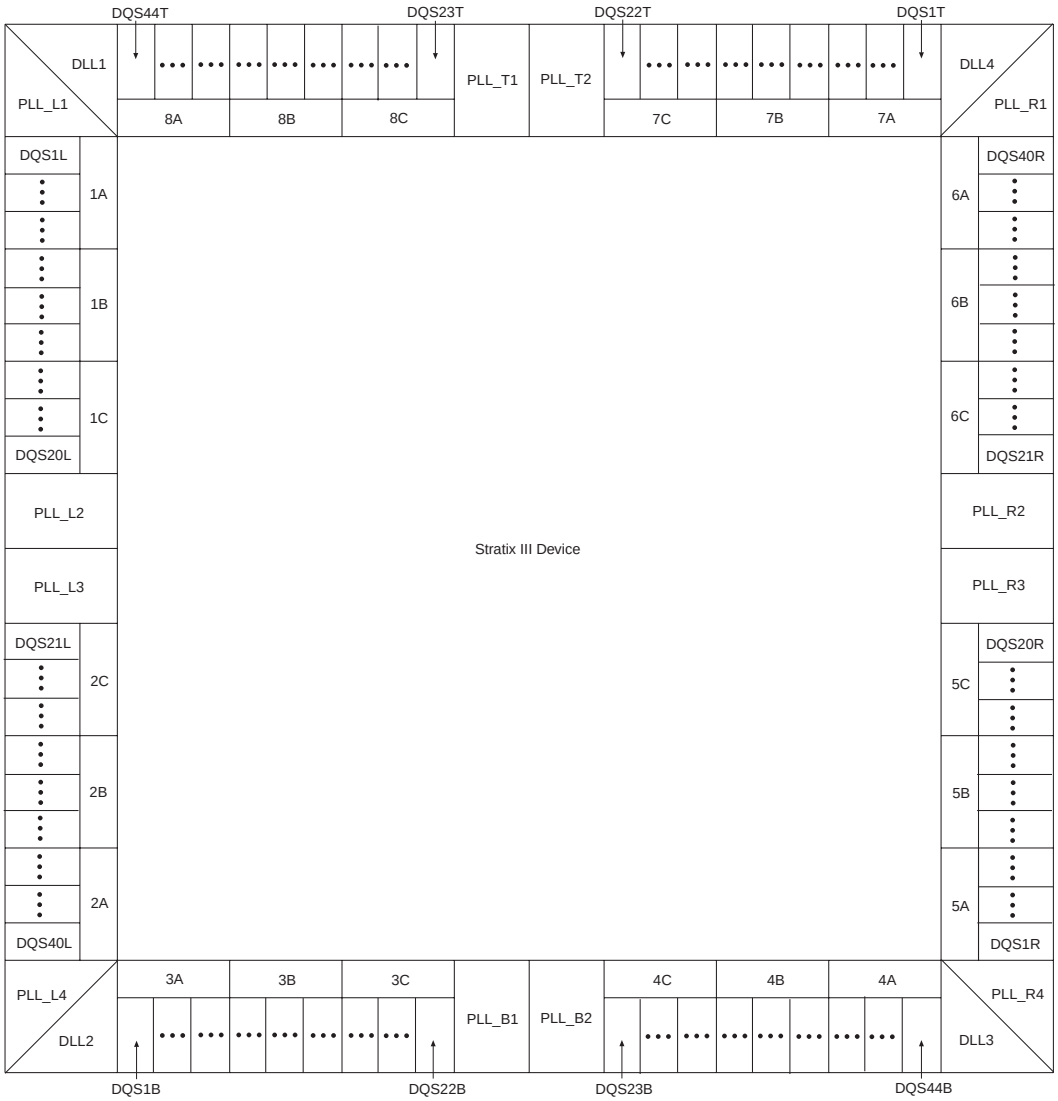
The DQS and DQSn pins are listed in the Stratix III pin tables as DQS*XY* and DQSn*XY*, respectively, where *X* denotes the DQS/DQ grouping number, and *Y* denotes whether the group is located on the top (*T*), bottom (*B*), left (*L*), or right (*R*) side of the device.

The corresponding DQ pins are marked as DQ*XY*, where *X* indicates which DQS group the pins belong to and *Y* indicates whether the group is located on the top (*T*), bottom (*B*), left (*L*), or right (*R*) side of the device. For example, DQS1L indicates a DQS pin, located on the left side of the device. See Figure 8–9 for illustrations. The DQ pins belonging to that group will be shown as DQ1L in the pin table.

The numbering scheme starts from the top left side of the device going counter-clockwise. Figure 8–9 shows how the DQS/DQ groups are numbered in the device. The top and bottom sides of the device can contain up to 44 ×4 DQS/DQ groups, and the left and right sides of the device can contain up to 40 ×4 DQS/DQ groups.

The parity, DM, BWSn, ECC, and QVLD pins are shown as DQ pins in the pin table. When not used as memory interface pins, these pins are available as regular I/O pins.

Figure 8–9. DQS Pins in Stratix III I/O Banks



The DQ pin numbering is based on ×4 mode. In ×4 mode, there are up to eight DQS/DQ groups per I/O bank. Each ×4 mode DQS/DQ group consists of a DQS pin, a DQSn pin, and four DQ pins. In ×8/×9 mode, the I/O bank combines two adjacent ×4 DQS/DQ groups; one pair of DQS and DQSn/CQn pins can drive all the DQ and parity pins in the new combined group that consists of up to 10 DQ pins (including parity or DM

and QVLD pins) and a pair of DQS and DQSn/CQn pins. Similarly, in ×16/×18 mode, the I/O bank combines four adjacent ×4 DQS/DQ groups to create a group with a maximum of 19 DQ pins (including parity or DM and QVLD pins) and a pair of DQS and DQSn/CQn pins. In ×32/×36 mode, the I/O bank combines eight adjacent ×4 DQS DQ groups together to create a group with a maximum of 37 DQ pins (including parity or DM and QVLD pins) and a pair of DQS and DQSn/CQn pins.

Stratix III modular I/O banks allow easy formation of the DQS/DQ groups. If all the pins in the I/O banks are user I/O pins and are not used for programming, R_{UP}/R_{DN} used for OCT calibration, or PLL clock output pins, you can divide the number of I/O pins in the bank by 6 to get the maximum possible number of ×4 groups. You can then divide that number by 2, 4, or 8 to get the maximum possible number of ×8/×9, ×16/×18 or ×32/×36, respectively (see Table 8–5). However, some of the pins in the I/O bank may be used for other functions.

Table 8–5. DQ/QS Group in Stratix III Modular I/O Banks

Modular I/O Bank Size	Maximum Possible Number of ×4 Groups *(1)*	Maximum Possible Number of ×8/×9 Groups	Maximum Possible Number of ×16/×18 Groups	Maximum Possible Number of ×32/×36 Groups
24 pins	4	2	1	0
32 pins	5	2	1	0
40 pins	6	3	1	0
48 pins	8	4	2	1

Note to Table 8–5:

(1) Some of the ×4 groups may use RUP/RDN pins. You cannot use these groups if you use the Stratix III calibrated OCT feature.

Optional Parity, DM, BWSn, ECC and QVLD Pins

You can use any of the DQ pins from the same DQS/DQ group for data as parity pins in Stratix III devices. The Stratix III device family supports parity in the ×8/×9, ×16/×18, and ×32/×36 modes. There is one parity bit available per eight bits of data pins. Use any of the DQ (or D) pins in the same DQS/DQ group as data for parity as they are treated, configured, and generated like a DQ pin.

The data mask (DM) pins are only required when writing to DDR3, DDR2, and DDR SDRAM, and RLDRAM II devices. QDRII+ and QDRII SRAM devices use the BWSn signal to select which byte to write into the memory. A low signal on the DM or BWSn signals indicates that the write

is valid. If the DM/BWSn signal is high, the memory will mask the DQ signals. If the system does not require write data masking, connect the memory DM pins low to indicate every write data is valid. You can use any of the DQ pins in the same DQS/DQ group as write data for the DM/BWSn signals. Each group of DQS and DQ signals in DDR3, DDR2, and DDR SDRAM devices requires a DM pin. There is one DM pin per RLDRAM II device and one BWSn pin per byte (eight bits) of QDRII+/QDRII SRAM data. Generate the DM or BWSn signals using DQ pins and configure the signals similarly as the DQ (or D) output signals. Stratix III devices do not support DM signal in ×4 DDR3 SDRAM or in ×4 DDR2 SDRAM interfaces with differential DQS signaling.

Some DDR3, DDR2, and DDR SDRAM devices or modules support error correction coding (ECC), which is a method of detecting and automatically correcting errors in data transmission. In a 72-bit DDR3, DDR2, or DDR SDRAM interface, typically eight ECC pins are used in addition to the 64 data pins. Connect the DDR3, DDR2, and DDR SDRAM ECC pins to a Stratix III device DQS/DQ group. These signals are also generated like DQ pins. The memory controller needs encoding and decoding logic for the ECC data. Designers can also use the extra byte of data for other error checking methods.

QVLD pins are used in RLDRAM II and QDRII+ SRAM interfaces to indicate the read data availability. There is one QVLD pin per memory device. A high on QVLD indicates that the memory is outputting the data requested. Similar to DQ inputs, this signal is edge-aligned with the read clock signals (CQ/CQn in QDRII+/QDRII SRAM and QK/QK# in RLDRAM II) and is sent half a clock cycle before data starts coming out of the memory. The QVLD pin is treated and supported like a DQ pin, so connect the QVLD pin to any available DQ pins in a read data group.

Refer to the "Data and Data Clock/Strobe Pins" on page 8–5 section for more information on the parity, ECC, and QVLD pins as these pins are treated as DQ pins.

Address and Control/Command Pins

Address and control/command signals are typically sent at single data rate. The only exception is in QDRII SRAM burst-of-two devices, where the read address needs to be captured on the rising edge of the clock while the write address needs to be captured on the falling edge of the clock by the memory. There is no special circuitry required for the address and control/command pins. You can use any of the user I/O pins in the same I/O bank as the data pins.

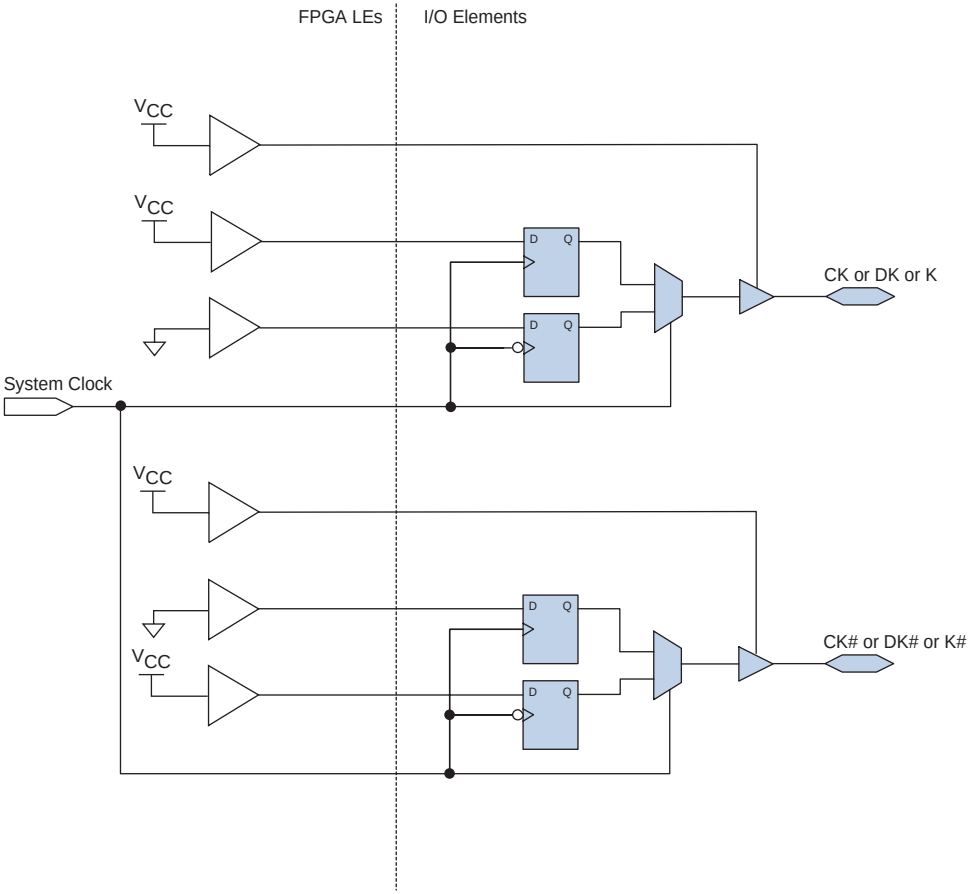
Memory Clock Pins

In addition to DQS (and CQn) signals to capture data, DDR3, DDR2, DDR SDRAM, and RLDRAM II use an extra pair of clocks, called CK and CK# signals, to capture the address and control/command signals. The CK/CK# signals should be generated to mimic the write data-strobe using Stratix III DDR I/O registers (DDIOs) to ensure that timing relationships between CK/CK# and DQS signals (t_{DQSS} in DDR3, DDR2, and DDR SDRAM or t_{CKDK} in RLDRAM II) are met. The device can use any I/O pins to generate CK/CK# signals for DDR2 and DDR SDRAM. However, Stratix III devices require available DQS or DQ pins in a separate DQS group for CK/CK# signals in DDR3 interfaces to access the write leveling circuitry. You can also generate RLDRAM II DK/DK# signals using Stratix III DDIOs on any available DQS or DQ pins.

QDRII+ and QDRII SRAM devices use the same clock (K/K#) to capture data, address, and control/command signals. Generate these signals using DDIOs in the same way as the D pins to ensure both K/K# and D signals are subjected to the same PVT variations.

Figure 8–10 shows the memory clock generation block diagram for Stratix III devices.

Figure 8–10. Memory Clock Generation Block Diagram



Stratix III External Memory Interface Features

Stratix III devices are rich with features that allow robust high-performance external memory interfacing. The ALTMEMPHY megafunction allows you to set these external memory interface features and helps set up the physical interface (PHY) best suited for your system. This section describes each Stratix III device feature that is used in external memory interfaces from the DQS phase-shift circuitry, DQS logic block, leveling multiplexers, dynamic OCT control block, IOE registers, IOE features, and the PLL.

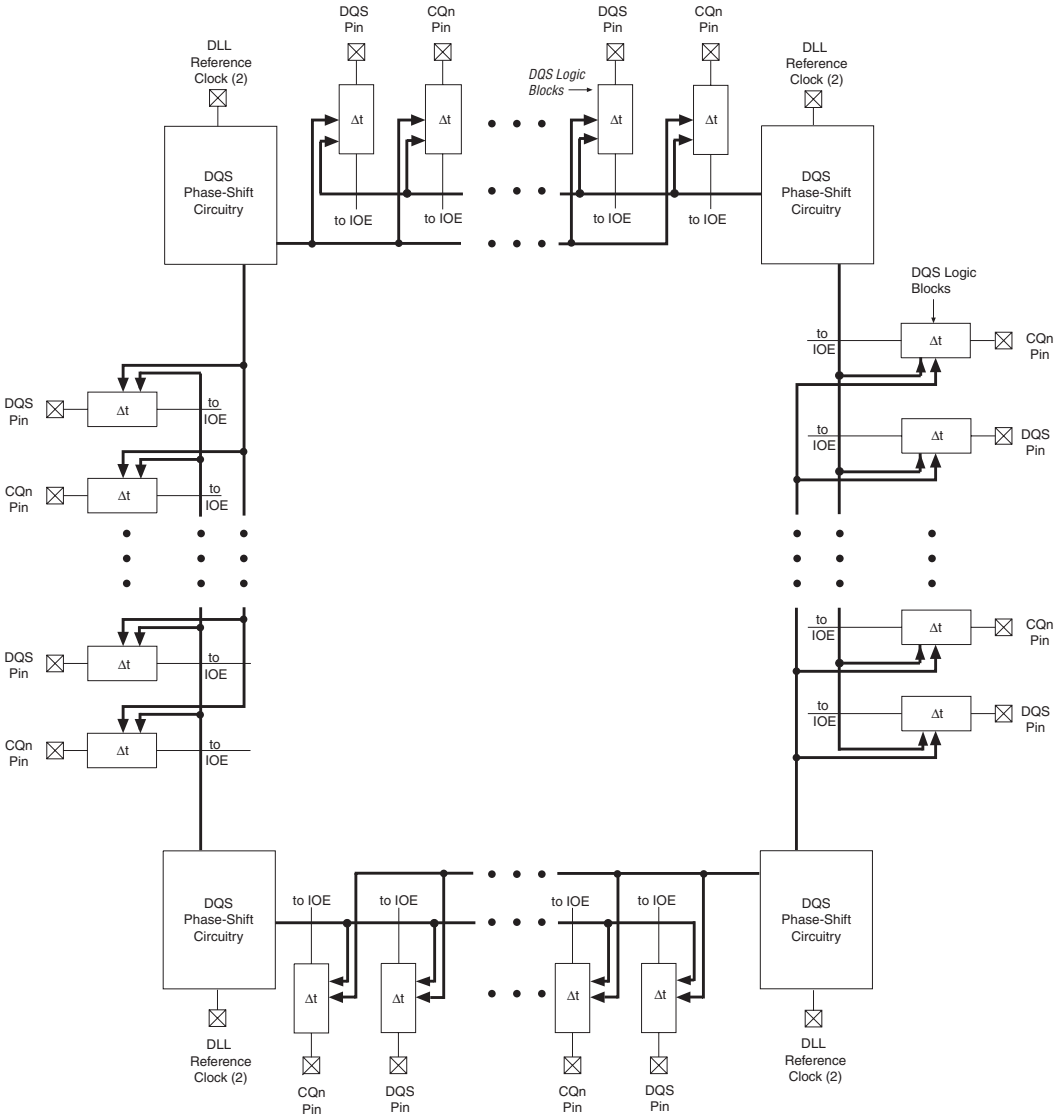
When using the Altera memory controller MegaCore® functions, the PHY is instantiated for you.

The ALTMEMPHY megafunction and the Altera memory controller MegaCore functions run at half the frequency of the I/O interface of the memory devices to allow better timing management in high-speed memory interfaces. Stratix III devices have built-in registers to convert data from full-rate (the I/O frequency) to half-rate (the controller frequency) and vice versa. These registers can be bypassed if your memory controller is not running at half the rate of the I/O frequency.

DQS Phase-Shift Circuitry

The Stratix III phase-shift circuitry provides phase shift to the DQS and CQn pins on read transactions, when the DQS and CQn pins are acting as input clocks or strobes to the FPGA. The DQS phase-shift circuitry consists of DLLs that are shared between multiple DQS pins and the phase-offset module to further fine-tune the DQS phase shift for different sides of the device. Figure 8–11 shows how the DQS phase-shift circuitry is connected to the DQS and CQn pins in the device.

Figure 8–11. DQS and CQn Pins and DQS Phase-Shift Circuitry *Note (1)*



Notes to Figure 8–11:

(1) Refer to the "DLL" on page 8–24 section for possible reference input clock pins for each DLL.

(2) Each DQS/CQn pin determines its phase shift with one of two possible DLL output settings.

The DQS phase-shift circuitry is connected to the DQS logic blocks that control each DQS or CQn pin. The DQS logic blocks allow the DQS delay settings to be updated concurrently at every DQS or CQn pin.

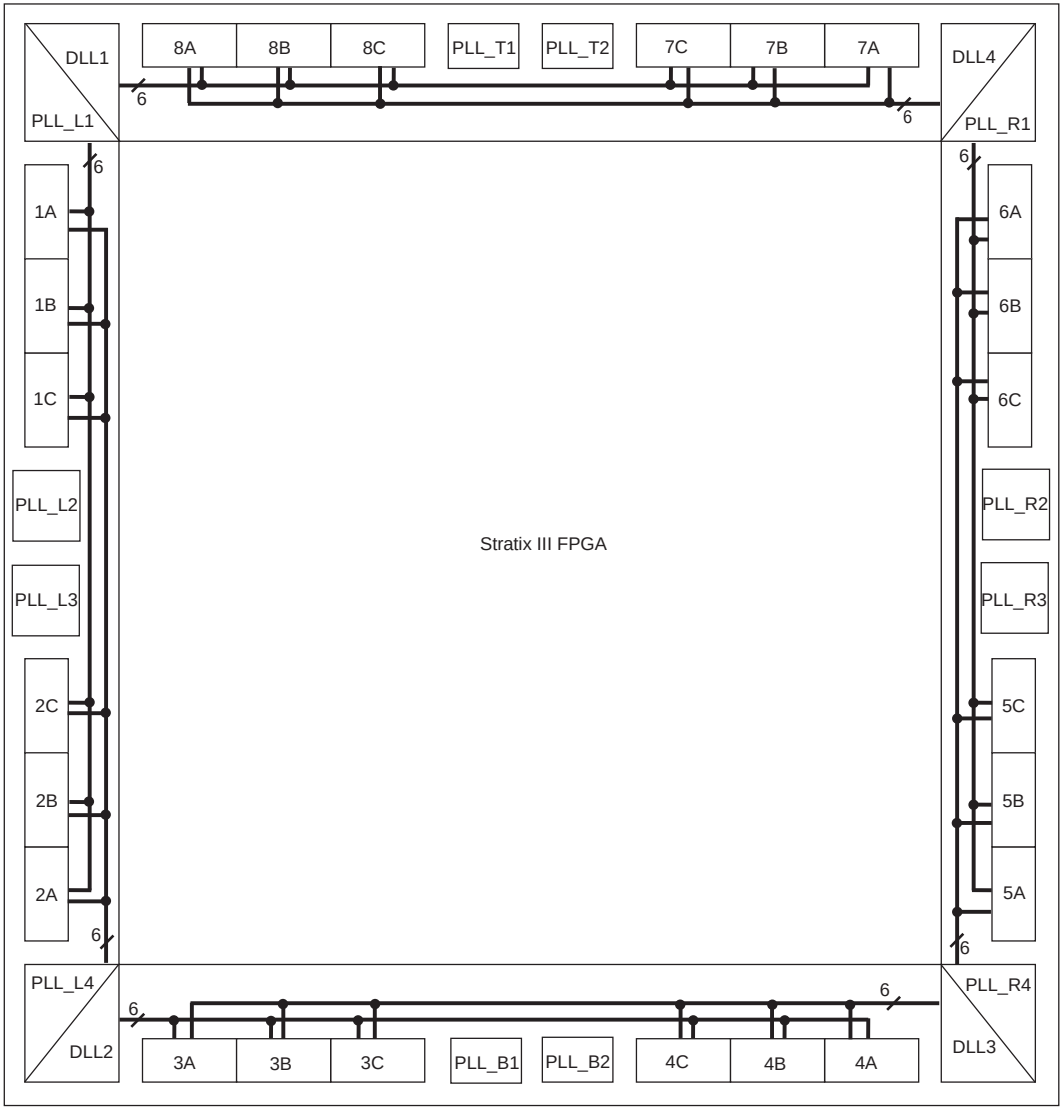
DLL

The DQS phase-shift circuitry uses a DLL to dynamically measure the clock period needed by the DQS/CQn pin. The DLL, in turn, uses a frequency reference to dynamically generate control signals for the delay chains in each of the DQS and CQn pins, allowing it to compensate for PVT variations. The DQS delay settings are Gray-coded to reduce jitter when the DLL updates the settings. The phase-shift circuitry needs a maximum of 1280 clock cycles to calculate the correct input clock period. Data should not be sent during these clock cycles since there is no guarantee it will be properly captured. As the settings from the DLL may not be stable until this lock period has elapsed, you should be aware that anything using these settings (including the leveling delay system) may be unstable during this period.

You can still use the DQS phase-shift circuitry for any memory interfaces that are less than 100 MHz. The DQS signal will be shifted by 2.5 ns. Even if the DQS signal is not shifted exactly to the middle of the DQ valid window, the I/O element should still be able to capture the data in low frequency applications where a large amount of timing margin is available.

There are four DLLs in a Stratix III device, located in each corner of the device. These four DLLs can support a maximum of four unique frequencies, with each DLL running at one frequency. Each DLL can have two outputs, which allow one Stratix III device to have eight different DLL phase shift settings. Figure 8–12 shows the DLL and I/O bank locations in Stratix III devices.

Figure 8–12. Stratix III DLL and I/O Bank Locations



The DLL can access the two adjacent sides from its location within the device. For example, DLL 1 on the top left of the device can access the top side (I/O banks 7A, 7B, 7C, 8A, 8B, 8C) and the left side of the device (I/O banks 1A, 1B, 1C, 2A, 2B, 2C). This means that each I/O bank is accessible by two DLLs, giving more flexibility to create multiple frequencies and

multiple-types interfaces. For example, you can design an interface spanning within one side of the device or within two sides adjacent to the DLL. The DLL outputs the same DQS delay settings for both sides of the device adjacent to the DLL.

Interfaces that span across two sides of the device are not recommended for high-performance memory interface applications.

Each bank can use settings from either or both DLLs the bank is adjacent to. For example, DQS1L can get its phase-shift settings from DLL1, while DQS2L gets its phase-shift settings from DLL2. Table 8–6 lists the DLL location and supported I/O banks for Stratix III devices.

Table 8–6. DLL Location and Supported I/O Banks

DLL	Location	Accessible I/O Banks
DLL1	Top left corner	1A, 1B, 1C, 2A, 2B, 2C, 7A, 7B, 7C, 8A, 8B, 8C
DLL2	Bottom left corner	1A, 1B, 1C, 2A, 2B, 2C, 3A, 3B, 3C, 4A, 4B, 4C
DLL3	Bottom right corner	3A, 3B, 3C, 4A, 4B, 4C, 5A, 5B, 5C, 6A, 6B, 6C
DLL4	Top right corner	5A, 5B, 5C, 6A, 6B, 6C, 7A, 7B, 7C, 8A, 8B, 8C

The reference clock for each DLL may come from PLL output clocks or any of the two dedicated clock input pins located in either side of the DLL. Tables 8–7 through 8–9 show the available DLL reference clock input resources for the Stratix III device family.

When you have a dedicated PLL to only generate the DLL input reference clock, set the PLL mode to *No Compensation*, or the Quartus II software will change it automatically. Because the PLL does not use any other outputs, it does not need to compensate for any clock paths.

Table 8–7. DLL Reference Clock Input for EP3SE50, EP3SL50 and EP3SL70 Devices

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL1	CLK15P, CLK15N, CLK14P, CLK14N	CLK0P, CLK0N, CLK1P, CLK1N	PLL_T1	PLL_L2
DLL2	CLK5P, CLK5N, CLK4P, CLK4N	CLK0P, CLK0N, CLK1P, CLK1N	PLL_B1	PLL_L2
DLL3	CLK5P, CLK5N, CLK4P, CLK4N	CLK10P, CLK10N, CLK11P, CLK11N	PLL_B1	PLL_R2
DLL4	CLK15P, CLK15N, CLK14P, CLK14N	CLK10P, CLK10N, CLK11P, CLK11N	PLL_T1	PLL_R2

Table 8–8. DLL Reference Clock Input for EP3SE80, EP3SE110, EP3SL110 and EP3SL150 Devices

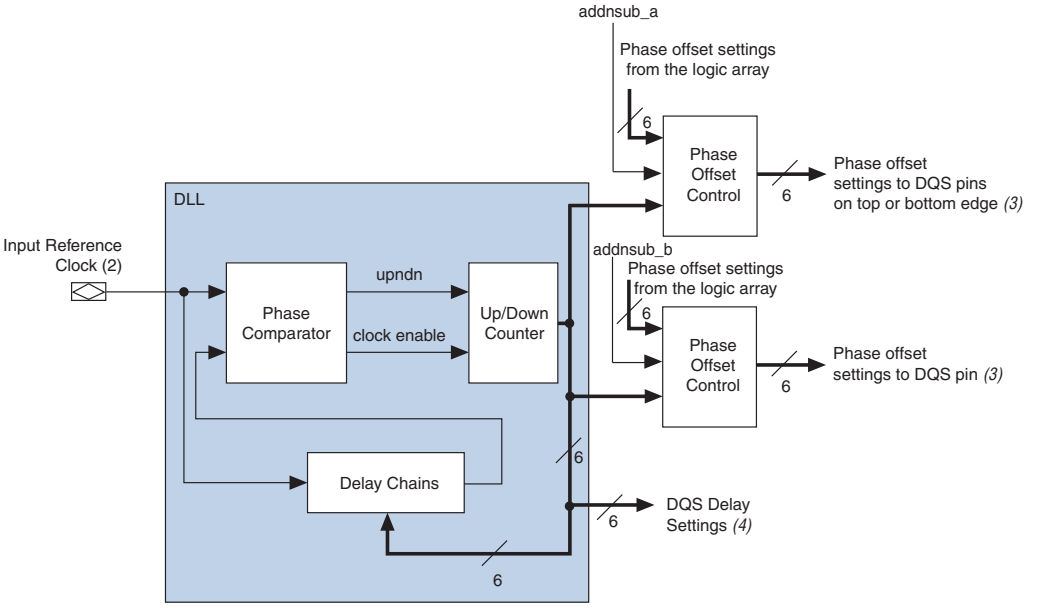
DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)
DLL1	CLK15P, CLK15N, CLK14P, CLK14N	CLK0P, CLK0N, CLK1P, CLK1N	PLL_T1	PLL_L2
DLL2	CLK5P, CLK5N, CLK4P, CLK4N	CLK2P, CLK2N, CLK3P, CLK3N	PLL_B1	PLL_L3
DLL3	CLK7P, CLK7N, CLK6P, CLK6N	CLK8P, CLK8N, CLK9P, CLK9N	PLL_B2	PLL_R3
DLL4	CLK13P, CLK13N, CLK12P, CLK12N	CLK10P, CLK10N, CLK11P, CLK11N	PLL_T2	PLL_R2

Table 8–9. DLL Reference Clock Input for EP3SL200, EP3SE260 and EP3SL340 Devices

DLL	CLKIN (Top/Bottom)	CLKIN (Left/Right)	PLL (Top/Bottom)	PLL (Left/Right)	PLL (Corner)
DLL1	CLK15P, CLK15N, CLK14P, CLK14N	CLK0P, CLK0N, CLK1P, CLK1N	PLL_T1	PLL_L2	PLL_L1
DLL2	CLK5P, CLK5N, CLK4P, CLK4N	CLK2P, CLK2N, CLK3P, CLK3N	PLL_B1	PLL_L3	PLL_L4
DLL3	CLK7P, CLK7N, CLK6P, CLK6N	CLK8P, CLK8N, CLK9P, CLK9N	PLL_B2	PLL_R3	PLL_R4
DLL4	CLK13P, CLK13N, CLK12P, CLK12N	CLK10P, CLK10N, CLK11P, CLK11N	PLL_T2	PLL_R2	PLL_R1

Figure 8–13 shows a simple block diagram of the DLL. The input reference clock goes into the DLL to a chain of up to 16 delay elements. The phase comparator compares the signal coming out of the end of the delay chain block to the input reference clock. The phase comparator then issues the `upndn` signal to the Gray-code counter. This signal increments or decrements a six-bit delay setting (DQS delay settings) that will increase or decrease the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

Figure 8–13. Simplified Diagram of the DQS Phase Shift Circuitry *Note (1)*



Notes to Figure 8–13:

(1) All features of the DQS phase-shift circuitry are accessible from the ALTMEMPHY megafunction in the Quartus II software.

(2) The input reference clock for the DQS phase-shift circuitry can come from a PLL output clock or an input clock pin. Refer to Tables 8–7 through 8–9 for exact PLL and input clock pin.

(3) Phase offset settings can only go to the DQS logic blocks.

(4) DQS delay settings can go to the logic array, the DQS logic block, and the leveling circuitry.

The DLL can be reset from either the logic array or a user I/O pin. Each time the DLL is reset, you must wait for 1280 clock cycles before you can capture the data properly.

The DLL can shift the incoming DQS signals by 0°, 22.5°, 30°, 36°, 45°, 60°, 67.5°, 72°, 90°, 108°, 120°, 135°, 144°, or 180°, depending on the DLL frequency mode. The shifted DQS signal is then used as the clock for the DQ IOE input registers.

All DQS and CQn pins, referenced to the same DLL, can have their input signal phase shifted by a different degree amount but all must be referenced at one particular frequency. For example, you can have a 90° phase shift on `DQS1T` and a 60° phase shift on `DQS2T`, referenced from a 200-MHz clock. Not all phase-shift combinations are supported, however.

The phase shifts on the DQS pins referenced by the same DLL must all be a multiple of 22.5° (up to 90°), a multiple of 30° (up to 120°), a multiple of 36° (up to 144°), or a multiple of 45° (up to 180°).

There are six different frequency modes for the Stratix III DLL, as shown in Table 8–10. Each frequency mode provides different phase shift selections. In frequency mode 0, 1, and 2, the 6-bit DQS delay settings vary with PVT to implement the phase-shift delay. In frequency modes 3, 4, and 5, only 5 bits of the DQS delay settings vary to implement the phase-shift delay; the most significant bit of the DQS delay setting is set to 0. Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter of the *Stratix III Device Handbook* for the frequency range of each mode.

Table 8–10. Stratix III DLL Frequency Modes

Frequency Mode	DQS Delay Setting Bus Width	Available Phase Shift	Number of Delay Chains
0	6 bits	22.5°, 45°, 67.5°, 90°	16
1	6 bits	30°, 60°, 90°, 120°	12
2	6 bits	36°, 72°, 108°, 144°	10
3	5 bits	30°, 60°, 90°, 120°	12
4	5 bits	36°, 72°, 108°, 144°	10
5	5 bits	45°, 90°, 135°, 180°	8

Note to Table 8–10:

(1) For the frequency range for each mode please refer to the *DC and Switching Characteristics* chapter of the Stratix III Handbook volume 2.

For the 0° shift, the DQS signal bypasses both the DLL and the DQS logic blocks. Since Stratix III DQS and DQ pins are designed such that the pin to IOE delays are matched, the skew between the DQ and DQS pin at the DQ IOE registers is negligible when the 0° shift is implemented. You can feed the DQS delay settings to the DQS logic block and the logic array.

The shifted DQS signal goes to the DQS bus to clock the IOE input registers of the DQ pins. The signal can also go into the logic array for resynchronization if you are not using the IOE resynchronization registers. The shifted CQn signal can only go to the active-low input register in the DQ IOE and is only used for QDRII+ and QDRII SRAM interfaces.

Phase Offset Control

Each DLL has two phase-offset modules and can provide two separate DQS delay settings with independent offset, one for the top / bottom I / O bank and one for the left / right I / O bank, so you can fine-tune the DQS phase shift settings between two different sides of the device. Even though you have independent phase offset control, the frequency of the interface using the same DLL has to be the same. You should use the phase offset control module for making small shifts to the input signal and use the DQS phase-shift circuitry for larger signal shifts. For example, if the DLL only offers a multiple of 30° phase shift, but your interface needs a 67.5° phase shift on the DQS signal, you can use two delay chains in the DQS logic blocks to give you 60° phase shift and use the phase offset control feature to implement the extra 7.5° phase shift.

You can either use a static phase offset or a dynamic phase offset to implement the additional phase shift. The available additional phase shift is implemented in 2's-complement in Gray code between settings –64 to +63 for frequency mode 0, 1, and 2, and between settings –32 to +31 for frequency modes 3, 4, and 5. The DQS phase shift is the sum of the DLL delay settings and the user selected phase offset settings which maxes out at setting 64 for mode frequency mode 0, 1, and 2, and maxes out at setting 32 for frequency modes 3, 4, and 5, so the actual physical offset setting range will be 64 or 32 subtracted by the DQS delay settings from the DLL.

When using this feature, you need to monitor the DQS delay settings to know how many offest you can add and subtract in the system.

For example, if the DLL determines that DQS delay settings of 28 is needed to achieve a 30º phase shift in DLL frequency mode 1, you can subtract up to 28 phase offset settings and you can add up to 35 phase offset settings to achieve the optimal delay that you need. However, if the same DQS delay settings of 28 is needed to achieve 30º phase shift in DLL frequency mode 3, you can still subtract up to 28 phase offset settings, but you can only add up to 3 phase offset settings before the DQS delay settings reach their maximum settings, because DLL frequency mode 3 only uses 5-bit DLL delay settings.

Each phase offset setting translates to a certain delay as specified in the *DC and Switching Characteristics of Stratix III Devices* chapter of the *Stratix III Device Handbook*.

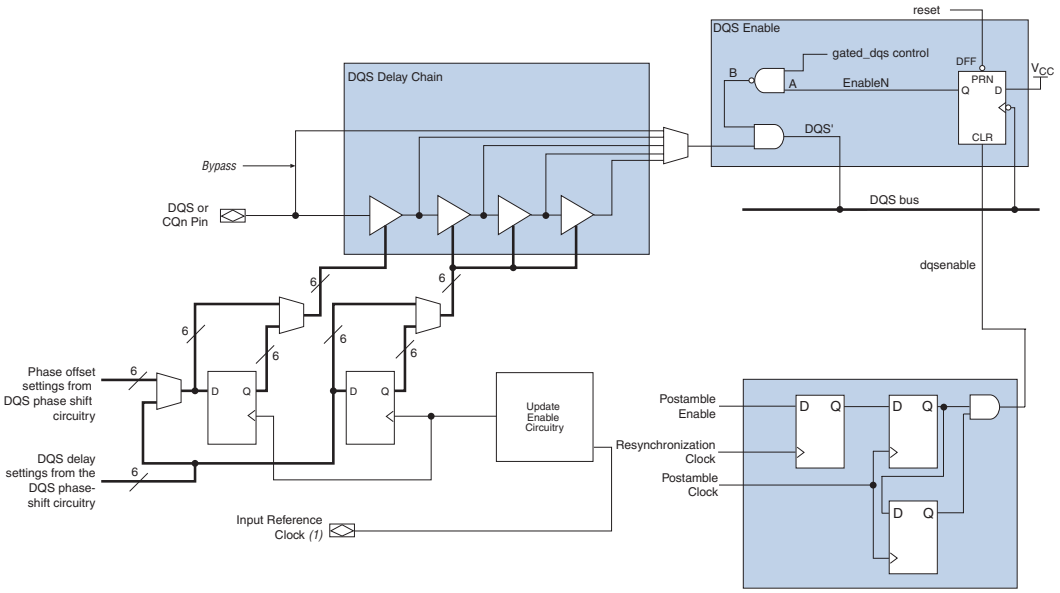
Refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook* for information on the value for each step.

When using the static phase offset, you can specify the phase offset amount in the ALTMEMPHY megafunction as a positive number for addition or a negative number for subtraction. You can also have a dynamic phase offset that is always added to, subtracted from, or both added to and subtracted from the DLL phase shift. When you always add or subtract, you can dynamically input the phase offset amount into the `dll_offset[5..0]` port. When you want to both add and subtract dynamically, you control the `addnsub` signal in addition to the `dll_offset[5..0]` signals.

DQS Logic Block

Each DQS and CQn pin is connected to a separate DQS logic block, which consists of the DQS delay chains, the update enable circuitry, and the DQS postamble circuitry (see Figure 8–14).

Figure 8–14. Stratix III DQS Logic Block



Note to Figure 8–14:

(1) The input reference clock for the DQS phase-shift circuitry can come from a PLL output clock or an input clock pin. Refer to Tables 8–7 through 8–9 for the exact PLL and input clock pin.

DQS Delay Chain

The DQS delay chains consist of a set of variable delay elements to allow the input DQS and CQn signals to be shifted by the amount specified by the DQS phase-shift circuitry or the logic array. There are four delay elements in the DQS delay chain; the first delay chain closest to the DQS pin can either be shifted by the DQS delay settings or by the sum of the DQS delay setting and the phase-offset setting. The number of delay chains required is transparent to the users because the ALTMEMPHY megafunction automatically sets it when you choose the operating frequency. The DQS delay settings can come from the DQS phase-shift circuitry on either end of the I/O banks or from the logic array.

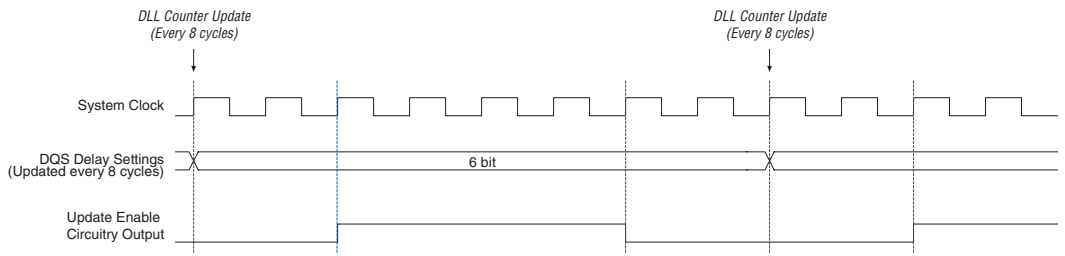
The delay elements in the DQS logic block have the same characteristics as the delay elements in the DLL. When the DLL is not used to control the DQS delay chains, you can input your own 6-bit or 5-bit settings using the dqs_delayctrlin[5..0] signals available in the ALTMEMPHY megafunction. These settings control 1, 2, 3, or all 4 delay elements in the DQS delay chains. The ALTMEMPHY megafunction can also dynamically choose the number of DQS delay chains needed for the system. The amount of delay is equal to the sum of the delay element's intrinsic delay and the product of the number of delay steps and the value of the delay steps.

You can also bypass the DQS delay chain to achieve 0° phase shift.

Update Enable Circuitry

Both the DQS delay settings and the phase-offset settings pass through a register before going into the DQS delay chains. The registers are controlled by the update enable circuitry to allow enough time for any changes in the DQS delay setting bits to arrive at all the delay elements. This allows them to be adjusted at the same time. The update enable circuitry enables the registers to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry or core logic to all the DQS logic blocks before the next change. It uses the input reference clock or a user clock from the core to generate the update enable output. The ALTMEMPHY megafunction uses this circuit by default. See Figure 8–15 for an example waveform of the update enable circuitry output.

Figure 8–15. DQS Update Enable Waveform

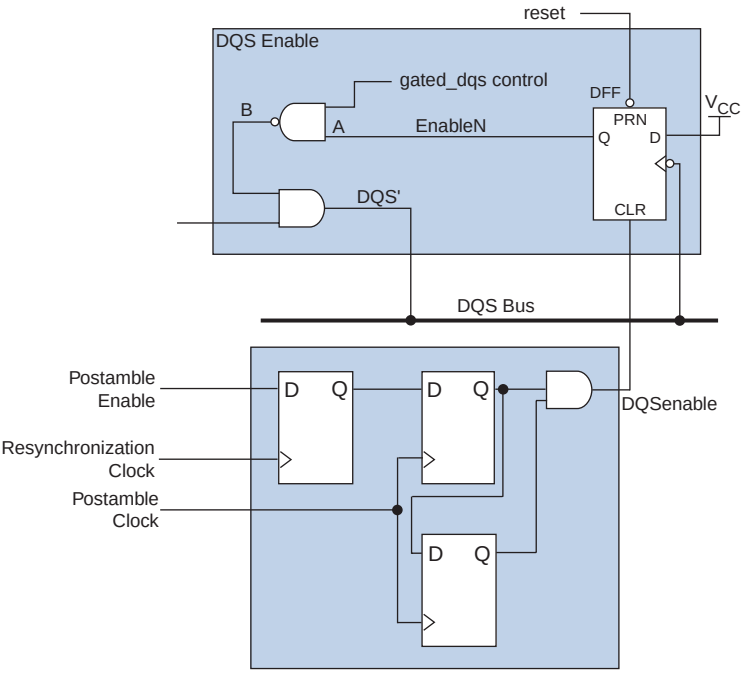


DQS Postamble Circuitry

For external memory interfaces that use a bidirectional read strobe like DDR3, DDR2, and DDR SDRAM, the DQS signal is low before going to or coming from a high-impedance state. The state where DQS is low, just after a high-impedance state, is called the preamble and the state where DQS is low, just before it returns to a high-impedance state, is called the

postamble. There are preamble and postamble specifications for both read and write operations in DDR3, DDR2, and DDR SDRAM. The DQS postamble circuitry, featured in Figure 8–16, ensures that data is not lost when there is noise on the DQS line at the end of a read postamble time. Stratix III devices have a dedicated postamble register that can be controlled to ground the shifted DQS signal used to clock the DQ input registers at the end of a read operation. This ensures that any glitches on the DQS input signals at the end of the read postamble time do not affect the DQ IOE registers.

Figure 8–16. Stratix III DQS Postamble Circuitry *Note (1)*



Note to Figure 8–16:

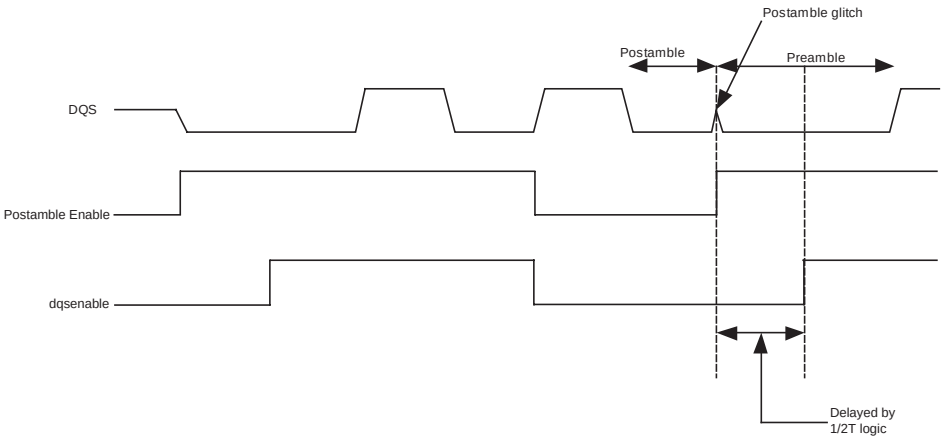
(1) The postamble clock can come from any of the delayed resynchronization clock taps although it is not necessarily of the same phase as the resynchronization clock.

In addition to the dedicated postamble register, Stratix III devices also have an HDR block inside the postamble enable circuitry. These registers are used if the controller is running at half the frequency of the I/Os.

The use of the HDR block as the first stage capture register in the postamble enable circuitry block in Figure 8–16 is optional. The HDR block is clocked by the half-rate resynchronization clock, which is the

output of the DIV2 circuit. There is an AND gate after the postamble register outputs that is used to avoid postamble glitches from a previous read burst on a non-consecutive read burst. This scheme allows a half-a-clock cycle latency for `dqsenable` assertion and zero latency for `dqsenable` deassertion as shown in Figure 8–17.

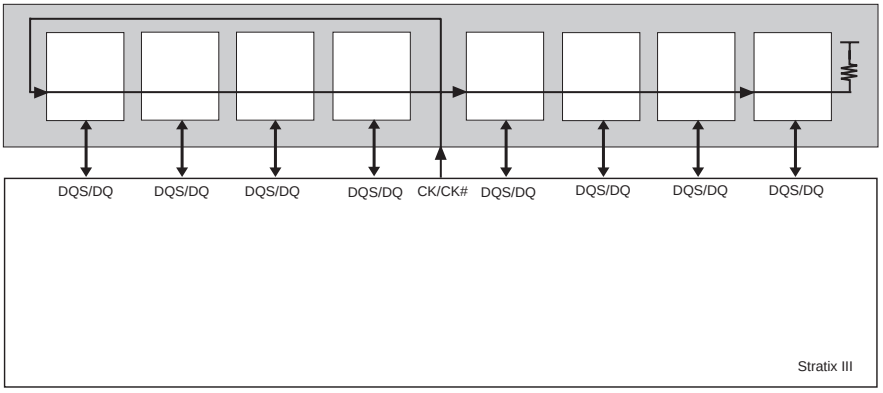
Figure 8–17. Avoiding Glitch on a Non-Consecutive Read Burst Waveform



Leveling Circuitry

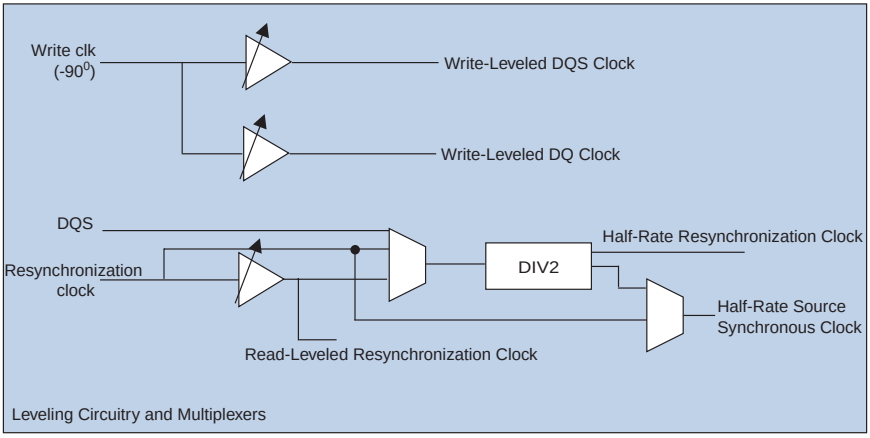
DDR3 SDRAM unbuffered modules use a fly-by clock distribution topology for better signal integrity. This means that the CK / CK# signals arrive at each DDR3 SDRAM device in the module at different times. The difference in arrival time between the first DDR3 SDRAM device and the last device on the module can be as long as 1.6 ns. Figure 8–18 shows the clock topology in DDR3 SDRAM unbuffered modules.

Figure 8–18. DDR3 SDRAM Unbuffered Module Clock Topology



Because the data and read strobe signals are still point-to-point, special consideration needs to be taken to ensure that the timing relationship between CK / CK# and DQS signals (t_{DQSS}) during a write is met at every device on the modules. Furthermore, read data coming back into the FPGA from the memory will also be staggered in a similar way. Stratix III FPGAs have leveling circuitry to take care of these two needs. There is one group of leveling circuitry per I / O bank, located in the middle of the I / O bank. These delay chains are PVT-compensated by the same DQS delay settings as the DLL and DQS delay chains. For frequencies equal to and above 400 MHz, the DLL uses eight delay chains such that each delay chain generates a 45º delay. The generated clock phases are distributed to every DQS logic block that is available in the I / O bank. The delay chain taps, then feeds a multiplexer controlled by the ALTMEMPHY megafunction to select which clock phases are to be used for that ×4 or ×8 DQS group. Each group can use a different tap output from the read-leveling / write-leveling delay chains to compensate for the different CK / CK# delay going into each device on the module. Figure 8–19 illustrates the Stratix III read and write leveling circuitry.

Figure 8–19. Stratix III Read and Write Leveling Delay Chains and Multiplexers



The –90° write clock of the ALTMEMPHY megafunction feeds the write-leveling circuitry to produce the clock to generate the DQS and DQ signals. During initialization, the ALTMEMPHY megafunction picks the correct write-leveled clock for the DQS and DQ clocks for each DQS / DQ group after sweeping all the available clocks in the write calibration process. The DQ clock output is –90° phase-shifted compared to the DQS clock output.

Similarly, the resynchronization clock feeds the read-leveling circuitry to produce the optimal resynchronization and postamble clock for each DQS / DQ group in the calibration process. The resynchronization and the postamble clocks can use different clock outputs from the leveling circuitry. The output from the read-leveling circuitry can also generate the half-rate resynchronization clock that goes to the FPGA fabric.

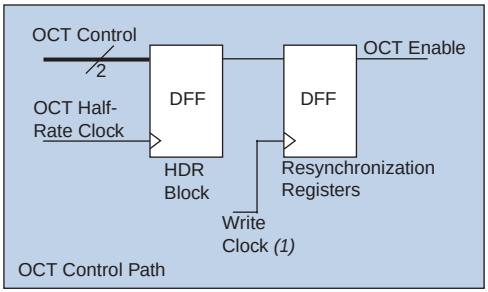
The ALTMEMPHY megafunction calibrates the alignment for read and write leveling dynamically during the initialization process.

Dynamic On-Chip Termination Control

Figure 8–20 shows the dynamic OCT control block. The block includes all the registers needed to dynamically turn on OCT during a read and turn OCT off during a write.

For more information refer to section "OCT" on page 8–43, or to the *Stratix III Device I/O Features* chapter in volume 1 of the Stratix III Device Handbook.

Figure 8–20. Stratix III Dynamic OCT Control Block



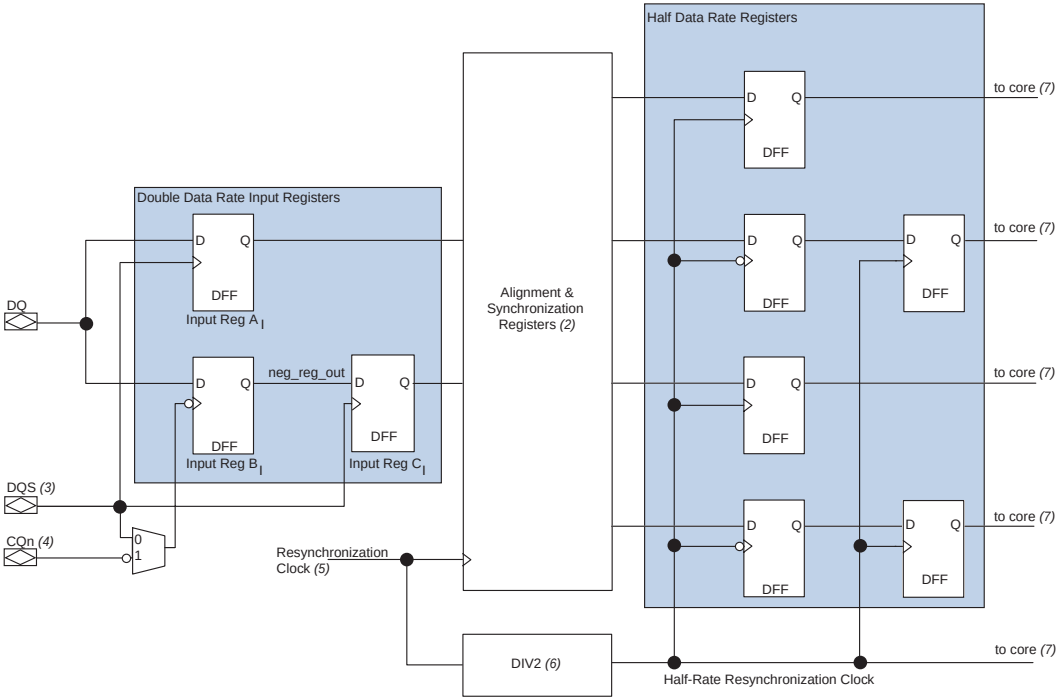
Note to Figure 8–20:
(1) Write clock comes from either the PLL or the write leveling delay chain.

I/O Element (IOE) Registers

The IOE registers have been expanded to allow source-synchronous systems to have faster register-to-register transfers and resynchronization. Both top / bottom and left / right IOEs have the same capability with left / right IOEs having extra features to support LVDS data transfer.

Figure 8–21 shows the registers available in the Stratix III input path. The input path consists of the DDR input registers, resynchronization registers, and HDR block. Each block of the input path can be bypassed.

Figure 8–21. Stratix III Input Path Registers *Note (1)*



Notes to Figure 8–21:

(1) Each register block in this path can be bypassed.
(2) There are up to three levels of resynchronization registers.
(3) The input clock can be from the DQS logic block (whether the postamble circuitry is bypassed or not) or from a global clock line.
(4) This input clock comes from the CQn logic block.
(5) This resynchronization clock can come either from the PLL or from the read-leveling delay chain.
(6) The divide-by-2 (DIV2) circuitry resides adjacent to the DQS logic block.
(7) The half-rate data and clock signals feed into a FIFO in the FPGA core.

There are three registers in the DDR input registers block. Two registers capture data on the positive and negative edges of the clock, while the third register aligns the captured data. You can choose to have the same clock for the positive edge and negative edge registers, or two different clocks (DQS for positive edge register, and CQn for negative edge register). The third register that aligns the captured data uses the same clock as the positive edge registers.

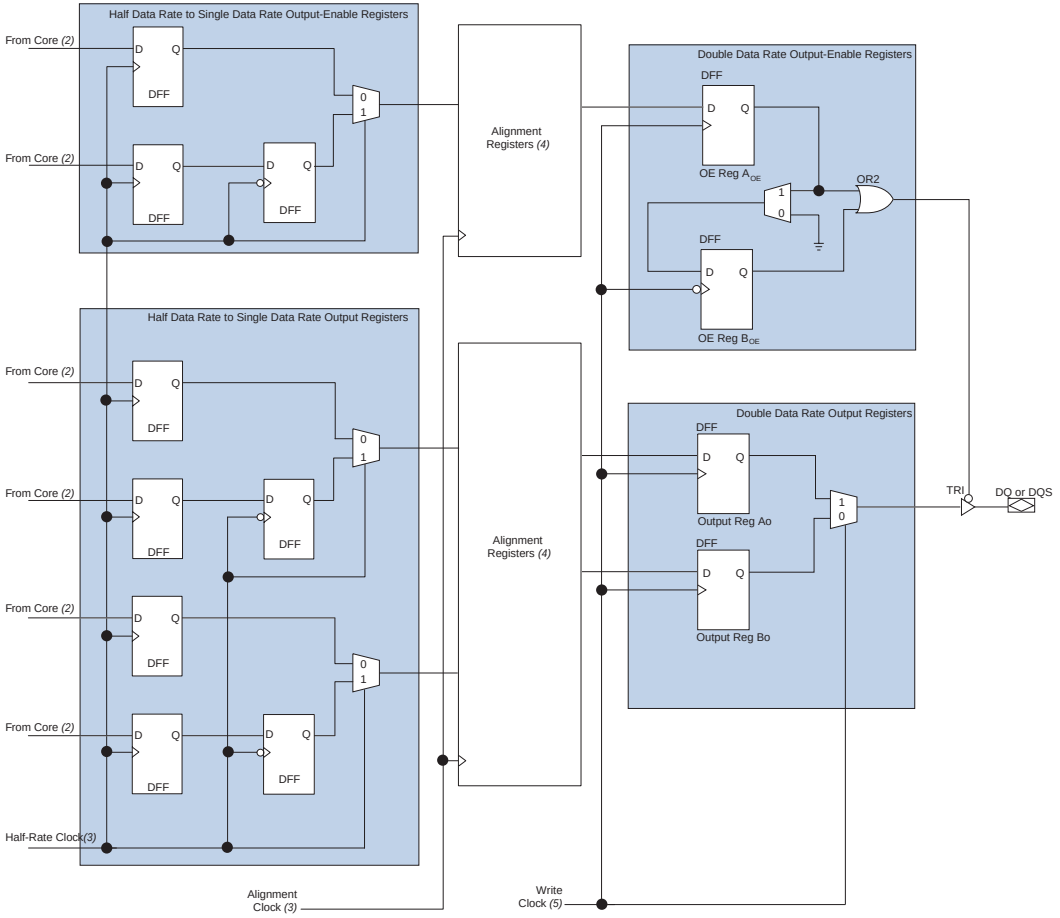
The resynchronization registers consist of up to three levels of registers to resynchronize the data to the system clock domain. These registers are clocked by the resynchronization clock that is either generated by the PLL

or the read-leveling delay chain. The outputs of the resynchronization registers can go straight to the core or to the HDR blocks, which are clocked by the divided-down resynchronization clock.

For more information about the read-leveling delay chain, refer to the "Leveling Circuitry" on page 8–36.

Figure 8–22 shows the registers available in the Stratix III output and output-enable paths. The path is divided into the HDR block, resynchronization registers, and output/output-enable registers. The device can bypass each block of the output and output-enable path.

Figure 8–22. Stratix III Output and Output-Enable Path Registers *Note (1)*



Notes to Figure 8–22:

(1) Each register block of the output and output enable paths can be bypassed.
(2) Data coming from the FPGA core are at half the frequency of the memory interface.
(3) Half-rate and alignment clocks come from the PLL.
(4) There are up to two levels of registers for data alignment. These registers are only used in DDR3 SDRAM interfaces.
(5) The write clock can come from either the PLL or from the write leveling delay chain. The DQ write clock and DQS write clock have a 90° offset between them.

The output path is designed to route combinatorial or registered SDR outputs and full-rate or half-rate DDR outputs from the FPGA core. Half-rate data is converted to full-rate using the HDR block, clocked by the half-rate clock from the PLL. The resynchronization registers are also clocked by the same 0° system clock, except in the DDR3 SDRAM interface. In DDR3 SDRAM interfaces, the leveling registers are clocked by the write-leveling clock.

For more information on the write leveling delay chain, refer to the "Leveling Circuitry" on page 8–36.

The output-enable path has structure similar to the output path. You can have a combinatorial or registered output in SDR applications and you can use half-rate or full-rate operation in DDR applications. You also have the resynchronization registers like the output path registers structure, ensuring that the output enable path goes through the same delay and latency as the output path.

IOE Features

This section briefly describes how OCT, programmable delay chains, programmable output delay, slew rate adjustment, and programmable drive strength can be useful in memory interfaces.

For more information about any of the features listed below, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

OCT

Stratix III devices feature dynamic calibrated OCT, in which the series termination (OCT R_S) is turned on when driving signals and turned off when receiving signals, while the parallel termination (OCT R_T) is turned off when driving signals and turned on when receiving signals. This feature complements the DDR3 / DDR2 SDRAM on-die termination (ODT), whereby the memory termination is turned off when the memory is sending data and turned on when receiving data. You can use OCT for other memory interfaces to improve signal integrity.

You cannot use the programmable drive strength and programmable slew rate features when using OCT R_S.

To use the dynamic calibrated OCT, you must use the R_{UP} and R_{DN} pins to calibrate the OCT calibration block. One OCT calibration block can be used to calibrate one type of termination with the same V_{CCIO} on the

entire device. There are up to ten OCT calibration blocks to allow for different types of terminations throughout the device. For more details, refer to "Dynamic On-Chip Termination Control" on page 8–39.

You have the option to use the OCT R_S feature with or without calibration. However, the OCT R_T feature is only available with calibration.

The R_{UP} and R_{DN} pins can also be used as DQ pins, so you cannot use the DQS / DQ groups where the R_{UP} and R_{DN} pins are located if you are planning to use dynamic calibrated OCT. The R_{UP} and R_{DN} pins are located in the first and the last ×4 DQS / DQ group on each side of the device.

You should use the OCT R_T/R_S setting for uni-directional read / write data and a dynamic OCT setting for bi-directional data signals.

Programmable IOE Delay Chains

The programmable delay chains in the Stratix III I / O registers can be used as deskewing circuitry. Each pin can have a different input delay from the pin to input register or a delay from the output register to the output pin to ensure that the bus has the same delay going into or out of the FPGA. This feature helps read and write time margins as it minimizes the uncertainties between signals in the bus.

Programmable Output Buffer Delay

In addition to allowing for output buffer duty cycle adjustment, the programmable output buffer delay chain allows you to adjust the delays between data bits in your output bus to introduce or compensate channel-to-channel skew. Incorporating skew to the output bus can help minimize simultaneous switching events by enabling smaller parts of the bus to switch simultaneously, instead of the whole bus. This feature is also particularly useful in DDR3 SDRAM interfaces where the memory system clock delay can be much larger than the data and data clock / strobe delay. You can use this delay chain to add delay to the data and data clock / strobe to better match the memory system clock delay.

Programmable Slew Rate Control

Stratix III devices provide four levels of static output slew rate control: 0, 1, 2, and 3, where 0 is the slowest slew rate setting and 3 is the fastest slew rate setting. The default setting for the HSTL and SSTL I / O standards is 3. A fast slew rate setting allows you to achieve higher I / O performance, while a slow slew-rate setting reduces system noise and signal overshoot. This feature is disabled if you are using the OCT Rs features.

Programmable Drive Strength

You can choose the optimal drive strength needed for your interface after performing a board simulation. Higher drive strength helps provide a larger voltage swing, which in turn provides bigger eye diagrams with greater timing margin. However, higher drive strengths typically require more power, faster slew rates and add to simultaneous switching noise. You can use the programmable slew rate control along with this feature to minimize simultaneous switching noise with higher drive strengths.

This feature is also disabled if you are using the OCT R_S feature, which is the default drive strength in Stratix III devices. You should use the OCT R_T/R_S setting for unidirectional read / write data and dynamic OCT setting for bidirectional data signals. You need to simulate the system to determine the drive strength needed for command, address, and clock signals.

PLL

PLLs are used to generate the memory interface controller clocks, like the 0° system clock, the –90° or 270° phase-shifted write clock, the half-rate PHY clock, and the resynchronization clock. The PLL reconfiguration feature can be used to calibrate the resynchronization phase shift to balance the setup and hold margin.

The VCO and counter setting combinations may be limited for high performance memory interfaces.

For more information about the Stratix III PLL, refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Conclusion

Stratix III devices have many features available to support existing and emerging external memory interfaces. The ALTMEMPHY megafunction, built to support the Stratix III memory interface features, allows customers to easily implement their data path for use with either their own controller or Altera's IP controller.

In Stratix III devices, most of the critical data transfers are taken care of for you in the IOE, alleviating the burden of having to close timing in the FPGA fabric. Furthermore, since most of the registers are in the IOE, data delays between registers are short, allowing the circuitry to work at a higher frequency. Dynamically calibrated OCT, slew rate adjustment, and programmable drive strength improve signal integrity, especially at higher frequencies of operation.

In addition, programmable delay chain and de-skew circuits allow Stratix III devices to achieve better margin for high performance memory interfaces. Dynamic calibration of resynchronization and postamble clocks guarantee high performance over PVT variations. Leveling circuitry enables Stratix III to support DDR3 modules, thus offering customers the choice of highest performance memory technologies. Stratix III devices also offer memory interface support in any of 24 modular I/O banks with up to four different frequencies of operations.

Document Revision History

Table 8–11 shows the revision history for this document.

Table 8–11. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Updated Figure 8–5, Figure 8–8, Figure 8–14, Figure 8–18, Figure 8–19, Figure 8–20, and Figure 8–21. Added new figure, Figure 8–17. Added memory support information for -4L in Table 8–1, Table 8–7, Table 8–8, and Table 8–9. Added new material to "Phase Offset Control" on page 8–31.	Minor updates to content.
November 2006 v1.0	Initial Release	—

9. High-Speed Differential I/O Interfaces and DPA in Stratix III Devices

SIII51009-1.1

Introduction

The Stratix® III device family offers up to 1.25-Gbps differential I/O capabilities to support source-synchronous communication protocols such as Utopia, Rapid I/O™, XSBI, SGMII, SFI, and SPI.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (located on left and right sides of the device)

For high-speed differential interfaces, Stratix III devices support the following differential I/O standards:

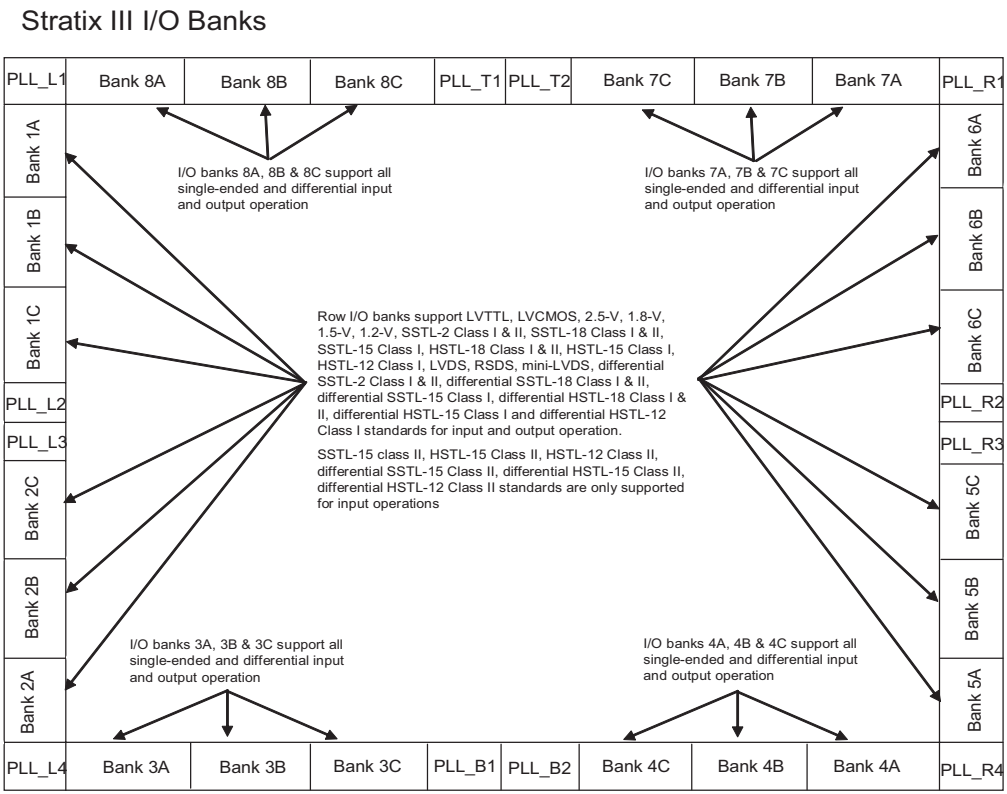
- Low Voltage Differential Signaling (LVDS)
- Mini-LVDS
- Reduced Swing Differential Signaling (RSDS)
- HSTL
- SSTL

HSTL and SSTL I/O standards can be used only for PLL clock inputs and outputs in differential mode.

I/O Banks

The Stratix III I/Os are divided into 16 to 24 I/O banks. The dedicated circuitry that supports high-speed differential I/Os is located in banks in the right side and left side of the device. Figure 9–1 shows the different banks and the I/O standards supported by the banks.

Figure 9–1. I/O Banks in Stratix III *Notes (1), (2), (3), (4), (5)*



Notes to Figure 9–1:

(1) Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted to support differential I/O operations.

(2) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip differential OCT support.

(3) Column I/O supports LVDS outputs using SE buffers and external resistor networks.

(4) Row I/O supports PCI/PCI-X without on-chip clamping diodes.

(5) The PLL blocks are shown for location purposes only and are not considered additional banks. The PLL input and output uses the I/Os in adjacent banks.

LVDS Channels

The Stratix III device supports LVDS at both side I/O banks and column I/O banks. There are true LVDS input and output buffers at side I/O banks. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Table 9–1 shows the LVDS channels supported in Stratix III Device Side I/O Banks.

Table 9–1. LVDS Channels Supported in Stratix III Device Side I/O Banks Note (1)

Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152 - Pin FineLine BGA	1517 - Pin FineLine BGA	1780 - Pin FineLine BGA
EP3SL50	48Rx + 48Tx	56Rx + 56Tx	—	—	—
EP3SL70	48Rx + 48Tx	56Rx + 56Tx	—	—	—
EP3SL110	—	56Rx + 56Tx	88Rx + 88Tx	—	—
EP3SL150	—	56Rx + 56Tx	88Rx + 88Tx	—	—
EP3SL200	—	—	88Rx + 88Tx	88Rx + 88Tx	—
EP3SL340	—	—	—	112Rx + 112Tx	132Rx + 132Tx
EP3SE50	48Rx + 48Tx	56Rx + 56Tx	—	—	—
EP3SE80	—	56Rx + 56Tx	88Rx + 88Tx	—	—
EP3SE110	—	56Rx + 56Tx	88Rx + 88Tx	—	—
EP3SE260	—	—	88Rx + 88Tx	112Rx + 112Tx	—

Note to Table 9–1:
(1) The numbers shown for each device / package combination include an equal number of Rx and Tx channels.

Table 9–2 shows the LVDS channels (Emulated) supported in Stratix III Device Column I/O Banks.

Table 9–2. LVDS Channels (Emulated) Supported in Stratix III Device Column I/O Banks Note (1)

Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152 - Pin FineLine BGA	1517 - Pin FineLine BGA	1780 - Pin FineLine BGA
EP3SL50	24Rx/Tx + 24Tx	64Rx/Tx + 64Tx	—	—	—
EP3SL70	24Rx/Tx + 24Tx	64Rx/Tx + 64Tx	—	—	—
EP3SL110	—	64Rx/Tx + 64Tx	96Rx/Tx + 96Tx	—	—
EP3SL150	—	64Rx/Tx + 64Tx	96Rx/Tx + 96Tx	—	—
EP3SL200	—	—	96Rx/Tx + 96Tx	128Rx/Tx + 128Tx	—
EP3SL340	—	—	—	128Rx/Tx + 128Tx	144Rx/Tx + 144Tx
EP3SE50	24Rx/Tx + 24Tx	64Rx/Tx + 64Tx	—	—	—
EP3SE80	—	64Rx/Tx + 64Tx	96Rx/Tx + 96Tx	—	—

Table 9–2. LVDS Channels (Emulated) Supported in Stratix III Device Column I/O Banks Note (1)

Device	484 - Pin FineLine BGA	780 - Pin FineLine BGA	1152 - Pin FineLine BGA	1517 - Pin FineLine BGA	1780 - Pin FineLine BGA
EP3SE110	—	64Rx/Tx + 64Tx	96Rx/Tx + 96Tx	—	—
EP3SE260	—	—	96Rx/Tx + 96Tx	128Rx/Tx + 128Tx	—

Note to Table 9–2:

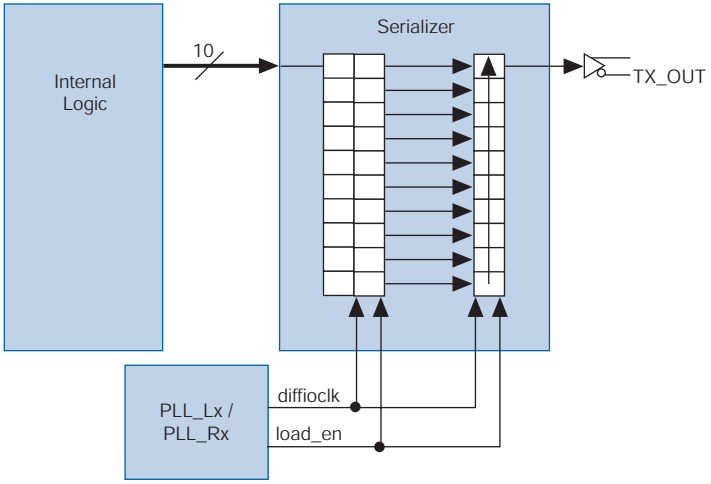
(1) LVDS input buffers at column I/O banks are true LVDS input buffers. All user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.

Differential Transmitter

The Stratix III transmitter has dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared analog PLL (left/right PLL). The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10-bits wide parallel data from the FPGA core, clocks it into the load registers, and serializes it using shift registers clocked by the left/right PLL before sending the data to the differential buffer. The most significant bit (MSB) of the parallel data is transmitted first.

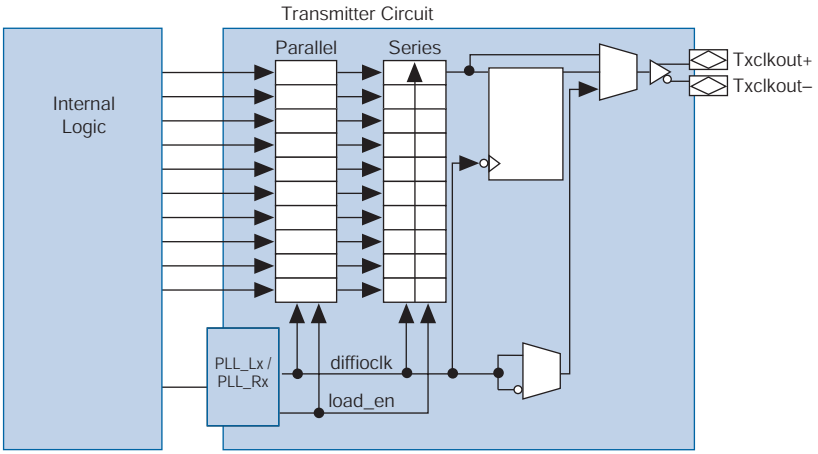
The load and shift registers are clocked by the load enable (`load_en`) signal and the `diffioclk` (clock running at serial data rate) signal generated from PLL_Lx (left PLL) or PLL_Rx (right PLL). The serialization factor can be statically set to ×4, ×6, ×7, ×8, or ×10 using the Quartus® II software. The load enable signal is derived from the serialization factor setting. Figure 9–2 is a block diagram of the Stratix III transmitter.

Figure 9–2. Stratix III Transmitter Block Diagram



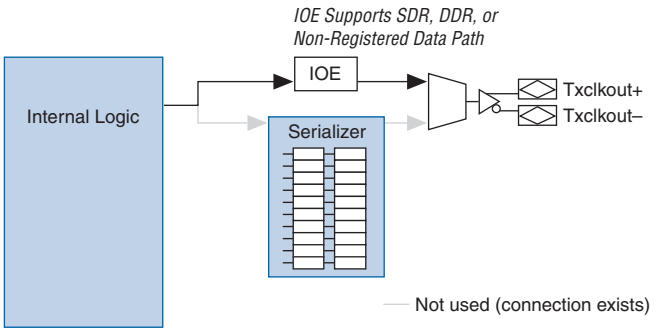
Any Stratix III transmitter data channel can be configured to generate a source synchronous transmitter clock output. This flexibility allows placing the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data rate to clock rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 717 MHz. The output clock can also be divided by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The left and right PLLs (PLL_Lx / PLL_Rx) provide additional support for other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard® software. Figure 9–3 shows the Stratix III transmitter in clock output mode.

Figure 9–3. Stratix III Transmitter in Clock Output Mode



The Stratix III serializer can be bypassed to support DDR (×2) and SDR (×1) operations to achieve a serialization factor of 2 and 1, respectively. The I / O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left / right PLL (PLL_Lx / PLL_Rx), or from the top / bottom (PLL_Tx / PLL_Bx) PLL. Figure 9–4 shows the serializer bypass path.

Figure 9–4. Stratix III Serializer Bypass



Differential Receiver

The Stratix III device has dedicated circuitry to receive high-speed differential signals. Figure 9–5 shows the block of the Stratix III receiver. The receiver has a differential buffer, a shared PLL_Lx / PLL_Rx, Dynamic

Phase Alignment (DPA) block, synchronization FIFO buffer, Data realignment block, and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in the Quartus II software assignment editor. The PLL receives the external source clock input that is transmitted with the data and generates different phases of the same clock. The DPA block chooses one of the clocks from the left / right PLL and aligns the incoming data on each channel.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the data realignment circuit inserts a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the Stratix III receiver is clocked by either a `dffioclk` signal or the DPA recovered clock. The deserialization factor can be statically set to 4, 6, 7, 8, or 10 by using the Quartus II software. The left / right PLLs (PLL_Lx / PLL_Rx) generate the load enable signal, which is derived from the deserialization factor setting.

The Stratix III deserializer can be bypassed in the Quartus II MegaWizard to support DDR(×2) or SDR(×1) operations. The DPA and the data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the left / right PLLs or from the top / bottom PLLs.

Figure 9–5. Receiver Block Diagram

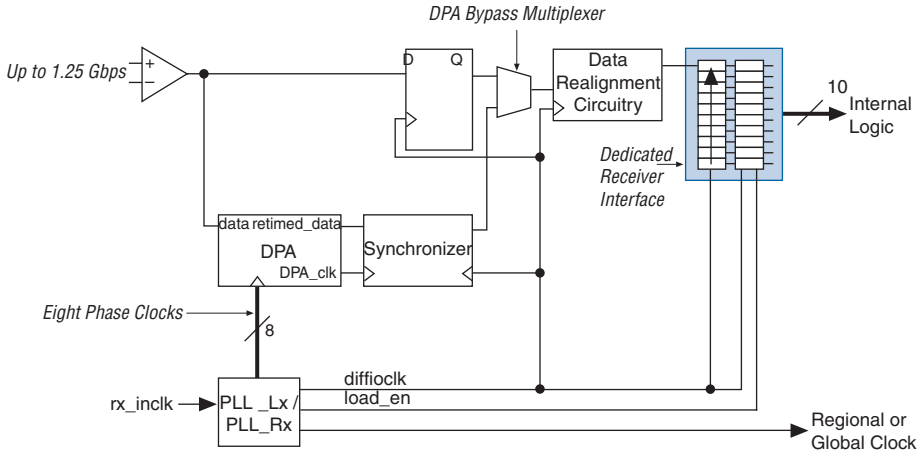
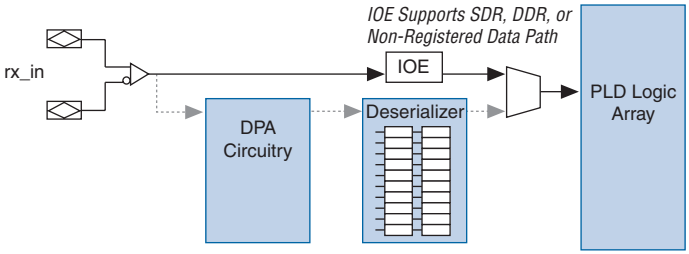


Figure 9–6 shows the deseralizer bypass data path.

Figure 9–6. Stratix III Deserializer Bypass



Receiver Data Realignment Circuit (Bit Slip)

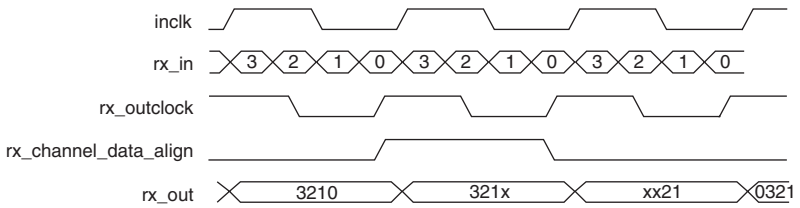
Skew in the transmitted data along with skew added by the link causes channel-to-channel skew on the received serial data streams. If the DPA is enabled, the received data is captured with different clock phases on each channel. This may cause the received data to be misaligned from channel to channel. To compensate for this channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

An optional RX_CHANNEL_DATA_ALIGN port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on the RX_CHANNEL_DATA_ALIGN. The following are requirements for the RX_CHANNEL_DATA_ALIGN signal:

- The minimum pulse width is one period of the parallel clock in the logic array
- The minimum low time between pulses is one period of parallel clock
- There is no maximum high or low time
- Valid data is available two parallel clock cycles after the rising edge of RX_CHANNEL_DATA_ALIGN

Figure 9–7 shows receiver output (RX_OUT) after one bit slip pulse with the deserialization factor set to 4.

Figure 9–7. Data Realignment Timing

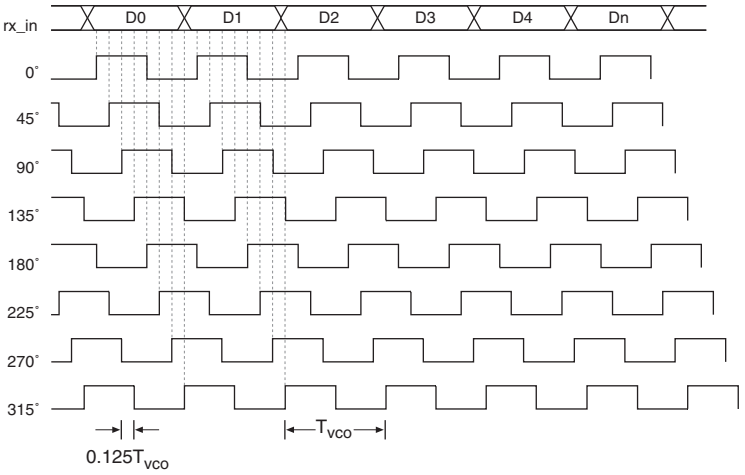


The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times, independent of the deserialization factor. An optional status port, RX_CDA_MAX, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

Dynamic Phase Aligner (DPA)

The DPA block takes in high-speed serial data from the differential input buffer and selects one of the eight phase clocks from the left / right PLL to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the received data and the selected phase is 1/8UI, which is the maximum quantization error of the DPA. The eight phases of the clock are equally divided, giving a 45-degree resolution. Figure 9–8 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 9–8. DPA Clock Phase to Serial Data Timing Relationship



The DPA block continuously monitors the phase of the incoming serial data and selects a new clock phase if needed. Users can prevent the DPA from selecting a new clock phase by asserting the optional RX_DPLL_HOLD port, which is available for each channel.

The DPA block requires a training pattern and a training sequence of at least 256 repetitions. The training pattern is not fixed, so you can use any training pattern with at least one transition on each channel. An optional output port, RX_DPA_LOCKED, is available to the internal logic to indicate when the DPA block has settled on the closest phase to the incoming data phase. The DPA block deasserts RX_DPA_LOCKED depending on the option selected in the Quartus II MegaWizard Plug-In Manager, when either a new phase is selected, or when the DPA has moved two phases in the same direction. The RX_DPA_LOCKED signal is synchronized to the DPA clock domain and should be considered as the initial indicator for the lock condition. Use data checkers to validate the data integrity.

An independent reset port, RX_RESET, is available to reset the DPA circuitry. The DPA circuitry must be retrained after reset.

Synchronizer

The synchronizer is a 1-bit × 6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the diffioclk that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's INCLK.

An optional port, RX_FIFO_RESET, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera recommends using RX_FIFO_RESET to reset the synchronizer when the DPA signals a loss-of-lock condition beyond the initial locking condition.

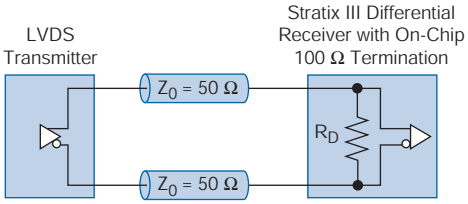
Differential I/O Termination

Stratix III devices provide a 100-ohm on-chip differential termination option on each differential receiver channel for LVDS standards. The on-chip termination saves board space by eliminating the need to add external resistors on the board. You can enable on-chip termination in the Quartus II software assignment editor.

On-chip differential termination is supported on all row I/O pins and SERDES block clock pins: CLK (0, 2, 9, and 11). It is not supported for column I/O pins, high speed clock pins CLK [1, 3, 8, 10], nor the corner PLL clock inputs.

Figure 9–9 illustrates device on-chip termination.

Figure 9–9. On-Chip Differential I/O Termination



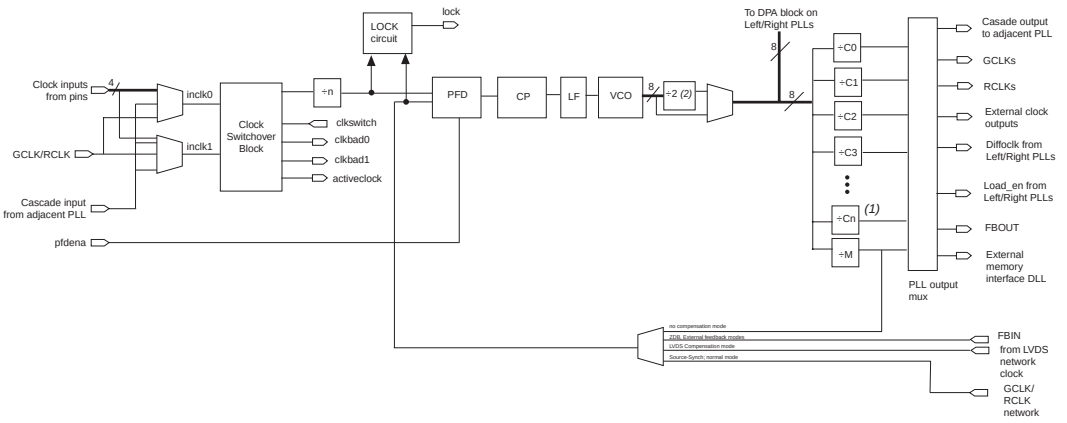
Left/Right PLLs (PLL_Lx/ PLL_Rx)

Stratix III devices contain up to eight left / right PLLs with up to four PLLs located on the left side and four on the right side of the device. The left PLLs can support high-speed differential I / O banks on the left side and the right PLLs can support banks on the right side of the device. The high-speed differential I / O receiver and transmitter channels use these left / right PLLs to generate the parallel global clocks (`rx`- or `tx`-clock) and high-speed clocks (`diffioclk`). Figure 9–1 shows the locations of the left / right PLLs. The PLL VCO operates at the clock frequency of the data rate. Each left / right PLL offers a single serial data rate support, but up to two separate serialization and / or deserialization factors (from the C0 and C1 left / right PLL clock outputs). Clock switchover and dynamic left / right PLL reconfiguration is available in high-speed differential I / O support mode.

For more details, refer to the *Clock Network and PLLs in Stratix III Devices* chapter in the *Stratix III Device Handbook*.

Figure 9–10 shows a simplified block diagram of the major components of the Stratix III PLL.

Figure 9–10. PLL Block Diagram *Notes (1), (2)*



Notes to Figure 9–10:

(1) n = 6 for Left / Right PLLs; n = 9 for Top / Bottom PLLs.

(2) This is the VCO post-scale counter K.

Clocking

The left / right PLLs feed into the differential transmitter and receive channels through the LVDS and DPA clock network. The center left / right PLLs can clock the transmitter and receive channels above and below them. The corner left / right PLLs can drive I / Os in the banks adjacent to them. The following two figures shows center and corner PLL clocking in Stratix III devices. More information on PLL clocking restrictions can be found in "Differential Pin Placement Guidelines" on page 9–19.

Figure 9–11. LVDS/DPA Clocks in Stratix III Devices with Center PLLs

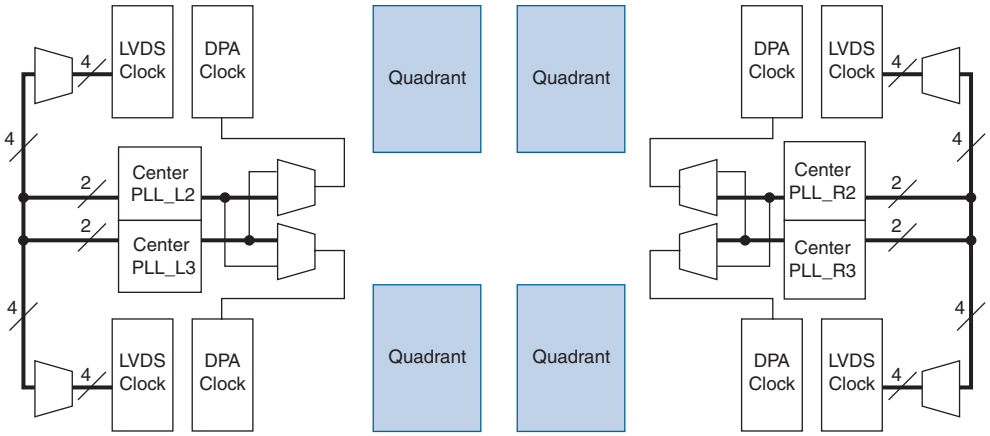
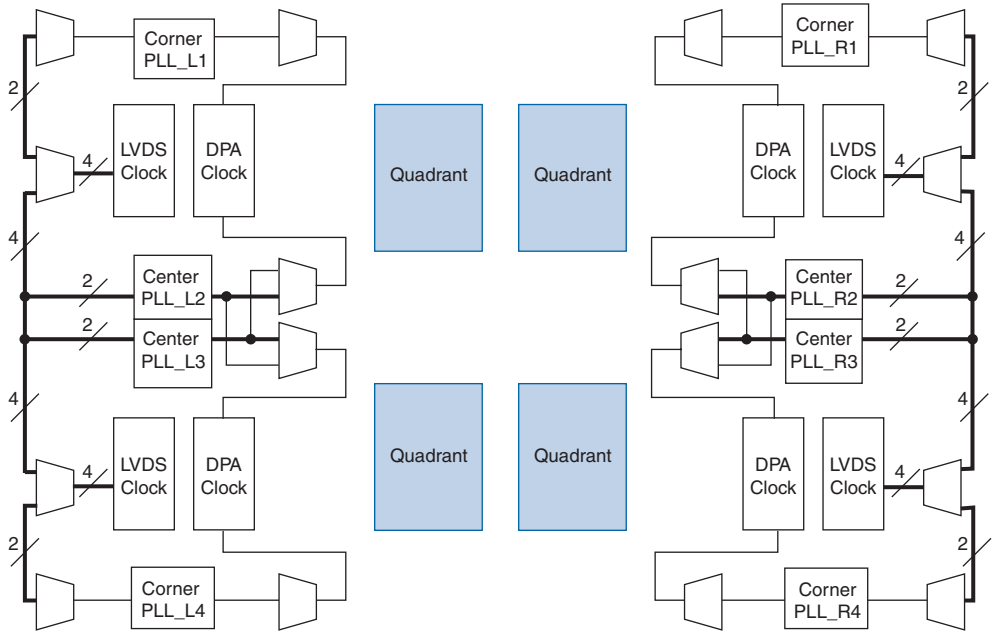


Figure 9–12. LVDS/DPA Clocks in Stratix III Devices with Center and Corner PLLs



Source Synchronous Timing Budget

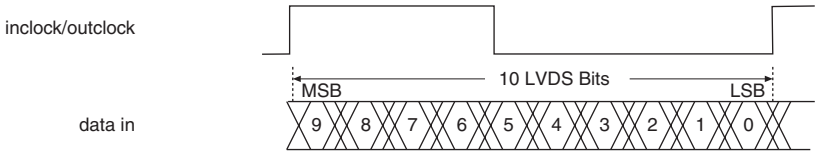
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix III devices. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix III devices, and how to use these timing parameters to determine a design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 9–13 shows the data bit orientation of the ×10 mode.

Figure 9–13. Bit Orientation in Quartus II Software



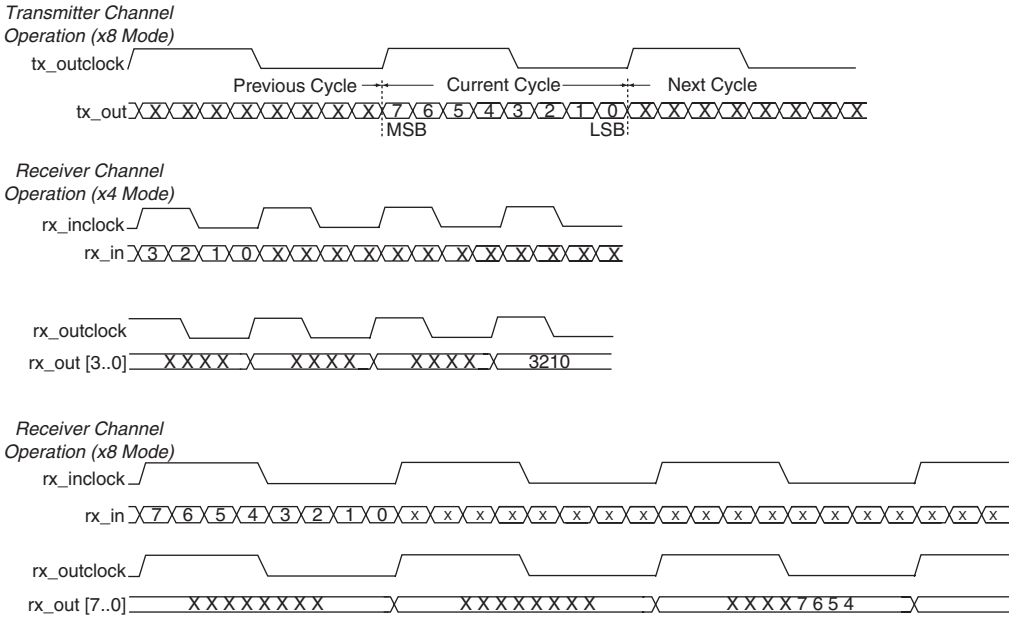
Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 9–14 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in Table 9–3.

Figure 9–14. Bit-Order and Word Boundary for One Differential Channel *Note (1)*



Note to Figure 9–14:

(1) These are only functional waveforms and are not intended to convey timing information.

Table 9–3 shows the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 9–3. Differential Bit Naming (Part 1 of 2)

Receiver Channel Data Number	Internal 8-bit parallel data	
	MSB position	LSB position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48

Table 9–3. Differential Bit Naming (Part 2 of 2)

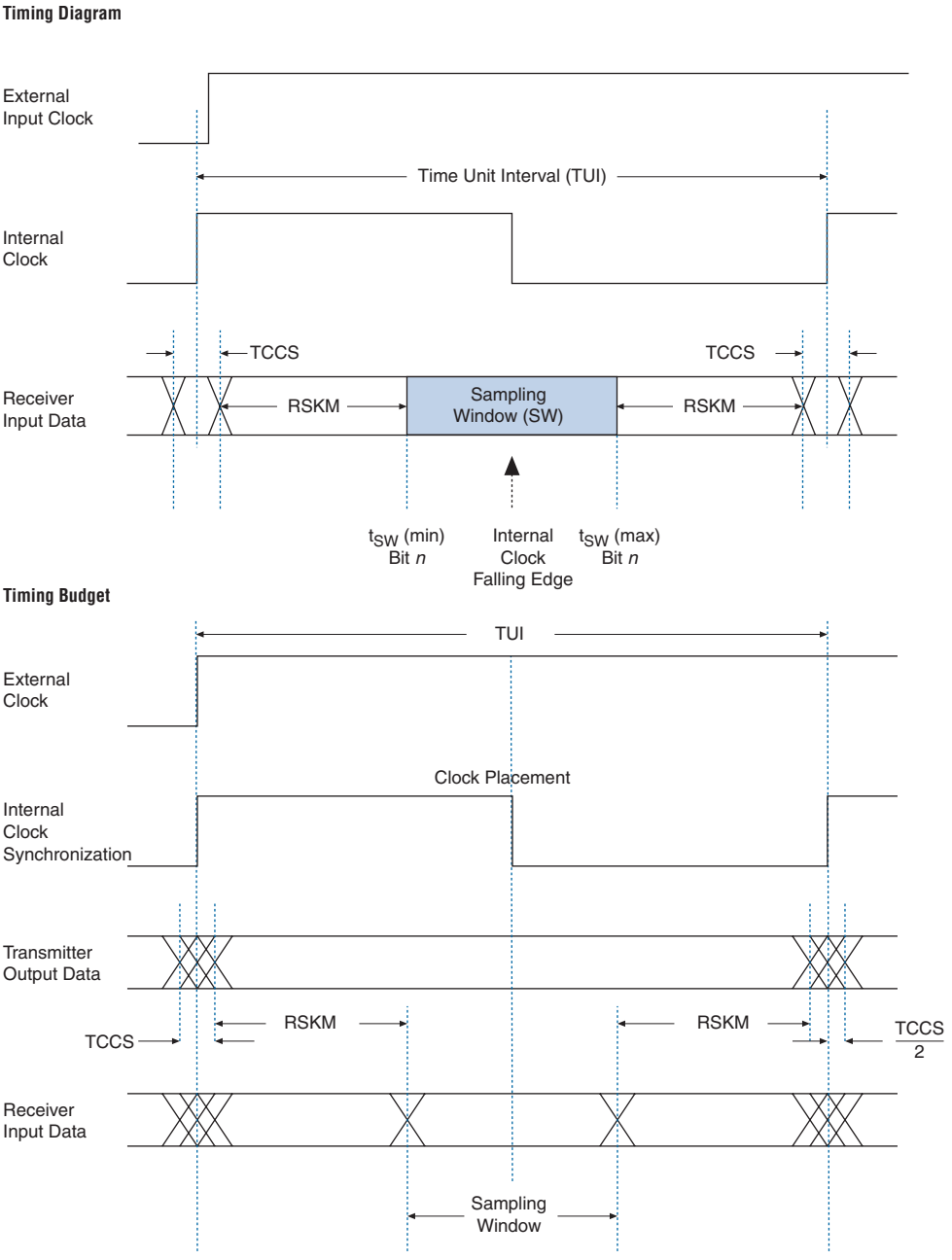
Receiver Channel Data Number	Internal 8-bit parallel data	
	MSB position	LSB position
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

Receiver Skew Margin for Non-DPA

Changes in system environment, such as temperature, media (cable, connector, or PCB) loading effect, the receiver's setup and hold times, and internal skew, reduce the sampling window for the receiver. The timing margin between the receiver's clock input and the data input sampling window is called Receiver Skew Margin (RSKM). Figure 9–15 shows the relationship between the RSKM and the receiver's sampling window.

Transmit channel-to-channel skew (TCCS), RSKM, and the sampling window specifications are used for high-speed source-synchronous differential signals without DPA. When using DPA, these specifications are exchanged for the simpler single DPA jitter tolerance specification. For instance, the receiver skew is why each input with DPA selects a different phase of the clock, thus removing the requirement for this margin. In the timing diagram, TSW represents time for the sampling window.

Figure 9–15. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA



Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and issues an error message if they are not met.

Since DPA usage adds some constraints on the placement of high-speed differential channels, this section is divided into pin placement guidelines with and without DPA usage.

Guidelines for DPA-Enabled Differential Channels

The Stratix III device has differential receivers and transmitters in I/O banks on the left and right sides of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When DPA-enabled channels are used in differential banks, you must adhere to the guidelines listed in the following sections.

DPA-enabled channels and Single-Ended I/Os

When there is a DPA channel enabled in a bank, single-ended I/Os are not allowed in the bank. Only differential I/O standards are allowed in the bank.

DPA-enabled Channel Driving Distance

- Each left/right PLL (in DPA mode) can drive up to 25 contiguous LAB rows. The 25 row limit includes any channels that are skipped during pin placement and any channels that are not bonded out to the pins. See Figure 9–16 for more details.
- Center left/right PLLs (in DPA mode) can drive up to 50 LAB rows (25 contiguous rows on the upper banks and 25 contiguous rows on the lower banks simultaneously, as shown in Figure 9–16).
- The 25 contiguous rows do not need to be adjacent to the driving PLL.

Figure 9–16. Left/Right PLL Driving Distance for DPA-Enabled Channels

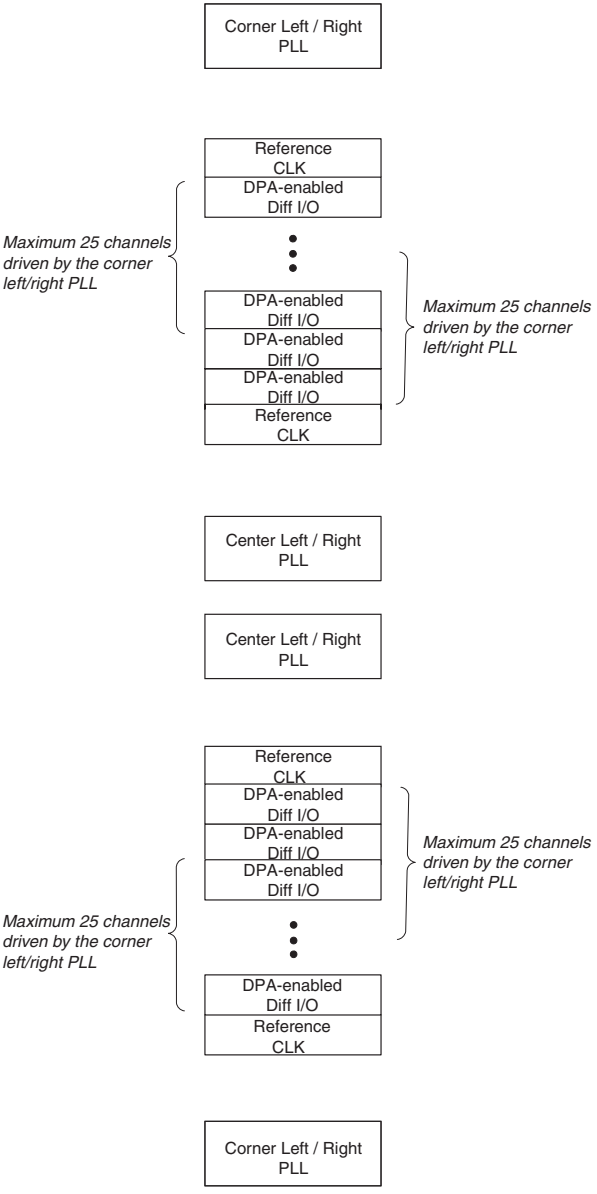


Figure 16.1

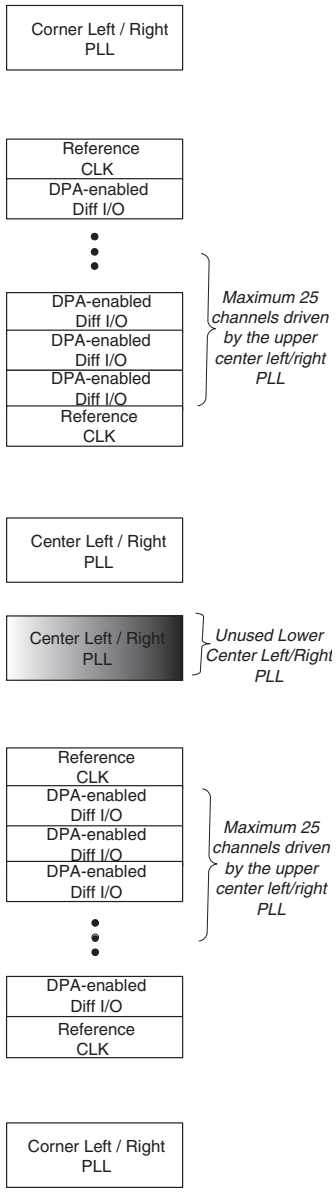
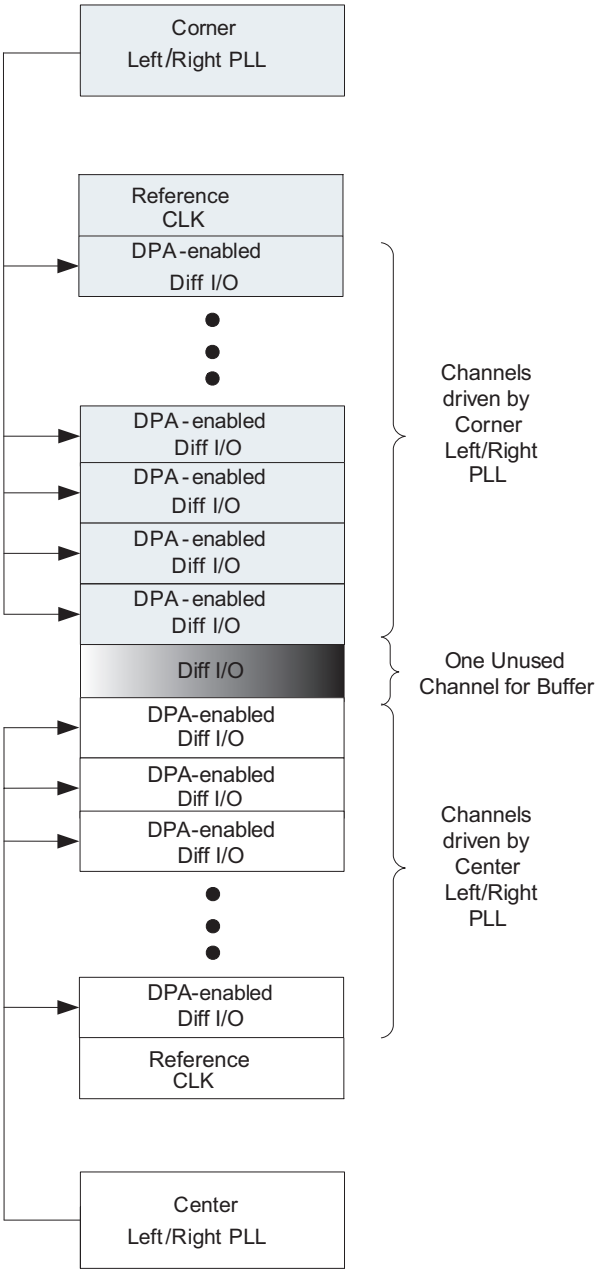


Figure 16.2

Using Corner and Center Left/Right PLLs

- If a differential bank is being driven by two left / right PLLs, where the corner left / right PLL is driving one group and the center left / right PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels (see Figure 9–17). The two groups can operate at independent frequencies.
- No separation is necessary if a single left / right PLL is driving DPA-enabled channels as well as DPA-disabled channels.

Figure 9–17. Corner and Center Left/Right PLLs Driving DPA-Enabled Differential I/Os in the Same Bank



Using Both Center Left/Right PLLs

- Both center left / right PLLs can be used to drive DPA-enabled channels simultaneously, as long as they drive these channels in their adjacent banks only, as shown in Figure 9–18 (18.1).
- If one of the center left / right PLLs drives the top and bottom banks, the other center left / right PLL cannot be used to drive differential channels, as shown in Figure 9–18 (18.2).
- If the top PLL_L2 / PLL_R2 drives DPA-enabled channels in the lower differential bank, the PLL_L3 / PLL_R3 cannot drive DPA-enabled channels in the upper differential banks and vice versa. In other words, the center left / right PLLs cannot drive cross-banks simultaneously, as shown in Figure 9–19.

Figure 9–18. Center Left/Right PLLs Driving DPA-Enabled Differential I/Os

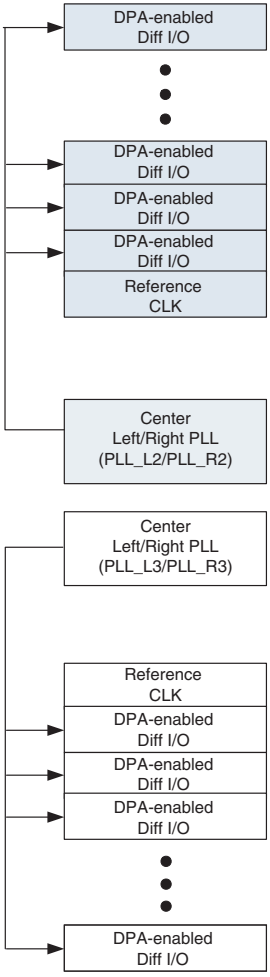


Figure 18.1

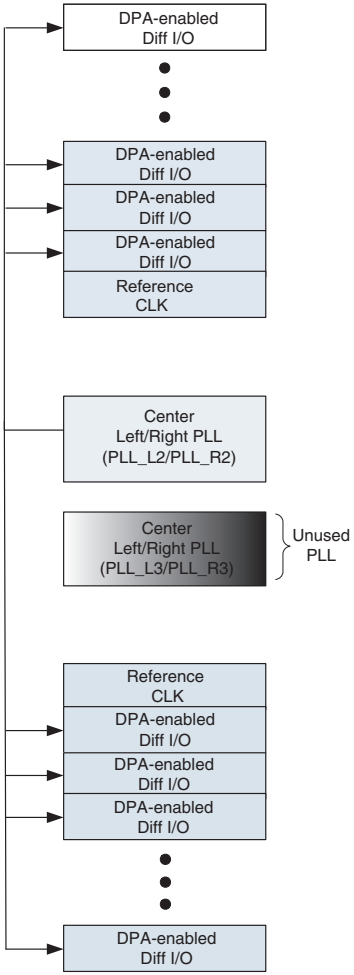
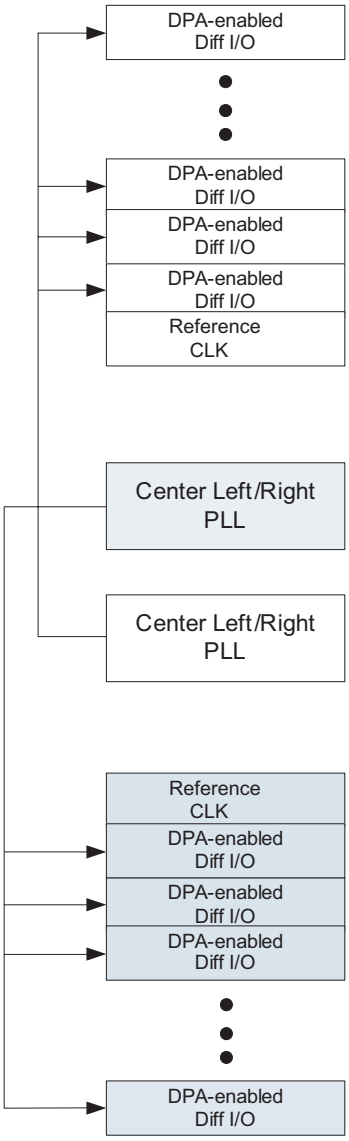


Figure 18.2

Figure 9–19. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left/Right PLLs



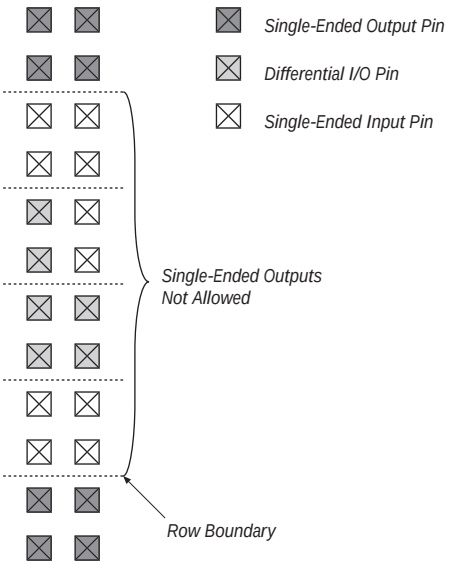
Guidelines for DPA-Disabled Differential Channels

When DPA-disabled channels are used in the left and right banks of a Stratix III device, you must adhere to the guidelines in the following sections.

DPA-Disabled Channels and Single-Ended I/Os

- Single-ended I/Os are allowed in the same I/O bank as long as the single-ended I/O standard uses the same VCCIO as the DPA-disabled differential I/O bank.
- Single-ended inputs can be in the same LAB row as a differential channel using the SERDES circuitry; however, IOE input registers are not available for the single-ended I/Os placed in the same LAB row as differential I/Os. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel. The input register must be implemented within the core logic.
- Single-ended output pins must be at least one LAB row away from differential I/O pins, as shown in Figure 9–20.

Figure 9–20. Single-Ended Output Pin Placement with Respect to the Differential I/O Pin



DPA-Disabled Channel Driving Distance

- Each left / right PLL can drive all the DPA-disabled channels in the entire bank.

Using Corner and Center Left/Right PLLs

- A corner left / right PLL can be used to drive all transmitter channels and a center left / right PLL can be used to drive all DPA-disabled receiver channels within the same differential bank. In other words, a transmitter channel and a receiver channel in the same LAB row can be driven by two different PLLs, as shown in Figure 9–21 (21.1).
- A corner left / right PLL and a center left / right PLL can drive duplex channels in the same differential bank as long as the channels driven by each PLL are not interleaved. No separation is necessary between the group of channels driven by the corner and center left / right PLLs. See Figure 9–21 (21.2) and Figure 9–22.

Figure 9–21. Corner and Center Left/Right PLLs Driving DPA-Disabled Differential I/Os in the Same Bank

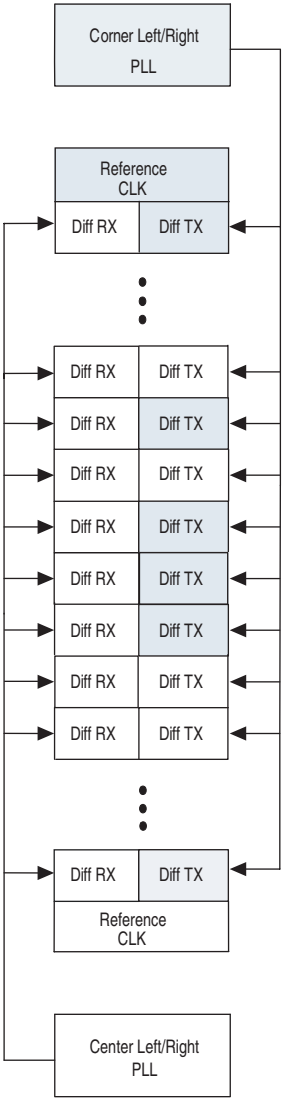


Figure 21.1

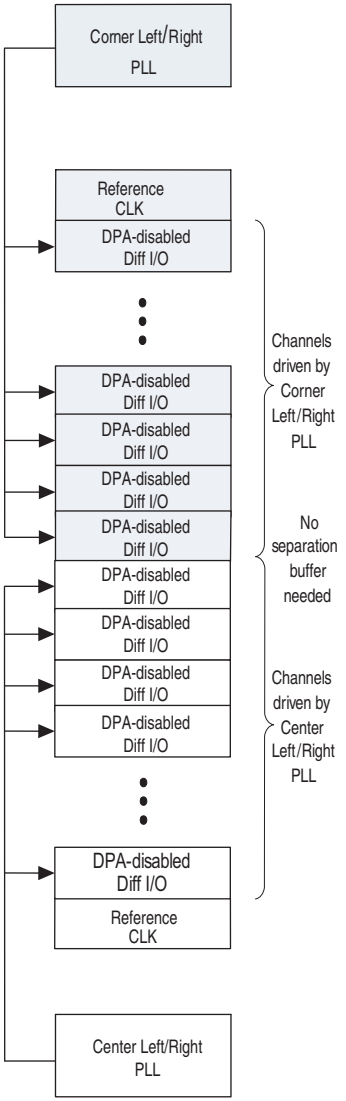
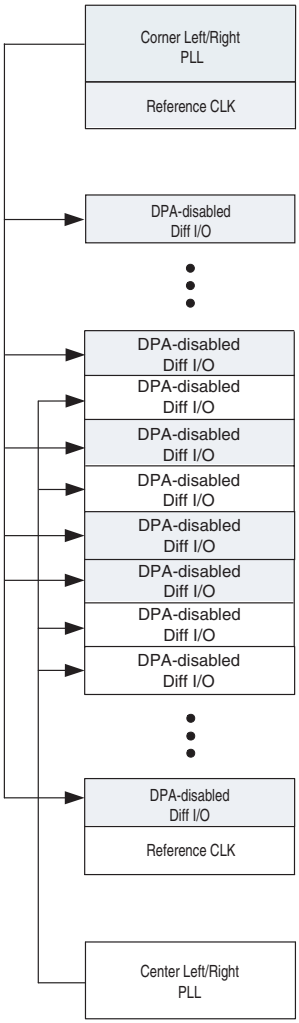


Figure 21.2

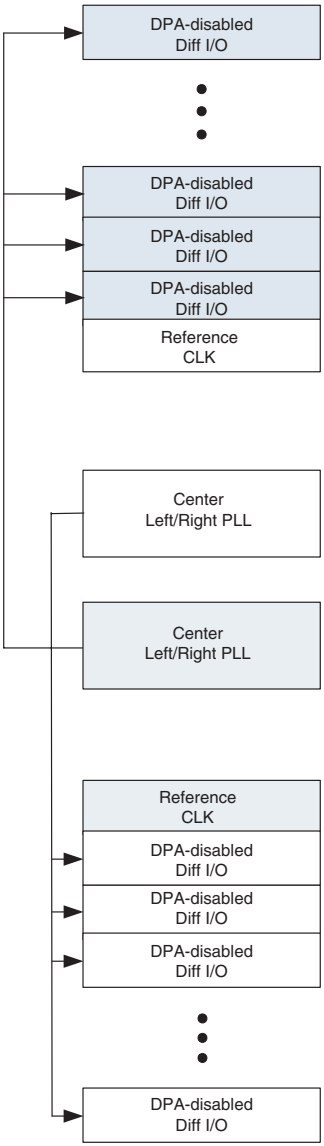
Figure 9–22. Invalid Placement of DPA-Disabled Differential I/Os Due to Interleaving of Channels Driven by the Corner and Center Left/Right PLLs



Using Both Center Left/Right PLLs

- Both center left / right PLLs can be used simultaneously to drive DPA-disabled channels on upper and lower differential banks. Unlike DPA-enabled channels, the center left / right PLLs can drive cross-banks. For example, the upper center left / right PLL can drive the lower differential bank at the same time the lower center left / right PLL is driving the upper differential bank and vice versa, as shown in Figure 9–23.

Figure 9–23. Both Center Left/Right PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Document Revision History

Table 9–4 shows the revision history for this document.

Table 9–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Minor changes to second paragraph of the section "Differential I/O Termination". Added Table 9–1 and Table 9–2.	—
November 2006 v1.0	Initial Release	—

Section III. Hot Socketing, Configuration, Remote Upgrades, and Testing

This section provides information on hot socketing and power-on reset, configuring Stratix® III devices, remote system upgrades, and IEEE 1149.1 (JTAG) Boundary-Scan Testing in the following sections:

- Chapter 10, Hot Socketing and Power-On Reset in Stratix III Devices
- Chapter 11, Configuring Stratix III Devices
- Chapter 12, Remote System Upgrades With Stratix III Devices
- Chapter 13, IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

10. Hot Socketing and Power-On Reset in Stratix III Devices

SIII51010-1.1

Introduction

This document contains information on hot socketing specifications, power-on reset requirements, and their implementation in Stratix® III devices.

Stratix III devices offer hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Stratix III device or a board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature also removes some of the difficulty when you use Stratix III devices on printed circuit boards (PCBs) that contain a mixture of 3.0, 2.5, 1.8, 1.5 and 1.2 V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Stratix III hot socketing feature provides:

- Board or device insertion and removal without external components or board manipulation.
- Support for any power-up sequence.
- Non-intrusive I/O buffers to system buses during hot insertion.

This section also discusses the power-on reset (POR) circuitry in Stratix III devices. The POR circuitry keeps the devices in the reset state until the power supplies are within operating range.

Stratix III Hot-Socketing Specifications

Stratix III devices are hot-socketing compliant without the need for any external components or special design requirements. Hot socketing support in Stratix III devices has the following advantages:

- You can drive the device before power-up without damaging it.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby not affecting other buses in operation.
- You can insert or remove a Stratix III device from a powered-up system board without damaging or interfering with normal system/board operation.

Devices Can Be Driven Before Power-Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix III devices before or during power-up or power-down without damaging the device. Stratix III devices support power-up or power-down of the V_{CCIO}, V_{CC}, V_{CCPGM}, and V_{CCPD} power supplies in any sequence in order to simplify system level design.

I/O Pins Remain Tri-Stated During Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the Stratix III device's output buffers are turned off during system power-up or power-down. Also, the Stratix III device does not drive out until the device is configured and working within recommended operating conditions.

Insertion or Removal of a Stratix III Device from a Powered-Up System

Devices that do not support hot-socketing can short power supplies when powered-up through the device signal pins. This irregular power-up can damage both the driving and driven devices and can disrupt card power-up.

A Stratix III device may be inserted into (or removed from) a powered-up system board without damaging or interfering with system-board operation.

You can power-up or power-down the V_{CCIO}, V_{CC}, V_{CCPGM}, and V_{CCPD} supplies in any sequence. The individual power supply ramp-up and ramp-down rates can range from 50 µs to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

For more information on the hot socketing specification, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Handbook* and the *Hot-Socketing and Power-Sequencing Feature and Testing for Altera Devices White Paper.*

A possible concern regarding hot-socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's power and ground planes. This condition can lead to latch-up and cause a low-impedance path from power to ground

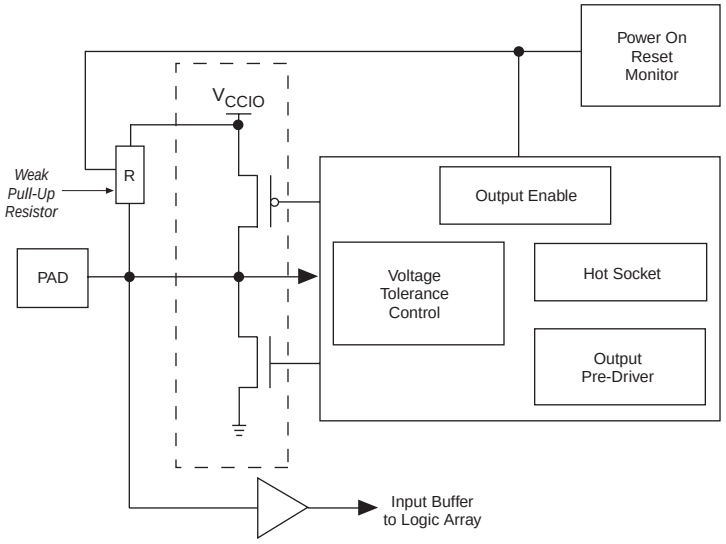
within the device. As a result, the device draws a large amount of current, possibly causing electrical damage. Nevertheless, Stratix III devices are immune to latch-up when hot-socketing.

Hot Socketing Feature Implementation in Stratix III Devices

The hot socketing feature turns off the output buffer during power-up and power-down of V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot socketing circuitry generates an internal HOTSCKT signal when the V_{CC}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage. The hot socketing circuitry is designed to prevent excess I/O leakage during power-up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot flip from the state set by the hot socketing circuit at this low voltage. Therefore, the hot socketing circuit has been removed on these configuration pins to make sure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power-up and power-down sequences.

Each I/O pin has the following circuitry shown in Figure 10–1.

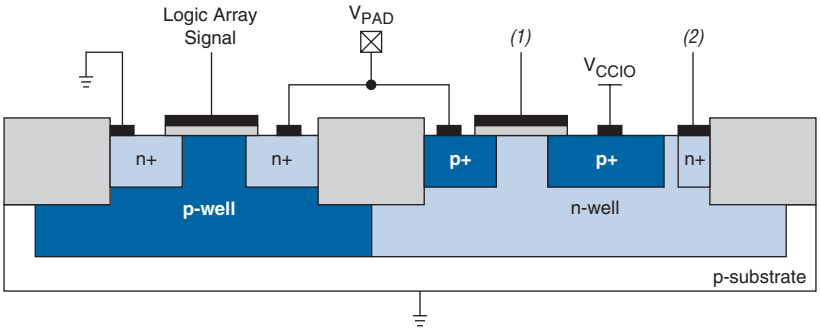
Figure 10–1. Hot Socketing Circuit Block Diagram for Stratix III Devices



The POR circuit monitors the voltage level of power supplies (V_{CC}, V_{CCL}, V_{CCPD}, V_{CCPGM} and V_{CCPT}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix III input/output element (IOE) keeps the I/O pins from floating. The 3.0-V tolerance control circuit permits the I/O pins to be driven by 3.0 V before V_{CCIO}, V_{CC}, V_{CCPD}, and/or V_{CCPGM} supplies are powered, and it prevents the I/O pins from driving out when the device is not in user mode.

Figure 10–2 shows a transistor-level cross section of the Stratix III device I/O buffers. This design prevents leakage current from I/O pins to the V_{CCIO} supply when V_{CCIO} is powered before the other voltage supplies or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.0-V tolerant circuit capacitance.

Figure 10–2. Transistor Level Diagram of a Stratix III Device I/O Buffers



Notes to Figure 10–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.

(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

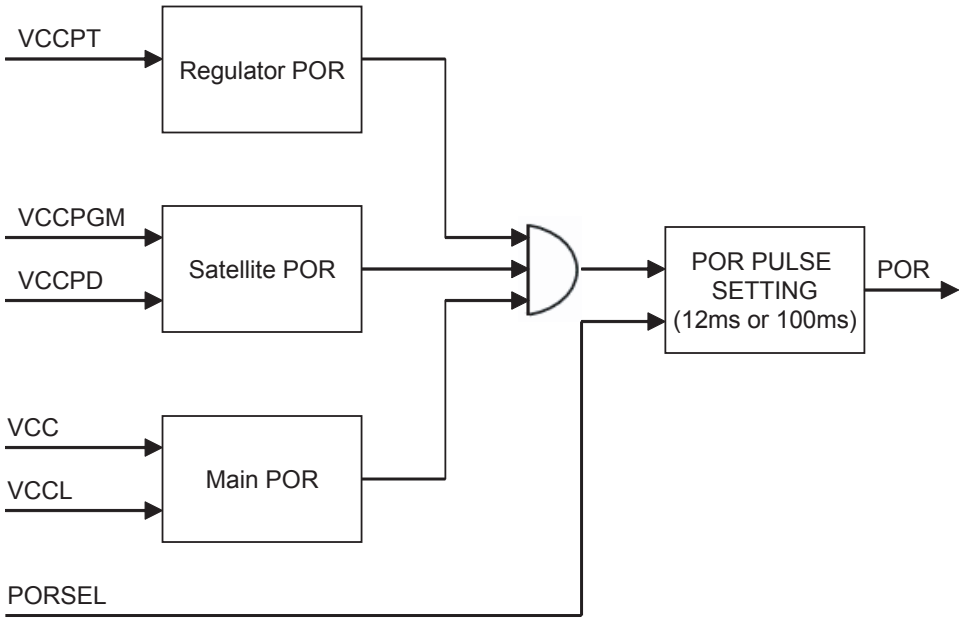
Power-On Reset Circuitry

When power is applied to a Stratix III device, a power-on-reset event occurs if the power supply reaches the recommended operating range within a certain period of time (specified as a maximum power supply ramp time; t_{RAMP}). The maximum power supply ramp time for Stratix III devices is 100 ms while the minimum power supply ramp time is 50 µs. Stratix III devices provide a dedicated input pin (PORSEL) to select a POR delay time of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR delay time is 100 ms. When the PORSEL pin is set to high, the POR delay time is 12 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device configuration. The satellite POR monitors V_{CCPD} and V_{CCPGM} power supplies that are used in the configuration buffers for device programming. The POR block also checks for functionality of I/O level shifters powered by V_{CCPD} and V_{CCPGM} during power-up mode. The main POR checks the V_{CC} and V_{CCL} supplies used in core. The internal configuration memory supply, which is used during device configuration, is checked by the regulator POR block and is gated in the main POR block for the final POR trip. A simplified block diagram of the POR block is shown in Figure 10–3.

All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Figure 10–3. Simplified POR Block Diagram



Power-On Reset Specifications

The POR circuit monitors the power supplies listed in Table 10–1:

Table 10–1. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V_{CC}	I/O registers power supply	1.1
V_{CCL}	Selectable core voltage power supply	0.9, 1.1
V_{CCPT}	Power supply for the programmable power technology	2.5
V_{CCPD}	I/O pre-driver power supply	2.5, 3.0
V_{CCPGM}	Configuration pins power supply	1.8, 2.5, 3.0

The POR circuit does not monitor the power supplies listed in Table 10–2:

Table 10–2. Power Supplies That Are Not Monitored by the POR Circuitry

Voltage Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	1.1
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	2.5

The POR specification is designed to ensure that all the circuits in the Stratix III device are at certain known states during power up.

The POR signal pulse width is programmable using the PORSEL input pin. When PORSEL is set to low, the POR signal pulse width is set to 100 ms. A POR pulse width of 100 ms allows serial flash devices with 65 ms to 100 ms internal POR delay to be powered-up and ready to receive the nSTATUS signal from Stratix III. When the PORSEL is set to high, the POR signal pulse width is set to 12 ms. A POR pulse width of 12 ms allows time for power supplies to ramp-up to full rail.

Refer to the *DC and Switching Characteristics* chapter, volume 2 of the *Stratix III Device Handbook* for more information on the POR specification.

Conclusion

Stratix III devices are hot-socketing compliant and allow successful device power-up without the need for any power sequencing. The POR circuitry keeps the devices in the reset state until the power supply voltage levels are within operating range.

Document Revision History

Table 10–3 shows the revision history for this document.

Table 10–3. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	All instances of VCCR changed to VCCPT in text, and in Figure 10–3, and Table 10–1.	—
November 2006 v1.0	Initial Release	—

11. Configuring Stratix III Devices

SIII51011-1.1

Introduction

This chapter contains complete information on the Stratix® III supported configuration schemes, how to execute the required configuration schemes, and all the necessary option pin settings.

Stratix III devices use SRAM cells to store configuration data. As SRAM memory is volatile, you must download configuration data to the Stratix III device each time the device powers up. You can configure Stratix III devices using one of four configuration schemes:

- Fast passive parallel (FPP)
- Fast active serial (AS)
- Passive serial (PS)
- Joint Test Action Group (JTAG)

All configuration schemes use either an external controller (for example, a MAX® II device or microprocessor), a configuration device, or a download cable. Refer to the "Configuration Features" on page 11–4 for more information.

Configuration Devices

There are two types of configuration devices to support different configuration solutions on a single-device or multi-device configuration chain:

- Enhanced configuration devices
- Serial configuration devices

The configuration devices are chosen based on the type of configuration scheme you use, the cost of the configuration solution, and whether cascading is required to support large configuration bitstreams.

The Altera® enhanced configuration devices (EPC16, EPC8, and EPC4) support a single-device configuration solution for high-density devices and can be used in the fast passive parallel (FPP) and passive serial (PS) configuration schemes. They are in-system programmability (ISP)-capable through their JTAG interface. The enhanced configuration devices are divided into two major blocks: the controller and the flash memory.

For information on enhanced configuration devices, refer to the *Enhanced Configuration Devices (EPC4, EPC8 and EPC16) Data Sheet* and the *Using Altera Enhanced Configuration Devices* chapters in volume 2 of the *Configuration Handbook*.

The largest enhanced configuration device supports 16 MBits of configuration bitstream. You may need to use the MAX II device, or use a microprocessor using a flash memory configuration method, or use the compression feature, to reduce the configuration file size of large Stratix III devices.

The Altera serial configuration devices (EPCS128, EPCS64, and EPCS16) support a single-device configuration solution for Stratix III devices and are used in the fast AS configuration scheme. Serial configuration devices offer a low-cost, low-pin count configuration solution.

For information on serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* in volume 2 of the *Configuration Handbook*.

The largest serial configuration device currently supports 64 MBits of configuration bitstream.

Configuration Schemes

Select the configuration scheme by driving the Stratix III device MSEL pins either high or low, as shown in Table 11–1. The MSEL pins are powered by the V_{CCPGM} power supply of the bank they reside in. The MSEL[2..0] pins have 5-kΩ internal pull-down resistors that are always active. During power-on reset (POR) and during reconfiguration, the MSEL pins have to be at LVTTL V_{IL} and V_{IH} levels to be considered a logic low and logic high.

To avoid any problems with detecting an incorrect configuration scheme, hard-wire the MSEL[] pins to V_{CCPGM} and GND, without any pull-up or pull-down resistors. Do not drive the MSEL[] pins by a microprocessor or another device.

Table 11–1. Stratix III Configuration Schemes (Part 1 of 2)

Configuration Scheme	MSEL2	MSEL1	MSEL0
Fast passive parallel (FPP)	0	0	0
Passive serial (PS)	0	1	0

Table 11–1. Stratix III Configuration Schemes (Part 2 of 2)			
Configuration Scheme	**MSEL2**	**MSEL1**	**MSEL0**
Fast AS (40 MHz) *(1)*	0	1	1
Remote system upgrade fast AS (40 MHz) *(1)*	0	1	1
FPP with design security feature and/or decompression enabled *(2)*	0	0	1
JTAG-based configuration *(4)*	*(3)*	*(3)*	*(3)*

Notes to Table 11–1:

(1) Stratix III only supports Fast AS configuration. You would need to use either EPCS16, EPCS64, or EPCS128 devices. The largest serial configuration device currently supports 64 MBits of configuration bitstream.

(2) These modes are only supported when using a MAX® II device or a microprocessor with flash memory for configuration. In these modes, the host system must output a DCLK that is 4× the data rate.

(3) Do not leave the MSEL pins floating. Connect them to V_{CCPGM} or ground. These pins support the non-JTAG configuration scheme used in production. If you only use JTAG configuration, you should connect the MSEL pins to ground.

(4) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

Table 11–2 shows the uncompressed raw binary file (**.rbf**) configuration file sizes for Stratix III devices.

Table 11–2. Stratix III Uncompressed Raw Binary File (.rbf) Sizes Note (1)		
Device	**Data Size (Mbits)**	**Data Size (MBytes)**
EP3SL50	22	2.75
EP3SL70	22	2.75
EP3SL110	47	5.875
EP3SL150	47	5.875
EP3SL200	66	8.25
EP3SE260	93	11.625
EP3SL340	120	15
EP3SE50	26	3.25
EP3SE80	48	6
EP3SE110	48	6

Note to Table 11–2:

(1) These values are preliminary.

Use the data in Table 11–2 to estimate the file size before design compilation. Different configuration file formats, such as a hexidecimal (**.hex**) or tabular text file (**.ttf**) format, will have different file sizes. Refer to Quartus® II software for the different types of configuration file and the file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device will have the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio is dependent on the design.

For more information on setting device configuration options or creating configuration files, refer to the *Software Settings* chapter in volume 2 of the *Configuration Handbook*.

Configuration Features

Stratix III devices offer design security, decompression, and remote system upgrade features. Design security using configuration bitstream encryption is available in Stratix III devices, which protects your designs. Stratix III devices can receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. You can make real-time system upgrades from remote locations of your Stratix III designs with the remote system upgrade feature.

Table 11–3 summarizes which configuration features you can use in each configuration scheme.

Table 11–3. Stratix III Configuration Features (Part 1 of 2)

Configuration Scheme	Configuration Method	Decompression	Design Security	Remote System Upgrade
FPP	MAX II device or a Microprocessor with flash memory	√*(1)*	√*(1)*	—
	Enhanced configuration device *(4)*	√*(2)*	—	—
Fast AS	Serial configuration device *(5)*	√	√	√*(3)*
PS	MAX II device or a Microprocessor with flash memory	√	√	—
	Enhanced configuration device *(4)*	√	√	—
	Download cable	√	√	—

Table 11–3. Stratix III Configuration Features (Part 2 of 2)

Configuration Scheme	Configuration Method	Decompression	Design Security	Remote System Upgrade
JTAG	MAX II device or a Microprocessor with flash memory	—	—	—
	Download cable	—	—	—

Notes to Table 11–3:

(1) In these modes, the host system must send a DCLK that is 4× the data rate.
(2) The enhanced configuration device decompression feature is available, while the Stratix III decompression feature is not available.
(3) Remote system upgrade is only available in the Fast AS configuration scheme. Only remote update mode is supported when using the Fast AS configuration scheme. Local update mode is not supported.
(4) The largest enhanced configuration device supports 16 MBits of configuration bitstream. You may need to use the Max II device, or us a microprocessor using the flash memory configuration method, or use the compression feature, to reduce the configuration file size of large Stratix III devices.
(5) The largest serial configuration device currently supports 64 MBits of configuration bitstream.

If your system already contains a common flash interface (CFI) flash memory, you can utilize it for the Stratix III device configuration storage as well. The MAX II parallel flash loader (PFL) feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Stratix III device. Both PS and FPP configuration modes are supported using this PFL feature.

For more information on PFL, refer to *AN 386: Using the MAX II Parallel Flash Loader with the Quartus II Software*.

For more information on programming Altera serial configuration devices, refer to "Programming Serial Configuration Devices" on page 11–38.

Configuration Data Decompression

Stratix III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Stratix III devices. During configuration, Stratix III devices decompress the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression typically reduces the configuration bitstream size by 35 to 55% based on the designs used.

Stratix III devices support decompression in the FPP (when using a MAX II device / microprocessor + flash), fast AS, and PS configuration schemes. The Stratix III decompression feature is not available in the FPP (when using enhanced configuration device) and JTAG configuration schemes.

When using FPP mode, the intelligent host must provide a DCLK that is 4× the data rate. Therefore, the configuration data must be valid for four DCLK cycles.

The decompression feature supported by Stratix III devices is different from the decompression feature in enhanced configuration devices (EPC16, EPC8, and EPC4), although they both use the same compression algorithm. The data decompression feature in the enhanced configuration devices allows them to store compressed data and decompresses the bitstream before transmitting it to the target devices. When using Stratix III devices in FPP mode with enhanced configuration devices, the decompression feature is available only in the enhanced configuration device, not in the Stratix III device.

In PS mode, use the Stratix III decompression feature because sending compressed configuration data reduces configuration time.

Do not use both the Stratix III device and the enhanced configuration device decompression feature simultaneously. The compression algorithm is not intended to be recursive and could expand the configuration file instead of compressing it further.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory, and decreases the time needed to transmit the bitstream to the Stratix III device. The time required by a Stratix III device to decompress a configuration file is less than the time needed to transmit the configuration data to the device.

There are two ways to enable compression for Stratix III bitstreams: before design compilation (in the **Compiler Settings** menu) and after design compilation (in the **Convert Programming Files** window).

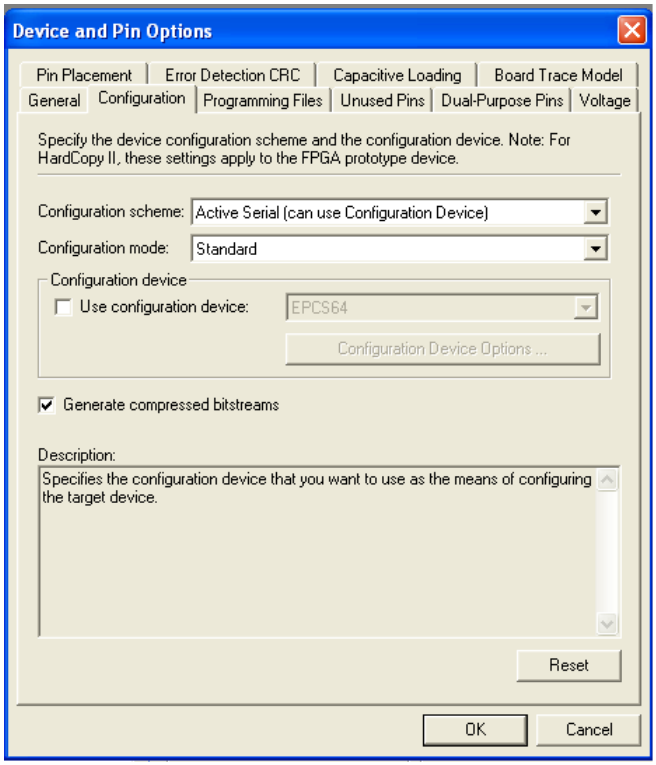
To enable compression in the project's **Compiler Settings** menu,

1. Select **Device** under the Assignments menu to bring up the **Settings** window.

2. After selecting your Stratix III device, open the **Device and Pin Options** window

3. In the Configuration settings tab, enable the check box for **Generate compressed bitstreams** (as shown in Figure 11–1).

Figure 11–1. Enabling Compression for Stratix III Bitstreams in Compiler Settings



You can also enable compression when creating programming files from the **Convert Programming Files** window.

1. Click **Convert Programming Files** (File menu).

2. Select the programming file type (**.pof**, **.sram, .hex**, **.rbf**, or **.ttf**).

3. For POF output files, select a configuration device.

4. In the **Input files to convert** box, select **SOF Data**.

5. Select **Add File** and add a Stratix III device SOF(s).

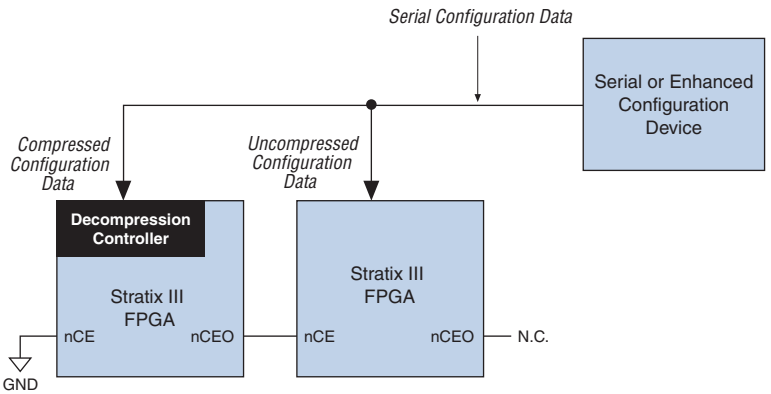
6. Select the name of the file you added to the **SOF Data** area and click **Properties**.

7. Check the **Compression** check box.

When multiple Stratix III devices are cascaded, you can selectively enable the compression feature for each device in the chain if you are using a serial configuration scheme. Figure 11–2 depicts a chain of two Stratix III devices. The first Stratix III device has compression enabled and therefore receives a compressed bitstream from the configuration device. The second Stratix III device has the compression feature disabled and receives uncompressed data.

In a multi-device FPP configuration chain (with a MAX II device / microprocessor + flash), all Stratix III devices in the chain must either enable or disable the decompression feature. You can not selectively enable the compression feature for each device in the chain because of the DATA and DCLK relationship.

Figure 11–2. Compressed and Uncompressed Configuration Data in the Same Configuration File



You can generate programming files for this setup from the **Convert Programming Files** window (File menu) in the Quartus II software.

Design Security Using Configuration Bitstream Encryption

Stratix III devices support decryption of configuration bitstream using the advanced encryption standard (AES) algorithm—the most advanced encryption algorithm available today. Both non-volatile and volatile key programming are supported using Stratix III devices. When using the design security feature, a 256-bit security key is stored in the Stratix III device. In order to successfully configure a Stratix III device that has the design security feature enabled, it must be configured with a configuration file that was encrypted using the same 256-bit security key. Non-volatile key programming does not require any external devices, such as a battery backup, for storage. However, for different applications, you can store the security keys in volatile memory in the Stratix III device. An external battery is needed for this volatile key storage.

When using a serial configuration scheme such as PS or fast AS, configuration time is the same whether or not the design security feature is enabled. If the FPP scheme is used with the design security or decompression feature, a 4× DCLK is required. This results in a slower configuration time when compared to the configuration time of a Stratix III device that has neither the design security, nor the decompression feature enabled.

For more information about this feature, refer to the *Design Security in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Remote System Upgrade

Stratix III devices feature remote update. For more information about this feature, refer to the *Remote System Upgrades with Stratix III Devices* in volume 2 of the *Stratix III Device Handbook*.

Power-On Reset Circuit

The POR circuit keeps the entire system in reset until the power supply voltage levels have stabilized on power-up. Upon power-up, the device does not release nSTATUS until V_{CCL}, V_{CC}, V_{CCPD}, and V_{CCPGM} are above the device's POR trip point. On power down, brown-out will occur if V_{CC} or V_{CCL} ramps down below the POR trip point and any of the V_{CC}, $V_{CCPD,}$ or V_{CCPGM} drops below the threshold voltage.

In Stratix III devices, a pin-selectable option (PORSEL) is provided that allows you to select between a typical POR time setting of 12 ms or 100 ms. In both cases, you can extend the POR time by using an external component to assert the nSTATUS pin low.

V_{CCPGM} Pins

Stratix III devices offer a new power supply, V_{CCPGM}, for all the dedicated configuration pins and dual function pins. Configuration voltage supported is 1.8 V, 2.5 V, and 3.0 V. Stratix III devices do not support 1.5 V configuration.

Use this pin to power all dedicated configuration inputs, dedicated configuration outputs, dedicated configuration bidirectional pins, and some of the dual functional pins that you use for configuration. With V_{CCPGM}, configuration input buffers do not have to share power lines with the regular I/O buffer in Stratix III devices.

The operating voltage for the configuration input pin is independent of the I/O banks power supply V_{CCIO} during the configuration. Therefore, no configuration voltage constraints on V_{CCIO} are needed in Stratix III devices.

V_{CCPD} Pins

Stratix III devices have a dedicated programming power supply, V_{CCPD}, which must be connected to 3.0 V /2.5 V in order to power the I/O pre-drivers, the JTAG input and output pins (TCK, TMS, TDI, TDO and TRST), and the design security circuitry.

V_{CCPGM} and V_{CCPD} must ramp-up from 0 V to the desired voltage level within 100 ms. If these supplies are not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.

For more information on the configuration pins power supply, refer to "Device Configuration Pins" on page 11–73.

Fast Passive Parallel Configuration

Fast passive parallel (FPP) configuration in Stratix III devices is designed to meet the continuously increasing demand for faster configuration times. Stratix III devices are designed with the capability of receiving byte-wide configuration data per clock cycle. Table 11–4 shows the MSEL pin settings when using the FPP configuration scheme.

Table 11–4. Stratix III MSEL Pin Settings for FPP Configuration Schemes

Configuration Scheme	MSEL2	MSEL1	MSEL0
FPP when not using the design security feature and/or decompression enabled	0	0	0
FPP with the design security feature and/or decompression enabled *(1)*	0	0	1

Note to Table 11–4:

(1) These modes are only supported when using a MAX II device or a microprocessor with flash memory for configuration. In these modes, the host system must output a DCLK that is 4× the data rate.

You can perform FPP configuration of Stratix III devices using an intelligent host, such as a MAX II device, a microprocessor, or an Altera enhanced configuration device. As the largest enhanced configuration device supports 16 MBits of configuration bitstream, you may need to use the MAX II device, or use a microprocessor using the flash memory configuration method, or use the compression feature, to reduce the configuration file size of large Stratix III devices.

FPP Configuration Using a MAX II Device as an External Host

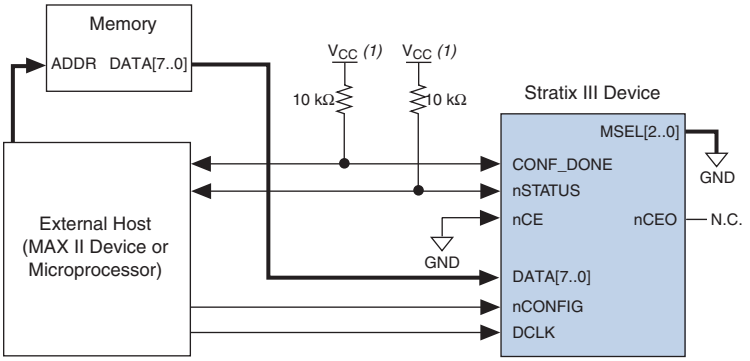
FPP configuration using compression and an external host provides the fastest method to configure Stratix III devices. In this configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device. You can store configuration data in **.rbf**, **.hex**, or **.ttf** format. When using the MAX II devices as an intelligent host, a design that controls the configuration process such as fetching the data from flash memory and sending it to the device must be stored in the MAX II device.

If you are using the Stratix III decompression and/or design security feature, the external host must be able to send a DCLK frequency that is 4× the data rate.

The 4× DCLK signal does not require an additional pin and is sent on the DCLK pin. The maximum DCLK frequency is 100 MHz, which results in a maximum data rate of 200 Mbps. If you are not using the Stratix III decompression or design security features, the data rate is 8× the DCLK frequency.

Figure 11–3 shows the configuration interface connections between the Stratix III device and a MAX II device for single device configuration.

Figure 11–3. Single Device FPP Configuration Using an External Host



Note to Figure 11–3:

(1) You should connect the resistor to a supply that provides an acceptable input signal for the device. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

Upon power-up, the Stratix III device goes through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. When PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power up and configuration, the user I/O pins and dual-purpose I/O pins have weak pull-up resistors, which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in the reset stage. To initiate configuration, the MAX II device must drive the nCONFIG pin from low to high.

V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device places the configuration data one byte at a time on the DATA[7..0] pins.

Stratix III devices receive configuration data on the DATA[7..0] pins and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. If you are using the Stratix III decompression and / or design security feature, configuration data is latched on the rising edge of every fourth DCLK cycle. After the configuration data is latched in, it is processed during the following three DCLK cycles.

Data is continuously clocked into the target device until CONF_DONE goes high. The CONF_DONE pin goes high one byte early in parallel configuration (FPP) modes. The last byte is required for serial configuration (AS and PS) modes. After the device has received the next to last byte of the configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ pull-up resistor. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

In Stratix III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Stratix III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation.

You can also synchronize initialization of multiple devices or delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the General tab of the **Device and Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. The CONF_DONE pin goes high one byte early in parallel configuration

(FPP) modes. The last byte is required for serial configuration (AS and PS) modes. After the CONF_DONE pin transitions high, CLKUSR is enabled after the time specified as t_{CD2CU}. After this time period elapses, Stratix III devices require 4,436 clock cycles to initialize properly and enter user mode. Stratix III devices support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. This **Enable INIT_DONE Output** option is available in the Quartus II software from the General tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it is high because of an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user-mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[7..0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[7..0] pins are available as user I/O pins after configuration. When you select the FPP scheme as a default in the Quartus II software, these I/O pins are tri-stated in user mode. To change this default option in the Quartus II software, select the Dual-Purpose Pins tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If you are using the Stratix III decompression and/or design security feature and need to stop DCLK, it can only be stopped three clock cycles after the last data byte was latched into the Stratix III device.

By stopping DCLK, the configuration circuit allows enough clock cycles to process the last byte of latched configuration data. When the clock restarts, the MAX II device must provide data on the DATA[7..0] pins prior to sending the first DCLK rising edge.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software from the General tab of the **Device and Pin Options** dialog box) is turned on, the device releases nSTATUS after a reset time-out period (maximum of 100 ms). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 ms) on nCONFIG to restart the configuration process.

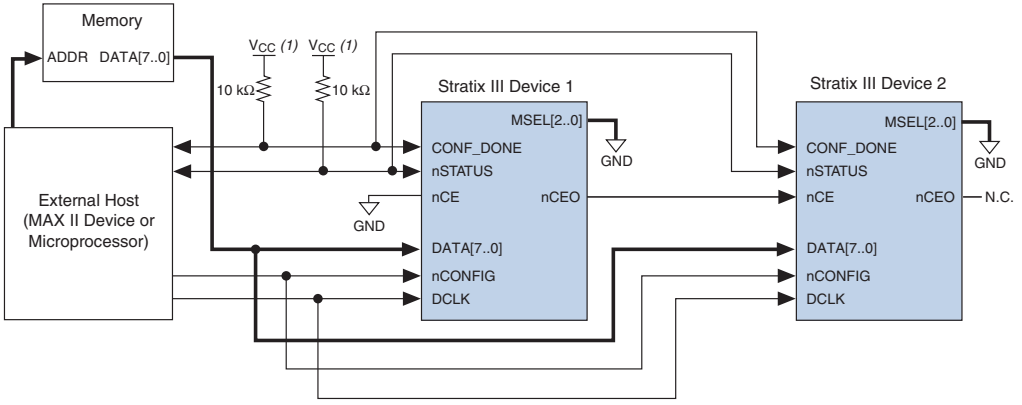
The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The MAX II device must monitor the CONF_DONE pin to detect errors and determine when programming completes. If all configuration data is sent, but the CONF_DONE or INIT_DONE signals have not gone high, the MAX II device will reconfigure the target device.

If you use the optional CLKUSR pin and the nCONFIG is pulled low to restart configuration during device initialization, you need to ensure CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 ms).

When the device is in user mode, initiating a reconfiguration is done by transitioning the nCONFIG pin low-to-high. The nCONFIG pin should be low for at least 2 ms. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Once nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

Figure 11–4 shows how to configure multiple devices using a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Stratix III devices are cascaded for multi-device configuration.

Figure 11–4. Multi-Device FPP Configuration Using an External Host



Note to Figure 11–4:

(1) You should connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O standard on the device and the external host.

In a multi-device FPP configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. The configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

All nSTATUS and CONF_DONE pins are tied together and if any device detects an error, configuration stops for the entire chain and you must reconfigure the entire chain. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

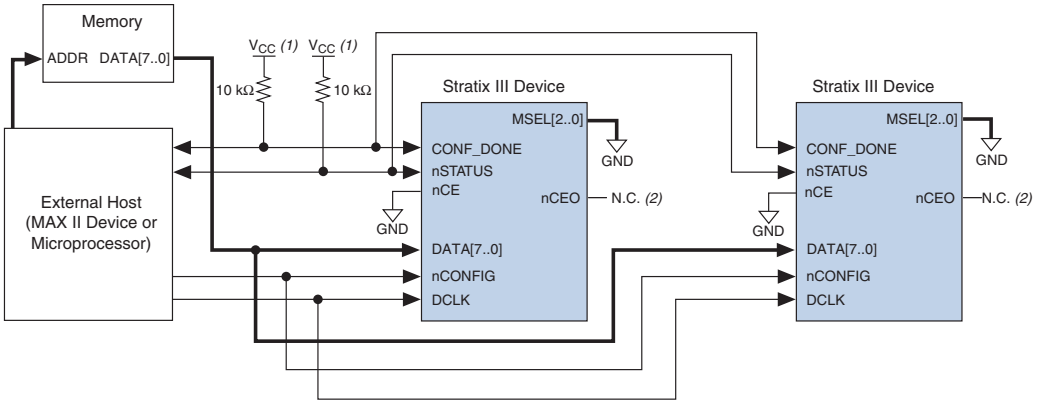
If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (maximum of 100 ms). After all nSTATUS pins are released and pulled high, the MAX II device tries to reconfigure the chain without pulsing

nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 ms) on nCONFIG to restart the configuration process.

In a multi-device FPP configuration chain, all Stratix III devices in the chain must either enable or disable the decompression and / or design security feature. You cannot selectively enable the decompression and / or design security feature for each device in the chain because of the DATA and DCLK relationship. If the chain contains devices that do not support design security, you should use a serial configuration scheme.

If a system has multiple devices that contain the same configuration data, tie all device nCE inputs to GND, and leave nCEO pins floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device. Devices must be the same density and package. All devices start and complete configuration at the same time. Figure 11–5 shows a multi-device FPP configuration when both Stratix III devices are receiving the same configuration data.

Figure 11–5. Multiple-Device FPP Configuration Using an External Host When Both Devices Receive the Same Data



Notes to Figure 11–5:

(1) You should connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I / O on the device and the external host.

(2) The nCEO pins of both Stratix III devices are left unconnected when configuring the same configuration data into multiple devices.

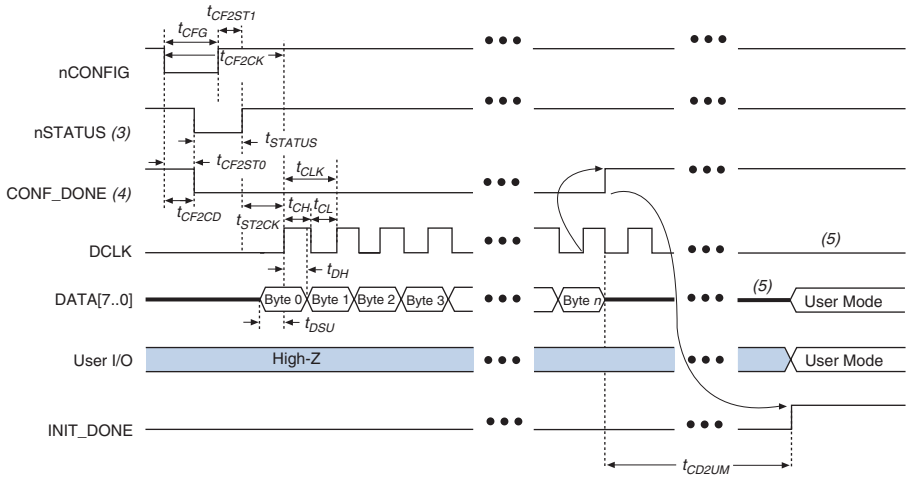
You can use a single configuration chain to configure Stratix III devices with other Altera devices that support FPP configuration, such as Stratix devices. To ensure that all devices in the chain complete configuration at the same time, or that an error flagged by one device initiates reconfiguration in all devices, tie all of the device CONF_DONE and nSTATUS pins together.

For more information on configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera Device Chains* in the *Configuration Handbook*.

FPP Configuration Timing

Figure 11–6 shows the timing waveform for FPP configuration when using a MAX II device as an external host. This waveform shows the timing when the decompression and the design security feature are not enabled.

Figure 11–6. FPP Configuration Timing Waveform *Notes (1), (2)*



Notes to Figure 11–6:

(1) You should use this timing waveform when the decompression and design security features are not used.
(2) The beginning of this waveform shows the device in user-mode. In user-mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
(3) Upon power-up, the Stratix III device holds nSTATUS low for the time of the POR delay.
(4) Upon power-up, before and during configuration, CONF_DONE is low.
(5) You should not leave DCLK floating after configuration. You should drive it high or low, whichever is more convenient.
(6) DATA[7..0] are available as user I/O pins after configuration. The state of these pins depends on the dual-purpose pin settings.

Table 11–5 defines the timing parameters for Stratix III devices for FPP configuration when the decompression and the design security features are not enabled.

Table 11–5. FPP Timing Parameters for Stratix III Devices *Notes (1), (2)*

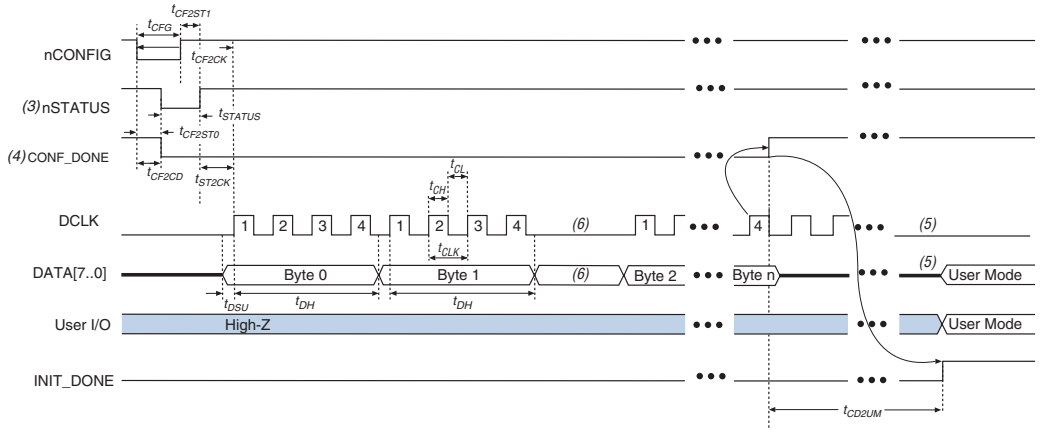
Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	800	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	10	100 *(3)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		100 *(3)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	100	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	4	—	ns
t_{CL}	DCLK low time	4	—	ns
t_{CLK}	DCLK period	10	—	ns
f_{MAX}	DCLK frequency	—	100	MHz
t_R	Input rise time	—	40	ns
t	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(4)*	20	100	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (4,436 × CLKUSR period)	—	—

Notes to Table 11–5:

(1) This information is preliminary.
(2) You should use these timing parameters when the decompression and design security features are not used.
(3) This value is obtainable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for starting up the device.

Figure 11–7 shows the timing waveform for FPP configuration when using a MAX II device as an external host. This waveform shows the timing when the decompression and / or the design security feature are enabled.

Figure 11–7. FPP Configuration Timing Waveform With Decompression or Design Security Feature Enabled
Notes (1), (2)



Notes to Figure 11–7:

(1) You should use this timing waveform when the decompression and / or design security features are used.
(2) The beginning of this waveform shows the device in user-mode. In user-mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
(3) Upon power-up, the Stratix III device holds nSTATUS low for the time of the POR delay.
(4) Upon power-up, before and during configuration, CONF_DONE is low.
(5) You should not leave DCLK floating after configuration. You should drive it high or low, whichever is more convenient.
(6) DATA[7..0] are available as user I / O pins after configuration. The state of these pins depends on the dual-purpose pin settings.
(7) If needed, you can pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[7..0] pins prior to sending the first DCLK rising edge.

Table 11–6 defines the timing parameters for Stratix III devices for FPP configuration when the decompression and / or the design security feature are enabled.

Table 11–6. FPP Timing Parameters for Stratix III Devices With Decompression or Design Security Feature Enabled Notes (1), (2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	800	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	10	100 (3)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		100 (3)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	100	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	30	—	ns
t_{CH}	DCLK high time	4	—	ns
t_{CL}	DCLK low time	4	—	ns
t_{CLK}	DCLK period	10	—	ns
f_{MAX}	DCLK frequency	—	100	MHz
t_{DATA}	Data rate	—	200	Mbps
t_R	Input rise time	—	40	ns
t	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (4)	20	100	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (4,436 × CLKUSR period)	—	—

Notes to Table 11–6:

(1) This information is preliminary.
(2) You should use these timing parameters when the decompression and design security features are used.
(3) This value is obtainable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for starting up the device.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* chapter in the *Configuration Handbook*.

FPP Configuration Using a Microprocessor

In this configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device.

All information in "FPP Configuration Using a MAX II Device as an External Host" on page 11–11 is also applicable when using a microprocessor as an external host. Refer to this section for all configuration and timing information.

FPP Configuration Using an Enhanced Configuration Device

In this configuration setup, an enhanced configuration device sends a byte of configuration data every DCLK cycle to the Stratix III device. Configuration data is stored in the configuration device.

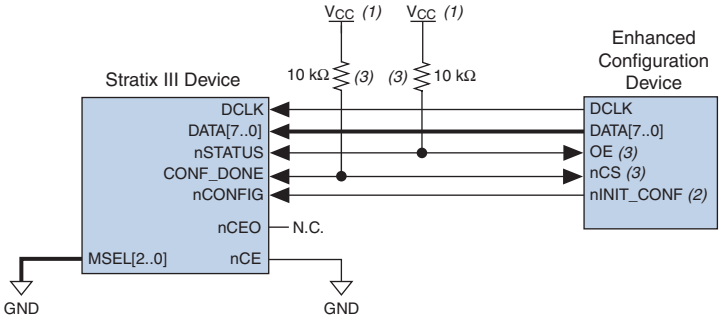
When configuring your Stratix III device using FPP mode and an enhanced configuration device, the enhanced configuration device decompression feature is available while the Stratix III decompression and design security features are not.

Figure 11–8 shows the configuration interface connections between a Stratix III device and the enhanced configuration device for a single device configuration.

The figures in this chapter only show the configuration-related pins and the configuration pin connections between the configuration device and the device.

For more information on the enhanced configuration device and flash interface pins, such as PGM[2..0], EXCLK, PORSEL, A[20..0], and DQ[15..0], refer to the *Enhanced Configuration Devices (EPC4, EPC8 and EPC16) Data Sheet*.

Figure 11–8. Single Device FPP Configuration Using an Enhanced Configuration Device



Notes to Figure 11–8:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up 10-kΩ resistor, check the **Disable nCS** and **OE pull-ups on configuration device** option when generating programming files.

You can find the value of the internal pull-up resistors on enhanced configuration devices in the *Enhanced Configuration Devices (EPC4, EPC8, and EPC16) Data Sheet*.

When using enhanced configuration devices, you can connect the device's nCONFIG pin to the nINIT_CONF pin of the enhanced configuration device, which allows the INIT_CONF JTAG instruction to initiate device configuration. You do not need to connect the nINIT_CONF pin if its functionality is not used. If nINIT_CONF is not used, nCONFIG must be pulled to V_{CC} through a 10-kΩ resistor. An internal pull-up resistor on the nINIT_CONF pin is always active in the enhanced configuration devices, which means you should not use an external pull-up resistor if nCONFIG is tied to nINIT_CONF.

Upon power-up, the Stratix III device goes through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. When PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS low, and tri-state all user I/O pins. The configuration

device also goes through a POR delay to allow the power supply to stabilize. You can set the POR time for enhanced configuration devices to either 100 ms or 2 ms, depending on its PORSEL pin setting. If the PORSEL pin is connected to GND, the POR delay is 100 ms. If the PORSEL pin is connected to V_{CC}, the POR delay is 2 ms. During this time, the configuration device drives its OE pin low. This low signal delays configuration because the OE pin is connected to the target device's nSTATUS pin.

When selecting a POR time, you need to ensure that the device completes power-up before the enhanced configuration device exits POR. Altera recommends that you use a 12 ms POR time for the Stratix III device, and that you use a 100 ms POR time for the enhanced configuration device.

When both devices complete POR, they release their open-drain OE or nSTATUS pin, which is then pulled high by a pull-up resistor. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors, which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

When the power supplies have reached the appropriate operating voltages, the target device senses the low-to-high transition on nCONFIG and initiates the configuration cycle. The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. You can delay the beginning of configuration by holding the nCONFIG or nSTATUS pin low.

V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} of the banks where the configuration and JTAG pins reside need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When nCONFIG goes high, the device comes out of reset and releases the nSTATUS pin, which is pulled high by a pull-up resistor. Enhanced configuration devices have an optional internal pull-up resistor on the OE pin. This option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you do not use this internal pull-up resistor, an external 10-kΩ pull-up resistor on the OE–nSTATUS line is required. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins.

When nSTATUS is pulled high, the configuration device's OE pin also goes high and the configuration device clocks data out to the device using the Stratix III device's internal oscillator. The Stratix III device receives configuration data on the DATA[7..0] pins and the clock is received on the DCLK pin. A byte of data is latched into the device on each rising edge of DCLK.

After the device has received all configuration data successfully, it releases the open-drain CONF_DONE pin which is pulled high by a pull-up resistor. Because CONF_DONE is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration devices have an optional internal pull-up resistor on the nCS pin. This option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you do not use this internal pull-up resistor, an external 10-kΩ pull-up resistor on the nCS-CONF_DONE line is required. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin.

In Stratix III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Stratix III device provides itself with enough clock cycles for proper initialization. You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. Supplying a clock on CLKUSR will not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, CLKUSR will be enabled after the time specified as t_{CD2CU}. After this time period elapses, Stratix III devices require 4,436 clock cycles to initialize properly and enter user mode. Stratix III devices support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin will be released and pulled high. In user-mode, the user

I/O pins will no longer have weak pull-up resistors and will function as assigned in your design. The enhanced configuration device will drive DCLK low and DATA[7..0] high at the end of configuration.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. Since the nSTATUS pin is tied to OE, the configuration device will also be reset. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box) is turned on, the device will automatically initiate reconfiguration if an error occurs. The Stratix III device releases its nSTATUS pin after a reset time-out period (maximum of 100 ms). When the nSTATUS pin is released and pulled high by a pull-up resistor, the configuration device reconfigures the chain. If this option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 ms to restart configuration. The external system can pulse nCONFIG if nCONFIG is under system control rather than tied to V_{CC}.

In addition, if the configuration device sends all of its data and then detects that CONF_DONE has not gone high, it recognizes that the device has not configured successfully. Enhanced configuration devices wait for 64 DCLK cycles after the last configuration bit was sent for CONF_DONE to reach a high state. In this case, the configuration device pulls its OE pin low, which in turn drives the target device's nSTATUS pin low. If the **Auto-restart configuration after error** option is set in the software, the target device resets and then releases its nSTATUS pin after a reset time-out period (maximum of 100 ms). When nSTATUS returns to a logic high level, the configuration device will try to reconfigure the device.

When CONF_DONE is sensed low after configuration, the configuration device recognizes that the target device has not configured successfully. Therefore, your system should not pull CONF_DONE low to delay initialization. Instead, you should use the CLKUSR option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain will initialize together if their CONF_DONE pins are tied together.

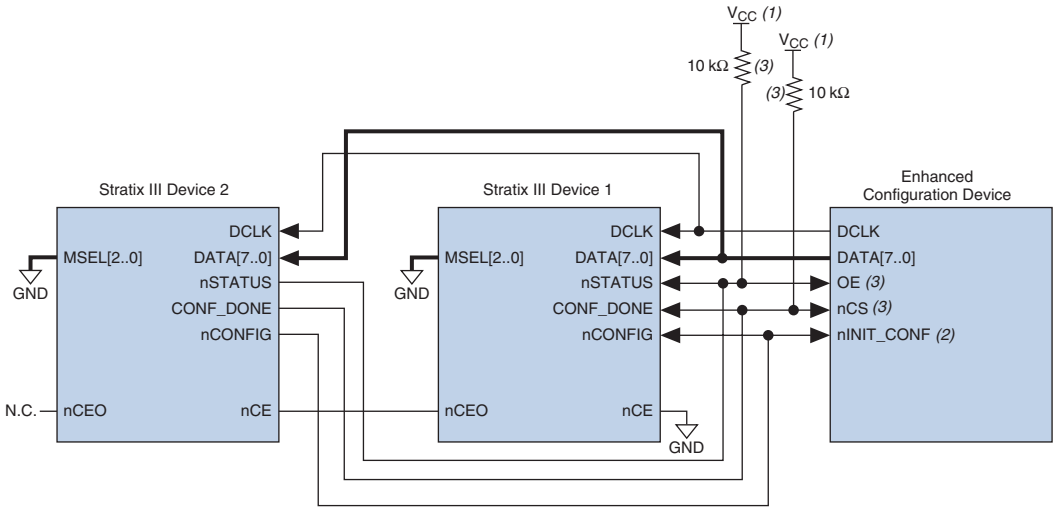
If you use the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, ensure CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 ms).

When the device is in user-mode, you can initialize a reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin should be low for at least 2 ms. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Because CONF_DONE is

pulled low, this activates the configuration device because it sees its nCS pin drive low. Once nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

Figure 11–9 shows how to configure multiple Stratix III devices with an enhanced configuration device. This circuit is similar to the configuration device circuit for a single device, except the Stratix III devices are cascaded for multi-device configuration.

Figure 11–9. Multi-Device FPP Configuration Using an Enhanced Configuration Device



Notes to Figure 11–9:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to configure the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} or through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-up resistors on the configuration device** option when generating programming files.

You cannot cascade enhanced configuration devices.

When performing a multi-device configuration, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multi-device configuration chains, refer to the *Software Settings* chapter in volume 2 of the *Configuration Handbook*.

In multi-device FPP configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Pay special attention to the configuration signals because they may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device.

When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

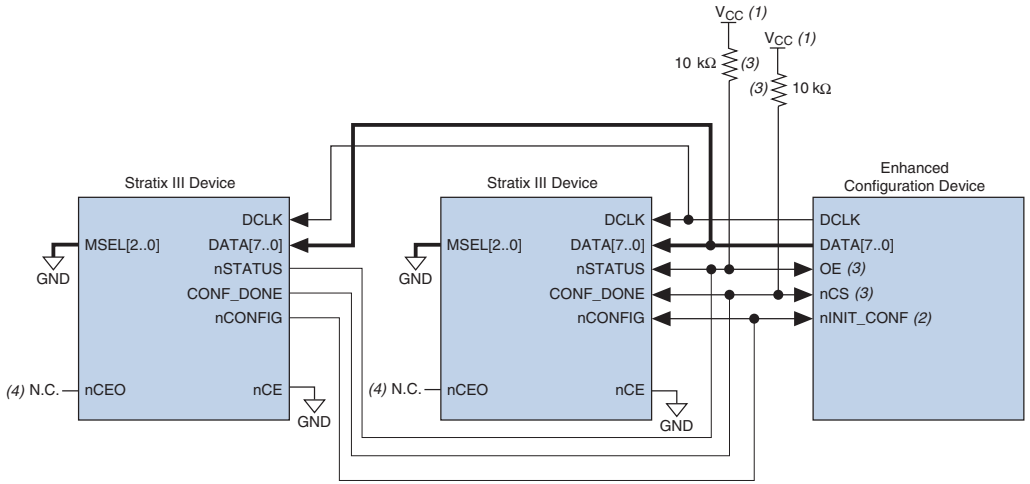
Since all nSTATUS and CONF_DONE pins are tied together, if any device detects an error, configuration stops for the entire chain and you must reconfigure the entire chain. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all devices, which causes them to enter a reset state. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices will automatically initiate reconfiguration if an error occurs. The devices will release their nSTATUS pins after a reset time-out period (maximum of 100 ms). When all the nSTATUS pins are released and pulled high, the configuration device tries to reconfigure the chain. If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 ms to restart configuration. The external system can pulse nCONFIG if nCONFIG is under system control rather than tied to V_{CC}.

Your system may have multiple devices that contain the same configuration data. To support this configuration scheme, all device nCE inputs are tied to GND, while nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for

every fourth device. Devices must be the same density and package. All devices will start and complete configuration at the same time. Figure 11–10 shows a multi-device FPP configuration when both Stratix III devices are receiving the same configuration data.

Figure 11–10. Multiple-Device FPP Configuration Using an Enhanced Configuration Device When Both devices Receive the Same Data



Notes to Figure 11–10:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-ups on the configuration device** option when generating programming files.

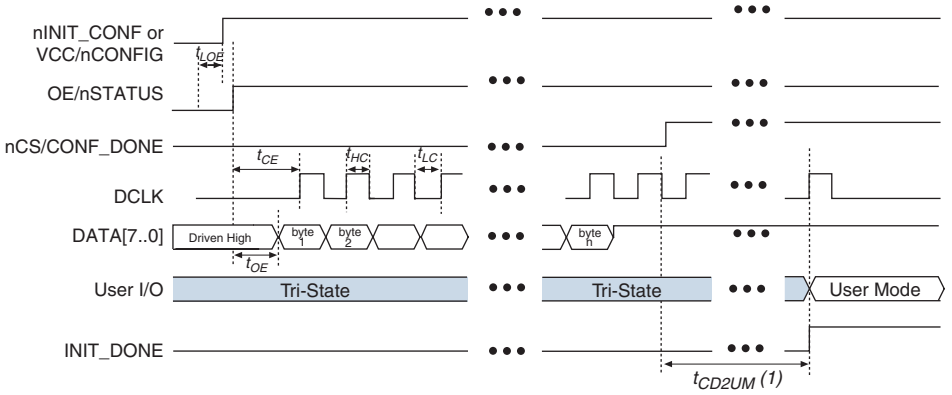
(4) The nCEO pins of both devices are left unconnected when configuring the same configuration data into multiple devices.

You can use a single enhanced configuration chain to configure multiple Stratix III devices with other Altera devices that support FPP configuration, such as Stratix and Stratix® GX devices. To ensure that all devices in the chain complete configuration at the same time, or that an error flagged by one device initiates reconfiguration in all devices, all of the device CONF_DONE and nSTATUS pins must be tied together.

For more information on configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera Device Chains* chapter in the *Configuration Handbook*.

Figure 11–11 shows the timing waveform for the FPP configuration scheme using an enhanced configuration device.

Figure 11–11. Stratix III FPP Configuration Using an Enhanced Configuration Device Timing Waveform



Note to Figure 11–11:
(1) The initialization clock can come from the Stratix III device's internal oscillator or the CLKUSR pin.

For timing information, refer to the *Enhanced Configuration Devices (EPC4, EPC8 and EPC16) Data Sheet* in the *Configuration Handbook.*

Device configuration options and how to create configuration files are discussed further in the *Software Settings* chapter of the *Configuration Handbook.*

Fast Active Serial Configuration (Serial Configuration Devices)

In the fast AS configuration scheme, Stratix III devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memory that feature a simple four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

The largest serial configuration device currently supports 64 MBits of configuration bitstream.

For more information on serial configuration devices, refer to the *Serial Configuration Devices Data Sheet* in the *Configuration Handbook.*

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Stratix III devices read configuration data via the serial interface, decompress data if necessary, and configure their SRAM cells. This scheme is referred to as the AS

configuration scheme because the Stratix III device controls the configuration interface. This scheme contrasts with the PS configuration scheme, where the configuration device controls the interface.

The Stratix III decompression and design security features are fully available when configuring your Stratix III device using fast AS mode.

Table 11–7 shows the MSEL pin settings when using the AS configuration scheme.

Table 11–7. Stratix III MSEL Pin Settings for AS Configuration Schemes *Note (1)*

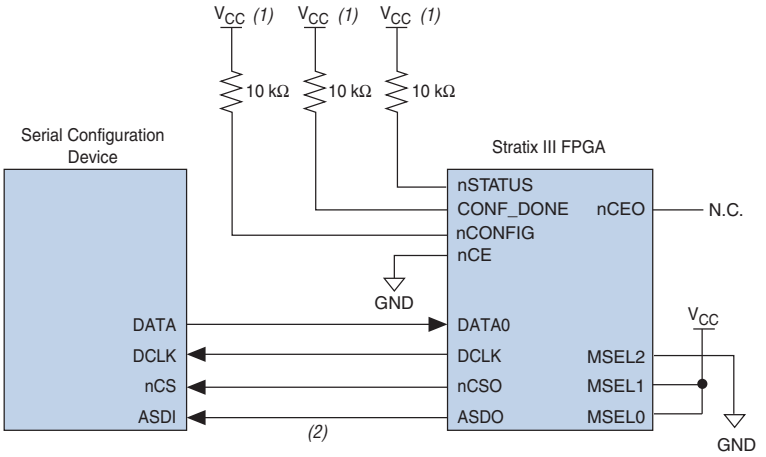
Configuration Scheme	MSEL2	MSEL1	MSEL0
Fast AS (40 MHz)	0	1	1
Remote system upgrade fast AS (40 MHz)	0	1	1

Note to Table 11–7:

(1) You would need to use either EPCS16, EPCS64, or EPCS128 devices. The largest serial configuration device currently supports 64 MBits of configuration bitstream.

Serial configuration devices have a four-pin interface: serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS). This four-pin interface connects to Stratix III device pins, as shown in Figure 11–12.

Figure 11–12. Single Device Fast AS Configuration



Notes to Figure 11–12:

(1) Connect the pull-up resistors to a 3.0-V supply.

(2) Stratix III devices use the ASDO-to-ASDI path to control the configuration device.

Upon power-up, the Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. If PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS and CONF_DONE low, and tri-state all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. After POR, the Stratix III device releases nSTATUS, which is pulled high by an external 10-kΩ pull-up resistor and enters configuration mode.

To begin configuration, power the V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} voltages (for the banks where the configuration and JTAG pins reside) to the appropriate voltage levels.

The serial clock (DCLK) generated by the Stratix III device controls the entire configuration cycle and provides the timing for the serial interface. Stratix III devices use an internal oscillator to generate DCLK. Using the MSEL[] pins, you can select to use a 40 MHz oscillator.

In fast AS configuration schemes, Stratix III devices drive out control signals on the falling edge of DCLK. The serial configuration device responds to the instructions by driving out configuration data on the falling edge of DCLK. Then the data is latched into the Stratix III device on the following falling edge of DCLK.

In configuration mode, Stratix III devices enable the serial configuration device by driving the nCSO output pin low, which connects to the chip select (nCS) pin of the configuration device. The Stratix III device uses the serial clock (DCLK) and serial data output (ASDO) pins to send operation commands and / or read address signals to the serial configuration device. The configuration device provides data on its serial data output (DATA) pin, which connects to the DATA0 input of the Stratix III devices.

After all configuration bits are received by the Stratix III device, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic high level. All AS configuration pins (DATA0, DCLK, nCSO, and ASDO) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by the weak internal pull-up resistors. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

In Stratix III devices, the initialization clock source is either the 10 MHz (typical) internal oscillator (separate from the active serial internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Stratix III device provides itself with enough clock cycles for proper initialization. You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device andand Pin Options** dialog box. When you enable the **user supplied start-up clock** option, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR will not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, CLKUSR is enabled after 600 ns. After this time period elapses, Stratix III devices require 4,436 clock cycles to initialize properly and enter user mode. Stratix III devices support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of

configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

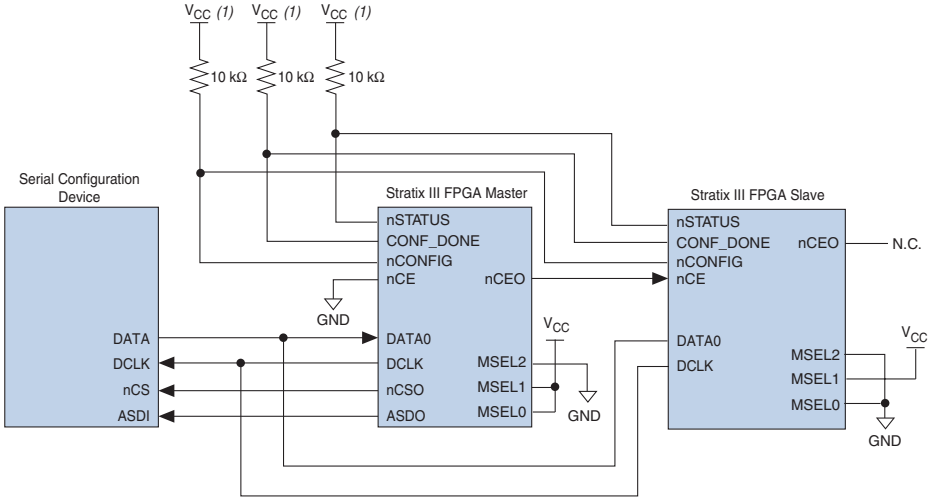
If an error occurs during configuration, Stratix III devices assert the nSTATUS signal low, indicating a data frame error, and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Stratix III device resets the configuration device by pulsing nCSO, releases nSTATUS after a reset time-out period (maximum of 100 ms), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 ms to restart configuration.

When the Stratix III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin should be low for at least 2 ms. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Once nCONFIG returns to a logic high level and nSTATUS is released by the Stratix III device, reconfiguration begins.

You can configure multiple Stratix III devices using a single serial configuration device. You can cascade multiple Stratix III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to ground. You must connect its nCEO pin to the nCE pin of the next device in the chain. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You must leave the nCEO pin of the last device unconnected. The nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA0 pins of each device in the chain are connected (refer to Figure 11–13).

This first Stratix III device in the chain is the configuration master and controls configuration of the entire chain. You must connect its MSEL pins to select the AS configuration scheme. The remaining Stratix III devices are configuration slaves. You must connect their MSEL pins to select the PS configuration scheme. Any other Altera device that supports PS configuration can also be part of the chain as a configuration slave. Figure 11–13 shows the pin connections for this setup.

Figure 11–13. Multi-Device Fast AS Configuration



Note to Figure 11–13:
(1) Connect the pull-up resistors to a 3.0-V supply.

As shown in Figure 11–13, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. But the subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart** configuration after error option, reconfiguration of the entire chain begins after a reset time-out period (maximum of 100 ms). If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The external system can pulse nCONFIG if it is under system control rather than tied to V_{CC}.

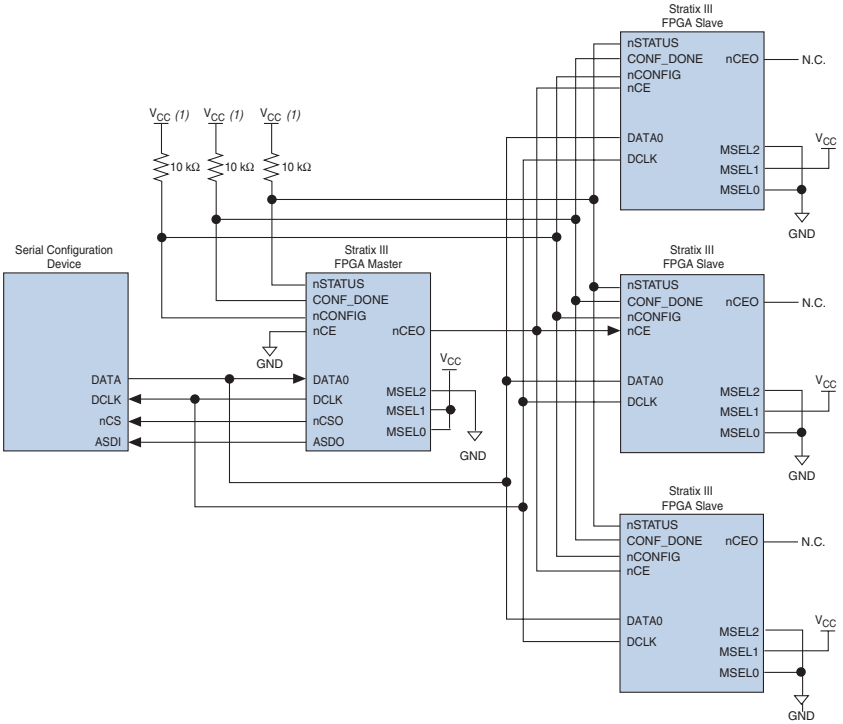
While you can cascade Stratix III devices, you cannot cascade or chain together serial configuration devices.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device and / or enable the compression feature. When configuring multiple devices, the size of the bitstream is the sum of the individual devices' configuration bitstreams.

A system may have multiple devices that contain the same configuration data. In active serial chains, you can implement this by storing two copies of the SOF in the serial configuration device. The first copy would configure the master Stratix III device; the second copy would configure all remaining slave devices concurrently. All slave devices must be the same density and package. The setup is similar to Figure 11–13, where the master is set up in active serial mode and the slave devices are set up in passive serial mode.

To configure four identical Stratix III devices with the same SOF, you could set up the chain similar to the example shown in Figure 11–14. The first device is the master device and its MSEL pins should be set to select AS configuration. The other three slave devices are set up for concurrent configuration and their MSEL pins should be set to select PS configuration. The nCEO pin from the master device drives the nCE input pins on all three slave devices, and the DATA and DCLK pins connect in parallel to all four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master drives nCE low and transmits the second copy of the configuration data to all three slave devices, configuring them simultaneously.

Figure 11–14. Multi-Device Fast AS Configuration When devices Receive the Same Data



Note to Figure 11–14:
(1) Connect the pull-up resistors to a 3.0-V supply.

Estimating Active Serial Configuration Time

Active serial configuration time is dominated by the time it takes to transfer data from the serial configuration device to the Stratix III device. This serial interface is clocked by the Stratix III DCLK output (generated from an internal oscillator). As the Stratix III device only supports fast AS configuration, the DCLK frequency needs to be set to 40 MHz (25 ns). Therefore, the minimum configuration time estimate for an EP3SL50 device (15 MBits of uncompressed data) is:

RBF Size × (minimum DCLK period / 1 bit per DCLK cycle) = estimated minimum configuration time

15 Mbits × (25 ns / 1 bit) = 375 ms

Enabling compression reduces the amount of configuration data that is transmitted to the Stratix III device, which also reduces configuration time. On average, compression reduces configuration time, depending on the design.

Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™ or ByteBlaster™ II download cable. Alternatively, you can program them using the Altera programming unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can perform in-system programming of serial configuration devices via the conventional AS programming interface or JTAG interface solution.

As serial configuration devices do not support the JTAG interface, the conventional method to program them is via the AS programming interface. The configuration data used to program serial configuration devices is downloaded via programming hardware.

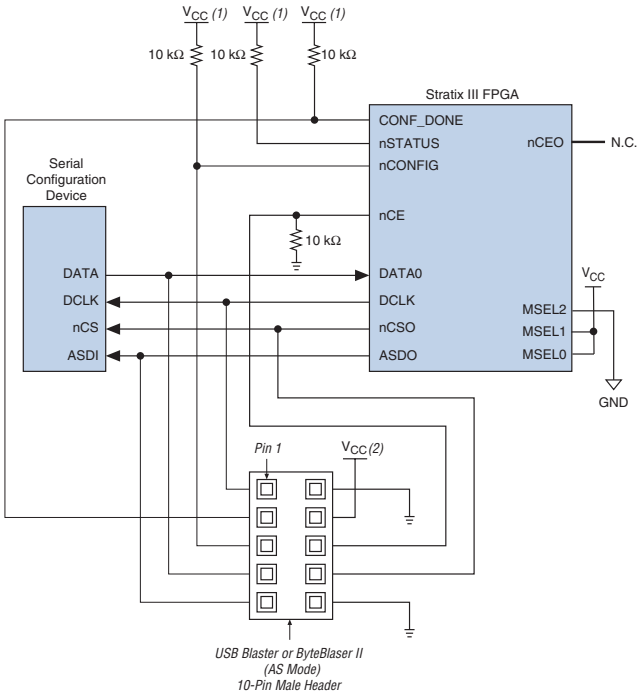
During in-system programming, the download cable disables device access to the AS interface by driving the nCE pin high. Stratix III devices are also held in reset by a low level on nCONFIG. After programming is complete, the download cable releases nCE and nCONFIG, allowing the pull-down and pull-up resistors to drive GND and V_{CC}, respectively. Figure 11–15 shows the download cable connections to the serial configuration device.

Altera has developed Serial FlashLoader (SFL); an in-system programming solution for serial configuration devices using the JTAG interface. This solution requires the Stratix III device to be a bridge between the JTAG interface and the serial configuration device.

For more information on SFL, refer to the *AN 370: Using the Serial FlashLoader with Quartus II Software.*

For more information on the USB Blaster download cable, refer to the *USB-Blaster USB Port Download Cable Data Sheet*. For more information on the ByteBlaster™ II cable, refer to the *ByteBlaster II Download Cable Data Sheet*.

Figure 11–15. In-System Programming of Serial Configuration Devices



Notes to Figure 11–15:

(1) Connect these pull-up resistors to 3.0-V supply.

(2) Power up the ByteBlaster II cable's V_{CC} with a 3.0-V supply.

You can program serial configuration devices with the Quartus II software using the Altera programming hardware and the appropriate configuration device programming adapter.

In production environments, you can program serial configuration devices using multiple methods. You can use Altera programming hardware or other third-party programming hardware to program blank serial configuration devices before they are mounted onto printed circuit boards (PCBs). Alternatively, you can use an on-board microprocessor to program the serial configuration device in-system using C-based software drivers provided by Altera.

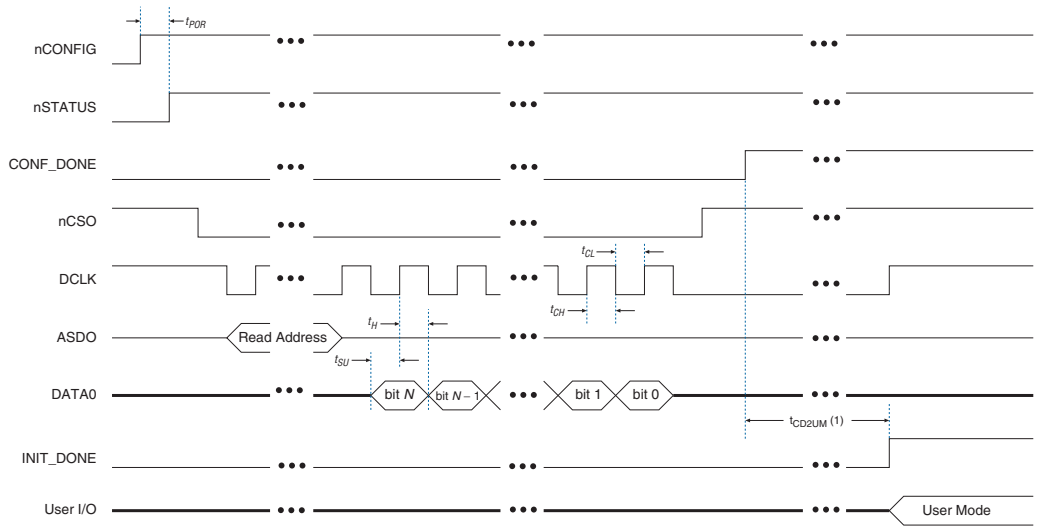
You can program a serial configuration device in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming, which can be easily customized to fit in different embedded systems. SRunner is able to read a raw programming data (**.rpd**) file and write to the serial

configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time with the Quartus II software.

For more information about SRunner, refer to *AN 418: SRunner: An Embedded Solution for EPCS Programming* and the source code on the Altera web site at **www.altera.com**.

For more information on programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* in the *Configuration Handbook*.

Figure 11–16. Fast AS Configuration Timing



Note to Figure 11–16:

(1) The initialization clock can come from the Stratix III device's internal oscillator or the CLKUSR pin.

Table 11–8 shows the fast AS timing parameters for Stratix III devices.

Table 11–8. Fast AS Timing Parameters for Stratix III Devices

Symbol	Parameter	Minimum	Typical	Maximum	Units
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	—	100	µs
t_{DSU}	Data setup time before falling edge on DCLK	7	—	—	ns
t_{DH}	Data hold time after falling edge on DCLK	0	—	—	ns
t_{CH}	DCLK high time	10	—	—	ns
t_{CL}	DCLK low time	10	—	—	ns
t_{CD2UM}	CONF_DONE high to user mode	20	—	100	µs

Passive Serial Configuration

You can program PS configuration of Stratix III devices using an intelligent host, such as a MAX II device or microprocessor with flash memory, an Altera configuration device, or a download cable. In the PS scheme, an external host (a MAX II device, embedded processor, configuration device, or host PC) controls configuration. As the largest enhanced configuration device supports 16 MBits of configuration bitstream, you may need to use the MAX II device, or use a microprocessor using the flash memory configuration method, or utilize the compression feature, to reduce the configuration file size of large Stratix III devices. Configuration data is clocked into the target Stratix III device via the DATA0 pin at each rising edge of DCLK.

The Stratix III decompression and design security features are fully available when configuring your Stratix III device using PS mode.

Table 11–9 shows the MSEL pin settings when using the PS configuration scheme.

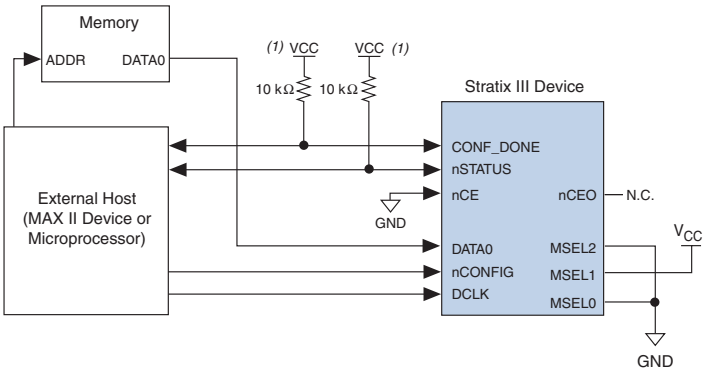
Table 11–9. Stratix III MSEL Pin Settings for PS Configuration Schemes

Configuration Scheme	MSEL2	MSEL1	MSEL0
PS	0	1	0

PS Configuration Using a MAX II Device as an External Host

In this configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device. You can store configuration data in **.rbf**, **.hex**, or .**ttf** format. Figure 11–17 shows the configuration interface connections between a Stratix III device and a MAX II device for single device configuration.

Figure 11–17. Single Device PS Configuration Using an External Host



Note to Figure 11–17:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

Upon power-up, Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. When PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. To initiate configuration, the MAX II device must generate a low-to-high transition on the nCONFIG pin.

V_{CC}, V_{CCIO}, V_{CCPGM} and V_{CCPD}, of the banks where the configuration and JTAG pins reside, need to be fully powered to the appropriate voltage levels in order to begin the configuration process.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device should place the configuration data one bit at a time on the DATA0 pin. If you are using configuration data in **.rbf**, **.hex**, or **.ttf** format, you must send the least significant bit (LSB) of each data byte first. For example, if the RBF contains the byte sequence 02 1B EE 01 FA, the serial bitstream you should transmit to the device is 0100-0000 1101-1000 0111-0111 1000-0000 0101-1111.

The Stratix III device receives configuration data on the DATA0 pin and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high. After the device has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-kΩ pull-up resistor. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

In Stratix III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you use the internal oscillator, the Stratix III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you supply a clock on CLKUSR, it will not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, CLKUSR will be enabled after the time specified as t_{CD2CU}. After this time period elapses**,** Stratix III devices require 4,436 clock cycles to initialize properly and enter user mode. Stratix III devices support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin will be released and pulled high. The MAX II device must be able to detect this low-to-high transition which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user-mode, the user I/O pins will no longer have weak pull-up resistors and will function as assigned in your design.

To ensure DCLK and DATA0 are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you chose the PS scheme as a default in the Quartus II software, this I/O pin is tri-stated in user mode and should be driven by the MAX II device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device and Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box) is turned on, the Stratix III device releases nSTATUS after a reset time-out period (maximum of 100 ms). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2ms) on nCONFIG to restart the configuration process.

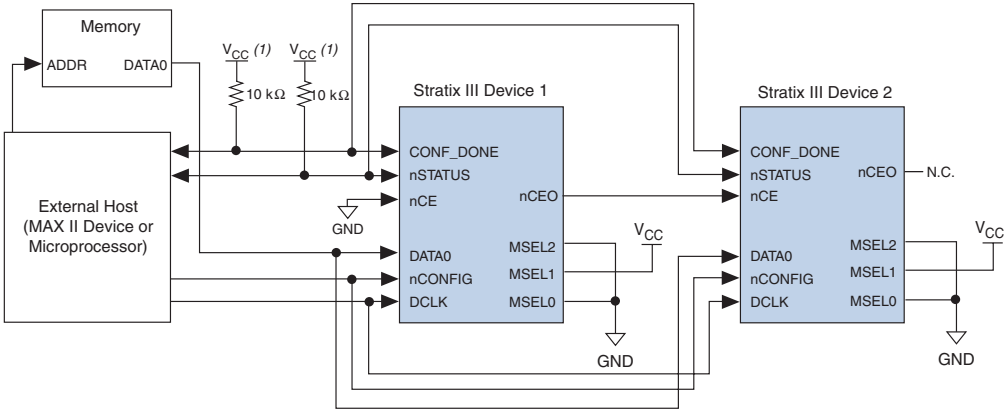
The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE have not gone high, the MAX II device must reconfigure the target device.

If you use the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, you need to ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 100 ms).

When the device is in user-mode, you can initiate a reconfiguration by transitioning the nCONFIG pin low-to-high. The nCONFIG pin must be low for at least 2 ms. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Once nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

Figure 11–18 shows how to configure multiple devices using a MAX II device. This circuit is similar to the PS configuration circuit for a single device, except Stratix III devices are cascaded for multi-device configuration.

Figure 11–18. Multi-Device PS Configuration Using an External Host



Note to Figure 11–18:

(1) You should connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

In multi-device PS configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS,

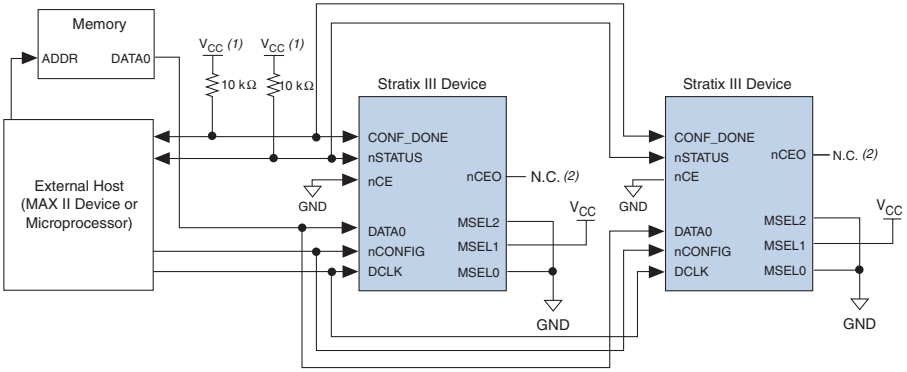
DCLK, DATA0, and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

Since all nSTATUS and CONF_DONE pins are tied together, if any device detects an error, configuration stops for the entire chain and you must reconfigure the entire chain. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (maximum of 100 ms). After all nSTATUS pins are released and pulled high, the MAX II device can try to reconfigure the chain without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 2 ms) on nCONFIG to restart the configuration process.

In your system, you can have multiple devices that contain the same configuration data. To support this configuration scheme, all device nCE inputs are tied to GND, while nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device. Devices must be the same density and package. All devices will start and complete configuration at the same time. Figure 11–19 shows multi-device PS configuration when both Stratix III devices are receiving the same configuration data.

Figure 11–19. Multiple-Device PS Configuration When Both devices Receive the Same Data



Notes to Figure 11–19:

(1) You should connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices are left unconnected when configuring the same configuration data into multiple devices.

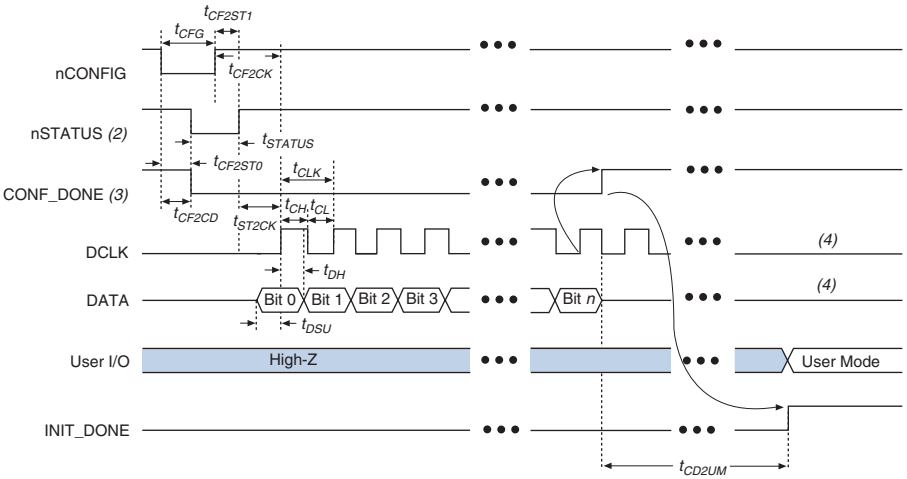
You can use a single configuration chain to configure Stratix III devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time, or that an error flagged by one device initiates reconfiguration in all devices, all of the device CONF_DONE and nSTATUS pins must be tied together.

For more information on configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera device Chains* chapter in the *Configuration Handbook*.

PS Configuration Timing

Figure 11–20 shows the timing waveform for PS configuration when using a MAX II device as an external host.

Figure 11–20. PS Configuration Timing Waveform (1)



Notes to Figure 11–20:

(1) The beginning of this waveform shows the device in user-mode. In user-mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
(2) Upon power-up, the Stratix III device holds nSTATUS low for the time of the POR delay.
(3) Upon power-up, before and during configuration, CONF_DONE is low.
(4) You should not leave DCLK floating after configuration. You should drive it high or low, whichever is more convenient. DATA[0] is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

Table 11–10 defines the timing parameters for Stratix III devices for PS configuration.

Table 11–10. PS Timing Parameters for Stratix III Devices Note (1) (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	800	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	800	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	10	100 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	100 (2)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	100	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	0	—	ns

Table 11–10. PS Timing Parameters for Stratix III Devices Note (1) (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CH}	DCLK high time	4	—	ns
t_{CL}	DCLK low time	4	—	ns
t_{CLK}	DCLK period	10	—	ns
f_{MAX}	DCLK frequency	—	100	MHz
t_R	Input rise time	—	40	ns
t	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode *(3)*	20	100	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (4,436 × CLKUSR period)	—	—

Notes to Table 11–10:

(1) This information is preliminary.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for starting the device.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* chapter in volume 2 of the *Configuration Handbook*.

An example PS design that uses a MAX II device as the external host for configuration will be available when the devices are available.

PS Configuration Using a Microprocessor

In this PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Stratix III device.

All information in the "PS Configuration Using a MAX II Device as an External Host" section is also applicable when using a microprocessor as an external host. Refer to that section for all configuration and timing information.

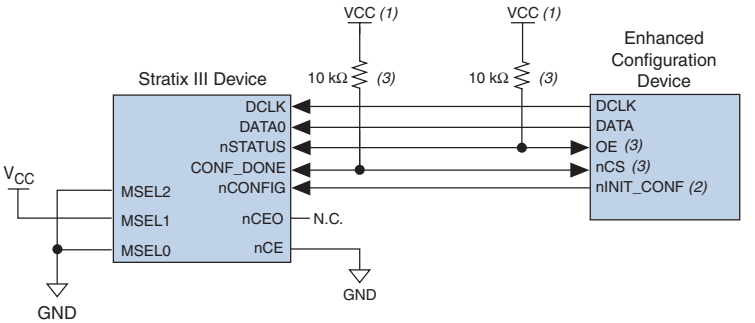
PS Configuration Using a Configuration Device

You can use an Altera enhanced configuration device to configure Stratix III devices using a serial configuration bitstream. Configuration data is stored in the configuration device. Figure 11–21 shows the configuration interface connections between a Stratix III device and a configuration device.

The figures in this chapter only show the configuration-related pins and the configuration pin connections between the configuration device and the device.

For more information on the enhanced configuration device and flash interface pins (such as PGM[2..0], EXCLK, PORSEL, A[20..0], and DQ[15..0]), refer to the *Enhanced Configuration Devices* (*EPC4*, *EPC8*, *and EPC16*) *Data Sheet* in volume 2 of the *Configuration Handbook*.

Figure 11–21. Single Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 11–21:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-ups on configuration device** option when generating programming files.

You can find the value of the internal pull-up resistors on enhanced configuration devices in the Operating Conditions table of the *Enhanced Configuration Devices* (*EPC4, EPC8, and EPC16*) D*ata Sheet*.

When using enhanced configuration devices, you can connect nCONFIG of the device to nINIT_CONF of the configuration device, which allows the INIT_CONF JTAG instruction to initiate device configuration. You do not need to connect the nINIT_CONF pin if its functionality is not used. An internal pull-up resistor on the nINIT_CONF pin is always active in the enhanced configuration devices, which means you should not use an external pull-up resistor if nCONFIG is tied to nINIT_CONF.

Upon power-up, the Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. If PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS low, and tri-state all user I/O pins. The configuration device also goes through a POR delay to allow the power supply to stabilize. You can set the POR time for enhanced configuration devices to either 100 ms or 2 ms, depending on its PORSEL pin setting. If the PORSEL pin is connected to GND, the POR delay is 100 ms. If the PORSEL pin is connected to V_{CC}, the POR delay is 2 ms. During this time, the configuration device drives its OE pin low. This low signal delays configuration because the OE pin is connected to the target device's nSTATUS pin.

When selecting a POR time, you need to ensure that the device completes power-up before the enhanced configuration device exits POR. Altera recommends that you choose a POR time for the Stratix III device of 12 ms, while selecting a POR time for the enhanced configuration device of 100 ms.

When both devices complete POR, they release their open-drain OE or nSTATUS pin, which is then pulled high by a pull-up resistor. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

When the power supplies have reached the appropriate operating voltages, the target device senses the low-to-high transition on nCONFIG and initiates the configuration cycle. The configuration cycle consists of three stages: reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. You can delay the beginning of configuration by holding the nCONFIG or nSTATUS pin low.

To begin configuration, power the V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} voltages (for the banks where the configuration and JTAG pins reside) to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the nSTATUS pin, which is pulled high by a pull-up resistor. Enhanced configuration devices have an optional internal pull-up resistor on the OE pin. This option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you do not use this internal pull-up resistor, an external 10-kΩ pull-up resistor on the OE-nSTATUS line is required. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins.

When nSTATUS is pulled high, OE of the configuration device also goes high and the configuration device clocks data out serially to the device using the Stratix III device's internal oscillator. The Stratix III devices receive configuration data on the DATA0 pin and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK.

After the device has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by a pull-up resistor. Since CONF_DONE is tied to the configuration device's nCS pin, the configuration device is disabled when CONF_DONE goes high. Enhanced configuration devices have an optional internal pull-up resistor on the nCS pin. This option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If this internal pull-up resistor is not used, an external 10-kΩpull-up resistor on the nCS-CONF_DONE line is required. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin.

In Stratix III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If you are using an internal oscillator, the Stratix III device supplies itself with enough clock cycles for proper initialization. You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. You can turn on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. Supplying a clock on CLKUSR will not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, CLKUSR will be enabled after the time specified as t_{CD2CU}. After this time period elapses, the Stratix III devices require 4,436 clock cycles to initialize properly and enter user mode. Stratix III devices support a CLKUSR f_{MAX} of 100 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device and Pin Options** dialog box. If you are using the INIT_DONE pin, it will be high due to an external 10-kΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. In user-mode, the user I/O pins will no longer have weak pull-up resistors and will function as assigned in your design. Enhanced configuration devices drive DCLK low and DATA0 high at the end of configuration.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. Since the nSTATUS pin is tied to OE, the configuration device will also be reset. If the **Auto-restart configuration after error** option, available in the Quartus II software, from the **General** tab of the **Device and Pin Options** dialog box, is turned on, the device automatically initiates reconfiguration if an error occurs. The Stratix III devices release the nSTATUS pin after a reset time-out period (maximum of 100 ms). When the nSTATUS pin is released and pulled high by a pull-up resistor, the configuration device reconfigures the chain. If this option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 ms to restart configuration. The external system can pulse nCONFIG if nCONFIG is under system control rather than tied to V_{CC}.

In addition, if the configuration device sends all of its data and then detects that CONF_DONE has not gone high, it recognizes that the device has not configured successfully. Enhanced configuration devices wait for 64 DCLK cycles after the last configuration bit was sent for CONF_DONE to reach a high state. In this case, the configuration device pulls its OE pin low, driving the target device's nSTATUS pin low. If the **Auto-restart configuration after error** option is set in the software, the target device resets and then releases its nSTATUS pin after a reset time-out period (maximum of 100 ms). When nSTATUS returns to a logic high level, the configuration device tries to reconfigure the device.

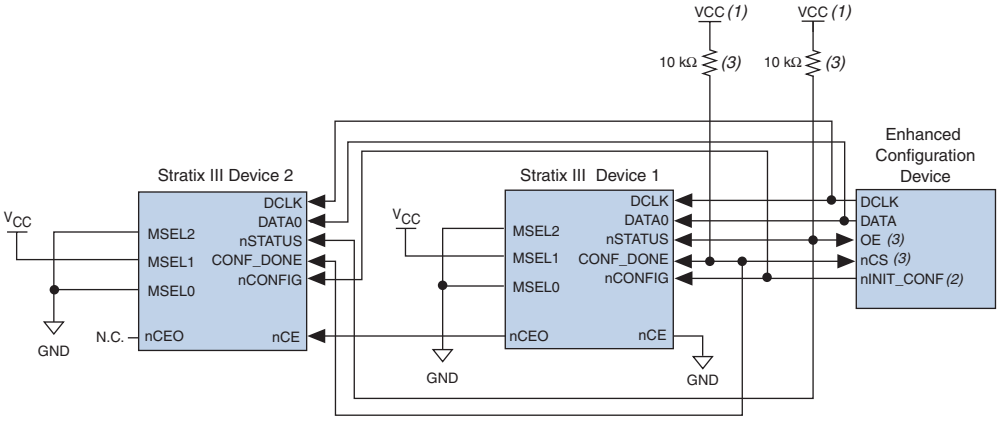
When CONF_DONE is sensed low after configuration, the configuration device recognizes that the target device has not configured successfully. Therefore, your system should not pull CONF_DONE low to delay initialization. Instead, use the CLKUSR option to synchronize the initialization of multiple devices that are not in the same configuration chain. Devices in the same configuration chain will initialize together if their CONF_DONE pins are tied together.

If you are using the optional CLKUSR pin and nCONFIG is pulled low to restart configuration during device initialization, you need to ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 100ms).

When the device is in user-mode, pulling the nCONFIG pin low initiates a reconfiguration. The nCONFIG pin should be low for at least 2 ms. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. Because CONF_DONE is pulled low, this activates the configuration device because it sees its nCS pin drive low. Once nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

Figure 11–22 shows how to configure multiple devices with an enhanced configuration device. This circuit is similar to the configuration device circuit for a single device, except Stratix III devices are cascaded for multi-device configuration.

Figure 11–22. Multi-Device PS Configuration Using an Enhanced Configuration Device



Notes to Figure 11–22:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-ups on configuration device** option when generating programming files.

You cannot cascade enhanced configuration devices.

When performing multi-device configuration, you must generate the configuration device's POF from each project's SOF. You can combine multiple SOFs using the **Convert Programming Files** window in the Quartus II software.

For more information on how to create configuration files for multi-device configuration chains, refer to the *Software Settings* chapter of the *Configuration Handbook*.

In multi-device PS configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, prompting the second device to begin configuration. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device.

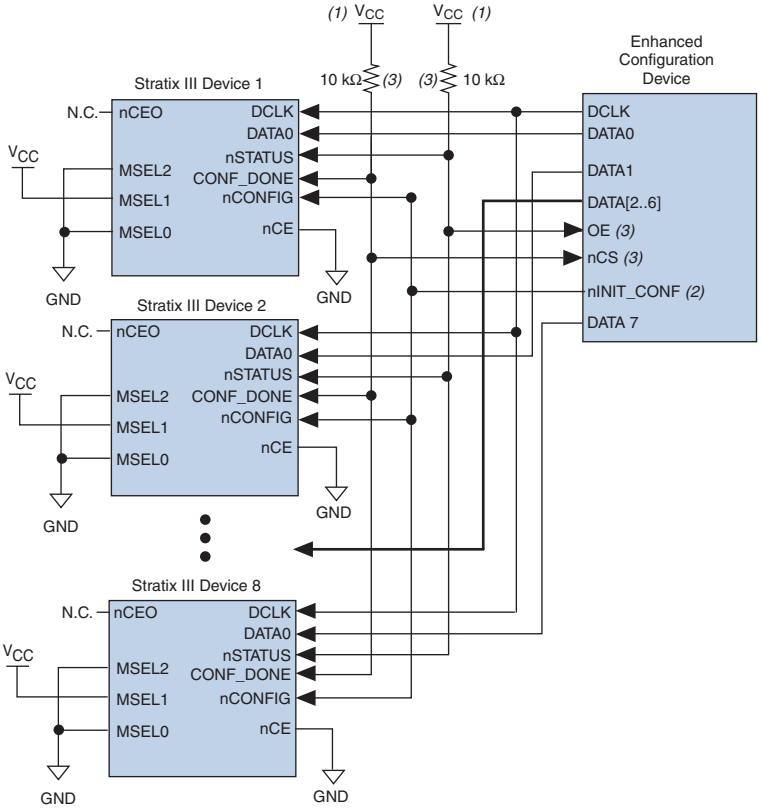
When configuring multiple devices, configuration does not begin until all devices release their OE or nSTATUS pins. Similarly, since all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

Since all nSTATUS and CONF_DONE pins are tied together, if any device detects an error, configuration stops for the entire chain and you must reconfigure the entire chain. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This low signal drives the OE pin low on the enhanced configuration device and drives nSTATUS low on all devices, causing them to enter a reset state. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices will automatically initiate reconfiguration if an error occurs. The devices will release their nSTATUS pins after a reset time-out period (maximum of 100 ms). When all the nSTATUS pins are released and pulled high, the configuration device tries to reconfigure the chain. If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 2 ms to restart configuration. The external system can pulse nCONFIG if nCONFIG is under system control rather than tied to V_{CC}.

The enhanced configuration devices also support parallel configuration of up to eight devices. The n-bit (= 1, 2, 4, or 8) PS configuration mode allows enhanced configuration devices to concurrently configure devices or a chain of devices. In addition, these devices do not have to be the same device family or density as they can be any combination of Altera devices. An individual enhanced configuration device DATA line is available for each targeted device. Each DATA line can also feed a daisy chain of devices. Figure 11–23 shows how to concurrently configure multiple devices using an enhanced configuration device.

Figure 11–23. Concurrent PS Configuration of Multiple Devices Using an Enhanced Configuration Device



Notes to Figure 11–23:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you have to pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS and OE pull-ups on configuration device** option when generating programming files.

The Quartus II software only allows the selection of n-bit PS configuration modes, where n must be 1, 2, 4, or 8. However, you can use these modes to configure any number of devices from 1 to 8. When configuring SRAM-based devices using n-bit PS modes, use Table 11–11 to select the appropriate configuration mode for the fastest configuration times.

Table 11–11. Recommended Configuration Using n-Bit PS Modes Note (1)

Number of Devices	Recommended Configuration Mode
1	1-bit PS
2	2-bit PS
3	4-bit PS
4	4-bit PS
5	8-bit PS
6	8-bit PS
7	8-bit PS
8	8-bit PS

Note to Table 11–11:

(1) Assume that each DATA line is only configuring one device, not a daisy chain of devices.

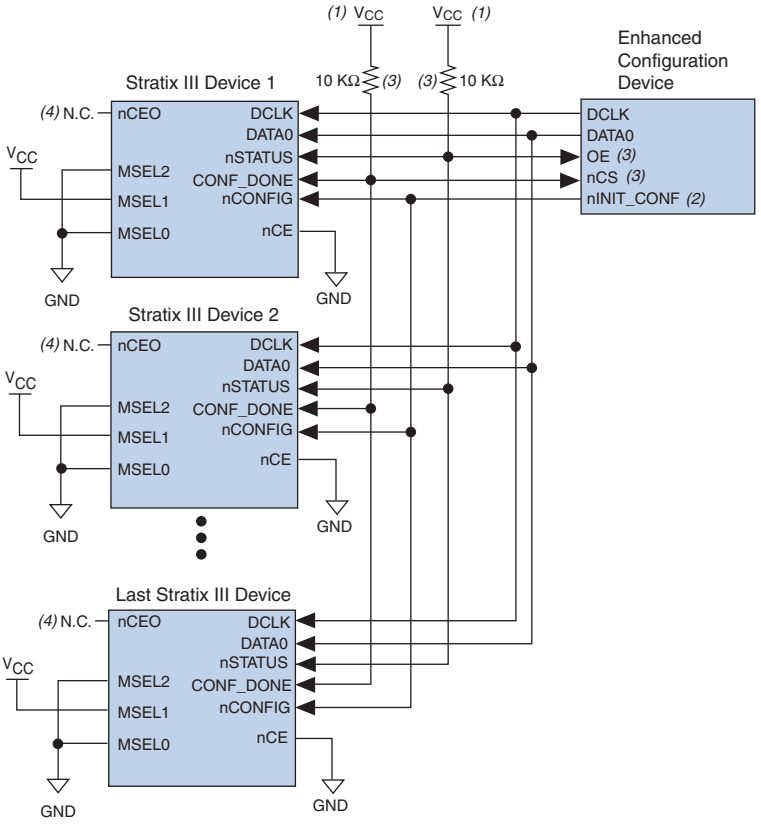
For example, if you configure three devices, you would use the 4-bit PS mode. For the DATA0, DATA1, and DATA2 lines, the corresponding SOF data is transmitted from the configuration device to the device. For DATA3, you can leave the corresponding Bit3 line blank in the Quartus II software. On the PCB, leave the DATA3 line from the enhanced configuration device unconnected.

Alternatively, you can daisy chain two devices to one DATA line while the other DATA lines drive one device each. For example, you could use the 2-bit PS mode to drive two devices with DATA Bit0 (two EP3SL50 devices) and the third device (EP3SL70 device) with DATA Bit1. This 2-bit PS configuration scheme requires less space in the configuration flash memory, but can increase the total system configuration time.

A system may have multiple devices that contain the same configuration data. To support this configuration scheme, all device nCE inputs are tied to GND, while nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered for every fourth device. Devices must be the same density and package. All devices will start and complete

configuration at the same time. Figure 11–24 shows multi-device PS configuration when the Stratix III devices are receiving the same configuration data.

Figure 11–24. Multiple-Device PS Configuration Using an Enhanced Configuration Device When devices Receive the Same Data



Notes to Figure 11–24:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) The nINIT_CONF pin is available on enhanced configuration devices and has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(3) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-ups on configuration device** option when generating programming files.

(4) The nCEO pins of all devices are left unconnected when configuring the same configuration data into multiple devices.

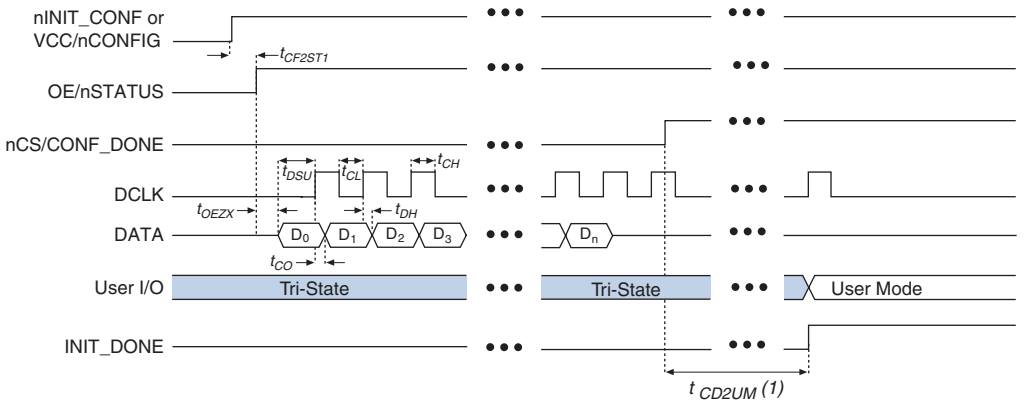
You cannot cascade enhanced configuration devices.

You can use a single configuration chain to configure Stratix III devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time, or that an error flagged by one device initiates reconfiguration in all devices, all of the device CONF_DONE and nSTATUS pins must be tied together.

For more information on configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera Device Chains* chapter in the *Configuration Handbook*.

Figure 11–25 shows the timing waveform for the PS configuration scheme using a configuration device.

Figure 11–25. Stratix III PS Configuration Using a Configuration Device Timing Waveform



Note to Figure 11–25:
(1) The initialization clock can come from the Stratix III device's internal oscillator or the CLKUSR pin.

For timing information, refer to the *Enhanced Configuration Devices (EPC4, EPC8 and EPC16) Data Sheet* or the *Configuration Devices for SRAM-Based LUT Devices Data Sheet* in the *Configuration Handbook*.

Device configuration options and how to create configuration files are discussed further in the *Software Settings* chapter of the *Configuration Handbook*.

PS Configuration Using a Download Cable

In this section, the generic term "download cable" includes the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial / USB communications cable, ByteBlaster II parallel port download cable, ByteBlaster MV™ parallel port download cable, and the EthernetBlaster™ download cable.

In PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device via the USB Blaster, MasterBlaster, ByteBlaster II, EthernetBlaster, or ByteBlasterMV cable.

Upon power-up, the Stratix III devices go through a POR. The POR delay is dependent on the PORSEL pin setting. When PORSEL is driven low, the POR time is approximately 100 ms. If PORSEL is driven high, the POR time is approximately 12 ms. During POR, the device will reset, hold nSTATUS low, and tri-state all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. If nIO_pullup is driven low during power-up and configuration, the user I/O pins and dual-purpose I/O pins will have weak pull-up resistors which are on (after POR) before and during configuration. If nIO_pullup is driven high, the weak pull-up resistors are disabled.

The configuration cycle consists of three stages: reset, configuration and initialization. While nCONFIG or nSTATUS are low, the device is in reset. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the nCONFIG pin.

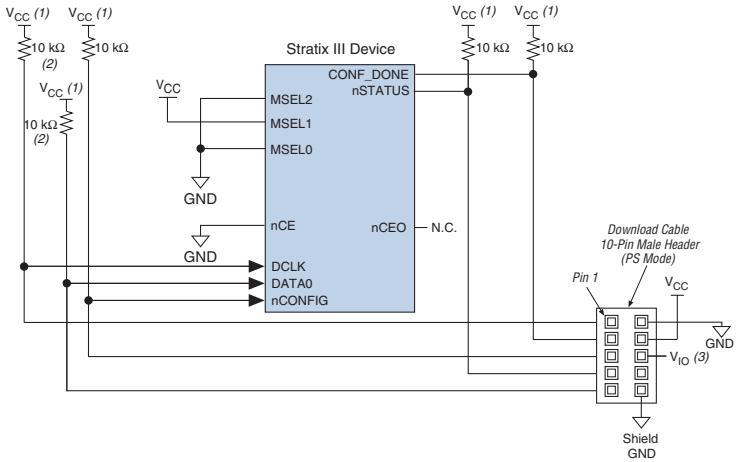
To begin configuration, power the V_{CC}, V_{CCIO}, V_{CCPGM}, and V_{CCPD} voltages (for the banks where the configuration and JTAG pins reside) to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-kΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. The programming hardware or download cable then places the configuration data one bit at a time on the device's DATA0 pin. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize.

When using a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs. Additionally, the **Enable user-supplied start-up clock** (**CLKUSR**) option has no affect on the device initialization since this

option is disabled in the SOF when programming the device using the Quartus II programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not need to provide a clock on CLKUSR when you are configuring the device with the Quartus II programmer and a download cable. Figure 11–26 shows PS configuration for Stratix III devices using a USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cable.

Figure 11–26. PS Configuration Using a USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV Cable



Notes to Figure 11–26:

(1) You should connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (V_{IO} pin), ByteBlaster II, or ByteBlasterMV cable.

(2) You only need the pull-up resistors on DATA0 and DCLK if the download cable is the only configuration scheme used on your board. This ensures that DATA0 and DCLK are not left floating after configuration. For example, if you are also using a configuration device, you do not need the pull-up resistors on DATA0 and DCLK.

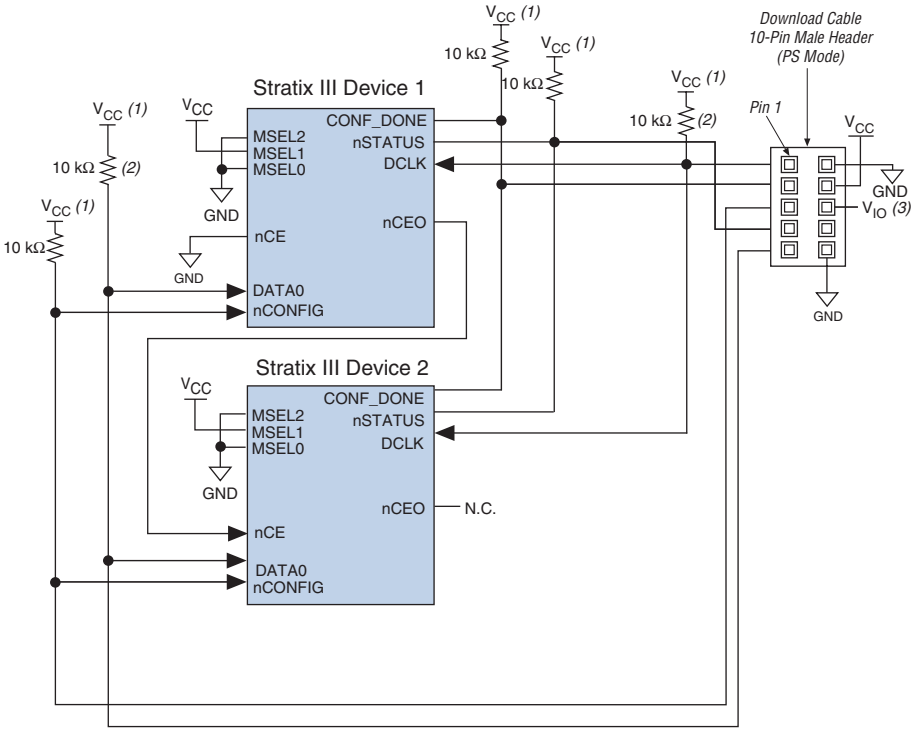
(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for active serial programming, otherwise it is a no connect.

You can use a download cable to configure multiple Stratix III devices by connecting each device's nCEO pin to the subsequent device's nCE pin. The first device's nCE pin is connected to GND while its nCEO pin is connected to the nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) are connected to every device in the chain. Because all CONF_DONE pins are tied together, all devices in the chain initialize and enter user mode at the same time.

In addition, because the nSTATUS pins are tied together, the entire chain halts configuration if any device detects an error. The **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs.

Figure 11–27 shows how to configure multiple Stratix III devices with a download cable.

Figure 11–27. Multi-Device PS Configuration using a USB Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV Cable



Notes to Figure 11–27:

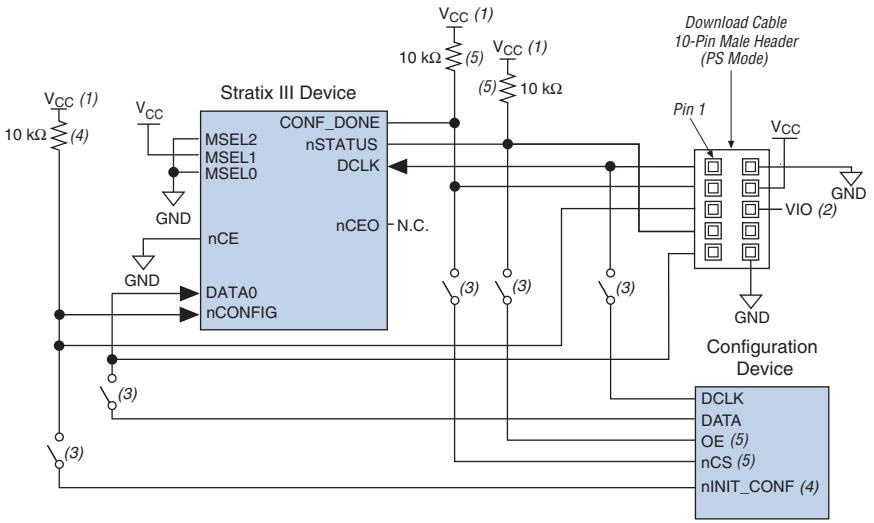
(1) You should connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (V_{IO} pin), ByteBlaster II, or ByteBlasterMV cable.

(2) You only need the pull-up resistors on DATA0 and DCLK if the download cable is the only configuration scheme used on your board. This is to ensure that DATA0 and DCLK are not left floating after configuration. For example, if you are also using a configuration device, you do not need the pull-up resistors on DATA0 and DCLK.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for active serial programming, otherwise it is a no connect.

If you are using a download cable to configure device(s) on a board that also has configuration devices, electrically isolate the configuration device from the target device(s) and cable. One way of isolating the configuration device is to add logic, such as a multiplexer, that can select between the configuration device and the cable. The multiplexer chip allows bidirectional transfers on the nSTATUS and CONF_DONE signals. Another option is to add switches to the five common signals (nCONFIG, nSTATUS, DCLK, DATA0, and CONF_DONE) between the cable and the configuration device. The last option is to remove the configuration device from the board when configuring the device with the cable. Figure 11–28 shows a combination of a configuration device and a download cable to configure the Stratix III device.

Figure 11–28. PS Configuration with a Download Cable and Configuration Device Circuit



Notes to Figure 11–28:

(1) You should connect the pull-up resistor to the same supply voltage as the configuration device.

(2) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for active serial programming, otherwise it is a no connect.

(3) You should not attempt configuration with a download cable while a configuration device is connected to a Stratix III device. Instead, you should either remove the configuration device from its socket when using the download cable or place a switch on the five common signals between the download cable and the configuration device.

(4) The nINIT_CONF pin (available on enhanced configuration devices only) has an internal pull-up resistor that is always active. This means you should not use an external pull-up resistor on the nINIT_CONF–nCONFIG line. You do not need to connect the nINIT_CONF pin if its functionality is not used. If you do not use nINIT_CONF, you must pull nCONFIG to V_{CC} through a 10-kΩ resistor.

(5) The enhanced configuration devices' OE and nCS pins have internal programmable pull-up resistors. If you use internal pull-up resistors, you should not use external pull-up resistors on these pins. The internal pull-up resistors are used by default in the Quartus II software. To turn off the internal pull-up resistors, check the **Disable nCS** and **OE pull-up resistors on configuration device** option when generating programming files.

For more information on how to use the USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cables, refer to the following data sheets:

- *USB Blaster USB Port Download Cable Data Sheet*
- *MasterBlaster Serial/USB Communications Cable Data Sheet*
- *ByteBlaster II Parallel Port Download Cable Data Sheet*
- *ByteBlasterMV Parallel Port Download Cable Data Sheet*

JTAG Configuration

The JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into the device. The Quartus II software automatically generates SOFs that can be used for JTAG configuration with a download cable in the Quartus II software programmer.

For more information on JTAG boundary-scan testing and commands available using Stratix III devices, refer to the following documents:

- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Stratix III Devices* chapter of the *Stratix III Device Handbook*
- *Jam Programming and Testing Language Specification*

Stratix III devices are designed such that JTAG instructions have precedence over any device configuration modes. Therefore, JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Stratix III devices during PS configuration, PS configuration is terminated and JTAG configuration begins.

You cannot use the Stratix III decompression or design security features if you are configuring your Stratix III device when using JTAG-based configuration.

A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have weak internal pull-up resistors (typically 25 kΩ). JTAG output pin TDO and all JTAG input pins are powered by the 2.5 V / 3.0 V V_{CCPD}. All the JTAG pins support only LVTTL I/O standard.

All user I/O pins are tri-stated during JTAG configuration. Table 11–12 explains each JTAG pin's function.

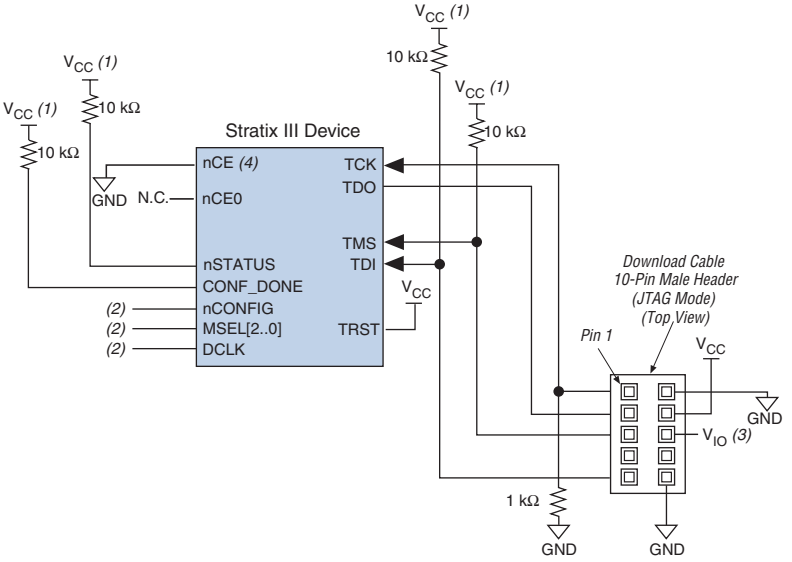
The TDO output is powered by the V_{CCPD} power supply of I/O bank 1A. For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* Chapter of the *Stratix III Device Handbook*.

Table 11–12. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in the rising edge of TCK. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, you must set up TMS before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to V_{CC}.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge while others occur at the falling edge. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to GND.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. The TRST pin is optional according to IEEE Std. 1149.1. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to GND.

During JTAG configuration, you can download data to the device on the PCB through the USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV download cable. Configuring devices through a cable is similar to programming devices in-system, except you should connect the TRST pin to V_{CC}. This ensures that the TAP controller is not reset. Figure 11–29 shows JTAG configuration of a single Stratix III device.

Figure 11–29. JTAG Configuration of a Single Device Using a Download Cable



Notes to Figure 11–29:

(1) You should connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (V_{IO} pin), ByteBlaster II, or ByteBlasterMV cable. The voltage supply can be connected to the V_{CCPD} of the device.

(2) You should connect the nCONFIG and MSEL[2..0] pins to support a non-JTAG configuration scheme. If you only use the JTAG configuration, connect nCONFIG to V_{CC}, and MSEL[2..0] to ground. Pull DCLK either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for active serial programming, otherwise it is a no connect.

(4) You must connect nCE to GND or driven low for successful JTAG configuration.

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the TDI pin to the TDO pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the TDO pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the state of CONF_DONE through the JTAG port. When Quartus II generates a JAM file (**.jam)** for a multi-device chain, it contains instructions so that all the devices in the chain will be initialized at the same time. If CONF_DONE is not high, the Quartus II software indicates that configuration has failed.

If CONF_DONE is high, the software indicates that configuration was successful. After the configuration bitstream is transmitted serially via the JTAG TDI port, the TCK port is clocked an additional 1,094 cycles to perform device initialization.

Stratix III devices have dedicated JTAG pins that always function as JTAG pins. Not only can you perform JTAG testing on Stratix III devices before and after, but also during configuration. While other device families do not support JTAG testing during configuration, Stratix III devices support the bypass, id code, and sample instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the CONFIG_IO instruction.

The CONFIG_IO instruction allows I/O buffers to be configured via the JTAG port and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Stratix III device or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG testing is complete, you must reconfigure the part via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Stratix III devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Stratix III devices, consider the dedicated configuration pins. Table 11–13 shows how these pins should be connected during JTAG configuration.

Table 11–13. Dedicated Configuration Pin Connections During JTAG Configuration (Part 1 of 2)

Signal	Description
nCE	On all Stratix III devices in the chain, nCE should be driven low by connecting it to ground, pulling it low via a resistor, or driving it by some control circuitry. For devices that are also in multi-device FPP, AS, or PS configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Stratix III devices in the chain, you can leave nCEO floating or connected to the nCE of the next device.
MSEL	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If you only use JTAG configuration, tie these pins to ground.

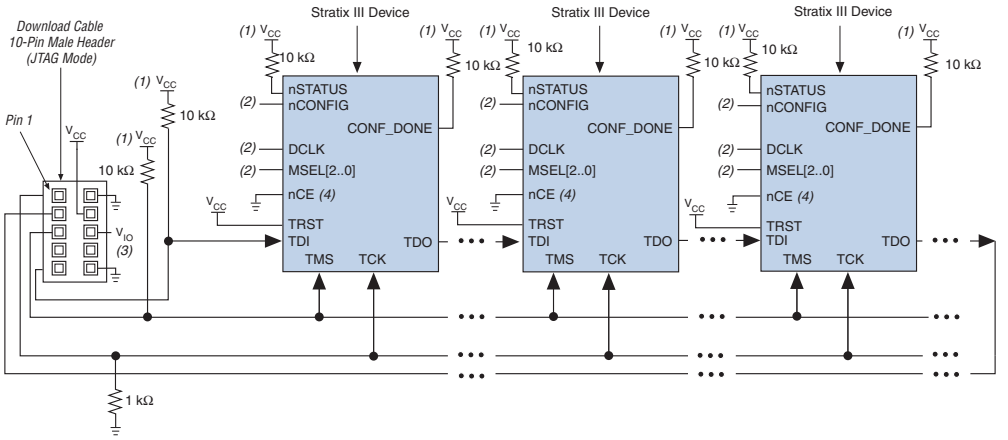
Table 11–13. Dedicated Configuration Pin Connections During JTAG Configuration (Part 2 of 2)

Signal	Description
nCONFIG	Driven high by connecting to V_{CC}, pulling up via a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CC} individually.
CONF_DONE	Pull to V_{CC} via a 10-kΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CC} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 11–30 shows multi-device JTAG configuration.

Figure 11–30. JTAG Configuration of Multiple Devices Using a Download Cable



Notes to Figure 11–30:

(1) You should connect the pull-up resistor to the same supply voltage as the USB Blaster, MasterBlaster (V_{IO} pin), ByteBlaster II, or ByteBlasterMV cable.

(2) You should connect the nCONFIG, MSEL[2..0] pins to support a non-JTAG configuration scheme. If you only use JTAG configuration, connect nCONFIG to V_{CC}, and MSEL[2..0] to ground. Pull DCLK either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCIO}. Refer to the *MasterBlaster Serial/USB Communications Cable Data Sheet* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB Blaster and ByteBlaster II cables, this pin is connected to nCE when it is used for active serial programming, otherwise it is a no connect.

(4) You must connect nCE to GND or driven low for successful JTAG configuration.

You must connect the nCE pin to GND or driven low during JTAG configuration. In multi-device FPP, AS, and PS configuration chains, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. In addition, the CONF_DONE and nSTATUS signals are all shared in multi-device FPP, AS, or PS configuration chains so the devices can enter user mode at the same time after configuration is complete. When the CONF_DONE and nSTATUS signals are shared among all the devices, you must configure every device when JTAG configuration is performed.

If you only use JTAG configuration, Altera recommends that you connect the circuitry as shown in Figure 11–30, where each of the CONF_DONE and nSTATUS signals are isolated, so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, make sure the nCE pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the nCEO of the previous device will drive the nCE of the next device low when it has successfully been JTAG configured.

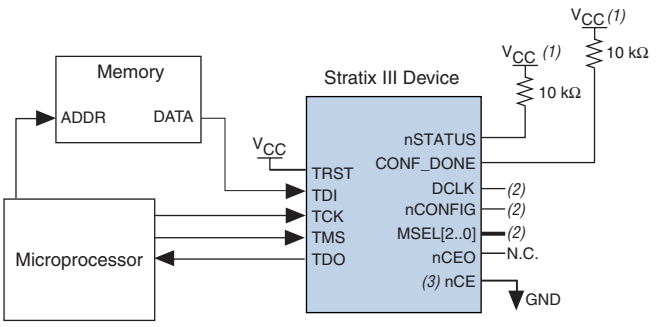
You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

JTAG configuration support has been enhanced and allows more than 17 Stratix III devices to be cascaded in a JTAG chain.

For more information on configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera Device Chains* chapter in the *Configuration Handbook*.

Figure 11–31 shows JTAG configuration of a Stratix III device with a microprocessor.

Figure 11–31. JTAG Configuration of a Single Device Using a Microprocessor



Notes to Figure 11–31:

(1) You should connect the pull-up resistor to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device.

(2) You should connect the nCONFIG and MSEL[2..0] pins to support a non-JTAG configuration scheme. If you use only the JTAG configuration, connect nCONFIG to V_{CC}, and MSEL[2..0] to ground. Pull DCLK either high or low, whichever is convenient on your board.

(3) You must connect nCE to GND or driven low for successful JTAG configuration.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard.

The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information on JTAG and Jam STAPL in embedded environments, refer to *AN 122: Using Jam STAPL for ISP and ICR via an Embedded Processor*. To download the jam player, visit the Altera web site at **www.altera.com**

Device Configuration Pins

The following tables describe the connections and functionality of all the configuration-related pins on the Stratix III devices. Table 11–14 summarizes the Stratix III configuration pins and their power supply.

Table 11–14. Stratix III Configuration Pin Summary Note (1) (Part 1 of 2)

Description	Input/Output	Dedicated	Powered By	Configuration Mode
TDI	Input	Yes	V_{CCPD}	JTAG
TMS	Input	Yes	V_{CCPD}	JTAG
TCK	Input	Yes	V_{CCPD}	JTAG
TRST	Input	Yes	V_{CCPD}	JTAG
TDO	Output	Yes	V_{CCPD}	JTAG
CRC_ERROR	Output	—	Pull-up	Optional, all modes
DATA0	Input	—	V_{CCPGM}/V_{CCIO}	All modes except JTAG
DATA[7..1]	Input	—	V_{CCPGM}/V_{CCIO}	FPP
INIT_DONE	Output	—	Pull-up	Optional, all modes
CLKUSR	Input	—	V_{CCPGM}/V_{CCIO}	Optional
nSTATUS	Bidirectional	Yes	Pull-up	All modes
nCE	Input	Yes	V_{CCPGM}	All modes
CONF_DONE	Bidirectional	Yes	Pull-up	All modes
nCONFIG	Input	Yes	V_{CCPGM}	All modes
PORSEL	Input	Yes	V_{CC}	All modes
ASDO	Output	Yes	V_{CCPGM}	AS

Table 11–14. Stratix III Configuration Pin Summary Note (1) (Part 2 of 2)

Description	Input/Output	Dedicated	Powered By	Configuration Mode
nCSO	Output	Yes	V_{CCPGM}	AS
DCLK	Input	Yes	V_{CCPGM}	PS, FPP
—	Output	—	V_{CCPGM}	AS
nIO_PULLUP	Input	Yes	V_{CC}	All modes
nCEO	Output	Yes	V_{CCPGM}	All modes
MSEL[2..0]	Input	Yes	V_{CC}	All modes

Note to Table 11–14:
(1) The total number of pins is 30; the total number of dedicated pins is 19.

Table 11–15 describes the dedicated configuration pins, which are required to be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration schemes.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 1 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
V_{CCPGM}	N/A	All	Power	Dedicated power pin. Use this pin to power all dedicated configuration inputs, dedicated configuration outputs, dedicated configuration bi-direction pins, and some of the dual functional pins that are used for configuration. You must connect this pin to 1.8-V, 2.5-V, or 3.0-V. V_{CCPGM} and must ramp-up from 0-V to 3.0-V within 100 ms. If V_{CCPGM} is not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow for a V_{CCPGM} ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.
V_{CCPD}	N/A	All	Power	Dedicated power pin. Use this pin to power the I/O pre-drivers, the JTAG input and output pins, and the design security circuitry. You must connect this pin to 2.5-V or 3.0-V depending on the I/O standards selected. For 3.0-V I/O standards, V_{CCPD} = 3.0 V; for 2.5-V or below I/O standards, V_{CCPD} = 2.5 V. V_{CCPD} must ramp-up from 0-V to 2.5-V / 3.0-V within 100 ms. If V_{CCPD} is not ramped up within this specified time, your Stratix III device will not configure successfully. If your system does not allow for a V_{CCPD} ramp-up time of 100 ms or less, you must hold nCONFIG low until all power supplies are stable.
PORSEL	N/A	All	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.8 V, 2.5 V, 3.0 V) selects a POR time of approximately 12 ms and a logic low selects POR time of approximately 100 ms. The PORSEL input buffer is powered by V_{CC} and has an internal 5-kΩ pull-down resistor that is always active. You should tie the PORSEL pin directly to V_{CCPGM} or GND.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 2 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nIO_PULLUP	N/A	All	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins and dual-purpose I/O pins (nCSO, nASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CLKUSR, INIT_DONE) are on or off before and during configuration. A logic high (1.8 V, 2.5 V, 3.0 V) turns off the weak internal pull-up resistors, while a logic low turns them on. The nIO–PULLUP input buffer is powered by V_{CC} and has an internal 5-kΩ pull-down resistor that is always active. You can tie the nIO–PULLUP directly to V_{CCPGM} or use a 1-kΩ pull-up resistor or tie it directly to GND.
MSEL[2..0]	N/A	All	Input	3-bit configuration input that sets the Stratix III device configuration scheme. Refer to Table 11–1 for the appropriate connections. You must hard-wire these pins to V_{CCPGM} or GND. The MSEL[2..0] pins have internal 5-kΩ pull-down resistors that are always active.
nCONFIG	N/A	All	Input	Configuration control input. Pulling this pin low during user-mode will cause the device to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate a reconfiguration. Configuration is possible only if this pin is high, except in JTAG programming mode when nCONFIG is ignored. If your configuration scheme uses an enhanced configuration device, you can tie nCONFIG to V_{CCPGM} through a 10-kΩ resistor to the configuration device's nINIT_CONF pin.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 3 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSTATUS	N/A	All	Bidirectional open-drain	The device drives nSTATUS low immediately after power-up and releases it after the POR time. During user mode and regular configuration, this pin is pulled high by an external 10-kΩ resistor. This pin, when driven low by Stratix III, indicates that the device is being initialized and has encountered an error during configuration. Status output. If an error occurs during configuration, nSTATUS is pulled low by the target device. Status input. If an external source drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device. If you use a configuration device, driving nSTATUS low will cause the configuration device to attempt to configure the device, but since the device ignores transitions on nSTATUS in user-mode, the device does not reconfigure. To initiate a reconfiguration, nCONFIG must be pulled low. The enhanced configuration devices' OE and nCS pins have optional internal programmable pull-up resistors. If you use internal pull-up resistors on the enhanced configuration device, you should not use external 10-kΩ pull-up resistors on these pins.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 4 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
nSTATUS (continued)	—	—	—	If V_{CCPGM} and V_{CCIO} are not fully powered up, the following could occur: ■ V_{CCPGM} and V_{CCIO} are powered high enough for the nSTATUS buffer to function properly, and nSTATUS is driven low. When V_{CCPGM} and V_{CCIO} are ramped up, POR trips and nSTATUS is released after POR expires. ■ V_{CCPGM} and V_{CCIO} are not powered high enough for the nSTATUS buffer to function properly. In this situation, nSTATUS might appear logic high, triggering a configuration attempt that would fail because POR did not yet trip. When V_{CCPD} and V_{CCIO} are powered up, nSTATUS is pulled low because POR did not yet trip. When POR trips after V_{CCPGM} and V_{CCIO} are powered up, nSTATUS is released and pulled high. At that point, reconfiguration is triggered and the device is configured.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 5 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	Status output. The target device drives the CONF_DONE pin low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-kΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device. The enhanced configuration devices' OE and nCS pins have optional internal programmable pull-up resistors. If you use internal pull-up resistors on the enhanced configuration device, you should not use external 10-kΩ pull-up resistors on these pins.
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user mode. In single device configuration, it should be tied low. In multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the device.
nCEO	N/A	All	Output	Output that drives low when device configuration is complete. In single device configuration, this pin is left floating. In multi-device configuration, this pin feeds the next device's nCE pin. The nCEO of the last device in the chain is left floating. The nCEO pin is powered by V_{CCPGM}.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 6 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
ASDO	N/A in AS mode, I/O in non-AS mode	AS	Output	Control signal from the Stratix III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, ASDO has an internal pull-up resistor that is always active.
nCSO	N/A in AS mode, I/O in non-AS mode	AS	Output	Output control signal from the Stratix III device to the serial configuration device in AS mode that enables the configuration device. In AS mode, nCSO has an internal pull-up resistor that is always active.
DCLK	N/A	Synchronous configuration schemes (PS, FPP, AS)	Input (PS, FPP) Output (AS)	In PS and FPP configuration, DCLK is the clock input used to clock data from an external source into the target device. Data is latched into the device on the rising edge of DCLK. In AS mode, DCLK is an output from the Stratix III device that provides timing for the configuration interface. In AS mode, DCLK has an internal pull-up resistor (typically 25 kΩ) that is always active. After configuration, this pin is tri-stated. In schemes that use a configuration device, DCLK will be driven low after configuration is done. In schemes that use a control host, DCLK should be driven either high or low, whichever is more convenient. Toggling this pin after configuration does not affect the configured device.

Table 11–15. Dedicated Configuration Pins on the Stratix III Device (Part 7 of 7)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DATA0	I/O	PS, FPP, AS	Input	Data input. In serial configuration modes, bit-wide configuration data is presented to the target device on the DATA0 pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings. After configuration, enhanced configuration devices drive this pin high.
DATA[7..1]	I/O	Parallel configuration schemes (FPP)	Inputs	Data inputs. Byte-wide configuration data is presented to the target device on DATA[7..0]. In serial configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..1] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings.

Table 11–16 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 11–16. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. Enable this pin by turning on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Use the Status pin to indicate when the device has initialized and is in user mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-kΩ pull-up resistor. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin is released and pulled high and the device enters user mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. Enable this pin by turning on the **Enable device-wide output enable** (**DEV_OE**) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset** (**DEV_CLRn**) option in the Quartus II software.

Table 11–17 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions. The TDI, TMS, and TRST have weak internal pull-up resistors while TCK has a weak internal pull-down resistor (typically 25 kΩ). If you plan to use the SignalTap® embedded logic array analyzer, you need to connect the JTAG pins of the Stratix III device to a JTAG header on your board.

Table 11–17. Dedicated JTAG Pins

Pin Name	User Mode	Pin Type	Description
TDI	N/A	Input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. The TDI pin is powered by the 2.5-V / 3.0-V V_{CCPD} supply. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to V_{CC}.
TDO	N/A	Output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. The TDO pin is powered by V_{CCPD} For recommendations on connecting a JTAG chain with multiple voltages across the devices in the chain, refer to the chapter *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by leaving this pin unconnected.
TMS	N/A	Input	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. The TMS pin is powered by the 2.5-V / 3.0-V V_{CCPD}. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting this pin to V_{CC}.
TCK	N/A	Input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. The TCK pin is powered by the 2.5-V / 3.0-V V_{CCPD} supply. It is expected that the clock input waveform have a nominal 50% duty cycle. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting TCK to GND.
TRST	N/A	Input	Active-low input to asynchronously reset the boundary-scan circuit. The TRST pin is optional according to IEEE Std. 1149.1. The TRST pin is powered by the 2.5-V / 3.0-V V_{CCPD} supply. You should hold TMS at 1 or you should keep TCK static while TRST is changed from 0 to 1. If the JTAG interface is not required on the board, you can disable the JTAG circuitry by connecting the TRST pin to GND.

Conclusion

You can configure Stratix III devices in a number of different schemes to fit your system's needs. In addition, configuration bitstream encryption, configuration data decompression, and remote system upgrade support supplement the Stratix III configuration solution.

Document Revision History

Table 11–18 shows the revision history for this document.

Table 11–18. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Removed Bank Column from Table 11–14.	—
November 2006 v1.0	Initial Release	—

12. Remote System Upgrades With Stratix III Devices

SIII51012-1.1

Introduction

This chapter describes the functionality and implementation of the dedicated remote system upgrade circuitry. It also defines several concepts related to remote system upgrade, including factory configuration, application configuration, remote update mode, and user watchdog timer. Additionally, this chapter provides design guidelines for implementing remote system upgrades with the supported configuration schemes.

System designers sometimes face challenges such as shortened design cycles, evolving standards, and system deployments in remote locations. Stratix® III devices help overcome these challenges with their inherent re-programmability and dedicated circuitry to perform remote system upgrades. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

Stratix III devices feature dedicated remote system upgrade circuitry. Soft logic (either the Nios® II embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to the Stratix series and helps to avoid system downtime.

Remote system upgrade is supported in fast active serial (AS) Stratix III configuration schemes. You can also implement remote system upgrade in conjunction with advanced Stratix III features such as real-time decompression of configuration data and design security using the advanced encryption standard (AES) for secure and efficient field upgrades. The largest serial configuration device currently supports 64 MBits of configuration bitstream.

Functional Description

The dedicated remote system upgrade circuitry in Stratix III devices manage remote configuration and provides error detection, recovery, and status information. User logic or a Nios II processor implemented in the Stratix III device logic array provides access to the remote configuration data source and an interface to the system's configuration memory.

Stratix III devices have remote system upgrade processes that involves the following steps:

1. A Nios II processor (or user logic) implemented in the Stratix III device logic array receives new configuration data from a remote location. The connection to the remote source uses a communication protocol such as the transmission control protocol / Internet protocol (TCP / IP), peripheral component interconnect (PCI), user datagram protocol (UDP), universal asynchronous receiver / transmitter (UART), or a proprietary interface.

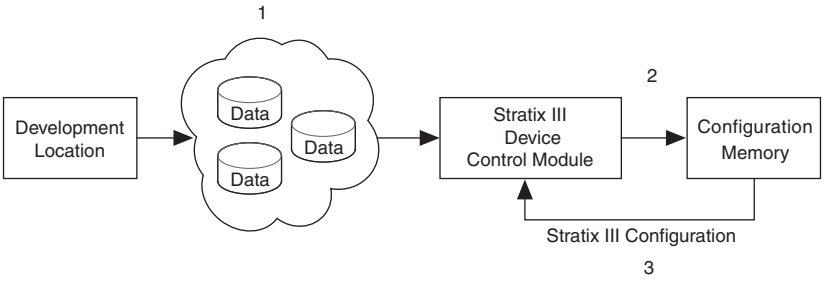
2. The Nios II processor (or user logic) stores this new configuration data in non-volatile configuration memory.

3. The Nios II processor (or user logic) initiates a reconfiguration cycle with the new or updated configuration data.

4. The dedicated remote system upgrade circuitry detects and recovers from any error(s) that might occur during or after the reconfiguration cycle, and provides error status information to the user design.

Figure 12–1 shows the steps required for performing remote configuration updates. (The numbers in the figure below coincide with the steps above.)

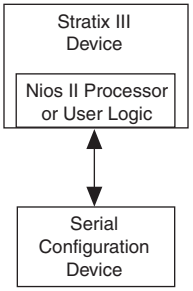
Figure 12–1. Functional Diagram of Stratix III Remote System Upgrade



Stratix III devices only support remote system upgrade in the single device Fast AS configuration scheme.

Figure 12–2 shows the block diagrams for implementing a remote system upgrade with the Stratix III Fast AS configuration scheme.

Figure 12–2. Remote System Upgrade Block Diagram for Stratix III Fast AS Configuration Scheme



You must set the mode select pins (MSEL[2..0]) to Fast AS mode to use the remote system upgrade in your system. Table 12–1 lists the MSEL pin settings for Stratix III devices in standard configuration mode and remote system upgrade mode. The following sections describe the remote update of remote system upgrade mode.

For more information on standard configuration schemes supported in Stratix III devices, refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook 1*.

Table 12–1. Stratix III Remote System Upgrade Modes

Configuration Scheme	MSEL[2..0]	Remote System Upgrade Mode
Fast AS (40 MHz) *(1)*	011	Standard
	011	Remote update

Note to Table 12–1:

(1) The EPCS16, EPCS64, and EPCS128 serial configuration devices support a DCLK up to 40 MHz. Refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* for more information.

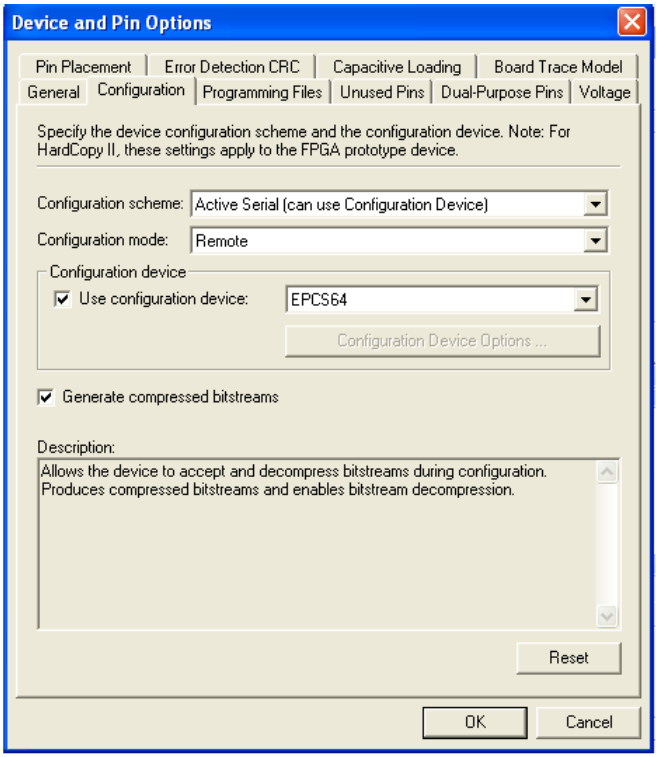
When using the Fast AS mode, you need to select the Remote Update mode in Quartus® II software and insert the altremote_update megafunction to access the circuitry. Refer to "altremote_update Megafunction" on page 12–15 for more information.

Enabling Remote Update

You can enable remote update for Stratix III devices in the Quartus II software before design compilation (in the Compiler Settings menu). To enable remote update in the project's compiler settings, perform the following steps in the Quartus II software:

1. On the Assignment menu, click **Device.** The **Settings** dialog box appears.
2. Click **Device and Pin Options.** The **Device and Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. From the Configuration scheme list, select **Active Serial** (can use Configuration Device) (Figure 12–3).
5. From the Configuration Mode list, select **Remote.** (Figure 12–3).
6. Click **OK.**
7. In the **Setting** dialog box, click **OK**.

Figure 12–3. Enabling Remote Update for Stratix III Devices in Compiler Settings



Configuration Image Types

When using a remote system upgrade, Stratix III device configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the Stratix III device that performs certain user-defined functions.

Each Stratix III device in your system requires one factory image or the addition of one or more application images. The factory image is a user-defined fall-back, or safe configuration, and is responsible for administering remote updates in conjunction with the dedicated circuitry. Application images implement user-defined functionality in the target Stratix III device. You may include the default application image functionality in the factory image.

A remote system upgrade involves storing a new application configuration image or updating an existing one via the remote communication interface. After an application configuration image is stored or updated remotely, the user design in the Stratix III device initiates a reconfiguration cycle with the new image. Any errors during or after this cycle are detected by the dedicated remote system upgrade circuitry and cause the device to automatically revert to the factory image. The factory image then performs error processing and recovery. The factory configuration is written to the serial configuration device only once by the system manufacturer and should not be remotely updated. On the other hand, application configurations may be remotely updated in the system. Both images can initiate system reconfiguration.

Remote System Upgrade Mode

Remote system upgrade has one mode of operation: remote update mode. The remote update mode allows you to determine the functionality of your system upon power-up and offers different features.

Overview

In remote update mode, Stratix III devices loads the factory configuration image upon power up. The user-defined factory configuration determines which application configuration is to be loaded and triggers a reconfiguration cycle. The factory configuration may also contain application logics.

When used with serial configuration devices, the remote update mode allows an application configuration to start at any flash sector boundary. This translates to a maximum of 128 pages in the EPCS64 device and 32 pages in the EPCS16 device, where the minimum size of each page is 512 KBits. Additionally, the remote update mode features a user watchdog timer that determines the validity of an application configuration.

Remote Update Mode

When a Stratix III device is first powered-up in remote update mode, it loads the factory configuration located at page zero (page registers `PGM[23:0] = 24'b0`). You should always store the factory configuration image for your system at page address zero. This corresponds to the start address location 0×000000 in the serial configuration device.

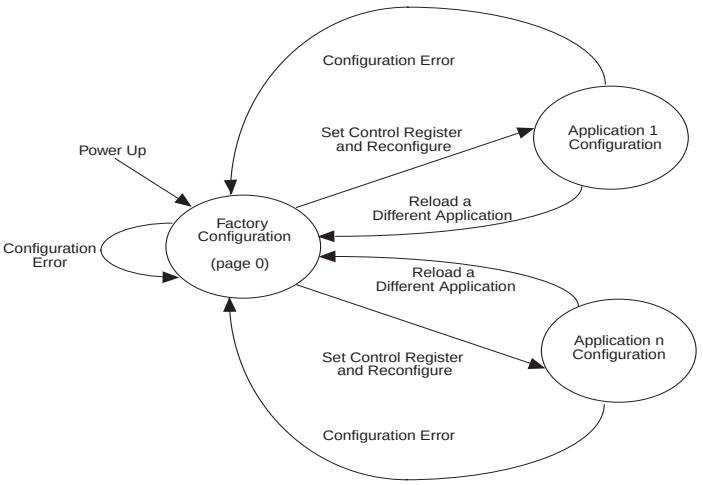
The factory image is user-designed and contains soft logic to:

- Process any errors based on status information from the dedicated remote system upgrade circuitry

- Communicate with the remote host and receive new application configurations and store this new configuration data in the local non-volatile memory device
- Determine which application configuration is to be loaded into the Stratix III device
- Enable or disable the user watchdog timer and load its time-out value (optional)
- Instruct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle

Figure 12–4 shows the transitions between the factory and application configurations in remote update mode.

Figure 12–4. Transitions Between Configurations in Remote Update Mode



After power up or a configuration error, the factory configuration logic is loaded automatically. The factory configuration also needs to specify whether to enable the user watchdog timer for the application configuration and if enabled, to include the timer setting information as well.

The user watchdog timer ensures that the application configuration is valid and functional. The timer must be continually reset within a specific amount of time during user mode operation of an application configuration. Only valid application configurations contain the logic to reset the timer in user mode. This timer reset logic should be part of a user-designed hardware and/or software health monitoring signal that indicates error-free system operation. If the timer is not reset in a specific amount of time; for example, the user application configuration detects a

functional problem or if the system hangs, the dedicated circuitry will update the remote system upgrade status register, triggering the loading of the factory configuration.

The user watchdog timer is automatically disabled for factory configurations. For more information about the user watchdog timer, refer to "User Watchdog Timer" on page 12–14.

If there is an error while loading the application configuration, the cause of the reconfiguration is written by the dedicated circuitry to the remote system upgrade status register. Actions that cause the remote system upgrade status register to be written are:

- nSTATUS driven low externally
- Internal CRC error
- User watchdog timer time out
- A configuration reset (logic array nCONFIG signal or external nCONFIG pin assertion to low)

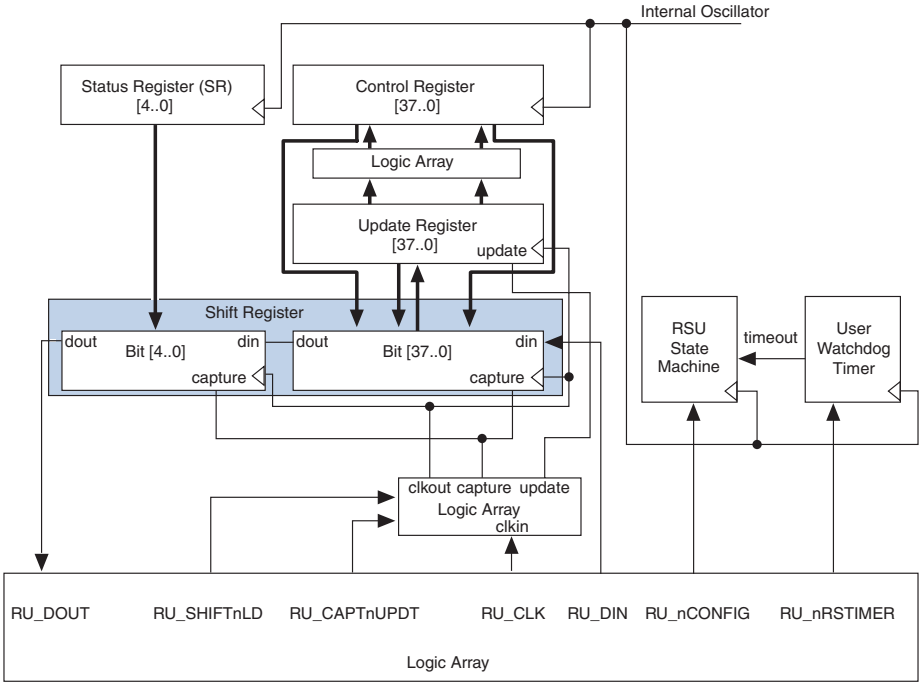
Stratix III devices automatically load the factory configuration located at page address zero. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for the reconfiguration. The factory configuration then takes appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

When Stratix III devices successfully load the application configuration, they enter into user mode. In user mode, the soft logic (Nios II processor or state machine and the remote communication interface) assists the Stratix III device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device, and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register and control register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and initiates system reconfiguration.

Dedicated Remote System Upgrade Circuitry

This section explains the implementation of the Stratix III remote system upgrade dedicated circuitry. The remote system upgrade circuitry is implemented in hard logic. This dedicated circuitry interfaces to the user-defined factory and application configurations implemented in the Stratix III device logic array to provide the complete remote configuration solution. The remote system upgrade circuitry contains the remote system upgrade registers, a watchdog timer, and a state machine that controls those components. Figure 12–5 shows the remote system upgrade block's data path.

Figure 12–5. Remote System Upgrade Circuit Data Path *Note (1)*



Note to Figure 12–4:

(1) `RU_DOUT`, `RU_SHIFTnLD`, `RU_CAPTnUPDT`, `RU_CLK`, `RU_DIN`, `RU_nCONFIG` and `RU_nRSTIMER` signals are internally controlled by the altremote_update megafunction.

Remote System Upgrade Registers

The remote system upgrade block contains a series of registers that store the page addresses, watchdog timer settings, and status information. These registers are detailed in Table 12–2.

Table 12–2. Remote System Upgrade Registers

Register	Description
Shift register	This register is accessible by the logic array and allows the update, status, and control registers to be written and sampled by user logic. Write access is enabled in remote update mode for factory configurations to allow writes to the update register.
Control register	This register contains the current page address, the user watchdog timer settings, and one bit specifying whether the current configuration is a factory configuration or an application configuration. During a read operation in an application configuration, this register is read into the shift register. When a reconfiguration cycle is initiated, the contents of the update register are written into the control register.
Update register	This register contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a capture in a factory configuration, this register is read into the shift register.
Status register	This register is written to by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

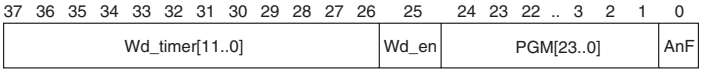
The remote system upgrade control and status registers are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer). However, the remote system upgrade shift and update registers are clocked by the user clock input (`RU_CLK`).

Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration page address and user watchdog timer settings. The control register functionality depends on the remote system upgrade mode selection. In remote update mode, the control register page address bits are set to all zeros (`24'b0 = 0×000000`) at power up in order to load the factory configuration. A factory configuration in remote update mode has write access to this register.

The control register bit positions are shown in Figure 12–6 and defined in Table 12–3. In the figure, the numbers show the bit position of a setting within a register. For example, bit number 8 is the enable bit for the watchdog timer.

Figure 12–6. Remote System Upgrade Control Register



The application-not-factory (AnF) bit indicates whether the current configuration loaded in the Stratix III device is the factory configuration or an application configuration. This bit is set low by the remote system upgrade circuitry when an error condition causes a fall-back to the factory configuration. When the AnF bit is high, the control register access is limited to read operations. When the AnF bit is low, the register allows write operations and disables the watchdog timer.

In remote update mode, factory configuration design sets this bit high (1'b1) when updating the contents of the update register with the application page address and watchdog timer settings.

Table 12–3. Remote System Upgrade Control Register Contents

Control Register Bit	Remote System Upgrade Mode	Value *(2)*	Definition
AnF *(1)*	Remote update	1'b0	Application not factory
PGM[23..0]	Remote update	24'b0×000000	AS configuration start address (StAdd[23..0])
Wd_en	Remote update	1'b0	User watchdog timer enable bit
Wd_timer[11..0]	Remote update	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {Wd_timer[11..0], 17'b0})

Note to Table 12–3:

(1) In remote update mode, the remote configuration block does not update the AnF bit automatically (you can update it manually).

(2) This is the default value of the control register bit.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include:

- Cyclic redundancy check (CRC) error during application configuration
- nSTATUS assertion by an external device due to an error
- Stratix III device logic array triggered a reconfiguration cycle, possibly after downloading a new application configuration image
- External configuration reset (nCONFIG) assertion
- User watchdog timer time out

Figure 12–7 and Table 12–4 specify the contents of the status register. The numbers in the figure show the bit positions within a 5-bit register.

Figure 12–7. Remote System Upgrade Status Register

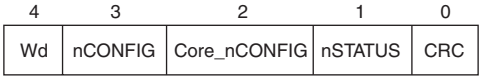


Table 12–4. Remote System Upgrade Status Register Contents

Status Register Bit	Definition	POR Reset Value
CRC (from configuration)	CRC error caused reconfiguration	1 bit '0'
nSTATUS	nSTATUS caused reconfiguration	1 bit '0'
CORE_nCONFIG *(1)*	Device logic array caused reconfiguration	1 bit '0'
nCONFIG	nCONFIG caused reconfiguration	1 bit '0'
Wd	Watchdog timer caused reconfiguration	1 bit '0'

Note to Table 12–4:

(1) Logic array reconfiguration forces the system to load the application configuration data into the Stratix III device. This occurs after the factory configuration specifies the appropriate application configuration page address by updating the update register.

Remote System Upgrade State Machine

The remote system upgrade control and update registers have identical bit definitions, but serve different roles (refer to Table 12–2). While both registers can only be updated when the device is loaded with a factory configuration image, the update register writes are controlled by the user logic; the control register writes are controlled by the remote system upgrade state machine.

In factory configurations, the user logic sends the AnF bit (set high), the page address, and the watchdog timer settings for the next application configuration bit to the update register. When the logic array configuration reset (RU_nCONFIG) goes high, the remote system upgrade state machine updates the control register with the contents of the update register and initiates system reconfiguration from the new application page.

In the event of an error or reconfiguration trigger condition, the remote system upgrade state machine directs the system to load a factory or application configuration (page zero or page one, based on the mode and error condition) by setting the control register accordingly. Table 12–5 lists the contents of the control register after such an event occurs for all possible error or trigger conditions.

The remote system upgrade status register is updated by the dedicated error monitoring circuitry after an error condition but before the factory configuration is loaded.

Table 12–5. Control Register Contents After an Error or Reconfiguration Trigger Condition

Reconfiguration Error/Trigger	Control Register Setting Remote Update
nCONFIG reset	All bits are 0
nSTATUS error	All bits are 0
CORE triggered reconfiguration	Update register
CRC error	All bits are 0
Wd time out	All bits are 0

Capture operations during factory configuration access the contents of the update register. This feature is used by the user logic to verify that the page address and watchdog timer settings were written correctly. Read operations in application configurations access the contents of the control register. This information is used by the user logic in the application configuration.

User Watchdog Timer

The user watchdog timer prevents a faulty application configuration from stalling the device indefinitely. The system uses the timer to detect functional errors after an application configuration is successfully loaded into the Stratix III device.

The user watchdog timer is a counter that counts down from the initial value loaded into the remote system upgrade control register by the factory configuration. The counter is 29-bits wide and has a maximum count value of 2^{29}. When specifying the user watchdog timer value, specify only the most significant 12 bits. The granularity of the timer setting is 2^{15} cycles. The cycle time is based on the frequency of the 10-MHz internal oscillator. Table 12–6 specifies the operating range of the 10-MHz internal oscillator.

Table 12–6. 10-MHz Internal Oscillator Specifications Note (1)

Minimum	Typical	Maximum	Units
5	6.5	10	MHz

Note to Table 12–6:
(1) These values are preliminary.

The user watchdog timer begins counting once the application configuration enters device user mode. This timer must be periodically reloaded or reset by the application configuration before the timer expires by asserting `RU_nRSTIMER`. If the application configuration does not reload the user watchdog timer before the count expires, a time-out signal is generated by the remote system upgrade dedicated circuitry. The time-out signal tells the remote system upgrade circuitry to set the user watchdog timer status bit (`Wd`) in the remote system upgrade status register and reconfigures the device by loading the factory configuration.

The user watchdog timer is not enabled during the configuration cycle of the device. Errors during configuration are detected by the CRC engine. Also, the timer is disabled for factory configurations. Functional errors should not exist in the factory configuration since it is stored and validated during production and is never updated remotely.

The user watchdog timer is disabled in factory configurations and during the configuration cycle of the application configuration. It is enabled after the application configuration enters user mode.

Quartus II Software Support

Quartus II software provides the flexibility to include the remote system upgrade interface between the Stratix III device logic array and the dedicated circuitry, generate configuration files for productions, and remote programming of the system configuration memory.

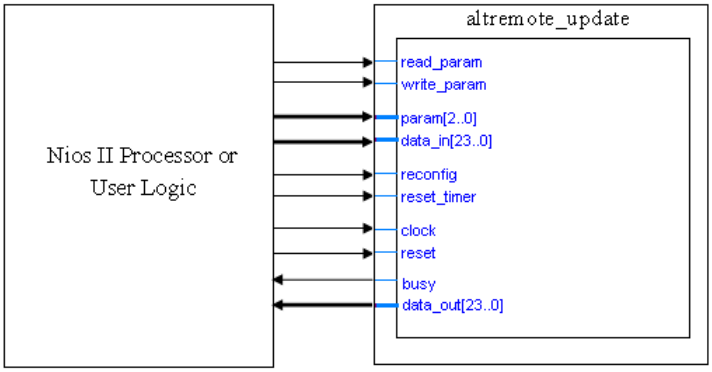
The implementation option **`altremote_update` megafunction** in Quartus II is for the interface between the remote system upgrade circuitry and the device logic array interface. Using the megafunction block instead of creating your own logic saves design time and offers more efficient logic synthesis and device implementation.

altremote_update Megafunction

The altremote_update megafunction provides a memory-like interface to the remote system upgrade circuitry and handles the shift register read / write protocol in Stratix III device logic. This implementation is suitable for designs that implement the factory configuration functions using a Nios II processor or user logic in the device.

Figure 12–8 shows the interface signals between the altremote_update megafunction and Nios II processor / user logic.

Figure 12–8. Interface Signals Between the altremote_update Megafunction and the Nios II Processor



For more information on the altremote_update Megafunction and the description of ports listed in Figure 12–8, refer to the *altremote_update Megafunction User Guide*.

Conclusion

Stratix III devices offer remote system upgrade capability, where you can upgrade a system in real-time through any network. Remote system upgrade helps to deliver feature enhancements and bug fixes without costly recalls, reduces time to market, and extends product life cycles. The dedicated remote system upgrade circuitry in Stratix III devices provides error detection, recovery, and status information to ensure reliable reconfiguration.

Document Revision History

Table 12–7 shows the revision history for this document.

Table 12–7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Minor text edits to page 4 and 5. Changes to Figure 12–2. Added Figure 12–3. Added a note to Figure 12–5. Added Figure 12–8. Added new section, "Enabling Remote Update" on page 12–4. Removed references to "Remote System Upgrade atom" and section of same title. Removed "Interface Signals Between Remote System Upgrade Circuitry and Stratix III Device Logic Array" section. Removed Table titled "Interface Signals between Remote System Upgrade Circuitry and Stratix III Device Logic Array." Removed footnote, table titled "Input Ports of the altremote_update Megafunction," table titled "Output Ports of the altremote_update Megafunction," and table titled "Parameter Settings for the altremote_update Megafunction" in section "altremote_update Megafunction" on page 12–15. Removed "System Design Guidelines Using Remote System Upgrade With Serial Configuration Devices" section.	Text edits, table and section removal, addition of figures.
November 2006 v1.0	Initial Release	—

13. IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices

SIII51013-1.1

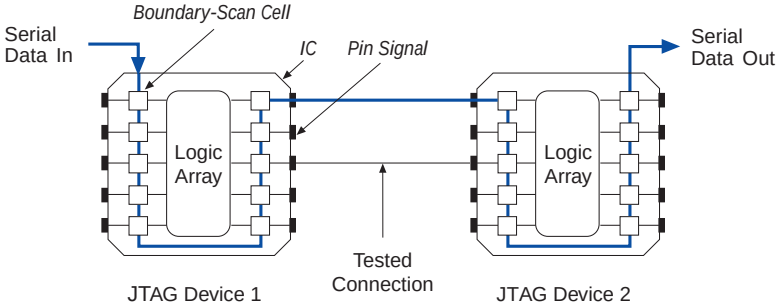
Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (such as, external test probes and "bed-of-nails" test fixture) harder to implement. As a result, cost savings from PCB space reductions increases the cost for traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to test efficiently components on PCBs with tight lead spacing.

BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 13–1 illustrates the concept of BST.

Figure 13–1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in Stratix® III devices, including:

- "IEEE Std. 1149.1 BST Architecture"
- "IEEE Std. 1149.1 Boundary-Scan Register"
- "IEEE Std. 1149.1 BST Operation Control"
- "I/O Voltage Support in JTAG Chain"
- "IEEE Std. 1149.1 BST Circuitry"
- "IEEE Std. 1149.1 BST for Configured Devices"
- "IEEE Std. 1149.1 BST Circuitry (Disabling)"
- "IEEE Std. 1149.1 BST Guidelines"
- "Boundary-Scan Description Language (BSDL) Support"

In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix III device in-circuit reconfiguration (ICR). However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For information on configuring Stratix III devices via the IEEE Std. 1149.1 circuitry, refer to the *Configuring Stratix III Devices*, *Hot Socketing and Power-On Reset in Stratix III Devices*, and the *Remote System Updates with Stratix III Devices* chapters in volume 1 of the *Stratix III Device Handbook*.

IEEE Std. 1149.1 BST Architecture

A Stratix III device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have weak internal pull-ups. The TDO output pin and all the JTAG input pins are powered by the 2.5-V/3.0-V V_{CCPD} supply of I/O Bank 1A. All user I/O pins are tri-stated during JTAG configuration.

For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to "I/O Voltage Support in JTAG Chain" on page 13–18.

Table 13–1 summarizes the functions of each of these pins.

Table 13–1. IEEE Std. 1149.1 Pin Descriptions (Part 1 of 2)

Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Signal applied to TDI is expected to change state at the falling edge of TCK. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.

Table 13–1. IEEE Std. 1149.1 Pin Descriptions (Part 2 of 2)

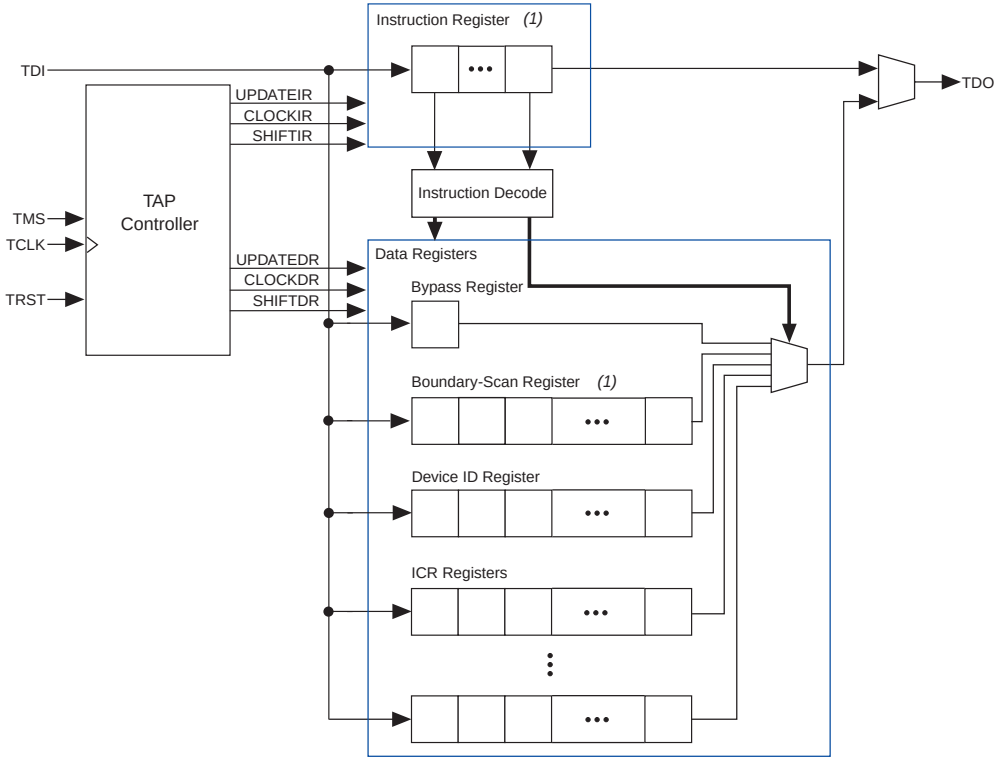
Pin	Description	Function
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the test access port (TAP) controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, you must set up TMS before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. During non-JTAG operation, Altera® recommends you drive TMS high.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. You should drive this pin low when not in boundary-scan operation. For non-JTAG users, you should permanently tie the pin to GND.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a one-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 13–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 13–2. IEEE Std. 1149.1 Circuitry



Note to Figure 13–2:

(1) For register lengths, see the device data sheet in the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information on the TAP controller, refer to "IEEE Std. 1149.1 BST Operation Control" on page 13–9. The TMS and TCK pins operate the TAP controller. The TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of three-bit peripheral elements that are associated with Stratix III I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

Refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook* for the Stratix III family device boundary-scan register lengths.

Figure 13–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 13–3. Boundary-Scan Register

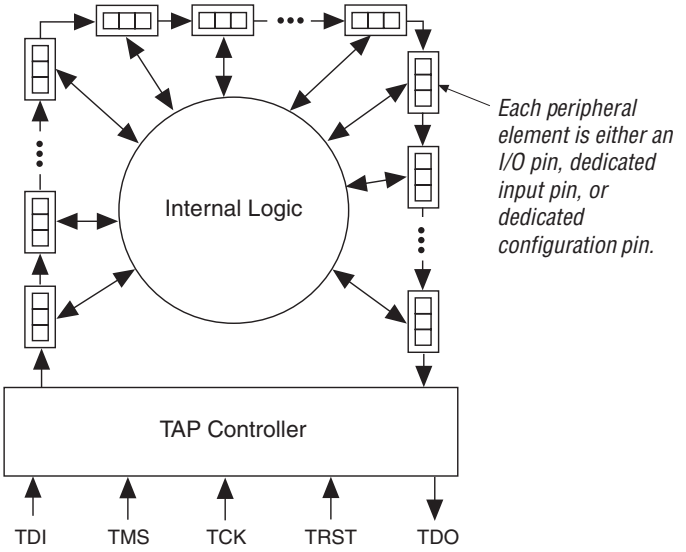


Table 13–2 shows the boundary-scan register length for Stratix III devices.

Table 13–2. Stratix III Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP3SL50	1506
EP3SL70	1506
EP3SL110	2274
EP3SL150	2274
EP3SL200	2682
EP3SL340	3402
EP3SE50	1506
EP3SE80	2274

Table 13–2. Stratix III Boundary-Scan Register Length	
Device	**Boundary-Scan Register Length**
EP3SE110	2274
EP3SE260	2970

Boundary-Scan Cells of a Stratix III Device I/O Pin

The Stratix III device three-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ, OEJ, and PIN_IN signals, while the update registers connect to external data through the PIN_OUT, and PIN_OE signals.

The global control signals for the IEEE Std. 1149.1 BST registers (such as shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The HIGHZ signal is high when executing the HIGHZ instruction. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 13–4 shows the Stratix III device's user I/O boundary-scan cell.

Figure 13–4. Stratix III Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

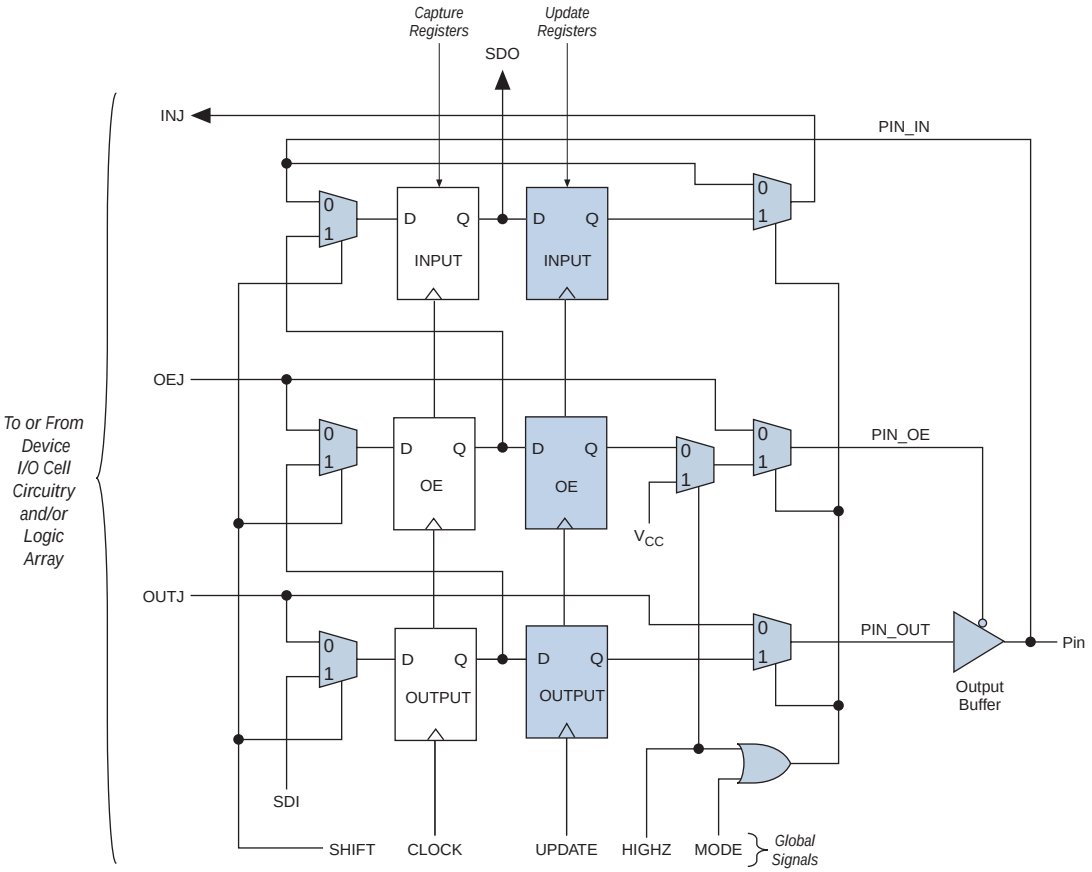


Table 13–3 describes the capture and update register capabilities of all boundary-scan cells within Stratix III devices.

Table 13–3. Stratix III Device Boundary Scan Cell Descriptions *Note (1)*

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	NA
Dedicated clock input	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to clock network or logic array
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated bidirectional *(5)*	OUTJ	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control and OUTJ drives to output buffer
Dedicated output *(6)*	OUTJ	0	0	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 13–3:

(1) TDI, TDO, TMS, TCK, TRST, all V_{CC} and GND pin types, VREF, and TEMP_DIODE pins do not have BSCs.
(2) No Connect (N.C.).
(3) This includes pins PLL_ENA, nCONFIG, MSEL0, MSEL1, MSEL2, nCE, PORSEL, and nIO_PULLUP.
(4) This includes pins CONF_DONE and nSTATUS.
(5) This includes pin DCLK.
(6) This includes pin nCEO.

IEEE Std. 1149.1 BST Operation Control

Stratix III devices support the IEEE Std. 1149.1 (JTAG) instructions shown in Table 13–4.

Table 13–4. Stratix III JTAG Instructions

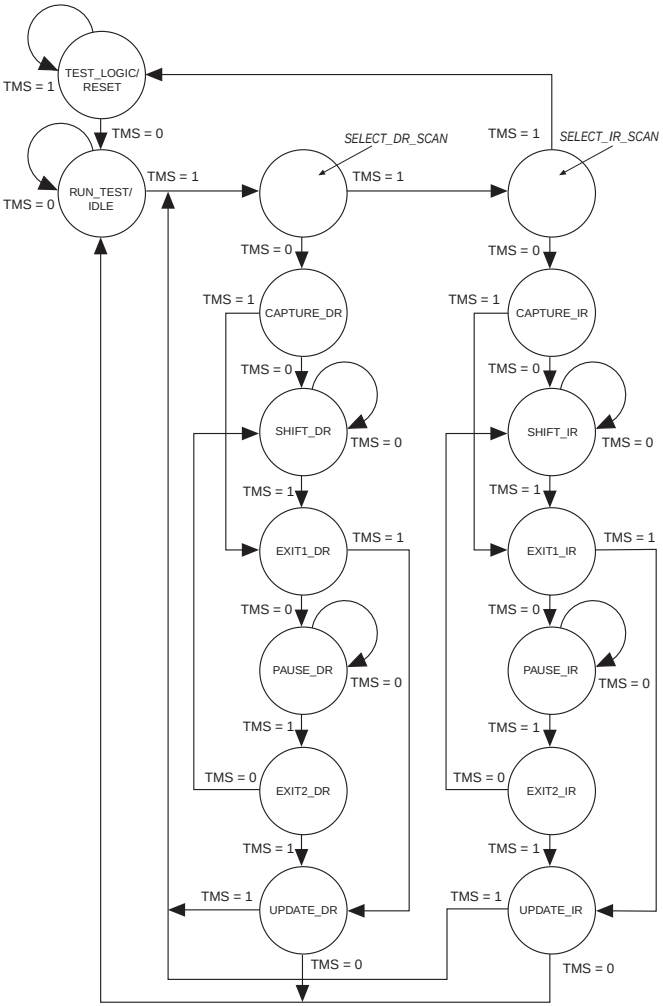
JTAG Instruction	Instruction Code	Description
SAMPLE / PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap® II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ *(1)*	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring a Stratix III device via the JTAG port with a USB Blaster™ , ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File, or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	00 0000 1101	Allows I/O reconfiguration through JTAG ports using the IOCSR for JTAG testing. Can be executed before, after, or during configurations.

Note to Table 13–4:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The IEEE Std. 1149.1 TAP controller, a 16-state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 13–5 shows the TAP controller state machine.

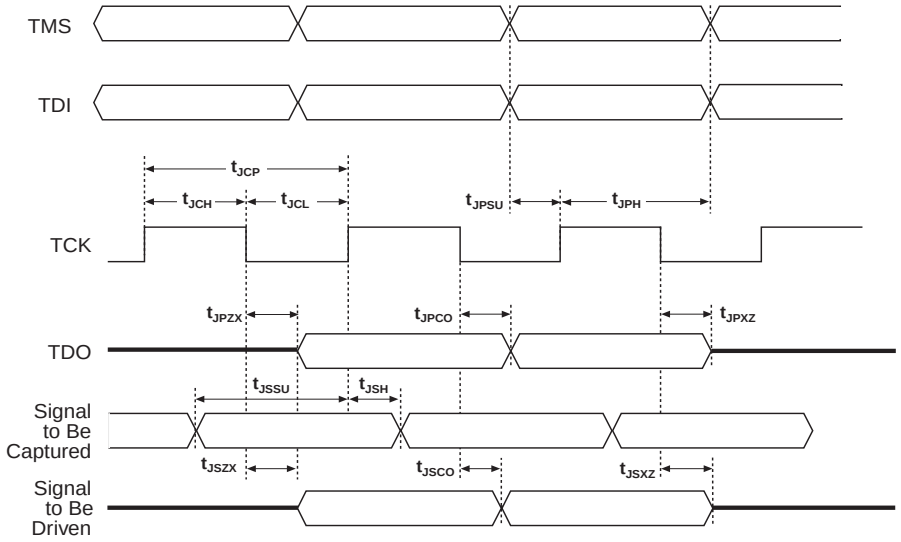
Figure 13–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, forcing the TAP controller to the TEST_LOGIC/RESET state is

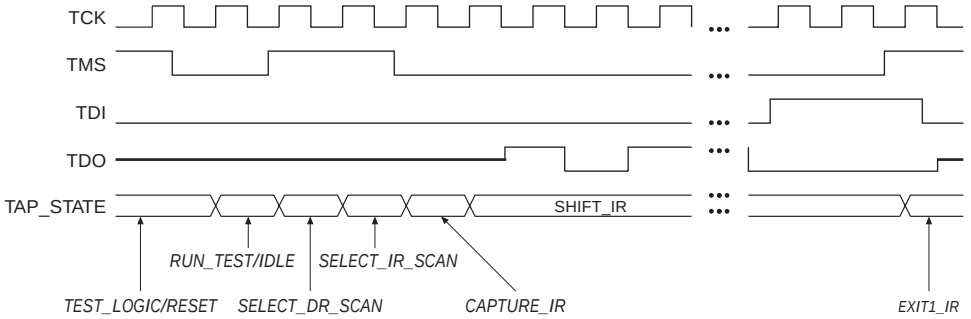
done by holding TMS high for five TCK clock cycles, or by holding the TRST pin low. Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS is held high (while TCK is clocked) or TRST is held low. Figure 13–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 13–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 13–7 represents the entry of the instruction code into the instruction register. It also shows the values of TCK, TMS, TDI, TDO, and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Figure 13–7. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code is clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS high to activate the EXIT1_IR state. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of three modes. The three serially shift test data instruction modes are discussed in the following sections:

- "SAMPLE / PRELOAD Instruction Mode" on page 13–12
- "EXTEST Instruction Mode" on page 13–14
- "BYPASS Instruction Mode" on page 13–16

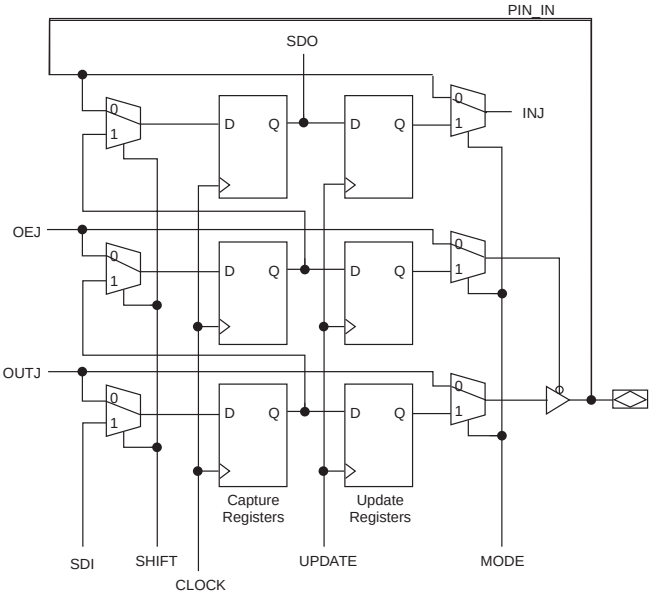
SAMPLE/PRELOAD Instruction Mode

The SAMPLE / PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, this instruction is most often used to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 13–8 shows the capture, shift, and update phases of the SAMPLE / PRELOAD mode.

Figure 13–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

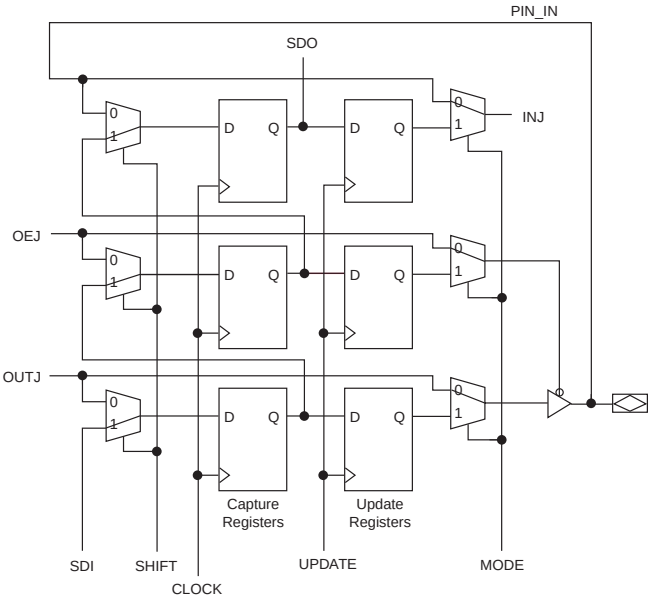
In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

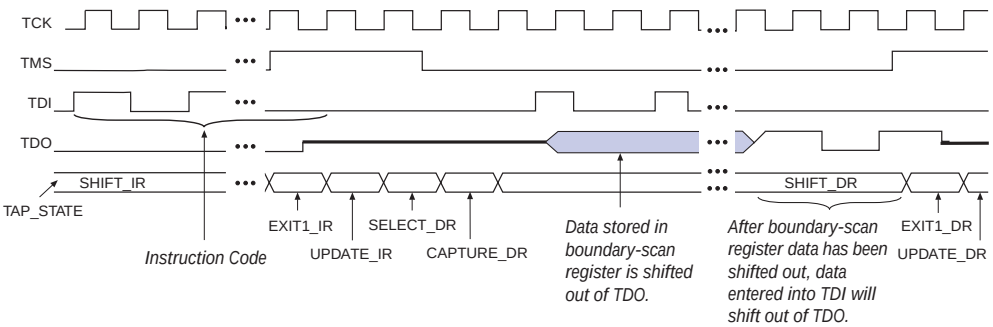
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The data stored in the update registers can be used for the EXTEST instruction.



During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through the capture registers around the device periphery and then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. You can then use this data in the EXTEST instruction mode. Refer to "EXTEST Instruction Mode" on page 13–14 for more information.

Figure 13–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 13–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

Use the EXTEST instruction mode primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, you can detect opens and shorts at pins of any device in the scan chain.

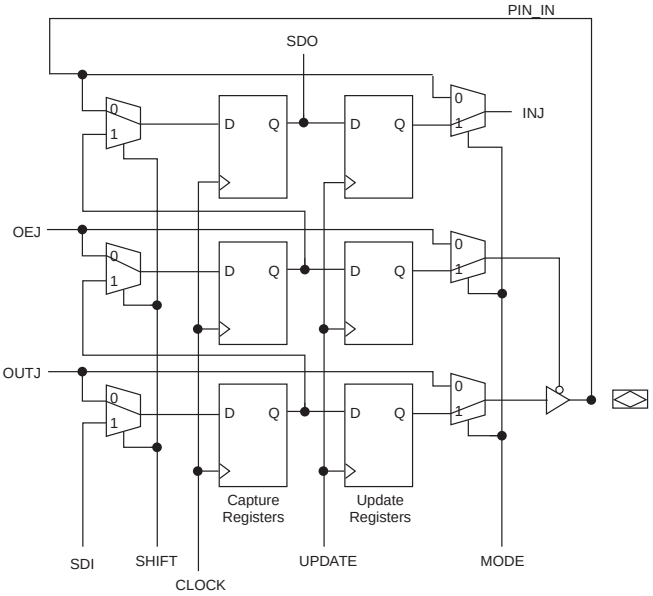
Figure 13–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 13–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_OUT, INJ, and allows the I/O pin to tri-state or drive a signal out.

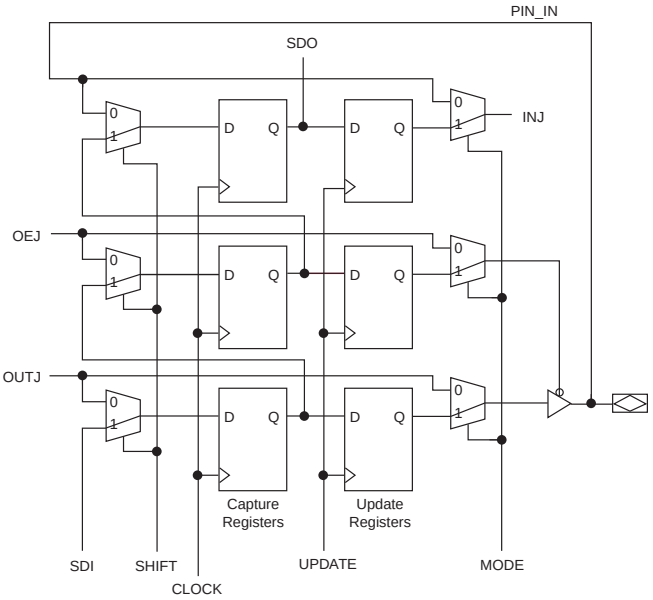
A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

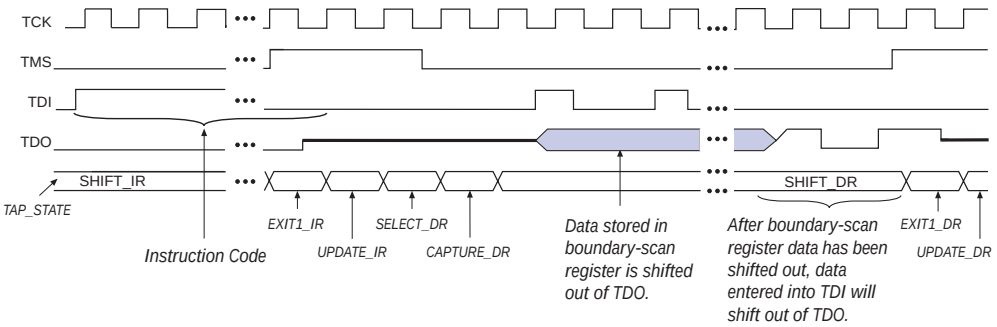
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_OUT, INJ, and allow the I/O pin to tri-state or drive a signal out.



EXTEST mode selects data differently than SAMPLE/PRELOAD mode. EXTEST chooses data from the update registers as the source of the output and output-enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data. Therefore, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. You can then store new test data in the update registers during the update phase.

The EXTEST waveform diagram in Figure 13–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

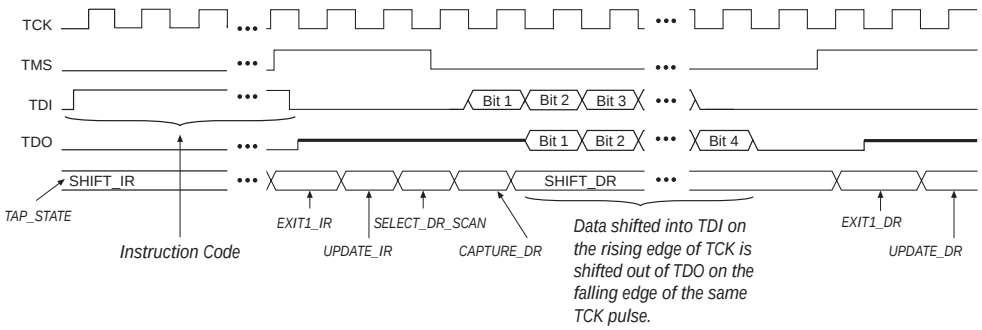
Figure 13–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all ones is loaded in the instruction register. This mode allows the boundary scan data to pass the selected device synchronously to adjacent devices when no test operation of the device is needed at the board level. The waveforms in Figure 13–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 13–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

Use the IDCODE instruction mode to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the TDI and TDO ports, and the device IDCODE is shifted out. Table 13–5 shows the IDCODE information for Stratix III devices.

Table 13–5. 32-Bit Stratix III Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP3SL50	0000	0010 0001 0000 1000	000 0110 1110	1
EP3SL70	0000	0010 0001 0000 0001	000 0110 1110	1
EP3SL110	0000	0010 0001 0000 1001	000 0110 1110	1
EP3SL150	0000	0010 0001 0000 0010	000 0110 1110	1
EP3SL200	0000	0010 0001 0000 0011	000 0110 1110	1
EP3SL340	0000	0010 0001 0000 0101	000 0110 1110	1
EP3SE50	0000	0010 0001 0000 0110	000 0110 1110	1
EP3SE80	0000	0010 0001 0000 1010	000 0110 1110	1
EP3SE110	0000	0010 0001 0000 0111	000 0110 1110	1
EP3SE260	0000	0010 0001 0000 0100	000 0110 1110	1

Notes to Table 13–5:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

USERCODE Instruction Mode

Use the USERCODE instruction mode to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When you select this instruction, the device identification register is connected between the TDI and TDO ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit USERCODE register. The UES is then shifted out through the device ID register.

The UES value is not user defined until after the device is configured. This is because the value is stored in the programmer object file (**.pof**) and only loaded to the device during configuration. Before configuration, the UES value is set to the default value.

CLAMP Instruction Mode

Use the CLAMP instruction mode to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the TDI and TDO ports. The state of all signals driven from the pins are completely defined by the data held in the boundary-scan register.

HIGHZ Instruction Mode

The HIGHZ instruction mode sets all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the TDI and TDO ports.

I/O Voltage Support in JTAG Chain

The JTAG chain supports several devices. However, you should use caution if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. The TDI of one Stratix III device connected in a chain to the TDO pins of another Stratix III device are powered by the V_{CCPD} (2.5 V / 3.0 V) suppl of I/O Bank 1A. You should connect V_{CCPD} according to the I/O standard used in the same bank. For 3.3 V and 3.0 V I/O standards,

you should connect V_{CCPD} to 3.0 V; for 2.5 V and below I/O standards, you should connect V_{CCPD} to 2.5 V. Table 13–6 shows board design recommendations to ensure proper JTAG chain operation.

Table 13–6. Supported TDO/TDI Voltage Combinations

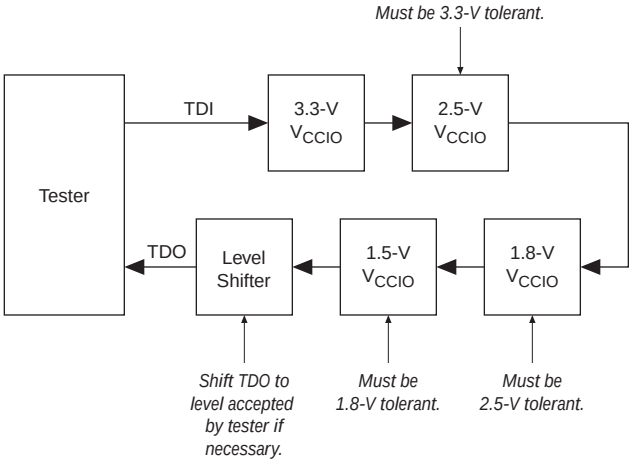
Device	TDI Input Buffer Power	Stratix III TDO V_{CCPD}	
		V_{CCPD} = 3.0 V	V_{CCPD} = 2.5 V
Stratix III	V_{CCPD} = 3.0V	✓(1)	✓(2)
	V_{CCPD} = 2.5V	✓(1)	✓(2)
Non-Stratix III	V_{CC} = 3.3 V	✓(1)	✓(2)
	V_{CC} = 2.5 V	✓(1), (3)	✓(2)
	V_{CC} = 1.8 V	✓(1), (3)	✓(2), (4)
	V_{CC} = 1.5 V	✓(1), (3)	✓(2), (4)

Notes to Table 13–6:

(1) The TDO output buffer meets V_{OH} (MIN) = 2.4 V.
(2) The TDO output buffer meets V_{OH} (MIN) = 2.0 V.
(3) Input buffer must be 3.0-V tolerant.
(4) Input buffer must be 2.5-V tolerant.

You can interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, you should build the JTAG chain in such a way that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter is used only to shift the TDO level to a level acceptable to the JTAG tester. Figure 13–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 13–13. JTAG Chain of Mixed Voltages



IEEE Std. 1149.1 BST Circuitry

Stratix III devices have dedicated JTAG pins and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. Not only can you perform BST on Stratix III FPGAs before and after, but also during configuration. Stratix III FPGAs support the BYPASS, IDCODE, and SAMPLE instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the CONFIG_IO instruction.

The CONFIG_IO instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Stratix III FPGA or you can wait for the configuration device to complete configuration. Once configuration is interrupted and JTAG BST is complete, you must reconfigure the part via JTAG (PULSE_CONFIG instruction) or by pulsing nCONFIG low.

When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Stratix III devices do not affect JTAG boundary-scan or configuration operations. Toggling these pins does not disrupt BST operation (other than the expected BST behavior).

When you design a board for JTAG configuration of Stratix III devices, you need to consider the connections for the dedicated configuration pins.

For more information on using the IEEE Std.1149.1 circuitry for device configuration, refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

IEEE Std. 1149.1 BST for Configured Devices

For a configured device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. Nevertheless, executing the SAMPLE instruction will turn on the input buffers in the output pins for sample operation. You can set the Quartus® II software to always enable the input buffers on a configured device so it behaves the same as an unconfigured device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause a slight increase in standby current because the unused input buffer is always on.

In the Quartus II software, complete the following:

1. From the assignments menu, select **Settings**.
2. Click **Assembler**.
3. Turn on **Always Enable Input Buffers**.

If you use the default setting with input disabled, you need to convert the default BSDL file to the design-specific BSDL file using the BSDL Customizer script. For more information regarding BSDL file, refer to "Boundary-Scan Description Language (BSDL) Support" on page 13–23.

IEEE Std. 1149.1 BST Circuitry (Disabling)

The IEEE Std. 1149.1 BST circuitry for Stratix III devices is enabled upon device power-up. Because the IEEE Std. 1149.1 BST circuitry is used for BST or in-circuit reconfiguration, you must enable the circuitry only at specific times as mentioned in, "IEEE Std. 1149.1 BST Circuitry" on page 13–20.

If you are not using the IEEE Std. 1149.1 circuitry in Stratix III, you should permanently disable the circuitry to ensure that you do not inadvertently enable it when it is not required.

Table 13–7 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Stratix III devices.

Table 13–7. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
TMS	V_{CCPD} supply of Bank 1A
TCK	GND
TDI	V_{CCPD} supply of Bank 1A
TDO	Leave open
TRST	GND

Note to Table 13–7:
(1) There is no software option to disable JTAG in Stratix III devices. The JTAG pins are dedicated.

IEEE Std. 1149.1 BST Guidelines

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the "10..." pattern does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
  - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.

Do NOT use the following private instructions as they may render the device inoperable:
11 0001 0000
00 1100 1001
11 0001 0011
11 0001 0111
You should take precautions not to invoke these instructions at any time.

- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when you enter the EXTEST mode. If the OEJ update register contains a 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during ICR. This instruction is supported before or after ICR, but not during ICR. Use the CONFIG_IO instruction to interrupt configuration and then perform testing, or wait for configuration to complete.
- If performing testing before configuration, hold the nCONFIG pin low.

For more information on boundary scan testing, contact Altera Applications.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, and failure diagnostics.

For more information on BSDL files for IEEE Std. 1149.1-compliant Stratix III devices and the BSDLCustomizer script, visit the Altera web site at **www.altera.com**.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Stratix III devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document Revision History

Table 13–8 shows the revision history for this document.

Table 13–8. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Updated Note 3 to Table 13–3. Updated Figure 13–6. Added Table 13–2, Table 13–4, Table 13–5, and Table 13–7. Removed opening paragraph and footnote for "IEEE Std. 1149.1 BST Operation Control" on page 13–9. Added warning on page 13-22.	Minor updates.
November 2006 v1.0	Initial Release	—

Section IV. Design Security and Single Event Upset (SEU) Mitigation

This section provides information on Design Security and Single Event Upset (SEU) Mitigation in Stratix® III devices.

- Chapter 14, Design Security in Stratix III Devices
- Chapter 15, SEU Mitigation in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

14. Design Security in Stratix III Devices

SIII51014-1.0

Introduction

This chapter provides an overview of the design security feature and its implementation on Stratix® III devices using advanced encryption standard (AES) as well as the security modes available in Stratix III devices for designers to utilize this new feature in their designs.

As Stratix III devices start to play a role in larger and more critical designs in competitive commercial and military environments, it is increasingly important to protect the designs from copying, reverse engineering, and tampering.

Stratix III devices address these concerns and are the industry's only high-density and high-performance devices with both volatile and non-volatile security feature support. Stratix III devices have the ability to decrypt configuration bitstreams using the AES algorithm, an industry standard encryption algorithm that is FIPS-197 certified. Stratix III devices have a design security feature which utilizes a 256-bit security key.

Altera® Stratix III devices store configuration data in static random access memory (SRAM) configuration cells during device operation. Because the SRAM memory is volatile, the SRAM cells must be loaded with configuration data each time the device powers-up. It is possible to intercept configuration data when it is being transmitted from the memory source (flash memory or a configuration device) to the device. The intercepted configuration data could then be used to configure another device.

When using the Stratix III design security feature, the security key is stored in the Stratix III device. Depending on the security mode, you can configure the Stratix III device using a configuration file that is encrypted with the same key, or for board testing, configured with a normal configuration file.

The design security feature is available when configuring Stratix III devices using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX® II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes. The design security feature is also available in remote update with fast AS configuration mode. The design security feature is not available when you are configuring your Stratix III device using FPP with an enhanced

configuration device, or Joint Test Action Group (JTAG)-based configuration. For more details, refer to "Supported Configuration Schemes" on page 14–6.

The largest serial configuration device currently supports 64 MBits of configuration bitstream. Please contact Altera Technical Support for more information on serial configuration device support for large Stratix III devices such as EP3SE260 and EP3SL340.

Stratix III Security Protection

Stratix III device designs are protected from copying, reverse engineering, and tampering using configuration bitstream encryption.

Security Against Copying

The security key is securely stored in the Stratix III device and cannot be read out through any interfaces. In addition, as configuration file read-back is not supported in Stratix III devices, the design information cannot be copied.

Security Against Reverse Engineering

Reverse engineering from an encrypted configuration file is very difficult and time consuming because the Stratix III configuration file formats are proprietary and the file contains million of bits which require specific decryption. Reverse engineering the Stratix III device is just as difficult because the device is manufactured on the most advanced 65-nm process technology.

Security Against Tampering

The non-volatile keys are one-time programmable. Once the *Tamper Protection* bit is set in the key programming file generated by the Quartus® II software, the Stratix III device can only be configured with configuration files encrypted with the same key.

For more information on why this feature is secured, refer to the *Stratix III Design Security White Paper*. Contact your local Altera sales representative to request this document.

AES Decryption Block

The main purpose of the AES decryption block is to decrypt the configuration bitstream prior to entering data decompression or configuration.

Prior to receiving encrypted data, you must enter and store the 256-bit security key in the device. You can choose between a non-volatile security key and a volatile security key with battery backup.

The steps for programming either key will be included in the *Stratix III Design Security Application Note* which will be available at a later date.

The security key is scrambled prior to storing it in the key storage in order to make it more difficult for anyone to retrieve the stored key via de-capsulation of the device.

Flexible Security Key Storage

Stratix III devices support two types of security keys programming: volatile and non-volatile keys. Table 14–1 shows the differences between volatile keys and non-volatile keys.

Table 14–1. Security Keys Options

Options	Volatile Key	Non-Volatile Key
Key programmability	Reprogrammable and erasable	One-time programmable
External battery	Required	Not required
Key programming method *(1)*	On-board	On and off board
Design protection	Secure against copying and reverse engineering	Secure against copying, reverse engineering, and tampering

Note to Table 14–1:
(1) Key programming is carried out via JTAG interface.

The non-volatile key can be programmed to the Stratix III device without an external battery. Also, there are no additional requirements to any of the Stratix III power supply inputs.

V_{CCBAT} is a dedicated power supply for the volatile key storage and not shared with other on-chip power supplies, such as V_{CCIO} or V_{CC}. V_{CCBAT} continuously supplies power to the volatile register regardless of the on-chip supply condition. The nominal voltage for this supply is 2.5 V,

while its valid operating range is from 1.0 to 3.0 V. If you do not use the volatile security key, you may connect the V_{CCBAT} to either ground or a 2.5 V power supply.

After power-up, you will need to wait 100 ms (PORSEL = 0) or 12 ms (PORSEL = 1) before beginning the key programming to ensure that V_{CCBAT} is at its full rail.

As an example, here are some lithium coin-cell type batteries used for volatile key storage purposes: BR1220 (-30° to +80°C) and BR2477A (-40°C to +125°C). For more information on battery specifications, refer to the *DC & Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

Stratix III Design Security Solution

Stratix III devices are SRAM-based devices. To provide design security, Stratix III devices require a 256-bit security key for configuration bitstream encryption.

You can carry out secure configuration in the following three steps, as shown in Figure 14–1:

1. Program the security key into the Stratix III device.

   Program the user-defined 256-bit AES keys to the Stratix III device through the JTAG interface.

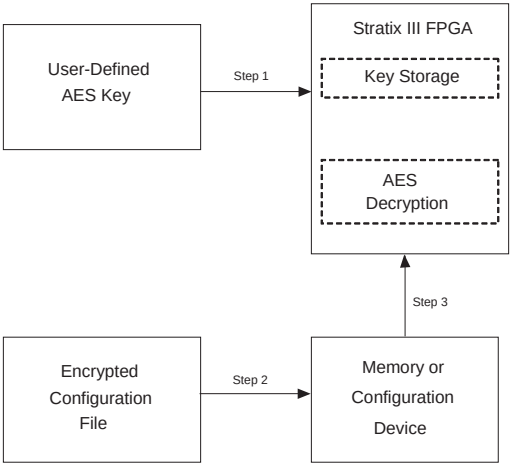
2. Encrypt the configuration file and store it in the external memory.

   Encrypt the configuration file with the same 256-bit keys used to program the Stratix III device. Encryption of the configuration file is done using the Quartus II software. The encrypted configuration file is then loaded into the external memory, such as a configuration or flash device.

3. Configure the Stratix III device.

   At system power-up, the external memory device sends the encrypted configuration file to the Stratix III device.

Figure 14–1. Design Security *Note (1)*



Note to Figure 14–1:
(1) Step 1, Step 2, and Step 3 correspond to the procedure detailed in the "Stratix III Design Security Solution" section.

Security Modes Available

There are several security modes available on the Stratix III device, which are as follows:

Volatile Key

Secure Operation with volatile key programmed and required external battery: this mode accepts both encrypted and unencrypted configuration bitstreams. Use the unencrypted configuration bitstream support for board-level testing only.

Non-Volatile Key

Secure Operation with one time programmable (OTP) security key programmed: this mode accepts both encrypted and unencrypted configuration bitstreams. Use the unencrypted configuration bitstream support for board level testing only.

Non-Volatile Key with Tamper Protection Bit Set

Secure Operation in tamper resistant mode with OTP security key programmed: only encrypted configuration bitstreams are allowed to configure the device.

No Key Operation

Only unencrypted configuration bitstreams are allowed to configure the device.

Table 14–2 summarizes the different security modes and the configuration bitstream supported for each mode.

Table 14–2. Security Modes Supported

Mode *(1)*	Function	Configuration File
Volatile key	Secure	Encrypted
	Board-level testing	Unencrypted
Non-volatile key	Secure	Encrypted
	Board-level testing	Unencrypted
Non-volatile key with *tamper protection* bit set	Secure (tamper resistant) *(2)*	Encrypted

Notes to Table 14–2:

(1) In the *No key* operation, only **unencrypted configuration file** is supported.

(2) The *tamper protection* bit setting does not prevent the device from being reconfigured.

Supported Configuration Schemes

The Stratix III device supports only selected configuration schemes, depending on the security mode you select when you encrypt the Stratix III device.

Figure 14–2 shows the restrictions of each security mode when encrypting Stratix III devices.

Figure 14–2. Stratix III Security Modes - Sequence & Restrictions

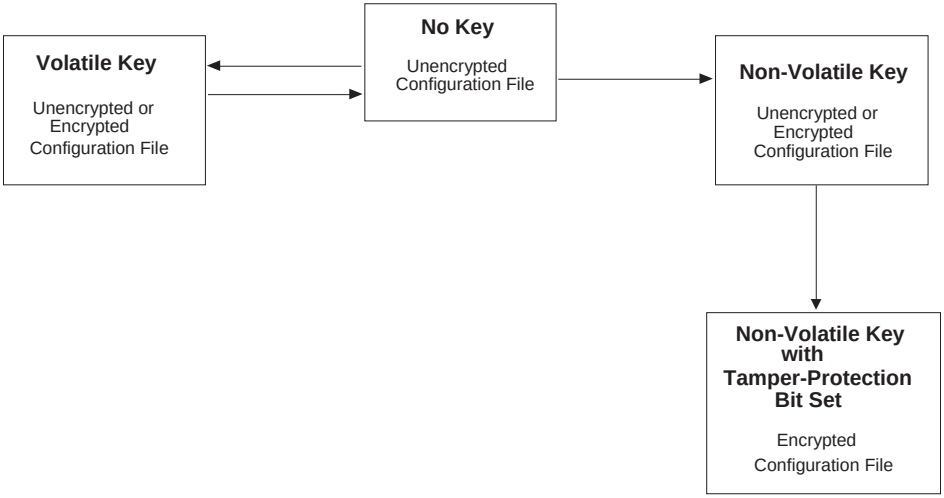


Table 14–3 shows the configuration modes allowed in each of the security modes.

Table 14–3. Allowed Configuration Modes for Various Security Modes *Note (1)* ***(Part 1 of 2)***

Security Mode	Configuration File	Allowed Configuration Modes
No key	Unencrypted	All configuration modes that do not engage the design security feature.
Secure with volatile key	Encrypted	• Passive serial with AES (and/or with decompression) • Fast passive parallel with AES (and/or with decompression) • Remote update fast AS with AES (and/or with decompression) • Fast AS (and/or with decompression)
Board-level testing with volatile key	Unencrypted	All configuration modes that do not engage the design security feature.

Table 14–3. Allowed Configuration Modes for Various Security Modes Note (1) (Part 2 of 2)

Security Mode	Configuration File	Allowed Configuration Modes
Secure with non-volatile key	Encrypted	• Passive serial with AES (and/or with decompression) • Fast passive parallel with AES (and/or with decompression) • Remote update fast AS with AES (and/or with decompression) • Fast AS (and/or with decompression)
Board-level testing with non-volatile key	Unencrypted	All configuration modes that do not engage the design security feature.
Secure in tamper resistant mode using non-volatile key with *tamper protection* set	Encrypted	• Passive serial with AES (and/or with decompression) • Fast passive parallel with AES (and/or with decompression) • Remote update fast AS with AES (and/or with decompression) • Fast AS (and/or with decompression)

Note to Figure 14–3:

(1) There is no impact to the configuration time required compared to unencrypted configuration modes except fast passive parallel with AES (and/or decompression) which requires DCLK of 4× the data rate.

The design security feature is available in all configuration methods, except in JTAG. Therefore, you can use the design security feature in FPP mode (when using external controller, such as a MAX II device or a microprocessor and a flash memory), or in fast AS and PS configuration schemes.

Table 14–4 summarizes the configuration schemes that support the design security feature both for volatile key and non-volatile key programming.

Table 14–4. Design Security Configuration Schemes Availability (Part 1 of 2)

Configuration Scheme	Configuration Method	Design Security
FPP	MAX II device or microprocessor and flash memory	✓ (1)
	Enhanced configuration device	
Fast AS	Serial configuration device	✓

Table 14–4. Design Security Configuration Schemes Availability (Part 2 of 2)

Configuration Scheme	Configuration Method	Design Security
PS	MAX II device or microprocessor and flash memory	✓
	Download cable	✓
JTAG	MAX II device or microprocessor and flash memory	
	Download cable	

Note to Table 14–4:
(1) In this mode, the host system must send a DCLK that is 4× the data rate.

You can use the design security feature with other configuration features, such as compression and remote system upgrade features. When you use compression with the design security feature, the configuration file is first compressed and then encrypted using the Quartus II software. During configuration, the Stratix III device first decrypts and then decompresses the configuration file.

Conclusion

The need for design security is increasing as devices move from glue logic to implementing critical system functions. Stratix III devices address this concern by providing built-in design security. These devices not only offer high density, fast performance, and cutting-edge features to meet your design needs, but also protect your designs against IP theft and tampering of your configuration files.

Document Revision History

Table 14–5 shows the revision history for this document.

Table 14–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
November 2006 v1.0	Initial Release	

15. SEU Mitigation in Stratix III Devices

SIII51015-1.1

Introduction

In critical applications such as avionics, telecommunications, system control, and military applications, it is important to be able to do the following:

- Confirm that the configuration data stored in an Stratix III device is correct.
- Alert the system to the occurrence of a configuration error.

The error detection feature has been enhanced in the Stratix® III family. The error detection and recovery time for single event upset (SEU) in Stratix III devices is reduced compared to Stratix II devices.

Information on SEU is located on the Products page of the Altera® website (**www.altera.com**).

Dedicated circuitry is built into Stratix III devices and consists of a cyclic redundancy check (CRC) error detection feature that can optionally check for SEUs continuously and automatically.

This section describes how to activate and use the error detection CRC feature when your Stratix III device is in user mode and describes how to recover from configuration errors caused by CRC errors.

For Stratix III devices, use of the error detection CRC feature is provided in the Quartus® II software starting with version 6.1.

Using CRC error detection for the Stratix III family has no impact on fitting or performance.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices.*

Error Detection Fundamentals

Error detection determines if the data received through a medium is corrupted during transmission. To accomplish this, the transmitter uses a function to calculate a checksum value for the data and appends the checksum to the original data frame. The receiver uses the same calculation methodology to generate a checksum for the received data frame and compares the received checksum to the transmitted checksum. If the two checksum values are equal, the received data frame is correct and no data corruption occurred during transmission or storage.

The error detection CRC feature uses the same concept. When Stratix III devices have been configured successfully and are in user mode, the error detection CRC feature ensures the integrity of the configuration data.

There are two CRC error checks. One always runs during configuration and a second optional CRC error check that runs in the background in user mode. Both CRC error checks use the same CRC polynomial but different error detection implementations. For more information, refer to "Configuration Error Detection" on page 15–2 and "User Mode Error Detection" on page 15–2.

Configuration Error Detection

In configuration mode, a frame-based CRC is stored within the configuration data and contains the CRC value for each data frame.

During configuration, the Stratix III device calculates the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or configuration is complete.

In Stratix III devices, the CRC value is calculated during the configuration stage. A parallel CRC engine generates 16 CRC check bits per frame and then stores them into registers. The configuration random access memory (CRAM) chain used for storing CRC check bits is 16 bits in width and its length is equal to the frame length of the device.

User Mode Error Detection

Stratix III devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells. This feature allows all CRAM contents to be read and verified to match a configuration-computed CRC value. Soft errors are changes in a CRAM's bit state due to an ionizing particle.

The error detection capability continuously computes the CRC of the configured CRAM bits and compares it with the pre-calculated CRC. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting `nCONFIG` low).

As soon as the device transitions into user mode, you can enable the error detection process if you enable the CRC error detection option. The internal 100 MHz configuration oscillator is divided down by a factor of 2 to 256 (at powers of 2) to be used as the clock source during the error detection process. You set the clock divide factor in the option setting in the Quartus II software.

A single 16-bit CRC calculation is done on a per-frame basis. Once it has finished the CRC calculation for a frame, the resulting 16-bit signature is hex 0000 if there are no detected CRAM bit errors in a frame by the error detection circuitry and the output signal CRC_ERROR is 0. If a CRAM bit error is detected by the circuitry within a frame in the device, the resulting signature is non-zero. This causes the CRC engine to start searching the error bit location.

The error detection in Stratix III devices calculates CRC check bits for each frame and will pull the CRC_ERROR pin high when it detects bit errors in the chip. Within a frame, it can detect all single-bit, double-bit, and three-bit errors. The probability of more than three CRAM bits being flipped by an SEU event is very low. In general, for all error patterns the probability of detection is 99.998%.

The CRC engine reports the bit location and determines the type of error for all single-bit errors and over 99.641% of double-adjacent errors. The probability of other error patterns is very low and report of location of bit flips is not guaranteed by the CRC engine.

You can also read-out the error bit location through the Joint Test Action Group (JTAG) and the core interface. You would need to shift these bits out through either the JTAG instruction, SHIFT_EDERROR_REG, or the core interface before the CRC detects the next error in another frame. If the next frame also has an error, you have to shift these bits out within the amount of time of one frame CRC verification. You can choose to extend this time interval by maximum 7-frame cycles, but this will slow down the error recovery time for the SEU event. Refer to Table 15–7 for the minimum update interval for Stratix III devices. If these bits are not shifted out before the next error location is found, the previous error location and error message is overwritten by the new information. The CRC circuit continues to run, and if an error is detected, you need to decide whether to complete a reconfiguration or to ignore the CRC error.

The error detection logic continues to calculate the CRC_ERROR and 16-bit signatures for the next frame of data regardless if any error has occurred in the current frame or not. You need to monitor these signals and take the appropriate actions if a soft error occurs.

The error detection circuitry in Stratix III devices uses a 16-bit CRC-ANSI standard (16-bit polynomial) as the CRC generator.

The computed 16-bit CRC signature for each frame is stored in the registers within the core. The total storage register size is 16 (number of bits per frame) × the number of frames.

The Stratix III device error detection feature does not check memory blocks and I/O buffers. These memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because these bits use flip-flops as storage elements that are more resistant to soft errors compared to CRAM cells.

The M144K TriMatrix memory block has a built-in error correction code block that checks and corrects the errors in the block. However, for logic array blocks (LABs) that are used as MLAB memory blocks, they are ignored during error detection verification. Thus, the CRC_ERROR signal may stay solid high or low depending on the error status of the previous checked CRAM frame.

For more information on error detection in the Stratix III TriMatrix memory blocks, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook.*

In order to provide testing capability of the error detection block, a JTAG instruction EDERROR_INJECT is provided. This instruction is able to change the content of the 21-bit JTAG fault injection register, used for error injection in Stratix III devices, hence enabling the testing of the error detection block.

You can only execute the EDERROR_INJECT JTAG instruction when the device is in user mode.

Table 15–1 shows the description of the EDERROR_INJECT JTAG instruction.

Table 15–1. EDERROR_INJECT JTAG Instruction

JTAG Instruction	Instruction Code	Description
EDERROR_INJECT	00 0001 0101	This instruction controls the 21-bit JTAG fault injection register, which is used for error injection.

You can use Jam™ files (**.jam**) to automate the testing and verification process. This is a powerful design feature that allows you to verify the CRC functionality in-system, on the fly, without having to reconfigure the device. You can then switch to the CRC circuit to check for real errors induced by an SEU.

You can introduce a single error, double errors, or double errors adjacent to each other to the configuration memory. This provides an extra way to facilitate design verification and system fault tolerance characterization. Use the JTAG fault injection register with `EDERROR_INJECT` instruction to flip the readback bits. The Stratix III device is then forced into error test mode.

The content of the JTAG fault injection register is not loaded into the fault injection register during the processing of the last and the first frame. It is only loaded at the end of this period.

You can only introduce error injection in the first data frame, but you can monitor the error information at any time. For more information on the JTAG fault injection register and fault injection register, refer to "Error Detection Registers" on page 15–10.

Table 15–2 shows how the fault injection register is implemented and describes error injection.

Table 15–2. Fault Injection Register

Bit	**Bit[20..19]**			**Bit[18..8]**	**Bit[7..0]**
Description	**Error Type**			**Byte Location of the Injected Error**	**Error Byte Value**
Content	Error Type *(1)*		Error Injection Type	Depicts the location of the injected error in the first data frame.	Depicts the location of the bit error and corresponds to the error injection type selection.
	Bit[20]	Bit[19]			
	0	1	Single byte error injection		
	1	0	double-adjacent byte error injection		
	0	0	no error injection		

Note to Table 15–2:

(1) Bit[20] and Bit[19] cannot both be set to 1 as this is not a valid selection. The error detection circuitry will decode it as no error injection.

After the test completes, Altera recommends that you reconfigure the device.

Automated Single Event Upset Detection

Stratix III devices offer on-chip circuitry for automated checking of single-event upset detection. Some applications that require the device to operate error-free in high-neutron flux environments require periodic checks to ensure continued data integrity. The error detection CRC feature ensures data reliability and is one of the best options for mitigating SEU.

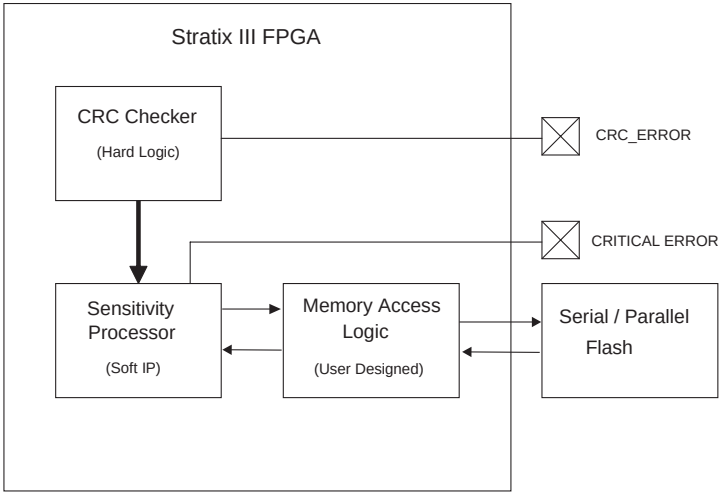
You can implement the error detection CRC feature with existing circuitry in Stratix III devices, eliminating the need for external logic. The CRC_ERROR pin reports a soft error when configuration CRAM data is corrupted, and you would have to decide whether to reconfigure the device or to ignore the error.

Critical Error Detection

Once the CRC circuit determines an error, a sensitivity processor determines the criticality of the identified error by accessing the masked configuration bitstream through the user-designed logic and alert the system for reconfiguration. If it is a non-critical error, the error detection circuitry will continue to calculate the CRC_ERROR and 16-bit signatures for the next data frame.

This feature uses a sensitivity processor reference design implementing a triple-module redundancy design technique to interface signals between the error detection block and the core IP logic. It implements three copies of the same circuit and performs a bit-wise "majority voting" on the output signals. The chance of three CRAM bits being flipped by an SEU event is very low. Figure 15–1 shows the critical error detection implementation block diagram.

Figure 15–1. Critical Error Detection Implementation Block Diagram



This reference design will be supported in future versions of the Quartus II software.

Error Detection Pin Description

Depending on the type of error detection feature you chose, you will need to use different error detection pins to monitor the data during user mode.

CRC_ERROR Pin

Table 15–3 describes the CRC_ERROR pin.

Table 15–3. CRC_ERROR Pin Description

Pin Name	Pin Type	Description
CRC_ERROR	I/O, output	Active high signal that indicates that the error detection circuit has detected errors in the configuration CRAM bits. This pin is optional and is used when the error detection CRC circuit is enabled. When the error detection CRC circuit is disabled, it is a user I/O pin. The CRC error output, when using the WYSIWYG function, is a dedicated path to the CRC_ERROR pin. The CRC_ERROR pin does not support open-drain or inversion.

CRITICAL ERROR Pin

The CRC_ERROR pin information for Stratix III devices is reported in *Device Pin-Outs* on the Literature page of the Altera website (**www.altera.com**). Table 15–4 describes the CRITICAL ERROR pin.

Table 15–4. CRITICAL ERROR Pin Description

Pin Name	Pin Type	Description
CRITICAL ERROR	I/O, output	Active high signal that indicates that the sensitivity processor reference design has detected errors in the configuration CRAM bits. This pin is optional and is used when the critical error detection is enabled.

The CRITICAL ERROR pin information for Stratix III devices will be included in *Device Pin-Outs* on the Literature page of the Altera website (**www.altera.com**) in the later revision.

Error Detection Block

You can enable the Stratix III device error detection block in the Quartus II software (refer to "Software Support" on page 15–13). This block contains the logic necessary to calculate the 16-bit CRC signature for the configuration CRAM bits in the device.

The CRC circuit continues running even if an error occurs. When a soft error occurs, the device sets the CRC_ERROR pin high. Two types of CRC detection checks the configuration bits:

- The first type is the CRAM error checking ability (16-bit CRC) during user mode, for use by the CRC_ERROR pin.
  - For each frame of data, the pre-calculated 16-bit CRC enters the CRC circuit right at the end of the frame data and determines whether there is an error or not.
  - If an error occurs, the search engine starts to find the location of the error.
  - The error messages can be shifted out through the JTAG instruction or core interface logics while the error detection block continues running.
  - The JTAG interface reads out the 16-bit CRC result for the first frame and also shifts the 16-bit CRC bits to the 16-bit CRC storage registers for test purpose.
  - Single error, double errors, or double errors adjacent to each other can be deliberately introduced to configuration memory for testing and design verification.
- The second type is the 16-bit CRC that is embedded in every configuration data frame.
  - During configuration, after a frame of data is loaded into the Stratix III device, the precomputed CRC is shifted into the CRC circuitry.
  - At the same time, the CRC value for the data frame shifted-in is calculated. If the precomputed CRC and calculated CRC values do not match, then nSTATUS is set low. Every data frame has a 16-bit CRC; therefore, there are many 16-bit CRC values for the whole configuration bitstream. Every device has different lengths of the configuration data frame.

The "Error Detection Block" section focuses on the first type, the 16-bit CRC only when the device is in user mode.

Error Detection Registers

There is one set of 16-bit registers in the error detection circuitry that store the computed CRC signature. A non-zero value on the syndrome register causes the CRC_ERROR pin to be set high. Figure 15–2 shows the block diagram of the error detection circuitry, the syndrome registers, and the error injection block.

Figure 15–2. Error Detection Block Diagram

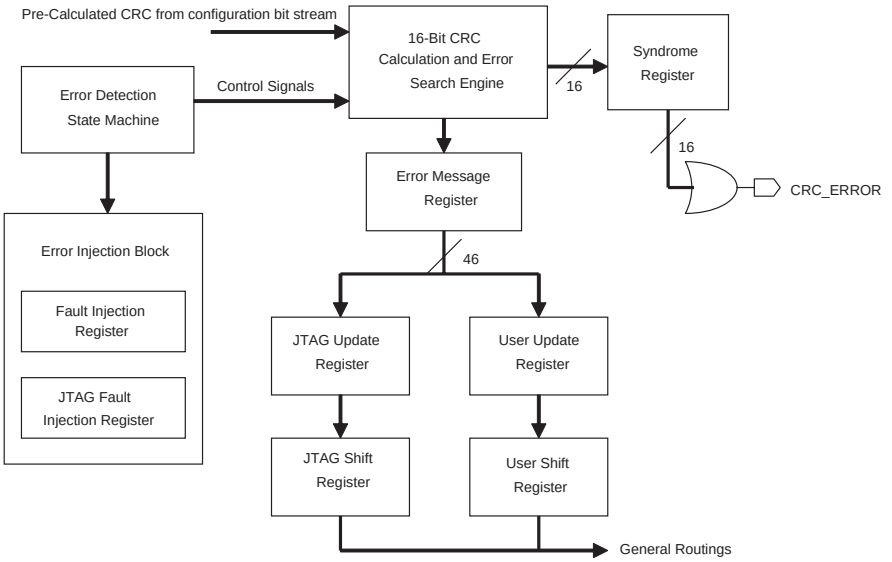


Table 15–5 defines the registers shown in Figure 15–2.

Table 15–5. Error Detection Registers (Part 1 of 2)

Register	Description
Syndrome Register	This register contains the CRC signature of the current frame through the error detection verification cycle. The CRC_ERROR signal is derived from the contents of this register.
Error Message Register	This 46-bit register contains information on the error type, location of the error and the actual syndrome. The types of errors and location reported are single and double-adjacent bit errors. The location bits for other types of errors are not identified by the Error Message Register. The content of the register can be shifted out through the JTAG SHIFT_EDERROR_REG instruction or to the core through the core interface.
JTAG Update Register	This register is automatically updated with the contents of the Error Message Register one cycle after the 46-bit register content is validated. It includes a clock enable which should be asserted prior to being sampled into the JTAG Shift Register. This requirement ensures that the JTAG Update Register is not being written into by the contents of the Error Message Register at exactly the same time that the JTAG Shift Register is reading its contents.
User Update Register	This register is automatically updated with the contents of the Error Message Register, one cycle after the 46-bit register content is validated. It includes a clock enable which should be asserted prior to being sampled into the User Shift Register. This requirement ensures that the User Update Register is not being written into by the contents of the Error Message Register at exactly the same time that the User Shift Register is reading its contents.
JTAG Shift Register	This register is accessible by the JTAG interface and allows the contents of the JTAG Update Register to be sampled and read out by JTAG instruction SHIFT_EDERROR_REG.
User Shift Register	This register is accessible by the core logic and allows the contents of the User Update Register to be sampled and read by user logic.

Table 15–5. Error Detection Registers (Part 2 of 2)	
Register	**Description**
JTAG Fault Injection Register	This 21-bit register is fully controlled by the JTAG instruction EDERROR_INJECT. This register holds the information of the error injection that you want in the bitstream.
Fault Injection Register	The content of the JTAG Fault Injection Register is loaded into this 21-bit register when it is being updated.

Error Detection Timing

When the CRC feature is enabled through the Quartus II software, the device automatically activates the CRC process upon entering user mode, after configuration, and after initialization is complete.

The CRC_ERROR pin is always pulled low at the end of the error detection cycle for a minimum of 31 cycles. Then it is pulled high at the end of the error location search, if there is a CRAM bit error. If the new CRC calculation does not contain any corrupted bits, the CRC_ERROR pin is driven low. The error detection runs until the device is reset.

The error detection circuitry runs off an internal configuration oscillator with a divisor that sets the maximum frequency. Table 15–6 shows the minimum and maximum error detection frequencies.

Table 15–6. Minimum and Maximum Error Detection Frequencies				
Device Type	**Error Detection Frequency**	**Maximum Error Detection Frequency**	**Minimum Error Detection Frequency**	**Valid Divisors (2^n)**
Stratix III	100 MHz / 2^n	50 MHz	390 kHz	1, 2, 3, 4, 5, 6, 7, 8

You can set a lower clock frequency by specifying a division factor in the Quartus II software (refer to "Software Support" on page 15–13). The divisor is a power of two (2), where *n* is between 1 and 8. The divisor ranges from 2 through 256. See the following equation:

$$\text{Error detection frequency} = \frac{100MHz}{2^n}$$

You need to monitor the error message to avoid missing information in the Error Message Register. The Error Message Register is updated whenever an error or errors occur. The minimum interval time between each update for the Error Message Register depends on the device and the error detection clock frequency. Table 15–7 shows the estimated minimum interval time between each update for the Error Message Register for Stratix III devices.

Table 15–7. Minimum Update Interval for Error Message Register *Note (1)*

Device	Timing Interval (µs)
EP3SL50	11
EP3SL70	11
EP3SL110	16
EP3SL150	16
EP3SL200	17
EP3SE260	21
EP3SL340	23
EP3SE50	11
EP3SE80	16
EP3SE110	16

Note to Table 15–7:
(1) These timing numbers are preliminary.

Software Support

The Quartus II software, starting with version 6.1, supports the error detection CRC feature for Stratix III devices. Enabling this feature generates the CRC_ERROR output to the optional dual purpose CRC_ERROR pin.

The error detection CRC feature is controlled by the **Device and Pin Options** dialog box in the Quartus II software.

Enable the error detection feature using CRC by performing the following steps:

1. Open the Quartus II software and load a project using a Stratix III device.

2. On the Assignments menu, click **Settings**. The **Settings** dialog box is shown.

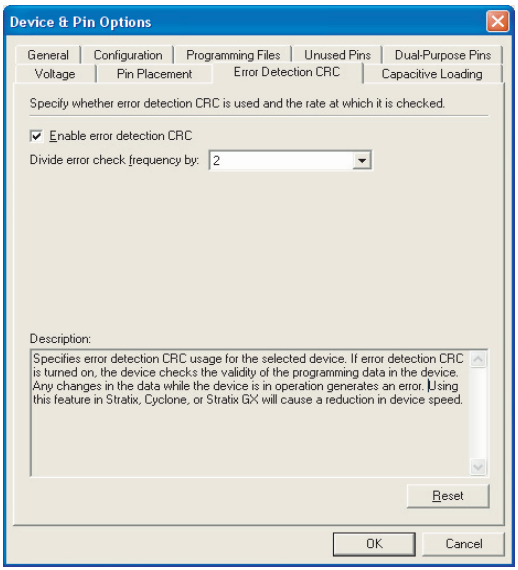
3. In the **Category** list, select **Device**. The **Device** page is shown.

4. Click **Device and Pin Options**. The **Device and Pin Options** dialog box is shown (see Figure 15–3).

5. In the **Device and Pin Options** dialog box, click the **Error Detection CRC** tab.

6. Turn on **Enable error detection CRC** (Figure 15–3).

Figure 15–3. Enabling the Error Detection CRC Feature in the Quartus II Software



7. In the **Divide error check frequency by** box, enter a valid divisor as documented in Table 15–6.

The divide value divides the frequency of the configuration oscillator output clock that clocks the CRC circuitry.

8. Click **OK**.

Recovering From CRC Errors

The system that the Stratix III device resides in must control the device reconfiguration. After detecting an error on the CRC_ERROR pin, strobing the nCONFIG signal low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the device.

When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications may require a design to account for these errors.

For more information, refer to the *SEU Mitigation In Stratix III White Paper* which will be available in early 2007.

Conclusion

The purpose of the error detection CRC feature is to detect a flip in any of the configuration CRAM bits in Stratix III devices due to a soft error. By using the error detection circuitry, you can continuously verify the integrity of the configuration CRAM bits.

For more information, refer to the *Robust SEU Mitigation with Stratix III FPGAs White Paper.*

Document Revision History

Table 15–8 shows the revision history for this document.

Table 15–8. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Minor edits to page 2, 3, 4, and 14. Updated Table 15–5.	Minor edits.
November 2006 v1.0	Initial Release	—

Section V. Power and Thermal Management

This section provides information on Power and Thermal Management for the Stratix® III devices.

- Chapter 16, Programmable Power and Temperature Sensing Diode in Stratix III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

16. Programmable Power and Temperature Sensing Diode in Stratix III Devices

SIII51016-1.1

Introduction

The total power of an FPGA includes static power and dynamic power. Static power is the power consumed by the FPGA when it is programmed but no clocks are operating, while dynamic power is comprised of the switching power when the device is configured and running. The dynamic power is calculated with the following equation:

Equation 16–1. Dynamic Power Equation

$$P = \frac{1}{2}CV^2 \times \text{frequency} \times \text{toggle rate}$$

From the equation, frequency and toggle rate are design-dependent. However, voltage can be varied to lower dynamic power consumption by the square value of the voltage difference. Stratix® III devices minimize static and dynamic power with advanced process optimizations, selectable core voltage, and the revolutionary programmable power technology. These technologies enable Stratix III designs to optimally meet design-specific performance requirements with the lowest possible power.

The Quartus® II software optimizes all designs with the Stratix III power technology to ensure performance is met at the lowest power consumption. This automatic process allows designers to concentrate on the functionality of their design, instead of the power consumption of the design.

Power consumption also affects thermal management. Stratix III offers a temperature sensing diode (TSD) with embedded analog-to-digital converter (ADC) circuitry which eliminates the need for an external temperature sensing chip on the board. The Stratix III TSD can self-monitor the device junction temperature and be used with external circuitry for activities such as controlling air flow to the FPGA.

Stratix III Power Technology

The following section provides details about Stratix III selectable core voltage and programmable power technology.

Selectable Core Voltage

Altera offers a series of low-voltage Stratix products that have the ability to power the core logic of the device with either a 0.9-V or 1.1-V power supply. This power supply, called V_{CCL}, powers the LAB, MLAB, DSP blocks, TriMatrix memory blocks, clock networks, and routing lines. The periphery, consisting of the I/O registers and their routing connections are powered by V_{CC} with a 1.1-V power supply. You can use the same 1.1-V power supply if you want both V_{CC} and V_{CCL} to be 1.1 V.

Lowering the core voltage reduces both static and dynamic power, but causes a reduction in performance. You need to set the correct core supply voltage in the Quartus II settings under **Operating Conditions**, since Quartus II analyzes the core power consumption and timing delays based on this selection. When you compile a design, you can select either 0.9-V or 1.1-V core voltage. You can compare the power and performance trade-offs of a 0.9-V core voltage compilation result and a 1.1-V core voltage compilation result and then choose the desirable core voltage for your design. Quartus II defaults the core voltage to 1.1 V.

Ensure that the board has a separate 0.9-V power supply to utilize the lower voltage option, and ensure that you connect V_{CCL} to the voltage level that you set in Quartus II. The Stratix III device cannot distinguish which core voltage level is used on the board. Connecting to the wrong voltage level will give you different timing delays and power consumption than what is reported by the Quartus II software.

Refer to the *AN 437: Power Optimization Techniques* for information about the selectable core voltage performance and power effects on sample designs.

Programmable Power Technology

In addition to the ability to change the core voltage, Stratix III also offers the ability to configure portions of the core, called tiles, for high-speed or low-power mode of operation performed by Quartus II without user intervention. This programmable power technology, used to reduce static power, utilizes an on-chip voltage regulator, powered by VCCPT. In a design compilation, Quartus II determines whether a tile needs to be in high-speed or low-power mode based on the timing constraints of the design.

Refer to *AN 437: Power Optimization Techniques* for more information about how Quartus II uses programmable power technology when compiling a design.

A Stratix III tile can consist of the following:

- MLAB/LAB pairs with routing to the pair
- MLAB/LAB pairs with routing to the pair and to adjacent DSP/memory block routing
- TriMatrix memory blocks
- DSP blocks
- I/O interfaces

All blocks and routing associated with the tile share the same setting of either high speed or low power. Tiles that include DSP blocks, memory blocks, or I/O interfaces are set to high-speed mode by default for optimum performance when used in the design. Unused DSP blocks, memory blocks, and I/O elements are set to low-power mode to minimize static power. Clock networks do not support the programmable power technology.

With programmable power technology, faster speed grade FPGAs may require less power, as there will be fewer high-speed MLAB and LAB pairs, compared to slower speed grade FPGAs. The slower speed grade device may need to use more high-speed MLAB and LAB pairs to meet the performance requirements, while the faster speed grade device can meet the performance requirements with MLAB and LAB pairs in low-power mode.

Quartus II can set unused, unshared inputs and unused device resources in the design in low-power mode to reduce static and dynamic power. Quartus II can set the following resources to low power when they are not used in the design:

- LABs and MLABs
- TriMatrix memory blocks
- External memory interface circuitry
- DSP blocks
- PLL
- SERDES and DPA blocks

If the PLL is instantiated in the design, asserting a reset high keeps the PLL in low power.

Relationship Between Selectable Core Voltage and Programmable Power Technology

Table 16–1 shows the Stratix III programmable power capabilities. Speed grade considerations can add to the permutations to give you flexibility in designing your system.

Table 16–1. Stratix III Programmable Power Capabilities

	Selectable Core Voltage	Programmable Power Technology
LAB	Yes	Yes
Routing	Yes	Yes
Memory Blocks	Yes	Fixed setting *(1)*
DSP Blocks	Yes	Fixed setting *(1)*
Global Clock Networks	Yes	No
I/O Elements	No	Fixed setting *(1)*

Note to Table 16–1:

(1) Tiles with DSP blocks, memory blocks, and I/O elements that are used in the design are always set to the high-speed mode. Unused DSP blocks, memory blocks, and I/O interfaces are set to low-power mode by default.

Stratix III External Power Supply Requirements

This section describes the different external power supplies needed to power Stratix III devices. Table 16–2 lists the external power supply pins for Stratix III devices. Some of the power supply pins can be supplied with the same external power supply, provided they need the same voltage level, as noted in the recommended board connection column. For possible values of each power supply, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in the *Stratix III Device Handbook*.

Table 16–2. Stratix III Power Supply Requirements

Power Supply Pin	Recommended Board Connection	Description
VCCL	VCCL	Selectable core voltage power supply
VCC	VCC	I/O registers power supply
VCCD_PLL	VCCD_PLL	PLL digital power supply
VCCA_PLL	VCCA_PLL *(1)*	PLL analog power supply
VCCPT		Power supply for the programmable power technology
VCCPGM	VCCPGM	Configuration pins power supply
VCCPD	VCCPD *(2)*	I/O pre-driver power supply
VCCIO	VCCIO *(1)*	I/O power supply
VCC_CLKIN		Differential clock input pins power supply (top and bottom I/O banks only)
VCCBAT	VCCBAT	Battery back-up power supply for design security volatile key register
VREF	VREF *(3)*	Power supply for the voltage-referenced I/O standards
GND	GND	Ground

Notes to Table 16–2:

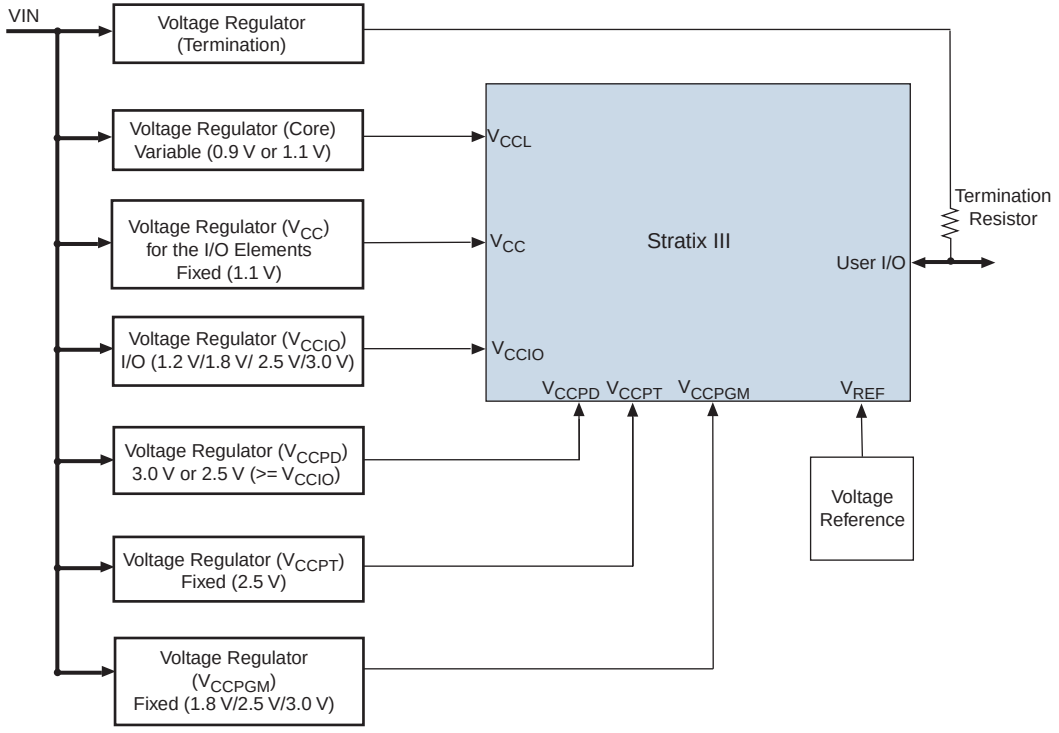
(1) Designers can minimize the number of external power supplies by shorting the two pins in the left column and supplying both pins with the power supply (if the voltage levels needed are the same).

(2) V_{CCPD} voltage must be equal to or greater than V_{CCIO}.

(3) There is one VREF pin per I/O bank. You can use an external power supply or a resistor divider network to supply this voltage.

Figure 16–1 shows an example of power management for Stratix III devices.

Figure 16–1. Stratix III Power Management Example



Temperature Sensing Diode

Knowing the junction temperature is crucial for thermal management. Historically, junction temperature is calculated using ambient or case temperature, junction-to-ambient (θ_{ja}) or junction-to-case (θ_{jc}) thermal resistance, and the device power consumption. A Stratix III device can monitor its die temperature with an embedded temperature sensing diode (TSD) with ± 5°C accuracy, so you can control the air flow to the device.

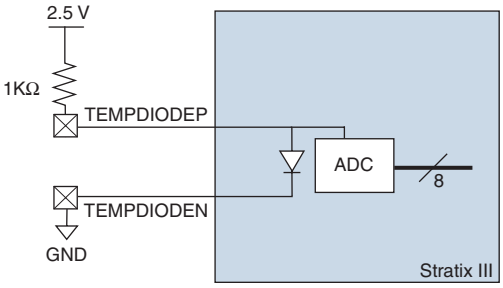
The Stratix III TSD uses the characteristics of a PN junction diode to determine die temperature. Stratix III also has built-in ADC circuitry, without an external temperature sensor. The ADC can be bypassed if designers want to use an external temperature sensor, similar to the Stratix II solution.

The following section describes the Stratix III TSD in detail.

External Pin Connections

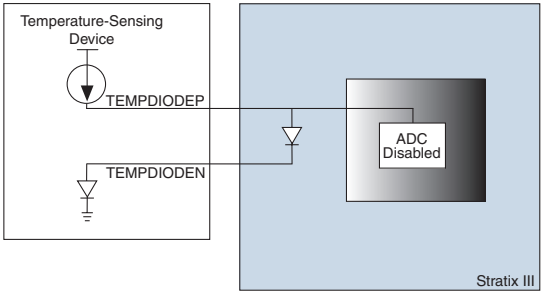
The Stratix III TSD, located in the top right corner of the die, requires two pins for voltage reference. When both TSD and ADC are used, connect the TEMPDIODEP pin to a 1-KΩ external resistor and connect the TEMPDIODEN pin to ground, as shown in Figure 16–2.

Figure 16–2. Connections When Both TSD and ADC are Used



The ADC circuit can be bypassed when the sensing diode is connected to an external temperature sensor. This scheme, shown in Figure 16–3, is very similar to the Stratix II TSD connection.

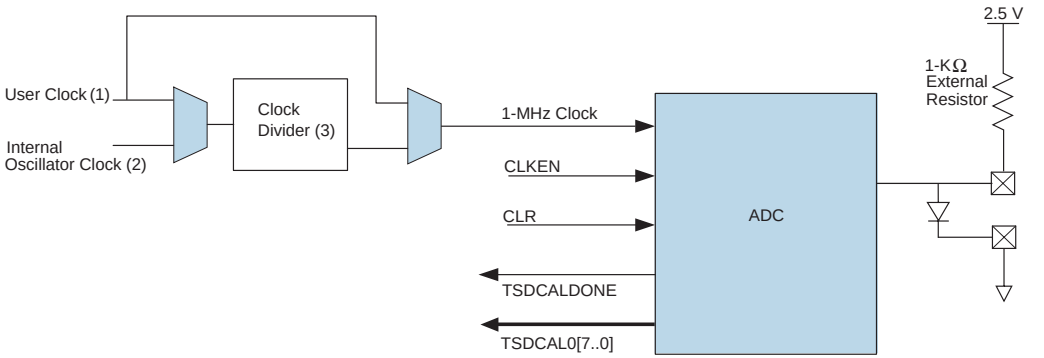
Figure 16–3. Connections When ADC is Bypassed



Architecture Description

Figure 16–4 shows the block diagram for Stratix III TSD circuitry, including the ADC block, accessible via WYSIWYG in the Quartus II software. The ports to the TSD and ADC are shown in Table 16–3. When the ADC is used, the Stratix III TSD has two different modes of operations: power-up mode and user mode. When you include the TSD in your design, the TSD circuit automatically calibrates itself upon power-up and reads the initial temperature of the die. In user mode, you can request for the ADC to convert the temperature sensed by the diode by asserting the `clken` signal. When not used, the ADC circuitry is disabled to reduce static power.

Figure 16–4. Stratix III Temperature Sensing Diode Block Diagram



Notes to Figure 16–4:

(1) The user clock must be provided in user mode. This signal only accepts either a 1-MHz or 40-MHz input clock.
(2) The internal oscillator clock is only available for power-up mode to calibrate the TSD and ADC circuitry.
(3) The clock divider block is bypassed when input to `CLK` is 1 MHz (set by user).

Table 16–3. Temperature Sensing Diode Ports

Port Name	Input/Output	Description
CLK	Input	Clock for ADC
CLKEN	Input	Clock enable and request signal
CLR	Input	Reset
TSDCALDONE	Output	Done signal for temperature reading
TSDCALO	Output	Eight-bit digital output showing the temperature read

The circuit consists of the sensing diode and an ADC block. The ADC block can accept either a 1-MHz or a 40-MHz clock that will be divided down to create a 1-MHz clock. In power-up mode, the clock comes from the internal oscillator. In user mode, you need to provide a user clock. The `clken` signal must be asserted to request a temperature sensing operation. The circuit then outputs an 8-bit digital reading (`TSDCALO[7..0]`) that maps to a specific temperature. The `TSDCALDONE` signal is asserted to indicate that the `TSDCALO` outputs are ready to be read.

Signals `TSDCALO[7..0]` shows the temperature read in 2's complement. Table 16–4 lists examples of the conversion from 2's complement to actual temperatures.

Table 16–4. Temperature Output Mapping Examples in 2's Complement

8-bit TSDCALO [7:0]	Temperature
00000000	0°C
00011001	25°C
01010101	85°C
01111101	125°C

Conclusion

As process geometries get smaller, power and thermal management is becoming more crucial in FPGA designs. Stratix III offers the programmable power technology and selectable core voltage options for low power operation. These features, along with the speed grade choices, can be used in different permutations to give the best power and performance combination. Taking advantage of the silicon, the Quartus II software is able to manipulate designs to use the best combination to achieve lowest power at the required performance.

For thermal management, the Stratix III temperature sensing diode uses an embedded analog-to-digital converter, enabling designers to easily incorporate this feature in their designs. Being able to monitor the junction temperature of the device at any time also allows designers to control air flow to the device and save power for the whole system.

Document Revision History

Table 16–5 shows the revision history for this document.

Table 16–5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
May 2007 v1.1	Replaced all instances of VCCR with VCCPT	Minor update.
November 2006 v1.0	Initial Release	—

Section VI. Packaging Information

This section provides packaging information for the Stratix® III device.

- Chapter 17, Stratix III Device Packaging Information

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

17. Stratix III Device Packaging Information

SIII51017-1.1

Introduction

This chapter provides package information for Altera® Stratix® III devices, including:

- Device and package cross reference
- Thermal resistance values
- Package outlines

Tables 1 shows which Stratix III devices, respectively, are available in FineLine BGA® (FBGA) packages.

Table 1. Stratix III Devices in FBGA Packages (Part 1 of 2)

Device	Package	Pins
EP3SL50	FineLine BGA - Flip Chip	484
	FineLine BGA - Flip Chip	780
EP3SL70	FineLine BGA - Flip Chip	484
	FineLine BGA - Flip Chip	780
EP3SL110	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152
EP3SL150	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152
EP3SL200	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152
	FineLine BGA - Flip Chip	1517
EP3SL340	FineLine BGA - Flip Chip	1152
	FineLine BGA - Flip Chip	1517
	FineLine BGA - Flip Chip	1760
EP3SE50	FineLine BGA - Flip Chip	484
	FineLine BGA - Flip Chip	780
EP3SE80	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152
EP3SE110	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152

Table 1. Stratix III Devices in FBGA Packages (Part 2 of 2)		
Device	**Package**	**Pins**
EP3SE260	FineLine BGA - Flip Chip	780
	FineLine BGA - Flip Chip	1152
	FineLine BGA - Flip Chip	1517

Thermal Resistance

For thermal resistance specifications for Stratix III devices, refer to the *Stratix Series Device Thermal Resistance Data Sheet*.

Package Outlines

Stratix III device package outlines can be downloaded from the *Device Packaging Specifications* web page.

Document Revision History

Table 2 shows the revision history for this document.

Table 2. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
May 2007 v1.1	Removed thermal resistance and package outline information and replaced with links referencing this information.	Minor update.
November 2006 v1.0	Initial Release	—

Stratix III Device Handbook, Volume 2

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SIII5V2-1.3

Contents

Chapter Revision Dates

The chapter in this book, *Stratix III Device Handbook, Volume 2*, was revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Stratix III Device Datasheet: DC and Switching Characteristics
Revised: *May 2007*
Part number: *SIII52001-1.3*

About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® III family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table :
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*

Visual Cue	Meaning
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>*.**pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

1. Stratix III Device Datasheet: DC and Switching Characteristics

SIII52001-1.3

Electrical Characteristics

Operating Conditions

When Stratix® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix III devices, system designers must consider the operating requirements discussed in this chapter. Stratix III devices are offered in both commercial and industrial grades. Commercial devices are offered in -2 (fastest), -3, and -4 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1–1. Stratix III Device Absolute Maximum Ratings (Part 1 of 2) *Note (1)*

Symbol	Parameter	Minimum	Maximum	Unit
V_{CCL}	Selectable core voltage power supply	-0.5	1.65	V
V_{CC}	I/O registers power supply	-0.5	1.65	V
V_{CCD_PLL}	PLL digital power supply	-0.5	1.65	V
V_{CCA_PLL}	PLL analog power supply	-0.5	3.75	V
V_{CCPT}	Programmable power technology power supply	-0.5	3.75	V
V_{CCPGM}	Configuration pins power supply	-0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V_{CCIO}	I/O power supply	-0.5	3.9	V
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	-0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.75	V
V_I	DC Input voltage	-0.5	4.0	V
T_J	Operating junction temperature	-55	125	°C

Table 1–1. Stratix III Device Absolute Maximum Ratings (Part 2 of 2) Note (1)				
Symbol	**Parameter**	**Minimum**	**Maximum**	**Unit**
I_{OUT}	DC output current, per pin	-25	40	mA
T_{STG}	Storage temperature (No bias)	-65	150	°C

Note to Table 1–1:
(1) Supply voltage specifications apply to voltage readings taken at the device pins, not the power supply.

Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over device lifetime. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device. A DC signal is equivalent to

100 % duty cycle. For example, a signal that overshoots to 4.25 V can only be at 4.25 V for 9 % over the lifetime of the device: for a device lifetime of 10 years, this amounts to 9/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions

Symbol	Parameter	Condition	Overshoot duration as % of high time	Unit
Vi(AC)	AC Input Voltage	4	100.000	%
		4.05	79.330	%
		4.1	46.270	%
		4.15	27.030	%
		4.2	15.800	%
		4.25	9.240	%
		4.3	5.410	%
		4.35	3.160	%
		4.4	1.850	%
		4.45	1.080	%
		4.5	0.630	%
		4.55	0.370	%
		4.6	0.220	%
		4.65	0.130	%
		4.7	0.074	%
		4.75	0.043	%
		4.8	0.025	%
		4.85	0.015	%

Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Stratix III devices. The steady-state voltage and current values expected from Stratix III devices are provided in Table 1–3. All supplies are required to monotonically reach their full-rail values within t_{RAMP}. Maximum allowed ripple on power supplies is bounded by the minimum and maximum specifications listed Table 1–3.

Table 1–3. Stratix III Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCL}	Selectable core voltage power supply for internal logic and input buffers	—	1.05	1.1	1.15	V
	Selectable core voltage power supply for internal logic and input buffers	—	0.86	0.9	0.94	V
V_{CC}	I/O registers power supply	—	1.05	1.1	1.15	V
V_{CCD_PLL}	PLL digital power supply	—	1.05	1.1	1.15	V
V_{CCA_PLL}	PLL analog power supply	—	2.375	2.5	2.625	V
V_{CCPT}	Power supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPGM}	Configuration pins power supply, 3.0 V	—	2.85	3	3.15	V
	Configuration pins power supply, 2.5 V	—	2.375	2.5	2.625	V
	Configuration pins power supply, 1.8 V	—	1.71	1.8	1.89	V
V_{CCPD} *(1)*	I/O pre-driver power supply, 3.0 V	—	2.85	3	3.15	V
	I/O pre-driver power supply, 2.5 V	—	2.375	2.5	2.625	V
V_{CCIO}	I/O power supply, 3.0 V	—	2.85	3	3.15	V
	I/O power supply, 2.5 V	—	2.375	2.5	2.625	V
	I/O power supply, 1.8 V	—	1.71	1.8	1.89	V
	I/O power supply, 1.5 V	—	1.425	1.5	1.575	V
	I/O power supply, 1.2 V	—	1.14	1.2	1.26	V
V_{CC_CLKIN}	Differential clock input power supply (top and bottom I/O banks only)	—	2.375	2.5	2.625	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	1.0	2.5	3.0	V
V_I	DC Input voltage	—	-0.3	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	-40	—	100	°C

Table 1–3. Stratix III Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{RAMP}	Power Supply Ramptime	Normal POR (PORSEL=0)	100 µs	—	100 ms	—
		Fast POR (PORSEL=1)	50 µs	—	12 ms	—

Note to Table 1–3:
(1) V_{CCPD} must be equal to or greater than V_{CCIO}.

DC Characteristics

This section lists the input pin capacitances, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with the resources used, use the Excel based Early Power Estimator to get supply current estimates for your design.

Table 1–4 lists supply current specifications for V_{CC_CLKIN} and V_{CCPGM}. Use the EPE to get supply current estimates for remaining power supplies.

Table 1–4. Supply Current Specifications for Vcc_clkin and Vccpgm

Symbol	Parameter	Min	Max	Unit
I_{CLKIN}	V_{CC_CLKIN} current specifications	0	250	mA
I_{PGM}	V_{CCPGM} current specifications	0	250	mA

I/O Pin Leakage Current

Table 1–5 defines Stratix III I/O Pin leakage current specifications.

Table 1–5. Stratix III I/O Pin Leakage Current Note (1), (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	-10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	-10	—	10	µA

Notes to Table 1–5:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5 and 1.2 V).

(2) 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

On-Chip Termination (OCT) Specifications

If OCT calibration is enabled, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 1–6 lists the Stratix III OCT calibration block accuracy specifcations.

Table 1–6. Stratix III On-Chip Termination Calibration Accuracy Specifications (Part 1 of 2) Note (1) - Preliminary

Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial	Industrial	
25-Ω R_S 3.0/2.5	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0/2.5 V	5	—	%
50-Ω R_S 3.0/2.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0/2.5 V	5	—	%
50-Ω R_T 2.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5 V	10	—	%
50-Ω R_S 1.8	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 1.8 V	5	—	%
50-Ω R_S 1.8	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	5	—	%
50-Ω R_T 1.8	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8 V	10	—	%
50-Ω R_S 1.5	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	8	—	%
50-Ω R_T 1.5	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.5 V	10	—	%
50-Ω R_S 1.2	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	8	—	%

Table 1–6. Stratix III On-Chip Termination Calibration Accuracy Specifications (Part 2 of 2) Note (1) - Preliminary					
Symbol	Description	Conditions	Calibration Accuracy		Unit
			Commercial	Industrial	
50-Ω R_T 1.2	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.2 V	10	—	%

Note to Table 1–6:
(1) OCT calibration accuracy is valid at the time of calibration only.

The accuracy listed in Table 1–6 is valid at the time of calibration. If the voltage or temperature changes, the termination resistance value varies. Table 1–7 lists the resistance tolerance for Stratix III on chip termination.

Table 1–7. On-Chip Termination Resistance Tolerance Specification for I/Os - Preliminary Note (1)				
Symbol	Description	Resistance Tolerance		Units
		Commercial Max	Industrial Max	
R_{OCT_UNCAL}	Internal series termination without calibration	30	—	%
R_{OCT_CAL}	Internal series termination with calibration	*(1)*	—	%

Note to Table 1–7:
(1) For resistance tolerance after power-up calibration, refer to Equation 1–1 and Table 1–8.

Table 1–8 lists OCT variation with temperature and voltage after power-up calibration. Use Table 1–8 and Equation 1–1 to determine OCT variation without re-calibration.

Equation 1–1. OCT Variation Without Re-Calibration *Note (1)*

$$R_{OCT} = R_{CAL}\left(1 + \frac{dR}{dT} \times \Delta T + \frac{dR}{dV} \times \Delta V\right)$$

Note to Equation 1–1:
(1) R_{CAL} is calibrated on chip termination at power up. ΔT and ΔV are variations in temperature and voltage w.r.t temperature and V_{CCIO} values respectively, at power up.

Table 1–8. On-Chip Termination Variation after Power-up Calibration *Note (1)*

Symbol	Description	V_{CCIO} (V)	Commercial Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3	0.029	%/mV
		2.5	0.036	%/mV
		1.8	0.033	%/mV
		1.5	0.033	%/mV
		1.2	0.033	%/mV
dR/dT	OCT variation with temperature without re-calibration	3	0.294	%/°C
		2.5	0.301	%/°C
		1.8	0.355	%/°C
		1.5	0.344	%/°C
		1.2	0.348	%/°C

Note to Table 1–8:
(1) Valid for V_{CCIO} range of +/- 5% and temperature range of 0° to 85° C.

Pin Capacitance

Table 1–9 shows the Stratix III device family pin capacitance.

Table 1–9. Stratix III Device Capacitance (Part 1 of 2) *Note (1)* *- Preliminary*

Symbol	Parameter	Typical	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	8	pF
C_{IOLR}	Input capacitance on left/right I/O pins	8	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	5	pF

Table 1–9. Stratix III Device Capacitance (Part 2 of 2) Note (1) - Preliminary			
Symbol	**Parameter**	**Typical**	**Unit**
C_{CLKLR}	Input capacitance on left/right dedicated clock input pins	5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	8	pF

Note to Table 1–9:
(1) Minimum and maximum values are pending silicon characterization.

Hot Socketing

Table 1–10 lists the hot socketing specifications for Stratix III devices.

Table 1–10. Stratix III Hot Socketing Specifications		
Symbol	**Parameter**	**Maximum**
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA for ≤10 ns

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for all I/O standards supported by Stratix III devices. Tables 1–11 to Table 1–16 show the Stratix III device family I/O standard specifications. Refer to Table 1–151 for explanation of terms used in the tables below. V_{OL} and V_{OH} values are valid at the corresponding I_{OL} and I_{OH}, respectively.

Table 1–11. Single-Ended I/O Standards Specifications

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V_{CCIO} - 0.2	0.1	-0.1
2.5 V LVTTL/ LVCMOS	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.2	2.1	0.1	-0.1
		2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
		2.5	2.625	-0.3	0.7	1.7	3.6	0.7	1.7	2	-2
1.8V LVTTL / LVCMOS	1.71	1.8	1.89	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} -0.45	2	-2
1.5 V LVTTL/ LVCMOS	1.425	1.5	1.575	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
1.2V LVTTL / LVCMOS	1.14	1.2	1.26	-0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	-2
3.0-V PCI	2.85	3	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	3.6	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 * V_{CCIO}	0.5 * V_{CCIO}	—	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	-0.5

Refer to the figure in "Single-Ended Voltage Referenced I/O Standard" in the Table 1–151 for voltage referenced receiver input waveform and explanation of terms used in the table below.

Table 1–12. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 CLASS I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 CLASS I, II	1.71	1.8	1.89	0.46 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 CLASS I, II	1.425	1.5	1.575	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	0.47 * V_{CCIO}	V_{REF}	0.53 * V_{CCIO}
HSTL-18 CLASS I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—

Table 1–12. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—

Table 1–13. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 CLASS I	-0.3	V_{REF} - 0.15	V_{REF} +0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	VTT - 0.57	VTT + 0.57	8.1	-8.1
SSTL-2 CLASS II	-0.3	V_{REF} - 0.15	V_{REF} +0.15	V_{CCIO} + 0.3	V_{REF} - 0.31	V_{REF} + 0.31	VTT - 0.76	VTT + 0.76	16.2	-16.2
SSTL-18 CLASS I	-0.3	V_{REF} -0.125	V_{REF} +0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	VTT - 0.475	VTT + 0.475	6.7	-6.7
SSTL-18 CLASS II	-0.3	V_{REF} -0.125	V_{REF} +0.125	V_{CCIO} + 0.3	V_{REF} -0.25	V_{REF} + 0.25	0.28	V_{CCIO} -0.28	13.4	-13.4
SSTL-15 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	-8
SSTL-15 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	-16
HSTL-18 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	8	-8
HSTL-18 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	16	-16
HSTL-15 CLASS I	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	8	-8
HSTL-15 CLASS II	-0.3	V_{REF} -0.1	V_{REF} +0.1	V_{CCIO} + 0.3	V_{REF} -0.2	V_{REF} + 0.2	0.4	V_{CCIO} -0.4	16	-16
HSTL-12 CLASS I	-0.15	V_{REF} - 0.08	V_{REF} +0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	-8
HSTL-12 CLASS II	-0.15	V_{REF} - 0.08	V_{REF} +0.08	V_{CCIO} + 0.15	V_{REF} -0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	-16

Refer to the figures for "Differential I/O Standards" in Table 1–151 for receiver input and transmitter output waveforms, and for all differential I/O standards (LVDS, mini-LVDS, RSDS).

Table 1–14. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO} (V)			$V_{SWING\ (DC)}$ (V)		$V_{X\ (AC)}$ (V)			$V_{SWING(\ AC)}$ (V)		$V_{OX\ (AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 CLASS I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.2	—	$V_{CCIO}/2$ + 0.2	0.6	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.15	—	$V_{CCIO}/2$ + 0.15
SSTL-18 CLASS I, II	1.71	1.8	1.89	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ - 0.125	—	$V_{CCIO}/2$ + 0.125
SSTL-15 CLASS I, II	1.425	1.5	1.575	0.2	—	—	$V_{CCIO}/2$	—	0.4	—	—	$V_{CCIO}/2$	—

Table 1–15. Differential HSTL I/O Standards Specifications

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 CLASS I	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 CLASS I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 CLASS I, II	1.14	1.2	1.26	0.2	—	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	—

Table 1–16. Differential I/O Standard Specifications (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (Row I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05 *(1)*	$D_{max} \leq 700$ Mbps	1.8 *(1)*	0.247	—	0.6	1.125	1.25	1.375
	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	1.05 *(1)*	D_{max} > 700 Mbps	1.55 *(1)*	—	—	—	—	—	—

Table 1–16. Differential I/O Standard Specifications (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
2.5 V LVDS (Column I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05 *(1)*	D_{max} ≤700 Mbps	1.8 *(1)*	0.247	—	0.6	1.0	1.25	1.5
	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	1.05 *(1)*	D_{max} > 700 Mbps	1.55 *(1)*	—	—	—	—	—	1.5
RSDS (Row I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
RSDS (Column I/O)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.5
Mini-LVDS (Row I/O)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.4
Mini-LVDS (Column I/0)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	0.5	1.2	1.5
LVPECL (Column I/0) *(3)*	2.375 *(4)*	2.5 *(4)*	2.625 *(4)*	300	—	—	0.6	D_{max} ≤700 Mbps	1.8 *(5)*	—	—	—	—	—	—
	—	—	—	—	—	—	0.6	D_{max} > 700 Mbps	1.6 *(5)*	—	—	—	—	—	—

Notes to Table 1–16:

(1) For data rate: D_{max} > 700 Mbps, the minimum input voltage is 1.0 V, the maximum input voltage is 1.6 V. For D_{max} ≤700 Mbps, the minimum input voltage is 0 V, the maximum input voltage is 1.85 V.

(2) R_L range: 90 ≤R_L ≤110 ohm.

(3) LVPECL specifications apply only to CLK input pins on column I/Os.

(4) Power supply for input differential buffer is V_{CC_CLKIN}.

(5) For data rate D_{max} > 700 Mbps, the minimum input voltage is 0.85 V, the maximum input voltage is 1.75 V. For data rate D_{max} ≤700 Mbps, the minimum input voltage is 0.45 V, the maximum input voltage is 1.95 V.

Power Consumption

Altera offers two ways to estimate power for a design: the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides better quality estimates based on the specifics of the design after the place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

See Table 1–4 for supply current estimates for V_{CCPGM} and V_{CC_CLKIN}. Use the EPE and PowerPlay Power Analyzer for current estimates of remaining power supplies.

For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapters in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Stratix III core and periphery blocks for commercial grade devices.

These characteristics can be designated as ***Preliminary*** and ***Final*** and each designation is defined below.

Preliminary

Preliminary characteristics are created using simulation results, process data, and other known parameters.

Final

Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage and junction temperature conditions. The upper-right hand corner of a table shows the designation as **Preliminary** or **Final**.

Core Performance Specifications

This sections describes the Clock Tree, PLL, DSP, TriMatrix, and Configuration and JTAG Specifications.

Clock Tree Specifications

Table 1–17 lists the clock tree performance specifications for the logic array, DSP blocks, and TriMatrix Memory blocks for Stratix III devices.

Table 1–17. Stratix III Clock Tree Performance (Part 1 of 2) - Preliminary

Device	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
EP3SL50	600	500	450	450	375	MHz
EP3SL70	600	500	450	450	375	MHz

Table 1–17. Stratix III Clock Tree Performance (Part 2 of 2) - Preliminary

Device	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
EP3SL110	600	500	450	450	375	MHz
EP3SL150	600	500	450	450	375	MHz
EP3SL200	600	500	450	450	375	MHz
EP3SE260	*(1)*	500	450	450	375	MHz
EP3SL340	*(1)*	500	450	450	375	MHz
EP3SE50	600	500	450	450	375	MHz
EP3SE80	600	500	450	450	375	MHz
EP3SE110	600	500	450	450	375	MHz

Note to Table 1–17:
(1) Device is not offered in -2 Speed Grade.

PLL Specifications

Table 1–18 describes the Stratix III PLL specifications when operating in both the commercial junction temperature range (0 to 85° C) and the industrial junction temperature range (-40 to 100° C). Refer to the figure in "PLL Specifications" in Table 1–151 for PLL block diagram.

Table 1–18. Stratix III PLL Specifications (Part 1 of 2) - Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	5	—	720 *(1)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{VCO}	PLL VCO operating range	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
t_{INCCJ}	Input clock cycle to cycle jitter	—	—	*(3)*	—
f_{OUT}	Output frequency for internal global or regional clock	—	—	717 *(2)*	MHz
f_{OUT_EXT}	Output frequency for external clock output	—	—	717 *(2)*	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{OUTPJ_DC}	Period jitter for dedicated clock output	—	—	*(3)*	ps
t_{OUTPJ_IO}	Period jitter for clock output on regular I/O	—	—	*(3)*	ps
t_{FCOMP}	External feedback clock compensation time	—	—	*(3)*	ns
$t_{CONFIGPLL}$	Time required to reconfigure PLL scan chain	—	*(3)*	—	scanclk cycles

Table 1–18. Stratix III PLL Specifications (Part 2 of 2) - Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	1	—	1	scanclk cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
t_{LOCK}	Time required to lock from end of device configuration	—	—	*(3)*	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	*(3)*	ms
f_{CLBW}	PLL closed-loop low bandwidth range	—	*(3)*	—	MHz
	PLL closed-loop medium bandwidth range	—	*(3)*	—	MHz
	PLL closed-loop high bandwidth range	—	*(3)*	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	*(3)*	—	ps
t_{ARESET}	Minimum pulse width on `areset` signal	10	—	—	ns

Notes to Table 1–18:
(1) f_{IN} is limited by I/O f_{max}.
(2) This specification is limited by the lower of the two: I/O f_{max} or f_{out} of the PLL.
(3) Pending silicon characterization.

DSP Block Specifications

Table 1–19 describes the Stratix III DSP block performance specifications.

Table 1–19. Stratix III DSP Block Performance Specifications (Part 1 of 2) Note (1) - Preliminary

Mode	Number of Multipliers	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
		V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
9×9-bit multiplier	1	490	405	375	375	300	MHz
12×12-bit multiplier	1	490	405	375	375	300	MHz
18×18-bit multiplier	1	550	455	420	420	340	MHz
36×36-bit multiplier	1	440	365	335	335	270	MHz
18×18-bit multiply accumulator	4	490	405	375	375	300	MHz
18×18-bit multiply adder	4	490	405	375	375	300	MHz
18×18-bit multiply adder-signed full precision	2	490	405	375	375	300	MHz
18×18-bit multiply adder with loopback *(2)*	2	390	320	300	240	180	MHz
36-bit shift (32 bit data)	1	440	365	335	335	270	MHz

Table 1–19. Stratix III DSP Block Performance Specifications (Part 2 of 2) Note (1) - Preliminary							
Mode	Number of Multipliers	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
		V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
Double mode	1	440	365	335	335	270	MHz

Note to Table 1–19:
(1) Maximum is for fully pipelined block with **Round** and **Saturation** disabled.
(2) Maximum for non-pipelined block with loopback input registers disabled and Round and Saturation disabled

TriMatrix Memory Block Specifications

Table 1–20 describes the Stratix III TriMatrix Memory Block specifications.

Table 1–20. Stratix III TriMatrix Memory Block Performance Specifications (Part 1 of 2) - Preliminary									
Memory Block Type	Mode	ALUTs	TriMatrix Memory	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
				V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
MLAB	Single port 64×10	0	1	600	500	450	450	375	MHz
	Simple dual-port 32x20 single clock	0	1	600	500	450	450	375	MHz
	Simple dual-port 64x10 single clock	0	1	600	500	450	450	375	MHz
M9K	Single-port 256×36	0	1	600	500	450	450	325	MHz
	Simple dual-port 256×36 single clock	0	1	600	500	450	450	325	MHz
	True dual port 512×18 single clock	0	1	600	500	450	450	325	MHz

Table 1–20. Stratix III TriMatrix Memory Block Performance Specifications (Part 2 of 2) - Preliminary

Memory Block Type	Mode	ALUTs	TriMatrix Memory	-2 Speed Grade	-3 Speed Grade	-4 Speed Grade	-4L Speed Grade		Unit
				V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 1.1V	V_{CCL} = 0.9V	
M144K	Single-port 2K×72	0	1	600	500	450	450	325	MHz
	Simple dual-port 2K×72 dual clock	0	1	600	500	450	450	325	MHz
	Simple dual-port 2K×64 dual clock (with ECC)	0	1	333	275	250	250	200	MHz
	True dual-port 4K×36 dual clock	0	1	600	500	450	450	325	MHz

Configuration and JTAG Specifications

Table 1–21 lists the Stratix III Configuration Mode Specifications.

Table 1–21. Stratix III Configuration Mode Specifications - Preliminary

Programming Mode	DCLK F_{max}	Unit
Passive Serial	100	MHz
Fast Passive Parallel *(1)*	100	MHz
Fast Active Serial	40	MHz
Remote Update only in Fast AS mode	10	MHz

Note to Table 1–21:

(1) Data rate must be 4× slower than the clock when Decompression and/or Encryption are used.

Table 1–22 shows the JTAG timing parameters and values for Stratix III devices. Refer to figure for "HIGH-SPEED I/O Block" in Table 1–151 for JTAG timing requirements.

Table 1–22. Stratix III JTAG Timing Parameters and Values - Preliminary

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU}(TDI)	JTAG port setup time for TDI	1	—	ns
t_{JPSU}(TMS)	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 *(1)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(1)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(1)*	ns

Note to Table 1–22:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.3 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Stratix III Temperature Sensing Diode Specifications

Table 1–23 lists the specifications for the Stratix III temperature sensing diode.

Table 1–23. Stratix III Temperature Sensing Diode Specifications - Preliminary

Symbol	Parameter	Min	Max	Unit
f_{TSD_INCLK}	TSD Input Clock Frequency (without CLK divider)	0.25	1.01	MHz
	TSD Input Clock Frequency (with CLK divider)	38	42	MHz
$t_{DUTY\_TSD\_INCLK}$	Duty Cycle of TSD Input Clock	45	55	%

Periphery Performance

This section describes the periphery performance, including High-Speed I/O and External Memory Interface, and OCT Calibration Block specifications.

High-Speed I/O Specifications

Refer to the Table 1–151 for definitions of high-speed timing specifications.

Table 1–24 shows the high-speed I/O timing for Stratix III devices.

Table 1–24. High Speed I/O Specifications for -2 Speed Grade *Notes (1), (2), (7)* **- Preliminary**

Symbol	Conditions	-2 Speed Grade			
		Min	Typ	Max	Unit
f_{HSCLK} (input clock frequency) $f_{HSCLK} = f_{HSDR} / W$	Clock boost factor W = 2 to 32 *(3)*	5 *(5)*	—	625	MHz
	Clock boost factor W = 1 (SERDES bypass)	5 *(5)*	—	600 *(6)*	MHz
	Clock boost factor W = 1 (SERDES used)	150	—	717	MHz
f_{HSDR} (data rate)	SERDES factor J = 4 to 10	150	—	1,250	Mbps
	SERDES factor J = 2, Uses DDR Registers	*(4)*	—	*(5)*	Mbps
	SERDES factor J = 1, Uses SDR Register	*(4)*	—	600 *(6)*	Mbps
$f_{HSDRDPA}$ (DPA data rate)	SERDES factor J = 4 to 10	150	—	1,250	Mbps
TCCS	All differential I/O standards		—	*(5)*	ps
SW	All differential I/O standards	*(5)*	—	*(5)*	ps
t_{OUTPJ_DC}	—	—	—	*(5)*	ps
t_{OUTPJ_IO}	—	—	—	*(5)*	ps
Output t_{RISE}	All differential I/O standards	—	—	*(5)*	ps
Output t_{FALL}	All differential I/O standards	—	—	*(5)*	ps
t_{DUTY}	tx output clock duty cycle	45	50	55	%
DPA run length	—	—	—	*(5)*	UI

Table 1–24. High Speed I/O Specifications for -2 Speed Grade Notes (1), (2), (7) - Preliminary					
Symbol	Conditions	-2 Speed Grade			
		Min	Typ	Max	Unit
DPA jitter tolerance	Data channel peak-to-peak jitter tolerance	(5)	—	—	UI

Notes to Table 1–24:
(1) When J = 4 to 10, the SERDES block is used.
(2) When J = 1 or 2, the SERDES block is bypassed.
(3) The input clock frequency and the W factor must satisfy the following Left/Right PLL output frequency specification: 150 MHz ≤nput clock frequency × W ≤1250 MHz.
(4) The minimum specification is dependent on the clock source (PLL and clock pin, for example) and the clock routing resource (global, regional, or local) utilized. The I/O differential buffer and input register do not have a minimum toggle rate.
(5) Pending silicon characterization.
(6) Same as Device Clock tree f_{max}.
(7) Specifications for -3 and -4 speed grades will be available after silicon characterization.

Table 1–25. DPA Lock Time Specifications - Preliminary						
Standard	Training Pattern	Transition Density	Min	Typ	Max	Unit
SPI-4	00000000001111111111	10%	256	—	—	Number of repetitions
Parallel Rapid I/O	00001111	25%	256	—	—	Number of repetitions
	10010000	50%	256	—	—	Number of repetitions
Miscellaneous	10101010	100%	256	—	—	Number of repetitions
	01010101	—	256	—	—	Number of repetitions

External Memory Interface Specifications

Table 1–26 to Table 1–32 list the external memory interface specifications for the Stratix III device family.

Use the following tables to perform memory interface timing analysis.

Table 1–26. Stratix III Maximum Clock Rate Support for External Memory Interfaces *Notes (1)*

Memory Standards	–2 Speed Grade (MHz)		–3 Speed Grade (MHz)		–4 Speed Grade (MHz)		-4L Speed Grade (MHz) *(2)*	
	Top/ Bottom I/O Banks	Left/ Right I/O Banks *(3)*	Top/ Bottom I/O Banks	Left/ Right I/O Banks *(3)*	Top/ Bottom I/O Banks	Left/ Right I/O Banks *(3)*	Top/ Bottom I/O Banks	Left/ Right I/O Banks
DDR3 SDRAM *(4)*	400 *(5)*	300	333	TBD *(6)*	333	TBD *(6)*	—	—
DDR2 SDRAM *(4)*	400 *(5)*	300	333	267	333	267	200	167
DDR SDRAM *(4)*	200	200	200	200	200	200	200	167
QDRII+ SRAM	350	300	300	250	300	250	—	—
QDRII SRAM	350	300	300	250	300	250	167	133
RLDRAM II	400	300	300	250	300	250	—	—

Notes to Table 1–26:

(1) Numbers are based on half-rate controller and are preliminary until characterization is final.
(2) Performance is based on 0.9-V core voltage. At 1.1-V core voltage, the -4L speed grade devices have the same performance as the -4 speed grade devices.
(3) Left/right I/O banks have lower maximum performance than the top/bottom I/O banks due to the left/right I/Os having higher pin capacitance to support the LVDS I/O standard.
(4) This applies for interfaces with both modules and components.
(5) DDR3/DDR2 SDRAM interfaces above 333 MHz requires the use of the deskew circuitry pending characterization.
(6) Support will be evaluated after characterization.

External Memory I/O Timing Specifications

Table 1–27 and Table 1–28 list Stratix III device timing uncertainties on the read and write data paths. Use these specifications to determine timing margins for source synchronous paths between the Stratix III FPGA and the external memory device. Refer to the figure for "SW (sampling window)" in Table 1–151.

Table 1–27. Sampling Window (SW) - Read Side (Part 1 of 2) - Preliminary

Commercial Speed Grade	Location	Memory Type	Sampling Window (ps)	
			Setup	Hold
-2	VIO	DDR2	250	250
-3	VIO	DDR2	300	300
-4	VIO	DDR2	374	374
-2	VIO	DDR3	250	250

Table 1–27. Sampling Window (SW) - Read Side (Part 2 of 2) - Preliminary

Commercial Speed Grade	Location	Memory Type	Sampling Window (ps)	
			Setup	Hold
-3	VIO	DDR3	300	300
-4	VIO	DDR3	374	374
-4	VIO	DDR1	250	250
-2	VIO	QDRII / II +	260	260
-3	VIO	QDRII / II +	303	303
-4	VIO	QDRII / II +	364	364
-2	VIO	RLDRAM II	250	250
-3	VIO	RLDRAM II	333	333
-4	VIO	RLDRAM II	400	400
-2	HIO	DDR2	250	250
-3	HIO	DDR2	280	280
-4	HIO	DDR2	375	375
-2	HIO	DDR3	250	250
-3	HIO	DDR3	300	300
-4	HIO	DDR3	374	374
-4	HIO	DDR1	250	250
-2	HIO	QDRII / II +	260	260
-3	HIO	QDRII / II +	312	312
-4	HIO	QDRII / II +	390	390
-2	HIO	RLDRAM	250	250
-3	HIO	RLDRAM	333	333
-4	HIO	RLDRAM	400	400

Table 1–28. Transmitter Channel-to-Channel Skew (TCCS) - Write Side (Part 1 of 2) - Preliminary

Commercial Speed Grade	Location	Memory Type	TCCS (ps)	
			Lead	Lag
-2	VIO	DDR2	267	267
-3	VIO	DDR2	321	321
-4	VIO	DDR2	400	400
-2	VIO	DDR3	267	267
-3	VIO	DDR3	321	321

Table 1–28. Transmitter Channel-to-Channel Skew (TCCS) - Write Side (Part 2 of 2) - Preliminary

Commercial Speed Grade	Location	Memory Type	TCCS (ps)	
			Lead	Lag
-4	VIO	DDR3	400	400
-4	VIO	DDR1	267	267
-2	VIO	QDRII / II +	277	277
-3	VIO	QDRII / II +	323	323
-4	VIO	QDRII / II +	388	388
-2	VIO	RLDRAM II	267	267
-3	VIO	RLDRAM II	356	356
-4	VIO	RLDRAM II	428	428
-2	HIO	DDR2	267	267
-3	HIO	DDR2	300	300
-4	HIO	DDR2	401	401
-2	HIO	DDR3	267	267
-3	HIO	DDR3	321	321
-4	HIO	DDR3	400	400
-4	HIO	DDR1	267	267
-2	HIO	QDRII / II +	277	277
-3	HIO	QDRII / II +	333	333
-4	HIO	QDRII / II +	416	416
-2	HIO	RLDRAM II	267	267
-3	HIO	RLDRAM II	321	321
-4	HIO	RLDRAM II	401	401

DLL and DQS Logic Block Specifications

Table 1–29 describes the DLL Frequency Range specifications for Stratix III devices.

Table 1–29. Stratix III DLL Frequency Range Specifications - Preliminary

Frequency Mode	Frequency Range (MHz)	Resolution (Degrees)
0	100–167	22.5
1	167-220	30
2	220–267	36
3	267-350	30

Table 1–29. Stratix III DLL Frequency Range Specifications - Preliminary		
Frequency Mode	**Frequency Range (MHz)**	**Resolution (Degrees)**
4	350-400	36
5	400	45

Table 1–30 describes the DQS Phase Offset Delay per stage for Stratix III devices.

Table 1–30. DQS Phase Offset Delay per Stage Notes (1), (2), (3) - Preliminary			
Speed Grade	**Min**	**Max**	**Unit**
-2	9	14	ps
-3	9	14	ps
-4	9	14	ps

Notes to Table 1–30:

(1) The delay settings are linear.

(2) The DQS phase shift is the sum of the DLL delay settings and the user selected phase offset settings. The valid settings for phase offset are -64 to +63 for frequency mode 0 and -32 to +31 for frequency modes 1, 2, and 3. You should continuously monitor the DLL delay settings to determine how many phase offset settings are available for your system.

(3) The typical value equals the average of the minimum and maximum values.

OCT Calibration Block Specifications

Table 1–31 shows the on-chip terminination calibration block specifications for Stratix III devices.

Table 1–31. On-Chip Termination Calibration Block Specification - Preliminary

Symbol	Description	Min	Typical	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
t_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT Rs and Rt calibration	—	1000	—	cycles
$t_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out per OCT calibration block	—	28	—	cycles
t_{RS_RT}	Time required to dynamically switch from Rs to Rt	—	2.5	—	ns

DCD Specifications

Table 1–32 lists the worst case duty cycle distortion for Stratix III devices. Detailed information on duty cycle distortion will be published after characterization.

Table 1–32. Duty Cycle Distortion on Stratix III I/O Pins *Notes (1), (2)* **- Preliminary**

Symbol	-2 Speed Grade		-3 Speed Grade		-4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	—
Output Duty Cycle *(2)*	45	55	45	55	45	55	%

Notes to Table 1–32:

(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree and IOE driving dedicated and general purpose I/O pins.

(2) Detailed DCD specifications pending silicon characterization.

I/O Timing

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix III device densities and speed grades. This section describes and specifies the performance of I/Os.

All specifications except the fast model are representative of worst-case supply voltage and junction temperature conditions. Fast model specifications are representative of best case process, supply voltage, and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.1.

Preliminary, Correlated and Final Timing

Timing models can have either preliminary, correlated or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 1–33 shows the status of the Stratix III device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Correlated numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Final timing numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Stratix III family devices have been completely characterized and no further changes to the timing model are expected.

Table 1–33. Stratix III Device Timing Model Status Note (1)

Device	Preliminary	Correlated	Final
EP3SL70	✓	—	—
EP3SL150	✓	—	—
EP3SL200	✓	—	—
EP3SL340	✓	—	—
EP3SE50	✓	—	—
EP3SE110	✓	—	—
EP3SE260	✓	—	—

Note to Table 1–33:

(1) EP3SL50, EP3SL110, and EP3SE80 devices are not supported in the Quartus II software verion 6.1.

I/O Timing Measurement Methodology

Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time (t_{SU}) and hold time (t_H). The Quartus II software uses the following equations to calculate t_{SU} and t_H timing for Stratix III devices input signals.

t_{SU} =

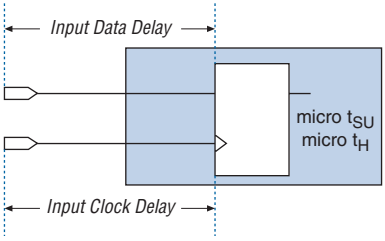
- + data delay from input pin to input register
- + micro setup time of the input register
- - clock delay from input pin to input register

t_H =

- - data delay from input pin to input register
- + micro hold time of the input register
- + clock delay from input pin to input register

Figure 1–1 shows the setup and hold timing diagram for input registers.

Figure 1–1. Input Register Setup and Hold Timing Diagram



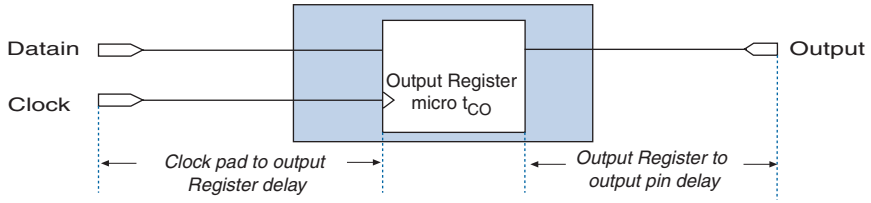
For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 1–34. The following equation describes clock pin to output pin timing for Stratix III devices.

The t_{CO} from clock pin to I/O pin =

- + delay from clock pad to I/O output register
- + IOE output register clock-to-output delay
- + delay from output register to output pin

Figure 1–2. Output Register Clock to Output Timing Diagram



Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 1–34.

2. Record the time to VMEAS.

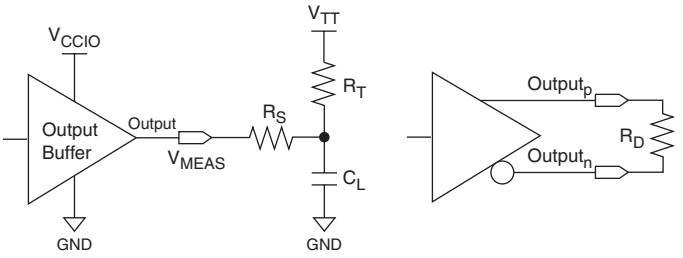
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to VMEAS.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 1–34 using the above equation. Figure 1–3 shows the model of the circuit that is represented by the output timing of the Quartus II software.

Figure 1–3. Output Register Clock to Output Timing Diagram



Notes to Figure 1–3:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

Table 1–34. Ouptut Timing Measurement methodology for Output Pins (Part 1 of 2)

I/O Standard	Loading and Terminations								Measurement Point
	R_S	R_D	R_T	V_{CCIO}	V_{CCPD}	V_{CC}	V_{TT}	C_L (pF)	V_{MEAS} (v)
LVTTL	—	—	—	2.85	2.85	1.05	—	0	1.425
LVCMOS	—	—	—	2.85	2.85	1.05	—	0	1.425
2.5v	—	—	—	2.375	2.375	1.05	—	0	1.1875
1.8v	—	—	—	1.71	2.375	1.05	—	0	0.855
1.5v	—	—	—	1.425	2.375	1.05	—	0	0.7125
1.2v	—	—	—	1.14	2.375	1.05	—	0	0.57
PCI	—	—	—	2.85	2.85	1.05	—	10	1.425
PCI-X	—	—	—	2.85	2.85	1.05	—	10	1.425
SSTL-2 CLASS I	25	—	50	2.325	2.325	1.02	1.099	0	1.1625
SSTL-2 CLASS II	25	—	25	2.325	2.325	1.02	1.099	0	1.1625
SSTL-18 CLASS I	25	—	50	1.66	2.325	1.02	0.773	0	0.83
SSTL-18 CLASS II	25	—	25	1.66	2.325	1.02	0.773	0	0.83
SSTL-15 CLASS I	25	—	50	1.375	2.325	1.02	0.634	0	0.6875
SSTL-15 CLASS II	25	—	25	1.375	2.325	1.02	0.634	0	0.6875
1.8v HSTL CLASS I	—	—	50	1.66	2.325	1.02	0.773	0	0.83
1.8v HSTL CLASS II	—	—	25	1.66	2.325	1.02	0.773	0	0.83

Table 1–34. Ouptut Timing Measurement methodology for Output Pins (Part 2 of 2)

I/O Standard	Loading and Terminations								Measurement Point
	R_S	R_D	R_T	V_{CCIO}	V_{CCPD}	V_{CC}	V_{TT}	C_L (pF)	V_{MEAS} (v)
1.5v HSTL CLASS I	—	—	50	1.375	2.325	1.02	0.634	0	0.6875
1.5v HSTL CLASS II	—	—	25	1.375	2.325	1.02	0.634	0	0.6875
1.2v HSTL CLASS I	—	—	50	1.09	2.325	1.02	0.512	0	0.545
1.2v HSTL CLASS II	—	—	25	1.09	2.325	1.02	0.512	0	0.545
Differential SSTL-2 CLASS I	25	—	50	2.325	2.325	1.02	1.099	0	1.1625
Differential SSTL-2 CLASS II	25	—	25	2.325	2.325	1.02	1.099	0	1.1625
Differential SSTL-18 CLASS I	25	—	50	1.66	2.325	1.02	0.773	0	0.83
Differential SSTL-18 CLASS II	25	—	25	1.66	2.325	1.02	0.773	0	0.83
1.8v Differential HSTL CLASS I	—	—	50	1.66	2.325	1.02	0.773	0	0.83
1.8v Differential HSTL CLASS II	—	—	25	1.66	2.325	1.02	0.773	0	0.83
1.5v Differential HSTL CLASS I	—	—	50	1.375	2.325	1.02	0.634	0	0.6875
1.5v Differential HSTL CLASS II	—	—	25	1.375	2.325	1.02	0.634	0	0.6875
LVDS	—	100	—	2.375	2.325	1.02	—	0	1.1875

Notes:
(1) Hypertransport is not supported by Stratix III.
(2) LVPECL outputs are not supported by Stratix III.
(3) Quartus timing conditions can be changed using the Advanced I/O Timing feature.
(4) V_{CC} is nominally 1.1 v less 50 mV (1.05 v).
(5) Terminated I/O standards require an additional 30 mV IR drop on Vcc (1.02 v).

I/O Default Capacitive Loading

See Figure 1–35 for default capacitive loading of different I/O standards

Table 1–35. Default Loading of Different I/O Standards for Stratix III

I/O Standard	Capacitive Load	Unit
3.0 V LVTTL	0	pF
3.0 V LVCMOS	0	pF
2.5 V LVTTL/LVCMOS	0	pF
1.8 V LVTTL/LVCMOS	0	pF
1.5 V LVTTL/LVCMOS	0	pF
3.0 V PCI	10	pF
3.0 V PCI-X	10	pF
SSTL-2 CLASS I	0	pF
SSTL-2 CLASS II	0	pF
SSTL-18 CLASS I	0	pF
SSTL-18 CLASS II	0	pF
1.5-V HSTL CLASS I	0	pF
1.5-V HSTL CLASS II	0	pF
1.8-V HSTL CLASS I	0	pF
1.8-V HSTL CLASS II	0	pF
1.2-V HSTL	0	pF
Differential SSTL-2 CLASS I	0	pF
Differential SSTL-2 CLASS II	0	pF
Differential SSTL-18 CLASS I	0	pF
Differential SSTL-18 CLASS II	0	pF
1.8-V Differential HSTL CLASS I	0	pF
1.8-V Differential HSTL CLASS II	0	pF
1.5-V Differential HSTL CLASS I	0	pF
1.5-V Differential HSTL CLASS II	0	pF
1.2-V Differential HSTL CLASS I	0	pF
1.2-V Differential HSTL CLASS II	0	pF
LVDS	0	pF

Programmable IOE Delay

Table 1–36 shows Stratix III IOE programmable delay settings. Refer to Figure 7-8 in the Stratix III Device I/O Features chapter for annotation of delays in the IOE.

Table 1–36. Stratix III IOE Programmable Delay

Parameter	Available Settings	-2 Speed Grade	
		Minimum Delay (ps)	Maximum Delay (ps)
T1	16	150	900
T2	8	330	700
T3	8	155	2581
T9	16	123	897
T10	7	118	377

Programmable Output Buffer Delay

Table 1–37 lists the delay chain settings that control the rising and falling edge delays of the output buffer. Default delay is 0ps.

Table 1–37. Programmable Output Buffer Delay

Symbol	Parameter	Typical	Units
D_{OUTBUF}	Rising and/or Falling Edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

User I/O Pin Timing

Table 1–38 to Table 1–108 show user I/O pin timing for Stratix III devices. I/O buffer t_{SU}, t_H, and t_{CO} are reported for the cases when I/O clock is driven by a non-PLL global clock (GCLK) and a PLL driven global clock (GCLK-PLL). For t_{SU}, t_H and t_{CO} using regional clock, add the value from the adder tables listed for each device to the GCLK/GCLK-PLL values for the device.

EP3SL70 I/O Timing Parameters

Table 1–38 through Table 1–42 show the maximum I/O timing parameters for EP3SL70 devices for single ended I/O standards.

Table 1–38 specifies EP3SL70 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–38. EP3SL70 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.544	-1.114	-1.184	-1.258	-1.220	-1.803	ns
		t_H	—	0.613	1.252	1.344	1.444	1.394	1.963	ns
	GCLK PLL	t_{SU}	—	0.445	0.839	1.000	1.211	1.139	1.096	ns
		t_H	—	-0.376	-0.701	-0.840	-1.025	-0.965	-0.936	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.544	-1.114	-1.184	-1.258	-1.220	-1.803	ns
		t_H	—	0.613	1.252	1.344	1.444	1.394	1.963	ns
	GCLK PLL	t_{SU}	—	0.445	0.839	1.000	1.211	1.139	1.096	ns
		t_H	—	-0.376	-0.701	-0.840	-1.025	-0.965	-0.936	ns
2.5 V	GCLK	t_{SU}	—	-0.549	-1.125	-1.196	-1.270	-1.232	-1.815	ns
		t_H	—	0.618	1.262	1.356	1.456	1.406	1.975	ns
	GCLK PLL	t_{SU}	—	0.440	0.828	0.988	1.199	1.127	1.084	ns
		t_H	—	-0.371	-0.691	-0.828	-1.013	-0.953	-0.924	ns
1.8 V	GCLK	t_{SU}	—	-0.559	-1.145	-1.220	-1.294	-1.256	-1.839	ns
		t_H	—	0.628	1.282	1.379	1.480	1.429	1.998	ns
	GCLK PLL	t_{SU}	—	0.430	0.808	0.964	1.175	1.103	1.060	ns
		t_H	—	-0.361	-0.671	-0.805	-0.989	-0.930	-0.901	ns
1.5 V	GCLK	t_{SU}	—	-0.539	-1.104	-1.173	-1.246	-1.208	-1.792	ns
		t_H	—	0.608	1.242	1.333	1.432	1.382	1.952	ns
	GCLK PLL	t_{SU}	—	0.450	0.849	1.011	1.223	1.151	1.107	ns
		t_H	—	-0.381	-0.711	-0.851	-1.037	-0.977	-0.947	ns
1.2 V	GCLK	t_{SU}	—	-0.482	-0.990	-1.039	-1.111	-1.073	-1.658	ns
		t_H	—	0.552	1.128	1.200	1.298	1.249	1.819	ns
	GCLK PLL	t_{SU}	—	0.507	0.963	1.145	1.358	1.286	1.241	ns
		t_H	—	-0.437	-0.825	-0.984	-1.171	-1.110	-1.080	ns

Table 1–38. EP3SL70 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.422	-0.867	-0.896	-0.966	-0.929	-1.515	ns
		t_H	—	0.492	1.007	1.059	1.155	1.106	1.678	ns
	GCLK PLL	t_{SU}	—	0.567	1.086	1.288	1.503	1.430	1.384	ns
		t_H	—	-0.497	-0.946	-1.125	-1.314	-1.253	-1.221	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.422	-0.867	-0.896	-0.966	-0.929	-1.515	ns
		t_H	—	0.492	1.007	1.059	1.155	1.106	1.678	ns
	GCLK PLL	t_{SU}	—	0.567	1.086	1.288	1.503	1.430	1.384	ns
		t_H	—	-0.497	-0.946	-1.125	-1.314	-1.253	-1.221	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.398	-0.816	-0.836	-0.907	-0.870	-1.455	ns
	GCLK PLL	t_{SU}	—	0.591	1.137	1.348	1.562	1.489	1.623	ns
		t_H	—	-0.520	-0.994	-1.180	-1.369	-1.309	1.444	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.398	-0.816	-0.836	-0.907	-0.870	-1.276	ns
	GCLK PLL	t_{SU}	—	0.591	1.137	1.348	1.562	1.489	-1.455	ns
		t_H	—	-0.520	-0.994	-1.180	-1.369	-1.309	1.623	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.384	-0.789	-0.804	-0.874	-0.837	1.623	ns
	GCLK PLL	t_{SU}	—	0.605	1.164	1.380	1.595	1.522	1.444	ns
		t_H	—	-0.533	-1.021	-1.212	-1.401	-1.341	-1.276	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.384	-0.789	-0.804	-0.874	-0.837	-1.423	ns
	GCLK PLL	t_{SU}	—	0.605	1.164	1.380	1.595	1.522	1.591	ns
		t_H	—	-0.533	-1.021	-1.212	-1.401	-1.341	1.476	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.398	-0.816	-0.836	-0.907	-0.870	1.476	ns
	GCLK PLL	t_{SU}	—	0.591	1.137	1.348	1.562	1.489	-1.308	ns
		t_H	—	-0.520	-0.994	-1.180	-1.369	-1.309	-1.423	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.398	-0.816	-0.836	-0.907	-0.870	1.623	ns
	GCLK PLL	t_{SU}	—	0.591	1.137	1.348	1.562	1.489	1.444	ns
		t_H	—	-0.520	-0.994	-1.180	-1.369	-1.309	-1.276	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.384	-0.789	-0.804	-0.874	-0.837	-1.455	ns
	GCLK PLL	t_{SU}	—	0.605	1.164	1.380	1.595	1.522	1.623	ns
		t_H	—	-0.533	-1.021	-1.212	-1.401	-1.341	1.444	ns

Table 1–38. EP3SL70 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.384	-0.789	-0.804	-0.874	-0.837	-1.276	ns
	GCLK PLL	t_{SU}	—	0.605	1.164	1.380	1.595	1.522	-1.455	ns
		t_H	—	-0.533	-1.021	-1.212	-1.401	-1.341	1.623	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.377	-0.774	-0.788	-0.858	-0.821	1.444	ns
	GCLK PLL	t_{SU}	—	0.612	1.179	1.396	1.611	1.538	-1.276	ns
		t_H	—	-0.540	-1.035	-1.228	-1.417	-1.357	-1.423	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.377	-0.774	-0.788	-0.858	-0.821	1.591	ns
	GCLK PLL	t_{SU}	—	0.612	1.179	1.396	1.611	1.538	1.476	ns
		t_H	—	-0.540	-1.035	-1.228	-1.417	-1.357	-1.308	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.544	-1.114	-1.184	-1.258	-1.220	-1.423	ns
		t_H	—	0.613	1.252	1.344	1.444	1.394	1.591	ns
	GCLK PLL	t_{SU}	—	0.445	0.839	1.000	1.211	1.139	1.476	ns
		t_H	—	-0.376	-0.701	-0.840	-1.025	-0.965	-1.308	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.544	-1.114	-1.184	-1.258	-1.220	-1.423	ns
		t_H	—	0.613	1.252	1.344	1.444	1.394	1.591	ns
	GCLK PLL	t_{SU}	—	0.445	0.839	1.000	1.211	1.139	1.476	ns
		t_H	—	-0.376	-0.701	-0.840	-1.025	-0.965	-1.308	ns

Table 1–39 specifies EP3SL70 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–39. EP3SL70 Row Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.466	-0.957	-1.007	-1.064	-1.035	-1.591	ns
		t_H	—	0.537	1.098	1.172	1.256	1.213	1.756	ns
	GCLK PLL	t_{SU}	—	0.516	0.985	1.166	1.391	1.312	1.296	ns
		t_H	—	-0.445	-0.844	-1.001	-1.199	-1.134	-1.131	ns

Table 1–39. EP3SL70 Row Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.466	-0.957	-1.007	-1.064	-1.035	-1.591	ns
		t_H	—	0.537	1.098	1.172	1.256	1.213	1.756	ns
	GCLK PLL	t_{SU}	—	0.516	0.985	1.166	1.391	1.312	1.296	ns
		t_H	—	-0.445	-0.844	-1.001	-1.199	-1.134	-1.131	ns
2.5 V	GCLK	t_{SU}	—	-0.471	-0.967	-1.018	-1.076	-1.047	-1.602	ns
		t_H	—	0.542	1.108	1.184	1.268	1.225	1.768	ns
	GCLK PLL	t_{SU}	—	0.511	0.975	1.155	1.379	1.300	1.285	ns
		t_H	—	-0.440	-0.834	-0.989	-1.187	-1.122	-1.119	ns
1.8 V	GCLK	t_{SU}	—	-0.486	-0.998	-1.055	-1.114	-1.083	-1.641	ns
		t_H	—	0.557	1.139	1.220	1.306	1.261	1.806	ns
	GCLK PLL	t_{SU}	—	0.500	0.949	1.124	1.348	1.270	1.252	ns
		t_H	—	-0.429	-0.808	-0.959	-1.156	-1.092	-1.087	ns
1.5 V	GCLK	t_{SU}	—	-0.465	-0.957	-1.007	-1.065	-1.035	-1.593	ns
		t_H	—	0.536	1.098	1.172	1.257	1.213	1.758	ns
	GCLK PLL	t_{SU}	—	0.521	0.990	1.172	1.397	1.318	1.300	ns
		t_H	—	-0.450	-0.849	-1.007	-1.205	-1.140	-1.135	ns
1.2 V	GCLK	t_{SU}	—	-0.408	-0.840	-0.871	-0.927	-0.898	-1.457	ns
		t_H	—	0.479	0.982	1.037	1.121	1.078	1.623	ns
	GCLK PLL	t_{SU}	—	0.578	1.107	1.308	1.535	1.455	1.436	ns
		t_H	—	-0.507	-0.965	-1.142	-1.341	-1.275	-1.270	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.340	-0.701	-0.709	-0.762	-0.735	-1.293	ns
		t_H	—	0.412	0.844	0.877	0.958	0.916	1.461	ns
	GCLK PLL	t_{SU}	—	0.642	1.241	1.464	1.693	1.612	1.594	ns
		t_H	—	-0.570	-1.098	-1.296	-1.497	-1.431	-1.426	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.340	-0.701	-0.709	-0.762	-0.735	-1.293	ns
		t_H	—	0.412	0.844	0.877	0.958	0.916	1.461	ns
	GCLK PLL	t_{SU}	—	0.642	1.241	1.464	1.693	1.612	1.594	ns
		t_H	—	-0.570	-1.098	-1.296	-1.497	-1.431	-1.426	ns

Table 1–39. EP3SL70 Row Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.300	-0.617	-0.612	-0.665	-0.638	-1.198	ns
		t_H	—	0.373	0.765	0.783	0.866	0.824	1.369	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.567	1.797	1.715	1.695	ns
		t_H	—	-0.613	-1.182	-1.396	-1.596	-1.529	-1.524	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.300	-0.617	-0.612	-0.665	-0.638	-1.198	ns
		t_H	—	0.373	0.765	0.783	0.866	0.824	1.369	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.567	1.797	1.715	1.695	ns
		t_H	—	-0.613	-1.182	-1.396	-1.596	-1.529	-1.524	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.286	-0.589	-0.580	-0.633	-0.605	-1.166	ns
		t_H	—	0.359	0.738	0.752	0.834	0.792	1.338	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.599	1.829	1.748	1.727	ns
		t_H	—	-0.627	-1.209	-1.427	-1.628	-1.561	-1.555	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.286	-0.589	-0.580	-0.633	-0.605	-1.166	ns
		t_H	—	0.359	0.738	0.752	0.834	0.792	1.338	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.599	1.829	1.748	1.727	ns
		t_H	—	-0.627	-1.209	-1.427	-1.628	-1.561	-1.555	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.300	-0.617	-0.612	-0.665	-0.638	-1.198	ns
		t_H	—	0.373	0.765	0.783	0.866	0.824	1.369	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.567	1.797	1.715	1.695	ns
		t_H	—	-0.613	-1.182	-1.396	-1.596	-1.529	-1.524	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.300	-0.617	-0.612	-0.665	-0.638	-1.198	ns
		t_H	—	0.373	0.765	0.783	0.866	0.824	1.369	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.567	1.797	1.715	1.695	ns
		t_H	—	-0.613	-1.182	-1.396	-1.596	-1.529	-1.524	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.286	-0.589	-0.580	-0.633	-0.605	-1.166	ns
		t_H	—	0.359	0.738	0.752	0.834	0.792	1.338	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.599	1.829	1.748	1.727	ns
		t_H	—	-0.627	-1.209	-1.427	-1.628	-1.561	-1.555	ns

Table 1–39. EP3SL70 Row Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.286	-0.589	-0.580	-0.633	-0.605	-1.166	ns
		t_H	—	0.359	0.738	0.752	0.834	0.792	1.338	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.599	1.829	1.748	1.727	ns
		t_H	—	-0.627	-1.209	-1.427	-1.628	-1.561	-1.555	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.279	-0.575	-0.564	-0.616	-0.589	-1.150	ns
		t_H	—	0.352	0.724	0.735	0.817	0.776	1.321	ns
	GCLK PLL	t_{SU}	—	0.707	1.372	1.615	1.846	1.764	1.743	ns
		t_H	—	-0.634	-1.223	-1.444	-1.645	-1.577	-1.572	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.279	-0.575	-0.564	-0.616	-0.589	-1.150	ns
		t_H	—	0.352	0.724	0.735	0.817	0.776	1.321	ns
	GCLK PLL	t_{SU}	—	0.707	1.372	1.615	1.846	1.764	1.743	ns
		t_H	—	-0.634	-1.223	-1.444	-1.645	-1.577	-1.572	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.466	-0.957	-1.007	-1.064	-1.035	-1.591	ns
		t_H	—	0.537	1.098	1.172	1.256	1.213	1.756	ns
	GCLK PLL	t_{SU}	—	0.516	0.985	1.166	1.391	1.312	1.296	ns
		t_H	—	-0.445	-0.844	-1.001	-1.199	-1.134	-1.131	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.466	-0.957	-1.007	-1.064	-1.035	-1.591	ns
		t_H	—	0.537	1.098	1.172	1.256	1.213	1.756	ns
	GCLK PLL	t_{SU}	—	0.516	0.985	1.166	1.391	1.312	1.296	ns
		t_H	—	-0.445	-0.844	-1.001	-1.199	-1.134	-1.131	ns

Table 1–40 specifies EP3SL70 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.458	4.171	4.679	4.932	4.606	5.103	ns
		GCLK PLL	t_{CO}	—	1.469	2.218	2.495	2.463	2.247	2.204	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.606	4.307	4.878	5.131	4.746	5.244	ns
		GCLK PLL	t_{CO}	—	1.617	2.354	2.694	2.662	2.387	2.345	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.666	4.386	4.933	5.186	4.833	5.330	ns
		GCLK PLL	t_{CO}	—	1.677	2.433	2.749	2.717	2.474	2.431	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	2.781	4.550	5.118	5.371	4.998	5.496	ns
		GCLK PLL	t_{CO}	—	1.792	2.597	2.934	2.902	2.639	2.597	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.606	4.307	4.877	5.130	4.746	5.244	ns
		GCLK PLL	t_{CO}	—	1.617	2.354	2.693	2.661	2.387	2.345	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.781	4.550	5.117	5.370	4.998	5.496	ns
		GCLK PLL	t_{CO}	—	1.792	2.597	2.933	2.901	2.639	2.597	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	2.836	4.626	5.182	5.435	5.077	5.574	ns
		GCLK PLL	t_{CO}	—	1.847	2.673	2.998	2.966	2.718	2.675	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	2.889	4.687	5.238	5.491	5.139	5.636	ns
		GCLK PLL	t_{CO}	—	1.900	2.734	3.054	3.022	2.780	2.737	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.544	4.332	4.947	5.200	4.775	5.272	ns
		GCLK PLL	t_{CO}	—	1.555	2.379	2.763	2.731	2.416	2.373	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.583	4.356	4.922	5.175	4.797	5.295	ns
		GCLK PLL	t_{CO}	—	1.594	2.403	2.738	2.706	2.438	2.396	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.831	4.701	5.322	5.575	5.152	5.650	ns
		GCLK PLL	t_{CO}	—	1.842	2.748	3.138	3.106	2.793	2.751	ns
2.5 V	16mA	GCLK	t_{CO}	—	2.864	4.760	5.419	5.672	5.214	5.712	ns
		GCLK PLL	t_{CO}	—	1.875	2.807	3.235	3.203	2.855	2.813	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	2mA	GCLK	t_{CO}	—	2.446	4.203	4.762	5.015	4.642	5.140	ns
		GCLK PLL	t_{CO}	—	1.457	2.250	2.578	2.546	2.283	2.241	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.508	4.320	4.991	5.244	4.761	5.258	ns
		GCLK PLL	t_{CO}	—	1.519	2.367	2.807	2.775	2.402	2.359	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.751	4.618	5.281	5.534	5.065	5.563	ns
		GCLK PLL	t_{CO}	—	1.762	2.665	3.097	3.065	2.706	2.664	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.578	4.365	4.963	5.216	4.805	5.303	ns
		GCLK PLL	t_{CO}	—	1.589	2.412	2.779	2.747	2.446	2.404	ns
1.8 V	10mA	GCLK	t_{CO}	—	2.840	4.727	5.374	5.627	5.177	5.675	ns
		GCLK PLL	t_{CO}	—	1.851	2.774	3.190	3.158	2.818	2.776	ns
1.8 V	12mA	GCLK	t_{CO}	—	2.911	4.873	5.594	5.847	5.329	5.827	ns
		GCLK PLL	t_{CO}	—	1.922	2.920	3.410	3.378	2.970	2.928	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.398	4.065	4.663	4.916	4.502	4.999	ns
		GCLK PLL	t_{CO}	—	1.409	2.112	2.479	2.447	2.143	2.100	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.666	4.525	5.140	5.393	4.976	5.473	ns
		GCLK PLL	t_{CO}	—	1.677	2.572	2.956	2.924	2.617	2.574	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.764	4.631	5.270	5.523	5.080	5.578	ns
		GCLK PLL	t_{CO}	—	1.775	2.678	3.086	3.054	2.721	2.679	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.689	4.487	5.113	5.366	4.934	5.432	ns
		GCLK PLL	t_{CO}	—	1.700	2.534	2.929	2.897	2.575	2.533	ns
1.5 V	10mA	GCLK	t_{CO}	—	2.855	4.774	5.468	5.721	5.224	5.722	ns
		GCLK PLL	t_{CO}	—	1.866	2.821	3.284	3.252	2.865	2.823	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	12mA	GCLK	t_{CO}	—	3.029	5.116	5.956	6.209	5.571	6.069	ns
		GCLK PLL	t_{CO}	—	2.040	3.163	3.772	3.740	3.212	3.170	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.674	4.585	5.368	5.621	5.012	5.510	ns
		GCLK PLL	t_{CO}	—	1.685	2.632	3.184	3.152	2.653	2.611	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.840	4.804	5.550	5.803	5.254	5.752	ns
		GCLK PLL	t_{CO}	—	1.851	2.851	3.366	3.334	2.895	2.853	ns
1.2 V	6mA	GCLK	t_{CO}	—	2.776	4.674	5.383	5.636	5.120	5.618	ns
		GCLK PLL	t_{CO}	—	1.787	2.721	3.199	3.167	2.761	2.719	ns
1.2 V	8mA	GCLK	t_{CO}	—	3.030	5.076	5.890	6.143	5.528	6.026	ns
		GCLK PLL	t_{CO}	—	2.041	3.123	3.706	3.674	3.169	3.127	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.156	3.703	4.159	4.412	4.126	4.624	ns
		GCLK PLL	t_{CO}	—	1.167	1.750	1.975	1.943	1.767	1.725	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.153	3.700	4.155	4.408	4.123	4.621	ns
		GCLK PLL	t_{CO}	—	1.164	1.747	1.971	1.939	1.764	1.722	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.156	3.708	4.164	4.417	4.131	4.629	ns
		GCLK PLL	t_{CO}	—	1.167	1.755	1.980	1.948	1.772	1.730	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.168	3.710	4.164	4.417	4.132	4.630	ns
		GCLK PLL	t_{CO}	—	1.179	1.757	1.980	1.948	1.773	1.731	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.163	3.717	4.176	4.429	4.140	4.638	ns
		GCLK PLL	t_{CO}	—	1.174	1.764	1.992	1.960	1.781	1.739	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.156	3.709	4.167	4.420	4.131	4.629	ns
		GCLK PLL	t_{CO}	—	1.167	1.756	1.983	1.951	1.772	1.730	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.160	3.718	4.179	4.432	4.141	4.639	ns
		GCLK PLL	t_{CO}	—	1.171	1.765	1.995	1.963	1.782	1.740	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.159	3.720	4.181	4.434	4.144	4.642	ns
		GCLK PLL	t_{CO}	—	1.170	1.767	1.997	1.965	1.785	1.743	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.157	3.718	4.179	4.432	4.142	4.640	ns
		GCLK PLL	t_{CO}	—	1.168	1.765	1.995	1.963	1.783	1.741	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.162	3.708	4.163	4.416	4.130	4.628	ns
		GCLK PLL	t_{CO}	—	1.173	1.755	1.979	1.947	1.771	1.729	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.178	3.743	4.204	4.457	4.167	4.665	ns
		GCLK PLL	t_{CO}	—	1.189	1.790	2.020	1.988	1.808	1.766	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.162	3.719	4.180	4.433	4.141	4.639	ns
		GCLK PLL	t_{CO}	—	1.173	1.766	1.996	1.964	1.782	1.740	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.161	3.720	4.182	4.435	4.143	4.641	ns
		GCLK PLL	t_{CO}	—	1.172	1.767	1.998	1.966	1.784	1.742	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.160	3.724	4.186	4.439	4.147	4.645	ns
		GCLK PLL	t_{CO}	—	1.171	1.771	2.002	1.970	1.788	1.746	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.168	3.738	4.202	4.455	4.162	4.660	ns
		GCLK PLL	t_{CO}	—	1.179	1.785	2.018	1.986	1.803	1.761	ns
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.163	3.732	4.195	4.448	4.155	4.653	ns
		GCLK PLL	t_{CO}	—	1.174	1.779	2.011	1.979	1.796	1.754	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.164	3.715	4.173	4.426	4.138	4.636	ns
		GCLK PLL	t_{CO}	—	1.175	1.762	1.989	1.957	1.779	1.737	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.178	3.747	4.211	4.464	4.172	4.670	ns
		GCLK PLL	t_{CO}	—	1.189	1.794	2.027	1.995	1.813	1.771	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.159	3.699	4.154	4.407	4.121	4.619	ns
		GCLK PLL	t_{CO}	—	1.170	1.746	1.970	1.938	1.762	1.720	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.160	3.702	4.158	4.411	4.124	4.622	ns
		GCLK PLL	t_{CO}	—	1.171	1.749	1.974	1.942	1.765	1.723	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.162	3.710	4.166	4.419	4.132	4.630	ns
		GCLK PLL	t_{CO}	—	1.173	1.757	1.982	1.950	1.773	1.731	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.166	3.717	4.174	4.427	4.140	4.638	ns
		GCLK PLL	t_{CO}	—	1.177	1.764	1.990	1.958	1.781	1.739	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.168	3.720	4.177	4.430	4.143	4.641	ns
		GCLK PLL	t_{CO}	—	1.179	1.767	1.993	1.961	1.784	1.742	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.219	3.754	4.207	4.460	4.176	4.674	ns
		GCLK PLL	t_{CO}	—	1.230	1.801	2.023	1.991	1.817	1.775	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.165	3.708	4.165	4.418	4.130	4.628	ns
		GCLK PLL	t_{CO}	—	1.176	1.755	1.981	1.949	1.771	1.729	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.165	3.711	4.170	4.423	4.133	4.631	ns
		GCLK PLL	t_{CO}	—	1.176	1.758	1.986	1.954	1.774	1.732	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.162	3.706	4.163	4.416	4.128	4.626	ns
		GCLK PLL	t_{CO}	—	1.173	1.753	1.979	1.947	1.769	1.727	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.164	3.715	4.173	4.426	4.138	4.636	ns
		GCLK PLL	t_{CO}	—	1.175	1.762	1.989	1.957	1.779	1.737	ns

Table 1–40. EP3SL70 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.173	3.729	4.189	4.442	4.152	4.650	ns
		GCLK PLL	t_{CO}	—	1.184	1.776	2.005	1.973	1.793	1.751	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.197	3.714	4.164	4.417	4.134	4.632	ns
		GCLK PLL	t_{CO}	—	1.208	1.761	1.980	1.948	1.775	1.733	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.176	3.727	4.189	4.442	4.150	4.648	ns
		GCLK PLL	t_{CO}	—	1.187	1.774	2.005	1.973	1.791	1.749	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.170	3.722	4.183	4.436	4.144	4.642	ns
		GCLK PLL	t_{CO}	—	1.181	1.769	1.999	1.967	1.785	1.743	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.180	3.740	4.204	4.457	4.163	4.661	ns
		GCLK PLL	t_{CO}	—	1.191	1.787	2.020	1.988	1.804	1.762	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.176	3.740	4.204	4.457	4.164	4.662	ns
		GCLK PLL	t_{CO}	—	1.187	1.787	2.020	1.988	1.805	1.763	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.176	3.739	4.202	4.455	4.162	4.660	ns
		GCLK PLL	t_{CO}	—	1.187	1.786	2.018	1.986	1.803	1.761	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.229	3.773	4.231	4.484	4.195	4.693	ns
		GCLK PLL	t_{CO}	—	1.240	1.820	2.047	2.015	1.836	1.794	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.154	5.047	5.700	5.953	5.508	6.005	ns
		GCLK PLL	t_{CO}	—	2.165	3.094	3.516	3.484	3.149	3.106	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.154	5.047	5.700	5.953	5.508	6.005	ns
		GCLK PLL	t_{CO}	—	2.165	3.094	3.516	3.484	3.149	3.106	ns

Table 1–41 specifies EP3SL70 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–41. EP3SL70 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.523	4.231	4.767	5.011	4.661	5.127	ns
		GCLK PLL	t_{CO}	—	1.541	2.289	2.594	2.556	2.314	2.240	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.587	4.289	4.857	5.101	4.714	5.181	ns
		GCLK PLL	t_{CO}	—	1.605	2.347	2.684	2.646	2.367	2.294	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.718	4.446	5.003	5.247	4.876	5.342	ns
		GCLK PLL	t_{CO}	—	1.736	2.504	2.830	2.792	2.529	2.455	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.616	4.313	4.867	5.111	4.747	5.213	ns
		GCLK PLL	t_{CO}	—	1.634	2.371	2.694	2.656	2.400	2.326	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.758	4.496	5.072	5.316	4.932	5.399	ns
		GCLK PLL	t_{CO}	—	1.776	2.554	2.899	2.861	2.585	2.512	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.620	4.453	5.081	5.325	4.892	5.358	ns
		GCLK PLL	t_{CO}	—	1.638	2.511	2.908	2.870	2.545	2.471	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.614	4.384	4.959	5.203	4.815	5.281	ns
		GCLK PLL	t_{CO}	—	1.632	2.442	2.786	2.748	2.468	2.394	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.819	4.664	5.293	5.537	5.111	5.577	ns
		GCLK PLL	t_{CO}	—	1.837	2.722	3.120	3.082	2.764	2.690	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.629	4.373	4.927	5.172	4.812	5.280	ns
		GCLK PLL	t_{CO}	—	1.643	2.426	2.748	2.710	2.459	2.387	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.660	4.508	5.191	5.436	4.941	5.410	ns
		GCLK PLL	t_{CO}	—	1.674	2.561	3.012	2.974	2.588	2.517	ns

Table 1–41. EP3SL70 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	6mA	GCLK	t_{CO}	—	2.752	4.653	5.358	5.603	5.097	5.566	ns
		GCLK PLL	t_{CO}	—	1.766	2.706	3.179	3.141	2.744	2.673	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.637	4.428	5.031	5.276	4.860	5.328	ns
		GCLK PLL	t_{CO}	—	1.651	2.481	2.852	2.814	2.507	2.435	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.542	4.288	4.862	5.107	4.721	5.189	ns
		GCLK PLL	t_{CO}	—	1.556	2.341	2.683	2.645	2.368	2.296	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.667	4.531	5.171	5.416	4.973	5.441	ns
		GCLK PLL	t_{CO}	—	1.681	2.584	2.992	2.954	2.620	2.548	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.802	4.683	5.381	5.626	5.128	5.597	ns
		GCLK PLL	t_{CO}	—	1.816	2.736	3.202	3.164	2.775	2.704	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.689	4.509	5.156	5.401	4.948	5.417	ns
		GCLK PLL	t_{CO}	—	1.703	2.562	2.977	2.939	2.595	2.524	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.792	4.893	5.792	6.037	5.313	5.782	ns
		GCLK PLL	t_{CO}	—	1.806	2.946	3.613	3.575	2.960	2.889	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.920	4.961	5.783	6.028	5.393	5.862	ns
		GCLK PLL	t_{CO}	—	1.934	3.014	3.604	3.566	3.040	2.969	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.112	3.634	4.088	4.332	4.047	4.514	ns
		GCLK PLL	t_{CO}	—	1.130	1.692	1.915	1.877	1.700	1.627	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.100	3.625	4.079	4.323	4.037	4.504	ns
		GCLK PLL	t_{CO}	—	1.118	1.683	1.906	1.868	1.690	1.617	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.105	3.626	4.079	4.323	4.038	4.505	ns
		GCLK PLL	t_{CO}	—	1.123	1.684	1.906	1.868	1.691	1.618	ns

Table 1–41. EP3SL70 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.119	3.651	4.112	4.357	4.066	4.535	ns
		GCLK PLL	t_{CO}	—	1.133	1.704	1.933	1.895	1.713	1.642	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.107	3.639	4.099	4.344	4.053	4.522	ns
		GCLK PLL	t_{CO}	—	1.121	1.692	1.920	1.882	1.700	1.629	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.107	3.646	4.108	4.353	4.060	4.529	ns
		GCLK PLL	t_{CO}	—	1.121	1.699	1.929	1.891	1.707	1.636	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.099	3.641	4.102	4.347	4.055	4.524	ns
		GCLK PLL	t_{CO}	—	1.113	1.694	1.923	1.885	1.702	1.631	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.097	3.638	4.100	4.345	4.053	4.522	ns
		GCLK PLL	t_{CO}	—	1.111	1.691	1.921	1.883	1.700	1.629	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.102	3.630	4.089	4.334	4.044	4.513	ns
		GCLK PLL	t_{CO}	—	1.116	1.683	1.910	1.872	1.691	1.620	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.104	3.644	4.105	4.350	4.058	4.527	ns
		GCLK PLL	t_{CO}	—	1.118	1.697	1.926	1.888	1.705	1.634	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.119	3.654	4.118	4.363	4.068	4.537	ns
		GCLK PLL	t_{CO}	—	1.133	1.707	1.939	1.901	1.715	1.644	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.108	3.649	4.114	4.359	4.063	4.532	ns
		GCLK PLL	t_{CO}	—	1.122	1.702	1.935	1.897	1.710	1.639	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.100	3.643	4.107	4.352	4.057	4.526	ns
		GCLK PLL	t_{CO}	—	1.114	1.696	1.928	1.890	1.704	1.633	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.114	3.632	4.088	4.333	4.045	4.514	ns
		GCLK PLL	t_{CO}	—	1.128	1.685	1.909	1.871	1.692	1.621	ns

Table 1–41. EP3SL70 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.105	3.631	4.090	4.335	4.045	4.514	ns
		GCLK PLL	t_{CO}	—	1.119	1.684	1.911	1.873	1.692	1.621	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.099	3.630	4.088	4.333	4.043	4.512	ns
		GCLK PLL	t_{CO}	—	1.113	1.683	1.909	1.871	1.690	1.619	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.101	3.633	4.092	4.337	4.047	4.516	ns
		GCLK PLL	t_{CO}	—	1.115	1.686	1.913	1.875	1.694	1.623	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.100	3.636	4.096	4.341	4.050	4.519	ns
		GCLK PLL	t_{CO}	—	1.114	1.689	1.917	1.879	1.697	1.626	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.109	3.634	4.089	4.334	4.047	4.516	ns
		GCLK PLL	t_{CO}	—	1.123	1.687	1.910	1.872	1.694	1.623	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.120	3.640	4.100	4.345	4.053	4.522	ns
		GCLK PLL	t_{CO}	—	1.134	1.693	1.921	1.883	1.700	1.629	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.114	3.643	4.105	4.350	4.057	4.526	ns
		GCLK PLL	t_{CO}	—	1.128	1.696	1.926	1.888	1.704	1.633	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.106	3.634	4.095	4.340	4.048	4.517	ns
		GCLK PLL	t_{CO}	—	1.120	1.687	1.916	1.878	1.695	1.624	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.123	3.656	4.124	4.369	4.070	4.539	ns
		GCLK PLL	t_{CO}	—	1.137	1.709	1.945	1.907	1.717	1.646	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.111	3.646	4.111	4.356	4.059	4.528	ns
		GCLK PLL	t_{CO}	—	1.125	1.699	1.932	1.894	1.706	1.635	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.114	3.658	4.125	4.370	4.072	4.541	ns
		GCLK PLL	t_{CO}	—	1.128	1.711	1.946	1.908	1.719	1.648	ns

Table 1–41. EP3SL70 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI	-	GCLK	t_{CO}	—	3.061	4.971	5.626	5.870	5.421	5.887	ns
		GCLK PLL	t_{CO}	—	2.079	3.029	3.453	3.415	3.074	3.000	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.061	4.971	5.626	5.870	5.421	5.887	ns
		GCLK PLL	t_{CO}	—	2.079	3.029	3.453	3.415	3.074	3.000	ns

Table 1–42 through Table 1–47 show the maximum I/O timing parameters for EP3SL70 devices for differential I/O standards.

Table 1–42 specifies EP3SL70 Column Pins Input Timing parameters for differential I/O standards.

Table 1–42. EP3SL70 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.381	-0.781	-0.796	-0.867	-0.830	-1.416	ns
		t_H	—	0.453	0.925	0.964	1.061	1.011	1.584	ns
	GCLK PLL	t_{SU}	—	0.611	1.176	1.393	1.607	1.534	1.492	ns
		t_H	—	-0.539	-1.032	-1.225	-1.413	-1.353	-1.324	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.381	-0.781	-0.796	-0.867	-0.830	-1.416	ns
		t_H	—	0.453	0.925	0.964	1.061	1.011	1.584	ns
	GCLK PLL	t_{SU}	—	0.611	1.176	1.393	1.607	1.534	1.492	ns
		t_H	—	-0.539	-1.032	-1.225	-1.413	-1.353	-1.324	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.388	-0.796	-0.812	-0.883	-0.846	-1.432	ns
		t_H	—	0.460	0.939	0.980	1.077	1.027	1.600	ns
	GCLK PLL	t_{SU}	—	0.604	1.161	1.377	1.591	1.518	1.476	ns
		t_H	—	-0.532	-1.018	-1.209	-1.397	-1.337	-1.308	ns

Table 1–42. EP3SL70 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.388	-0.796	-0.812	-0.883	-0.846	-1.432	ns
		t_H	—	0.460	0.939	0.980	1.077	1.027	1.600	ns
	GCLK PLL	t_{SU}	—	0.604	1.161	1.377	1.591	1.518	1.476	ns
		t_H	—	-0.532	-1.018	-1.209	-1.397	-1.337	-1.308	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.402	-0.823	-0.844	-0.916	-0.879	-1.464	ns
		t_H	—	0.473	0.966	1.012	1.109	1.059	1.632	ns
	GCLK PLL	t_{SU}	—	0.590	1.134	1.345	1.558	1.485	1.444	ns
		t_H	—	-0.519	-0.991	-1.177	-1.365	-1.305	-1.276	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.402	-0.823	-0.844	-0.916	-0.879	-1.464	ns
		t_H	—	0.473	0.966	1.012	1.109	1.059	1.632	ns
	GCLK PLL	t_{SU}	—	0.590	1.134	1.345	1.558	1.485	1.444	ns
		t_H	—	-0.519	-0.991	-1.177	-1.365	-1.305	-1.276	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.388	-0.796	-0.812	-0.883	-0.846	-1.432	ns
		t_H	—	0.460	0.939	0.980	1.077	1.027	1.600	ns
	GCLK PLL	t_{SU}	—	0.604	1.161	1.377	1.591	1.518	1.476	ns
		t_H	—	-0.532	-1.018	-1.209	-1.397	-1.337	-1.308	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.388	-0.796	-0.812	-0.883	-0.846	-1.432	ns
		t_H	—	0.460	0.939	0.980	1.077	1.027	1.600	ns
	GCLK PLL	t_{SU}	—	0.604	1.161	1.377	1.591	1.518	1.476	ns
		t_H	—	-0.532	-1.018	-1.209	-1.397	-1.337	-1.308	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.402	-0.823	-0.844	-0.916	-0.879	-1.464	ns
		t_H	—	0.473	0.966	1.012	1.109	1.059	1.632	ns
	GCLK PLL	t_{SU}	—	0.590	1.134	1.345	1.558	1.485	1.444	ns
		t_H	—	-0.519	-0.991	-1.177	-1.365	-1.305	-1.276	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.402	-0.823	-0.844	-0.916	-0.879	-1.464	ns
		t_H	—	0.473	0.966	1.012	1.109	1.059	1.632	ns
	GCLK PLL	t_{SU}	—	0.590	1.134	1.345	1.558	1.485	1.444	ns
		t_H	—	-0.519	-0.991	-1.177	-1.365	-1.305	-1.276	ns

Table 1–42. EP3SL70 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.426	-0.874	-0.904	-0.975	-0.938	-1.524	ns
		t_H	—	0.496	1.014	1.067	1.164	1.115	1.687	ns
	GCLK PLL	t_{SU}	—	0.566	1.083	1.285	1.499	1.426	1.384	ns
		t_H	—	-0.496	-0.943	-1.122	-1.310	-1.249	-1.221	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.426	-0.874	-0.904	-0.975	-0.938	-1.524	ns
		t_H	—	0.496	1.014	1.067	1.164	1.115	1.687	ns
	GCLK PLL	t_{SU}	—	0.566	1.083	1.285	1.499	1.426	1.384	ns
		t_H	—	-0.496	-0.943	-1.122	-1.310	-1.249	-1.221	ns

Table 1–43 specifies EP3SL70 Row Pins Input Timing parameters for differential I/O standards.

Table 1–43. EP3SL70 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.417	-0.854	-0.888	-0.954	-0.919	-1.478	ns
		t_H	—	0.488	0.996	1.055	1.147	1.099	1.645	ns
	GCLK PLL	t_{SU}	—	0.589	1.133	1.337	1.563	1.484	1.467	ns
		t_H	—	-0.517	-0.987	-1.167	-1.364	-1.299	-1.297	ns
MINI-LVDS	GCLK	t_{SU}	—	-0.417	-0.854	-0.888	-0.954	-0.919	-1.478	ns
		t_H	—	0.488	0.996	1.055	1.147	1.099	1.645	ns
	GCLK PLL	t_{SU}	—	0.589	1.133	1.337	1.563	1.484	1.467	ns
		t_H	—	-0.517	-0.987	-1.167	-1.364	-1.299	-1.297	ns
RSDS	GCLK	t_{SU}	—	-0.417	-0.854	-0.888	-0.954	-0.919	-1.478	ns
		t_H	—	0.488	0.996	1.055	1.147	1.099	1.645	ns
	GCLK PLL	t_{SU}	—	0.589	1.133	1.337	1.563	1.484	1.467	ns
		t_H	—	-0.517	-0.987	-1.167	-1.364	-1.299	-1.297	ns

Table 1–43. EP3SL70 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.341	-0.700	-0.710	-0.774	-0.740	-1.300	ns
		t_H	—	0.413	0.844	0.878	0.968	0.921	1.468	ns
	GCLK PLL	t_{SU}	—	0.707	1.372	1.614	1.844	1.763	1.744	ns
		t_H	—	-0.634	-1.223	-1.443	-1.643	-1.576	-1.573	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.341	-0.700	-0.710	-0.774	-0.740	-1.300	ns
		t_H	—	0.413	0.844	0.878	0.968	0.921	1.468	ns
	GCLK PLL	t_{SU}	—	0.707	1.372	1.614	1.844	1.763	1.744	ns
		t_H	—	-0.634	-1.223	-1.443	-1.643	-1.576	-1.573	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.348	-0.715	-0.726	-0.790	-0.756	-1.316	ns
		t_H	—	0.420	0.858	0.894	0.984	0.937	1.484	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.598	1.827	1.747	1.728	ns
		t_H	—	-0.627	-1.209	-1.426	-1.626	-1.560	-1.556	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.348	-0.715	-0.726	-0.790	-0.756	-1.316	ns
		t_H	—	0.420	0.858	0.894	0.984	0.937	1.484	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.598	1.827	1.747	1.728	ns
		t_H	—	-0.627	-1.209	-1.426	-1.626	-1.560	-1.556	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.362	-0.742	-0.758	-0.823	-0.789	-1.348	ns
		t_H	—	0.433	0.885	0.926	1.016	0.969	1.516	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.566	1.795	1.714	1.696	ns
		t_H	—	-0.613	-1.182	-1.395	-1.594	-1.528	-1.525	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.362	-0.742	-0.758	-0.823	-0.789	-1.348	ns
		t_H	—	0.433	0.885	0.926	1.016	0.969	1.516	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.566	1.795	1.714	1.696	ns
		t_H	—	-0.613	-1.182	-1.395	-1.594	-1.528	-1.525	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.348	-0.715	-0.726	-0.790	-0.756	-1.316	ns
		t_H	—	0.420	0.858	0.894	0.984	0.937	1.484	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.598	1.827	1.747	1.728	ns
		t_H	—	-0.627	-1.209	-1.426	-1.626	-1.560	-1.556	ns

Table 1–43. EP3SL70 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.348	-0.715	-0.726	-0.790	-0.756	-1.316	ns
		t_H	—	0.420	0.858	0.894	0.984	0.937	1.484	ns
	GCLK PLL	t_{SU}	—	0.700	1.358	1.598	1.827	1.747	1.728	ns
		t_H	—	-0.627	-1.209	-1.426	-1.626	-1.560	-1.556	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.362	-0.742	-0.758	-0.823	-0.789	-1.348	ns
		t_H	—	0.433	0.885	0.926	1.016	0.969	1.516	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.566	1.795	1.714	1.696	ns
		t_H	—	-0.613	-1.182	-1.395	-1.594	-1.528	-1.525	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.362	-0.742	-0.758	-0.823	-0.789	-1.348	ns
		t_H	—	0.433	0.885	0.926	1.016	0.969	1.516	ns
	GCLK PLL	t_{SU}	—	0.686	1.330	1.566	1.795	1.714	1.696	ns
		t_H	—	-0.613	-1.182	-1.395	-1.594	-1.528	-1.525	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.386	-0.793	-0.818	-0.882	-0.848	-1.408	ns
		t_H	—	0.456	0.933	0.981	1.071	1.025	1.571	ns
	GCLK PLL	t_{SU}	—	0.641	1.235	1.456	1.684	1.604	1.586	ns
		t_H	—	-0.569	-1.092	-1.288	-1.488	-1.423	-1.418	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.386	-0.793	-0.818	-0.882	-0.848	-1.408	ns
		t_H	—	0.456	0.933	0.981	1.071	1.025	1.571	ns
	GCLK PLL	t_{SU}	—	0.641	1.235	1.456	1.684	1.604	1.586	ns
		t_H	—	-0.569	-1.092	-1.288	-1.488	-1.423	-1.418	ns

Table 1–44 specifies EP3SL70 Column Pins Output Timing parameters for differential I/O standards.

Table 1–44. EP3SL70 Column Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns

Table 1–44. EP3SL70 Column Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_3R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.044	3.991	4.515	4.789	4.646	5.130	ns
		GCLK PLL	t_{CO}	—	1.056	2.041	2.333	2.323	2.290	2.230	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.972	3.844	4.342	4.614	4.473	4.957	ns
		GCLK PLL	t_{CO}	—	0.984	1.894	2.160	2.148	2.117	2.057	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.964	3.829	4.324	4.596	4.455	4.939	ns
		GCLK PLL	t_{CO}	—	0.976	1.879	2.142	2.130	2.099	2.039	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.964	3.829	4.324	4.596	4.455	4.939	ns
		GCLK PLL	t_{CO}	—	0.976	1.879	2.142	2.130	2.099	2.039	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.965	3.831	4.326	4.598	4.457	4.941	ns
		GCLK PLL	t_{CO}	—	0.977	1.881	2.144	2.132	2.101	2.041	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.964	3.828	4.323	4.595	4.454	4.938	ns
		GCLK PLL	t_{CO}	—	0.976	1.878	2.141	2.129	2.098	2.038	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.961	3.822	4.316	4.588	4.447	4.931	ns
		GCLK PLL	t_{CO}	—	0.973	1.872	2.134	2.122	2.091	2.031	ns

Table 1–44. EP3SL70 Column Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.960	3.820	4.313	4.585	4.444	4.928	ns
		GCLK PLL	t_{CO}	—	0.972	1.870	2.131	2.119	2.088	2.028	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.961	3.822	4.316	4.588	4.447	4.931	ns
		GCLK PLL	t_{CO}	—	0.973	1.872	2.134	2.122	2.091	2.031	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.956	3.812	4.304	4.576	4.435	4.919	ns
		GCLK PLL	t_{CO}	—	0.968	1.862	2.122	2.110	2.079	2.019	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.953	3.807	4.298	4.570	4.429	4.913	ns
		GCLK PLL	t_{CO}	—	0.965	1.857	2.116	2.104	2.073	2.013	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.959	3.819	4.312	4.584	4.443	4.927	ns
		GCLK PLL	t_{CO}	—	0.971	1.869	2.130	2.118	2.087	2.027	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.947	3.794	4.283	4.554	4.413	4.898	ns
		GCLK PLL	t_{CO}	—	0.959	1.844	2.101	2.088	2.057	1.998	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.954	3.809	4.300	4.572	4.431	4.915	ns
		GCLK PLL	t_{CO}	—	0.966	1.859	2.118	2.106	2.075	2.015	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.949	3.799	4.289	4.560	4.419	4.904	ns
		GCLK PLL	t_{CO}	—	0.961	1.849	2.107	2.094	2.063	2.004	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.953	3.806	4.297	4.569	4.428	4.912	ns
		GCLK PLL	t_{CO}	—	0.965	1.856	2.115	2.103	2.072	2.012	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.951	3.803	4.293	4.565	4.424	4.908	ns
		GCLK PLL	t_{CO}	—	0.963	1.853	2.111	2.099	2.068	2.008	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.950	3.801	4.291	4.563	4.422	4.906	ns
		GCLK PLL	t_{CO}	—	0.962	1.851	2.109	2.097	2.066	2.006	ns

Table 1–44. EP3SL70 Column Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.943	3.786	4.273	4.545	4.404	4.888	ns
		GCLK PLL	t_{CO}	—	0.955	1.836	2.091	2.079	2.048	1.988	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.969	3.839	4.336	4.608	4.467	4.951	ns
		GCLK PLL	t_{CO}	—	0.981	1.889	2.154	2.142	2.111	2.051	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.964	3.829	4.324	4.596	4.455	4.939	ns
		GCLK PLL	t_{CO}	—	0.976	1.879	2.142	2.130	2.099	2.039	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.961	3.823	4.317	4.589	4.448	4.932	ns
		GCLK PLL	t_{CO}	—	0.973	1.873	2.135	2.123	2.092	2.032	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.964	3.829	4.324	4.596	4.455	4.939	ns
		GCLK PLL	t_{CO}	—	0.976	1.879	2.142	2.130	2.099	2.039	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.962	3.825	4.319	4.591	4.450	4.934	ns
		GCLK PLL	t_{CO}	—	0.974	1.875	2.137	2.125	2.094	2.034	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.954	3.808	4.299	4.571	4.430	4.914	ns
		GCLK PLL	t_{CO}	—	0.966	1.858	2.117	2.105	2.074	2.014	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.956	3.813	4.305	4.577	4.436	4.920	ns
		GCLK PLL	t_{CO}	—	0.968	1.863	2.123	2.111	2.080	2.020	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.967	3.834	4.330	4.602	4.461	4.945	ns
		GCLK PLL	t_{CO}	—	0.979	1.884	2.148	2.136	2.105	2.045	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.960	3.820	4.313	4.585	4.444	4.928	ns
		GCLK PLL	t_{CO}	—	0.972	1.870	2.131	2.119	2.088	2.028	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.962	3.824	4.318	4.590	4.449	4.933	ns
		GCLK PLL	t_{CO}	—	0.974	1.874	2.136	2.124	2.093	2.033	ns

Table 1–44. EP3SL70 Column Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.960	3.821	4.315	4.586	4.446	4.930	ns
		GCLK PLL	t_{CO}	—	0.972	1.871	2.133	2.120	2.090	2.030	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.957	3.814	4.306	4.578	4.437	4.921	ns
		GCLK PLL	t_{CO}	—	0.969	1.864	2.124	2.112	2.081	2.021	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.951	3.803	4.293	4.565	4.424	4.908	ns
		GCLK PLL	t_{CO}	—	0.963	1.853	2.111	2.099	2.068	2.008	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.954	3.809	4.300	4.572	4.431	4.915	ns
		GCLK PLL	t_{CO}	—	0.966	1.859	2.118	2.106	2.075	2.015	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.958	3.816	4.309	4.581	4.440	4.924	ns
		GCLK PLL	t_{CO}	—	0.970	1.866	2.127	2.115	2.084	2.024	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.957	3.814	4.306	4.578	4.437	4.921	ns
		GCLK PLL	t_{CO}	—	0.969	1.864	2.124	2.112	2.081	2.021	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.955	3.810	4.302	4.573	4.432	4.917	ns
		GCLK PLL	t_{CO}	—	0.967	1.860	2.120	2.107	2.076	2.017	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.953	3.807	4.298	4.570	4.429	4.913	ns
		GCLK PLL	t_{CO}	—	0.965	1.857	2.116	2.104	2.073	2.013	ns

Table 1–45 specifies EP3SL70 Row Pins Output Timing parameters for differential I/O standards.

Table 1–45. EP3SL70 Row Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	t_{CO}	—	2.012	3.926	4.445	4.714	4.575	5.033	ns
		GCLK PLL	t_{CO}	—	1.022	1.972	2.257	2.242	2.212	2.129	ns
LVDS_E_1R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
MINI-LVDS	-	GCLK	t_{CO}	—	2.012	3.926	4.445	4.714	4.575	5.033	ns
		GCLK PLL	t_{CO}	—	1.022	1.972	2.257	2.242	2.212	2.129	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
RSDS	-	GCLK	t_{CO}	—	2.012	3.926	4.445	4.714	4.575	5.033	ns
		GCLK PLL	t_{CO}	—	1.022	1.972	2.257	2.242	2.212	2.129	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.011	3.924	4.443	4.711	4.572	5.031	ns
		GCLK PLL	t_{CO}	—	1.021	1.970	2.255	2.239	2.209	2.127	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.948	3.797	4.292	4.559	4.422	4.880	ns
		GCLK PLL	t_{CO}	—	0.958	1.843	2.104	2.087	2.059	1.976	ns

Table 1–45. EP3SL70 Row Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.940	3.780	4.273	4.540	4.402	4.861	ns
		GCLK PLL	t_{CO}	—	0.950	1.826	2.085	2.068	2.039	1.957	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.939	3.777	4.270	4.536	4.399	4.858	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.082	2.064	2.036	1.954	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.938	3.775	4.267	4.534	4.397	4.855	ns
		GCLK PLL	t_{CO}	—	0.948	1.821	2.079	2.062	2.034	1.951	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.937	3.773	4.265	4.531	4.394	4.853	ns
		GCLK PLL	t_{CO}	—	0.947	1.819	2.077	2.059	2.031	1.949	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.932	3.763	4.253	4.519	4.382	4.841	ns
		GCLK PLL	t_{CO}	—	0.942	1.809	2.065	2.047	2.019	1.937	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.932	3.763	4.253	4.519	4.382	4.841	ns
		GCLK PLL	t_{CO}	—	0.942	1.809	2.065	2.047	2.019	1.937	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.926	3.752	4.240	4.506	4.369	4.828	ns
		GCLK PLL	t_{CO}	—	0.936	1.798	2.052	2.034	2.006	1.924	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.928	3.755	4.244	4.510	4.373	4.832	ns
		GCLK PLL	t_{CO}	—	0.938	1.801	2.056	2.038	2.010	1.928	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.927	3.754	4.243	4.508	4.372	4.831	ns
		GCLK PLL	t_{CO}	—	0.937	1.800	2.055	2.036	2.009	1.927	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.925	3.750	4.238	4.504	4.367	4.826	ns
		GCLK PLL	t_{CO}	—	0.935	1.796	2.050	2.032	2.004	1.922	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.916	3.732	4.217	4.482	4.345	4.805	ns
		GCLK PLL	t_{CO}	—	0.926	1.778	2.029	2.010	1.982	1.901	ns

Table 1–45. EP3SL70 Row Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.948	3.796	4.291	4.558	4.420	4.879	ns
		GCLK PLL	t_{CO}	—	0.958	1.842	2.103	2.086	2.057	1.975	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.941	3.781	4.275	4.541	4.404	4.863	ns
		GCLK PLL	t_{CO}	—	0.951	1.827	2.087	2.069	2.041	1.959	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.937	3.773	4.265	4.531	4.394	4.853	ns
		GCLK PLL	t_{CO}	—	0.947	1.819	2.077	2.059	2.031	1.949	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.944	3.788	4.282	4.548	4.411	4.870	ns
		GCLK PLL	t_{CO}	—	0.954	1.834	2.094	2.076	2.048	1.966	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.937	3.774	4.266	4.532	4.395	4.854	ns
		GCLK PLL	t_{CO}	—	0.947	1.820	2.078	2.060	2.032	1.950	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.937	3.774	4.266	4.532	4.395	4.854	ns
		GCLK PLL	t_{CO}	—	0.947	1.820	2.078	2.060	2.032	1.950	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.936	3.772	4.264	4.530	4.393	4.852	ns
		GCLK PLL	t_{CO}	—	0.946	1.818	2.076	2.058	2.030	1.948	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.932	3.764	4.254	4.520	4.383	4.842	ns
		GCLK PLL	t_{CO}	—	0.942	1.810	2.066	2.048	2.020	1.938	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.927	3.754	4.243	4.508	4.372	4.831	ns
		GCLK PLL	t_{CO}	—	0.937	1.800	2.055	2.036	2.009	1.927	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.928	3.756	4.245	4.511	4.374	4.833	ns
		GCLK PLL	t_{CO}	—	0.938	1.802	2.057	2.039	2.011	1.929	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.936	3.771	4.263	4.529	4.392	4.851	ns
		GCLK PLL	t_{CO}	—	0.946	1.817	2.075	2.057	2.029	1.947	ns

Table 1–45. EP3SL70 Row Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.932	3.763	4.253	4.519	4.382	4.841	ns
		GCLK PLL	t_{CO}	—	0.942	1.809	2.065	2.047	2.019	1.937	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.928	3.756	4.245	4.511	4.374	4.833	ns
		GCLK PLL	t_{CO}	—	0.938	1.802	2.057	2.039	2.011	1.929	ns

Table 1–46 through Table 1–47 show EP3SL70 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–46 specifies EP3SL70 Column Pin delay adders when using the Regional Clock.

Table 1–46. EP3SL70 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	—	0.098	0.199	0.213	0.229	0.221	0.31	ns
RCLK PLL input adder	—	0.003	0.006	-0.009	-0.034	-0.02	-0.014	ns
RCLK output adder	—	-0.141	-0.24	-0.267	-0.283	-0.267	-0.321	ns
RCLK PLL output adder	—	0.407	0.879	1.087	1.051	0.943	1.363	ns

Table 1–47 specifies EP3SL70 Row Pin delay adders when using the Regional Clock.

Table 1–47. EP3SL70 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	—	0.09	0.186	0.2	0.215	0.207	0.287	ns
RCLK PLL input adder	—	-0.002	-0.01	-0.026	-0.05	-0.036	-0.045	ns
RCLK output adder	—	-0.09	-0.186	-0.2	-0.215	-0.207	-0.287	ns
RCLK PLL output adder	—	0.002	0.01	0.026	0.05	0.036	0.045	ns

EP3SL150 I/O Timing Parameters

Table 1–48 through Table 1–51 show the maximum I/O timing parameters for EP3SL150 devices for single ended I/O standards.

Table 1–48 specifies EP3SL150 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–48. EP3SL150 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.658	-1.347	-1.436	-1.530	-1.481	-2.165	ns
		t_H	—	0.727	1.485	1.596	1.716	1.655	2.325	ns
	GCLK PLL	t_{SU}	—	0.469	0.888	1.077	1.320	1.231	1.213	ns
		t_H	—	-0.400	-0.750	-0.917	-1.134	-1.057	-1.053	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.658	-1.347	-1.436	-1.530	-1.481	-2.165	ns
		t_H	—	0.727	1.485	1.596	1.716	1.655	2.325	ns
	GCLK PLL	t_{SU}	—	0.469	0.888	1.077	1.320	1.231	1.213	ns
		t_H	—	-0.400	-0.750	-0.917	-1.134	-1.057	-1.053	ns
2.5 V	GCLK	t_{SU}	—	-0.663	-1.358	-1.448	-1.542	-1.493	-2.177	ns
		t_H	—	0.732	1.495	1.608	1.728	1.667	2.337	ns
	GCLK PLL	t_{SU}	—	0.464	0.877	1.065	1.308	1.219	1.201	ns
		t_H	—	-0.395	-0.740	-0.905	-1.122	-1.045	-1.041	ns

Table 1–48. EP3SL150 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	GCLK	t_{SU}	—	-0.673	-1.378	-1.472	-1.566	-1.517	-2.201	ns
		t_H	—	0.742	1.515	1.631	1.752	1.690	2.360	ns
	GCLK PLL	t_{SU}	—	0.454	0.857	1.041	1.284	1.195	1.177	ns
		t_H	—	-0.385	-0.720	-0.882	-1.098	-1.022	-1.018	ns
1.5 V	GCLK	t_{SU}	—	-0.653	-1.337	-1.425	-1.518	-1.469	-2.154	ns
		t_H	—	0.722	1.475	1.585	1.704	1.643	2.314	ns
	GCLK PLL	t_{SU}	—	0.474	0.898	1.088	1.332	1.243	1.224	ns
		t_H	—	-0.405	-0.760	-0.928	-1.146	-1.069	-1.064	ns
1.2 V	GCLK	t_{SU}	—	-0.596	-1.223	-1.291	-1.383	-1.334	-2.020	ns
		t_H	—	0.666	1.361	1.452	1.570	1.510	2.181	ns
	GCLK PLL	t_{SU}	—	0.531	1.012	1.222	1.467	1.378	1.358	ns
		t_H	—	-0.461	-0.874	-1.061	-1.280	-1.202	-1.197	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.536	-1.100	-1.148	-1.238	-1.190	-1.877	ns
		t_H	—	0.606	1.240	1.311	1.427	1.367	2.040	ns
	GCLK PLL	t_{SU}	—	0.591	1.135	1.365	1.612	1.522	1.501	ns
		t_H	—	-0.521	-0.995	-1.202	-1.423	-1.345	-1.338	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.536	-1.100	-1.148	-1.238	-1.190	-1.877	ns
		t_H	—	0.606	1.240	1.311	1.427	1.367	2.040	ns
	GCLK PLL	t_{SU}	—	0.591	1.135	1.365	1.612	1.522	1.501	ns
		t_H	—	-0.521	-0.995	-1.202	-1.423	-1.345	-1.338	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.512	-1.049	-1.088	-1.179	-1.131	-1.817	ns
	GCLK PLL	t_{SU}	—	0.615	1.186	1.425	1.671	1.581	1.985	ns
		t_H	—	-0.544	-1.043	-1.257	-1.478	-1.401	1.561	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.512	-1.049	-1.088	-1.179	-1.131	-1.393	ns
	GCLK PLL	t_{SU}	—	0.615	1.186	1.425	1.671	1.581	-1.817	ns
		t_H	—	-0.544	-1.043	-1.257	-1.478	-1.401	1.985	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.498	-1.022	-1.056	-1.146	-1.098	1.985	ns
	GCLK PLL	t_{SU}	—	0.629	1.213	1.457	1.704	1.614	1.561	ns
		t_H	—	-0.557	-1.070	-1.289	-1.510	-1.433	-1.393	ns

Table 1–48. EP3SL150 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.498	-1.022	-1.056	-1.146	-1.098	-1.785	ns
	GCLK PLL	t_{SU}	—	0.629	1.213	1.457	1.704	1.614	1.953	ns
		t_{H}	—	-0.557	-1.070	-1.289	-1.510	-1.433	1.593	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.512	-1.049	-1.088	-1.179	-1.131	1.593	ns
	GCLK PLL	t_{SU}	—	0.615	1.186	1.425	1.671	1.581	-1.425	ns
		t_{H}	—	-0.544	-1.043	-1.257	-1.478	-1.401	-1.785	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.512	-1.049	-1.088	-1.179	-1.131	1.985	ns
	GCLK PLL	t_{SU}	—	0.615	1.186	1.425	1.671	1.581	1.561	ns
		t_{H}	—	-0.544	-1.043	-1.257	-1.478	-1.401	-1.393	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.498	-1.022	-1.056	-1.146	-1.098	-1.817	ns
	GCLK PLL	t_{SU}	—	0.629	1.213	1.457	1.704	1.614	1.985	ns
		t_{H}	—	-0.557	-1.070	-1.289	-1.510	-1.433	1.561	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.498	-1.022	-1.056	-1.146	-1.098	-1.393	ns
	GCLK PLL	t_{SU}	—	0.629	1.213	1.457	1.704	1.614	-1.817	ns
		t_{H}	—	-0.557	-1.070	-1.289	-1.510	-1.433	1.985	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.491	-1.007	-1.040	-1.130	-1.082	1.561	ns
	GCLK PLL	t_{SU}	—	0.636	1.228	1.473	1.720	1.630	-1.393	ns
		t_{H}	—	-0.564	-1.084	-1.305	-1.526	-1.449	-1.785	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.491	-1.007	-1.040	-1.130	-1.082	1.953	ns
	GCLK PLL	t_{SU}	—	0.636	1.228	1.473	1.720	1.630	1.593	ns
		t_{H}	—	-0.564	-1.084	-1.305	-1.526	-1.449	-1.425	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.658	-1.347	-1.436	-1.530	-1.481	-1.785	ns
		t_{H}	—	0.727	1.485	1.596	1.716	1.655	1.953	ns
	GCLK PLL	t_{SU}	—	0.469	0.888	1.077	1.320	1.231	1.593	ns
		t_{H}	—	-0.400	-0.750	-0.917	-1.134	-1.057	-1.425	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.658	-1.347	-1.436	-1.530	-1.481	-1.785	ns
		t_{H}	—	0.727	1.485	1.596	1.716	1.655	1.953	ns
	GCLK PLL	t_{SU}	—	0.469	0.888	1.077	1.320	1.231	1.593	ns
		t_{H}	—	-0.400	-0.750	-0.917	-1.134	-1.057	-1.425	ns

Table 1–49 specifies EP3SL150 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–49. EP3SL150 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.574	-1.177	-1.244	-1.320	-1.281	-1.934	ns
		t_H	—	0.645	1.318	1.409	1.512	1.459	2.099	ns
	GCLK PLL	t_{SU}	—	0.543	1.036	1.246	1.505	1.408	1.414	ns
		t_H	—	-0.472	-0.895	-1.081	-1.313	-1.230	-1.249	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.574	-1.177	-1.244	-1.320	-1.281	-1.934	ns
		t_H	—	0.645	1.318	1.409	1.512	1.459	2.099	ns
	GCLK PLL	t_{SU}	—	0.543	1.036	1.246	1.505	1.408	1.414	ns
		t_H	—	-0.472	-0.895	-1.081	-1.313	-1.230	-1.249	ns
2.5 V	GCLK	t_{SU}	—	-0.579	-1.187	-1.255	-1.332	-1.293	-1.945	ns
		t_H	—	0.650	1.328	1.421	1.524	1.471	2.111	ns
	GCLK PLL	t_{SU}	—	0.538	1.026	1.235	1.493	1.396	1.403	ns
		t_H	—	-0.467	-0.885	-1.069	-1.301	-1.218	-1.237	ns
1.8 V	GCLK	t_{SU}	—	-0.591	-1.210	-1.283	-1.360	-1.321	-1.974	ns
		t_H	—	0.662	1.351	1.448	1.552	1.499	2.139	ns
	GCLK PLL	t_{SU}	—	0.528	1.006	1.211	1.469	1.373	1.379	ns
		t_H	—	-0.457	-0.865	-1.046	-1.277	-1.195	-1.214	ns
1.5 V	GCLK	t_{SU}	—	-0.570	-1.169	-1.235	-1.311	-1.273	-1.926	ns
		t_H	—	0.641	1.310	1.400	1.503	1.451	2.091	ns
	GCLK PLL	t_{SU}	—	0.549	1.047	1.259	1.518	1.421	1.427	ns
		t_H	—	-0.478	-0.906	-1.094	-1.326	-1.243	-1.262	ns
1.2 V	GCLK	t_{SU}	—	-0.513	-1.052	-1.099	-1.173	-1.136	-1.790	ns
		t_H	—	0.584	1.194	1.265	1.367	1.316	1.956	ns
	GCLK PLL	t_{SU}	—	0.606	1.164	1.395	1.656	1.558	1.563	ns
		t_H	—	-0.535	-1.022	-1.229	-1.462	-1.378	-1.397	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.448	-0.921	-0.946	-1.018	-0.981	-1.636	ns
		t_H	—	0.520	1.064	1.114	1.214	1.162	1.804	ns
	GCLK PLL	t_{SU}	—	0.669	1.292	1.544	1.807	1.708	1.712	ns
		t_H	—	-0.597	-1.149	-1.376	-1.611	-1.527	-1.544	ns

Table 1–49. EP3SL150 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.448	-0.921	-0.946	-1.018	-0.981	-1.636	ns
		t_H	—	0.520	1.064	1.114	1.214	1.162	1.804	ns
	GCLK PLL	t_{SU}	—	0.669	1.292	1.544	1.807	1.708	1.712	ns
		t_H	—	-0.597	-1.149	-1.376	-1.611	-1.527	-1.544	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.405	-0.829	-0.840	-0.911	-0.876	-1.531	ns
		t_H	—	0.478	0.977	1.011	1.112	1.062	1.702	ns
	GCLK PLL	t_{SU}	—	0.714	1.387	1.654	1.918	1.818	1.822	ns
		t_H		-0.641	-1.239	-1.483	-1.717	-1.632	-1.651	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.405	-0.829	-0.840	-0.911	-0.876	-1.531	ns
		t_H	—	0.478	0.977	1.011	1.112	1.062	1.702	ns
	GCLK PLL	t_{SU}	—	0.714	1.387	1.654	1.918	1.818	1.822	ns
		t_H	—	-0.641	-1.239	-1.483	-1.717	-1.632	-1.651	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.391	-0.801	-0.808	-0.879	-0.843	-1.499	ns
		t_H	—	0.464	0.950	0.980	1.080	1.030	1.671	ns
	GCLK PLL	t_{SU}	—	0.728	1.415	1.686	1.950	1.851	1.854	ns
		t_H	—	-0.655	-1.266	-1.514	-1.749	-1.664	-1.682	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.391	-0.801	-0.808	-0.879	-0.843	-1.499	ns
		t_H	—	0.464	0.950	0.980	1.080	1.030	1.671	ns
	GCLK PLL	t_{SU}	—	0.728	1.415	1.686	1.950	1.851	1.854	ns
		t_H	—	-0.655	-1.266	-1.514	-1.749	-1.664	-1.682	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.405	-0.829	-0.840	-0.911	-0.876	-1.531	ns
		t_H	—	0.478	0.977	1.011	1.112	1.062	1.702	ns
	GCLK PLL	t_{SU}	—	0.714	1.387	1.654	1.918	1.818	1.822	ns
		t_H	—	-0.641	-1.239	-1.483	-1.717	-1.632	-1.651	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.405	-0.829	-0.840	-0.911	-0.876	-1.531	ns
		t_H	—	0.478	0.977	1.011	1.112	1.062	1.702	ns
	GCLK PLL	t_{SU}	—	0.714	1.387	1.654	1.918	1.818	1.822	ns
		t_H	—	-0.641	-1.239	-1.483	-1.717	-1.632	-1.651	ns

Table 1–49. EP3SL150 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.391	-0.801	-0.808	-0.879	-0.843	-1.499	ns
		t_H	—	0.464	0.950	0.980	1.080	1.030	1.671	ns
	GCLK PLL	t_{SU}	—	0.728	1.415	1.686	1.950	1.851	1.854	ns
		t_H	—	-0.655	-1.266	-1.514	-1.749	-1.664	-1.682	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.391	-0.801	-0.808	-0.879	-0.843	-1.499	ns
		t_H	—	0.464	0.950	0.980	1.080	1.030	1.671	ns
	GCLK PLL	t_{SU}	—	0.728	1.415	1.686	1.950	1.851	1.854	ns
		t_H	—	-0.655	-1.266	-1.514	-1.749	-1.664	-1.682	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.384	-0.787	-0.792	-0.862	-0.827	-1.483	ns
		t_H	—	0.457	0.936	0.963	1.063	1.014	1.654	ns
	GCLK PLL	t_{SU}	—	0.735	1.429	1.702	1.967	1.867	1.870	ns
		t_H	—	-0.662	-1.280	-1.531	-1.766	-1.680	-1.699	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.384	-0.787	-0.792	-0.862	-0.827	-1.483	ns
		t_H	—	0.457	0.936	0.963	1.063	1.014	1.654	ns
	GCLK PLL	t_{SU}	—	0.735	1.429	1.702	1.967	1.867	1.870	ns
		t_H	—	-0.662	-1.280	-1.531	-1.766	-1.680	-1.699	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.574	-1.177	-1.244	-1.320	-1.281	-1.934	ns
		t_H	—	0.645	1.318	1.409	1.512	1.459	2.099	ns
	GCLK PLL	t_{SU}	—	0.543	1.036	1.246	1.505	1.408	1.414	ns
		t_H	—	-0.472	-0.895	-1.081	-1.313	-1.230	-1.249	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.574	-1.177	-1.244	-1.320	-1.281	-1.934	ns
		t_H	—	0.645	1.318	1.409	1.512	1.459	2.099	ns
	GCLK PLL	t_{SU}	—	0.543	1.036	1.246	1.505	1.408	1.414	ns
		t_H	—	-0.472	-0.895	-1.081	-1.313	-1.230	-1.249	ns

Table 1–50 specifies EP3SL150 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.573	4.404	4.931	5.206	4.868	5.466	ns
		GCLK PLL	t_{CO}	—	1.446	2.170	2.420	2.356	2.157	2.091	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.721	4.540	5.130	5.405	5.008	5.607	ns
		GCLK PLL	t_{CO}	—	1.594	2.306	2.619	2.555	2.297	2.232	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.781	4.619	5.185	5.460	5.095	5.693	ns
		GCLK PLL	t_{CO}	—	1.654	2.385	2.674	2.610	2.384	2.318	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	2.896	4.783	5.370	5.645	5.260	5.859	ns
		GCLK PLL	t_{CO}	—	1.769	2.549	2.859	2.795	2.549	2.484	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.721	4.540	5.129	5.404	5.008	5.607	ns
		GCLK PLL	t_{CO}	—	1.594	2.306	2.618	2.554	2.297	2.232	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.896	4.783	5.369	5.644	5.260	5.859	ns
		GCLK PLL	t_{CO}	—	1.769	2.549	2.858	2.794	2.549	2.484	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	2.951	4.859	5.434	5.709	5.339	5.937	ns
		GCLK PLL	t_{CO}	—	1.824	2.625	2.923	2.859	2.628	2.562	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	3.004	4.920	5.490	5.765	5.401	5.999	ns
		GCLK PLL	t_{CO}	—	1.877	2.686	2.979	2.915	2.690	2.624	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.659	4.565	5.199	5.474	5.037	5.635	ns
		GCLK PLL	t_{CO}	—	1.532	2.331	2.688	2.624	2.326	2.260	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.698	4.589	5.174	5.449	5.059	5.658	ns
		GCLK PLL	t_{CO}	—	1.571	2.355	2.663	2.599	2.348	2.283	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	12mA	GCLK	t_{CO}	—	2.946	4.934	5.574	5.849	5.414	6.013	ns
		GCLK PLL	t_{CO}	—	1.819	2.700	3.063	2.999	2.703	2.638	ns
2.5 V	16mA	GCLK	t_{CO}	—	2.979	4.993	5.671	5.946	5.476	6.075	ns
		GCLK PLL	t_{CO}	—	1.852	2.759	3.160	3.096	2.765	2.700	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.561	4.436	5.014	5.289	4.904	5.503	ns
		GCLK PLL	t_{CO}	—	1.434	2.202	2.503	2.439	2.193	2.128	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.623	4.553	5.243	5.518	5.023	5.621	ns
		GCLK PLL	t_{CO}	—	1.496	2.319	2.732	2.668	2.312	2.246	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.866	4.851	5.533	5.808	5.327	5.926	ns
		GCLK PLL	t_{CO}	—	1.739	2.617	3.022	2.958	2.616	2.551	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.693	4.598	5.215	5.490	5.067	5.666	ns
		GCLK PLL	t_{CO}	—	1.566	2.364	2.704	2.640	2.356	2.291	ns
1.8 V	10mA	GCLK	t_{CO}	—	2.955	4.960	5.626	5.901	5.439	6.038	ns
		GCLK PLL	t_{CO}	—	1.828	2.726	3.115	3.051	2.728	2.663	ns
1.8 V	12mA	GCLK	t_{CO}	—	3.026	5.106	5.846	6.121	5.591	6.190	ns
		GCLK PLL	t_{CO}	—	1.899	2.872	3.335	3.271	2.880	2.815	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.513	4.298	4.915	5.190	4.764	5.362	ns
		GCLK PLL	t_{CO}	—	1.386	2.064	2.404	2.340	2.053	1.987	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.781	4.758	5.392	5.667	5.238	5.836	ns
		GCLK PLL	t_{CO}	—	1.654	2.524	2.881	2.817	2.527	2.461	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.879	4.864	5.522	5.797	5.342	5.941	ns
		GCLK PLL	t_{CO}	—	1.752	2.630	3.011	2.947	2.631	2.566	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	8mA	GCLK	t_{CO}	—	2.804	4.720	5.365	5.640	5.196	5.795	ns
		GCLK PLL	t_{CO}	—	1.677	2.486	2.854	2.790	2.485	2.420	ns
1.5 V	10mA	GCLK	t_{CO}	—	2.970	5.007	5.720	5.995	5.486	6.085	ns
		GCLK PLL	t_{CO}	—	1.843	2.773	3.209	3.145	2.775	2.710	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.144	5.349	6.208	6.483	5.833	6.432	ns
		GCLK PLL	t_{CO}	—	2.017	3.115	3.697	3.633	3.122	3.057	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.789	4.818	5.620	5.895	5.274	5.873	ns
		GCLK PLL	t_{CO}	—	1.662	2.584	3.109	3.045	2.563	2.498	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.955	5.037	5.802	6.077	5.516	6.115	ns
		GCLK PLL	t_{CO}	—	1.828	2.803	3.291	3.227	2.805	2.740	ns
1.2 V	6mA	GCLK	t_{CO}	—	2.891	4.907	5.635	5.910	5.382	5.981	ns
		GCLK PLL	t_{CO}	—	1.764	2.673	3.124	3.060	2.671	2.606	ns
1.2 V	8mA	GCLK	t_{CO}	—	3.145	5.309	6.142	6.417	5.790	6.389	ns
		GCLK PLL	t_{CO}	—	2.018	3.075	3.631	3.567	3.079	3.014	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.271	3.936	4.411	4.686	4.388	4.987	ns
		GCLK PLL	t_{CO}	—	1.144	1.702	1.900	1.836	1.677	1.612	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.268	3.933	4.407	4.682	4.385	4.984	ns
		GCLK PLL	t_{CO}	—	1.141	1.699	1.896	1.832	1.674	1.609	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.271	3.941	4.416	4.691	4.393	4.992	ns
		GCLK PLL	t_{CO}	—	1.144	1.707	1.905	1.841	1.682	1.617	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.283	3.943	4.416	4.691	4.394	4.993	ns
		GCLK PLL	t_{CO}	—	1.156	1.709	1.905	1.841	1.683	1.618	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.278	3.950	4.428	4.703	4.402	5.001	ns
		GCLK PLL	t_{CO}	—	1.151	1.716	1.917	1.853	1.691	1.626	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.271	3.942	4.419	4.694	4.393	4.992	ns
		GCLK PLL	t_{CO}	—	1.144	1.708	1.908	1.844	1.682	1.617	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.275	3.951	4.431	4.706	4.403	5.002	ns
		GCLK PLL	t_{CO}	—	1.148	1.717	1.920	1.856	1.692	1.627	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.274	3.953	4.433	4.708	4.406	5.005	ns
		GCLK PLL	t_{CO}	—	1.147	1.719	1.922	1.858	1.695	1.630	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.272	3.951	4.431	4.706	4.404	5.003	ns
		GCLK PLL	t_{CO}	—	1.145	1.717	1.920	1.856	1.693	1.628	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.277	3.941	4.415	4.690	4.392	4.991	ns
		GCLK PLL	t_{CO}	—	1.150	1.707	1.904	1.840	1.681	1.616	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.293	3.976	4.456	4.731	4.429	5.028	ns
		GCLK PLL	t_{CO}	—	1.166	1.742	1.945	1.881	1.718	1.653	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.277	3.952	4.432	4.707	4.403	5.002	ns
		GCLK PLL	t_{CO}	—	1.150	1.718	1.921	1.857	1.692	1.627	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.276	3.953	4.434	4.709	4.405	5.004	ns
		GCLK PLL	t_{CO}	—	1.149	1.719	1.923	1.859	1.694	1.629	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.275	3.957	4.438	4.713	4.409	5.008	ns
		GCLK PLL	t_{CO}	—	1.148	1.723	1.927	1.863	1.698	1.633	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.283	3.971	4.454	4.729	4.424	5.023	ns
		GCLK PLL	t_{CO}	—	1.156	1.737	1.943	1.879	1.713	1.648	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.278	3.965	4.447	4.722	4.417	5.016	ns
		GCLK PLL	t_{CO}	—	1.151	1.731	1.936	1.872	1.706	1.641	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.279	3.948	4.425	4.700	4.400	4.999	ns
		GCLK PLL	t_{CO}	—	1.152	1.714	1.914	1.850	1.689	1.624	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.293	3.980	4.463	4.738	4.434	5.033	ns
		GCLK PLL	t_{CO}	—	1.166	1.746	1.952	1.888	1.723	1.658	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.274	3.932	4.406	4.681	4.383	4.982	ns
		GCLK PLL	t_{CO}	—	1.147	1.698	1.895	1.831	1.672	1.607	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.275	3.935	4.410	4.685	4.386	4.985	ns
		GCLK PLL	t_{CO}	—	1.148	1.701	1.899	1.835	1.675	1.610	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.277	3.943	4.418	4.693	4.394	4.993	ns
		GCLK PLL	t_{CO}	—	1.150	1.709	1.907	1.843	1.683	1.618	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.281	3.950	4.426	4.701	4.402	5.001	ns
		GCLK PLL	t_{CO}	—	1.154	1.716	1.915	1.851	1.691	1.626	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.283	3.953	4.429	4.704	4.405	5.004	ns
		GCLK PLL	t_{CO}	—	1.156	1.719	1.918	1.854	1.694	1.629	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.334	3.987	4.459	4.734	4.438	5.037	ns
		GCLK PLL	t_{CO}	—	1.207	1.753	1.948	1.884	1.727	1.662	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.280	3.941	4.417	4.692	4.392	4.991	ns
		GCLK PLL	t_{CO}	—	1.153	1.707	1.906	1.842	1.681	1.616	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.280	3.944	4.422	4.697	4.395	4.994	ns
		GCLK PLL	t_{CO}	—	1.153	1.710	1.911	1.847	1.684	1.619	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.277	3.939	4.415	4.690	4.390	4.989	ns
		GCLK PLL	t_{CO}	—	1.150	1.705	1.904	1.840	1.679	1.614	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.279	3.948	4.425	4.700	4.400	4.999	ns
		GCLK PLL	t_{CO}	—	1.152	1.714	1.914	1.850	1.689	1.624	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.288	3.962	4.441	4.716	4.414	5.013	ns
		GCLK PLL	t_{CO}	—	1.161	1.728	1.930	1.866	1.703	1.638	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.312	3.947	4.416	4.691	4.396	4.995	ns
		GCLK PLL	t_{CO}	—	1.185	1.713	1.905	1.841	1.685	1.620	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.291	3.960	4.441	4.716	4.412	5.011	ns
		GCLK PLL	t_{CO}	—	1.164	1.726	1.930	1.866	1.701	1.636	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.285	3.955	4.435	4.710	4.406	5.005	ns
		GCLK PLL	t_{CO}	—	1.158	1.721	1.924	1.860	1.695	1.630	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.295	3.973	4.456	4.731	4.425	5.024	ns
		GCLK PLL	t_{CO}	—	1.168	1.739	1.945	1.881	1.714	1.649	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.291	3.973	4.456	4.731	4.426	5.025	ns
		GCLK PLL	t_{CO}	—	1.164	1.739	1.945	1.881	1.715	1.650	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.291	3.972	4.454	4.729	4.424	5.023	ns
		GCLK PLL	t_{CO}	—	1.164	1.738	1.943	1.879	1.713	1.648	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.344	4.006	4.483	4.758	4.457	5.056	ns
		GCLK PLL	t_{CO}	—	1.217	1.772	1.972	1.908	1.746	1.681	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.269	5.280	5.952	6.227	5.770	6.368	ns
		GCLK PLL	t_{CO}	—	2.142	3.046	3.441	3.377	3.059	2.993	ns

Table 1–50. EP3SL150 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.269	5.280	5.952	6.227	5.770	6.368	ns
		GCLK PLL	t_{CO}	—	2.142	3.046	3.441	3.377	3.059	2.993	ns

Table 1–51 specifies EP3SL150 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–51. EP3SL150 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.633	4.454	5.008	5.270	4.910	5.474	ns
		GCLK PLL	t_{CO}	—	1.513	2.236	2.513	2.440	2.216	2.121	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.697	4.512	5.098	5.360	4.963	5.528	ns
		GCLK PLL	t_{CO}	—	1.577	2.294	2.603	2.530	2.269	2.175	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.828	4.669	5.244	5.506	5.125	5.689	ns
		GCLK PLL	t_{CO}	—	1.708	2.451	2.749	2.676	2.431	2.336	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.726	4.536	5.108	5.370	4.996	5.560	ns
		GCLK PLL	t_{CO}	—	1.606	2.318	2.613	2.540	2.302	2.207	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.868	4.719	5.313	5.575	5.181	5.746	ns
		GCLK PLL	t_{CO}	—	1.748	2.501	2.818	2.745	2.487	2.393	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.730	4.676	5.322	5.584	5.141	5.705	ns
		GCLK PLL	t_{CO}	—	1.610	2.458	2.827	2.754	2.447	2.352	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.724	4.607	5.200	5.462	5.064	5.628	ns
		GCLK PLL	t_{CO}	—	1.604	2.389	2.705	2.632	2.370	2.275	ns

Table 1–51. EP3SL150 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	12mA	GCLK	t_{CO}	—	2.929	4.887	5.534	5.796	5.360	5.924	ns
		GCLK PLL	t_{CO}	—	1.809	2.669	3.039	2.966	2.666	2.571	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.735	4.588	5.158	5.423	5.055	5.617	ns
		GCLK PLL	t_{CO}	—	1.614	2.367	2.660	2.587	2.354	2.259	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.766	4.723	5.422	5.687	5.184	5.747	ns
		GCLK PLL	t_{CO}	—	1.645	2.502	2.924	2.851	2.483	2.389	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.858	4.868	5.589	5.854	5.340	5.903	ns
		GCLK PLL	t_{CO}	—	1.737	2.647	3.091	3.018	2.639	2.545	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.743	4.643	5.262	5.527	5.103	5.665	ns
		GCLK PLL	t_{CO}	—	1.622	2.422	2.764	2.691	2.402	2.307	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.648	4.503	5.093	5.358	4.964	5.526	ns
		GCLK PLL	t_{CO}	—	1.527	2.282	2.595	2.522	2.263	2.168	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.773	4.746	5.402	5.667	5.216	5.778	ns
		GCLK PLL	t_{CO}	—	1.652	2.525	2.904	2.831	2.515	2.420	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.908	4.898	5.612	5.877	5.371	5.934	ns
		GCLK PLL	t_{CO}	—	1.787	2.677	3.114	3.041	2.670	2.576	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.795	4.724	5.387	5.652	5.191	5.754	ns
		GCLK PLL	t_{CO}	—	1.674	2.503	2.889	2.816	2.490	2.396	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.898	5.108	6.023	6.288	5.556	6.119	ns
		GCLK PLL	t_{CO}	—	1.777	2.887	3.525	3.452	2.855	2.761	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.026	5.176	6.014	6.279	5.636	6.199	ns
		GCLK PLL	t_{CO}	—	1.905	2.955	3.516	3.443	2.935	2.841	ns

Table 1–51. EP3SL150 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.222	3.857	4.329	4.591	4.296	4.861	ns
		GCLK PLL	t_{CO}	—	1.102	1.639	1.834	1.761	1.602	1.508	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.210	3.848	4.320	4.582	4.286	4.851	ns
		GCLK PLL	t_{CO}	—	1.090	1.630	1.825	1.752	1.592	1.498	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.215	3.849	4.320	4.582	4.287	4.852	ns
		GCLK PLL	t_{CO}	—	1.095	1.631	1.825	1.752	1.593	1.499	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.225	3.866	4.343	4.608	4.309	4.872	ns
		GCLK PLL	t_{CO}	—	1.104	1.645	1.845	1.772	1.608	1.514	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.213	3.854	4.330	4.595	4.296	4.859	ns
		GCLK PLL	t_{CO}	—	1.092	1.633	1.832	1.759	1.595	1.501	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.213	3.861	4.339	4.604	4.303	4.866	ns
		GCLK PLL	t_{CO}	—	1.092	1.640	1.841	1.768	1.602	1.508	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.205	3.856	4.333	4.598	4.298	4.861	ns
		GCLK PLL	t_{CO}	—	1.084	1.635	1.835	1.762	1.597	1.503	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.203	3.853	4.331	4.596	4.296	4.859	ns
		GCLK PLL	t_{CO}	—	1.082	1.632	1.833	1.760	1.595	1.501	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.208	3.845	4.320	4.585	4.287	4.850	ns
		GCLK PLL	t_{CO}	—	1.087	1.624	1.822	1.749	1.586	1.492	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.210	3.859	4.336	4.601	4.301	4.864	ns
		GCLK PLL	t_{CO}	—	1.089	1.638	1.838	1.765	1.600	1.506	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.225	3.869	4.349	4.614	4.311	4.874	ns
		GCLK PLL	t_{CO}	—	1.104	1.648	1.851	1.778	1.610	1.516	ns

Table 1–51. EP3SL150 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.214	3.864	4.345	4.610	4.306	4.869	ns
		GCLK PLL	t_{CO}	—	1.093	1.643	1.847	1.774	1.605	1.511	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.206	3.858	4.338	4.603	4.300	4.863	ns
		GCLK PLL	t_{CO}	—	1.085	1.637	1.840	1.767	1.599	1.505	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.220	3.847	4.319	4.584	4.288	4.851	ns
		GCLK PLL	t_{CO}	—	1.099	1.626	1.821	1.748	1.587	1.493	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.211	3.846	4.321	4.586	4.288	4.851	ns
		GCLK PLL	t_{CO}	—	1.090	1.625	1.823	1.750	1.587	1.493	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.205	3.845	4.319	4.584	4.286	4.849	ns
		GCLK PLL	t_{CO}	—	1.084	1.624	1.821	1.748	1.585	1.491	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.207	3.848	4.323	4.588	4.290	4.853	ns
		GCLK PLL	t_{CO}	—	1.086	1.627	1.825	1.752	1.589	1.495	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.206	3.851	4.327	4.592	4.293	4.856	ns
		GCLK PLL	t_{CO}	—	1.085	1.630	1.829	1.756	1.592	1.498	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.215	3.849	4.320	4.585	4.290	4.853	ns
		GCLK PLL	t_{CO}	—	1.094	1.628	1.822	1.749	1.589	1.495	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.226	3.855	4.331	4.596	4.296	4.859	ns
		GCLK PLL	t_{CO}	—	1.105	1.634	1.833	1.760	1.595	1.501	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.220	3.858	4.336	4.601	4.300	4.863	ns
		GCLK PLL	t_{CO}	—	1.099	1.637	1.838	1.765	1.599	1.505	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.212	3.849	4.326	4.591	4.291	4.854	ns
		GCLK PLL	t_{CO}	—	1.091	1.628	1.828	1.755	1.590	1.496	ns

Table 1–51. EP3SL150 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.229	3.871	4.355	4.620	4.313	4.876	ns
		GCLK PLL	t_{CO}	—	1.108	1.650	1.857	1.784	1.612	1.518	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.217	3.861	4.342	4.607	4.302	4.865	ns
		GCLK PLL	t_{CO}	—	1.096	1.640	1.844	1.771	1.601	1.507	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.220	3.873	4.356	4.621	4.315	4.878	ns
		GCLK PLL	t_{CO}	—	1.099	1.652	1.858	1.785	1.614	1.520	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.171	5.194	5.867	6.129	5.670	6.234	ns
		GCLK PLL	t_{CO}	—	2.051	2.976	3.372	3.299	2.976	2.881	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.171	5.194	5.867	6.129	5.670	6.234	ns
		GCLK PLL	t_{CO}	—	2.051	2.976	3.372	3.299	2.976	2.881	ns

Table 1–52 through Table 1–55 show the maximum I/O timing parameters for EP3SL150 devices for differential I/O standards.

Table 1–52 specifies EP3SL150 Column Pins Input Timing parameters for differential I/O standards.

Table 1–52. EP3SL150 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.483	-0.991	-1.023	-1.110	-1.064	-1.746	ns
		t_H	—	0.555	1.135	1.191	1.304	1.245	1.914	ns
	GCLK PLL	t_{SU}	—	0.639	1.234	1.479	1.728	1.637	1.617	ns
		t_H	—	-0.567	-1.090	-1.311	-1.534	-1.456	-1.449	ns

Table 1–52. EP3SL150 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.483	-0.991	-1.023	-1.110	-1.064	-1.746	ns
		t_H	—	0.555	1.135	1.191	1.304	1.245	1.914	ns
	GCLK PLL	t_{SU}	—	0.639	1.234	1.479	1.728	1.637	1.617	ns
		t_H	—	-0.567	-1.090	-1.311	-1.534	-1.456	-1.449	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.490	-1.006	-1.039	-1.126	-1.080	-1.762	ns
		t_H	—	0.562	1.149	1.207	1.320	1.261	1.930	ns
	GCLK PLL	t_{SU}	—	0.632	1.219	1.463	1.712	1.621	1.601	ns
		t_H	—	-0.560	-1.076	-1.295	-1.518	-1.440	-1.433	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.490	-1.006	-1.039	-1.126	-1.080	-1.762	ns
		t_H	—	0.562	1.149	1.207	1.320	1.261	1.930	ns
	GCLK PLL	t_{SU}	—	0.632	1.219	1.463	1.712	1.621	1.601	ns
		t_H	—	-0.560	-1.076	-1.295	-1.518	-1.440	-1.433	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.504	-1.033	-1.071	-1.159	-1.113	-1.794	ns
		t_H	—	0.575	1.176	1.239	1.352	1.293	1.962	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.431	1.679	1.588	1.569	ns
		t_H	—	-0.547	-1.049	-1.263	-1.486	-1.408	-1.401	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.504	-1.033	-1.071	-1.159	-1.113	-1.794	ns
		t_H	—	0.575	1.176	1.239	1.352	1.293	1.962	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.431	1.679	1.588	1.569	ns
		t_H	—	-0.547	-1.049	-1.263	-1.486	-1.408	-1.401	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.490	-1.006	-1.039	-1.126	-1.080	-1.762	ns
		t_H	—	0.562	1.149	1.207	1.320	1.261	1.930	ns
	GCLK PLL	t_{SU}	—	0.632	1.219	1.463	1.712	1.621	1.601	ns
		t_H	—	-0.560	-1.076	-1.295	-1.518	-1.440	-1.433	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.490	-1.006	-1.039	-1.126	-1.080	-1.762	ns
		t_H	—	0.562	1.149	1.207	1.320	1.261	1.930	ns
	GCLK PLL	t_{SU}	—	0.632	1.219	1.463	1.712	1.621	1.601	ns
		t_H	—	-0.560	-1.076	-1.295	-1.518	-1.440	-1.433	ns

Table 1–52. EP3SL150 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.504	-1.033	-1.071	-1.159	-1.113	-1.794	ns
		t_H	—	0.575	1.176	1.239	1.352	1.293	1.962	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.431	1.679	1.588	1.569	ns
		t_H	—	-0.547	-1.049	-1.263	-1.486	-1.408	-1.401	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.504	-1.033	-1.071	-1.159	-1.113	-1.794	ns
		t_H	—	0.575	1.176	1.239	1.352	1.293	1.962	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.431	1.679	1.588	1.569	ns
		t_H	—	-0.547	-1.049	-1.263	-1.486	-1.408	-1.401	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.528	-1.084	-1.131	-1.218	-1.172	-1.854	ns
		t_H	—	0.598	1.224	1.294	1.407	1.349	2.017	ns
	GCLK PLL	t_{SU}	—	0.594	1.141	1.371	1.620	1.529	1.509	ns
		t_H	—	-0.524	-1.001	-1.208	-1.431	-1.352	-1.346	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.528	-1.084	-1.131	-1.218	-1.172	-1.854	ns
		t_H	—	0.598	1.224	1.294	1.407	1.349	2.017	ns
	GCLK PLL	t_{SU}	—	0.594	1.141	1.371	1.620	1.529	1.509	ns
		t_H	—	-0.524	-1.001	-1.208	-1.431	-1.352	-1.346	ns

Table 1–53 specifies EP3SL150 Row Pins Input Timing parameters for differential I/O standards.

Table 1–53. EP3SL150 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.523	-1.071	-1.119	-1.203	-1.158	-1.813	ns
		t_H	—	0.594	1.213	1.286	1.396	1.338	1.980	ns
	GCLK PLL	t_{SU}	—	0.619	1.194	1.428	1.689	1.591	1.597	ns
		t_H	—	-0.547	-1.048	-1.258	-1.490	-1.406	-1.427	ns

Table 1–53. EP3SL150 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
MINI-LVDS	GCLK	t_{SU}	—	-0.523	-1.071	-1.119	-1.203	-1.158	-1.813	ns
		t_H	—	0.594	1.213	1.286	1.396	1.338	1.980	ns
	GCLK PLL	t_{SU}	—	0.619	1.194	1.428	1.689	1.591	1.597	ns
		t_H	—	-0.547	-1.048	-1.258	-1.490	-1.406	-1.427	ns
RSDS	GCLK	t_{SU}	—	-0.523	-1.071	-1.119	-1.203	-1.158	-1.813	ns
		t_H	—	0.594	1.213	1.286	1.396	1.338	1.980	ns
	GCLK PLL	t_{SU}	—	0.619	1.194	1.428	1.689	1.591	1.597	ns
		t_H	—	-0.547	-1.048	-1.258	-1.490	-1.406	-1.427	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.447	-0.917	-0.941	-1.023	-0.979	-1.635	ns
		t_H	—	0.519	1.061	1.109	1.217	1.160	1.803	ns
	GCLK PLL	t_{SU}	—	0.737	1.433	1.705	1.970	1.870	1.874	ns
		t_H	—	-0.664	-1.284	-1.534	-1.769	-1.683	-1.703	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.447	-0.917	-0.941	-1.023	-0.979	-1.635	ns
		t_H	—	0.519	1.061	1.109	1.217	1.160	1.803	ns
	GCLK PLL	t_{SU}	—	0.737	1.433	1.705	1.970	1.870	1.874	ns
		t_H	—	-0.664	-1.284	-1.534	-1.769	-1.683	-1.703	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.454	-0.932	-0.957	-1.039	-0.995	-1.651	ns
		t_H	—	0.526	1.075	1.125	1.233	1.176	1.819	ns
	GCLK PLL	t_{SU}	—	0.730	1.419	1.689	1.953	1.854	1.858	ns
		t_H	—	-0.657	-1.270	-1.517	-1.752	-1.667	-1.686	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.454	-0.932	-0.957	-1.039	-0.995	-1.651	ns
		t_H	—	0.526	1.075	1.125	1.233	1.176	1.819	ns
	GCLK PLL	t_{SU}	—	0.730	1.419	1.689	1.953	1.854	1.858	ns
		t_H	—	-0.657	-1.270	-1.517	-1.752	-1.667	-1.686	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.468	-0.959	-0.989	-1.072	-1.028	-1.683	ns
		t_H	—	0.539	1.102	1.157	1.265	1.208	1.851	ns
	GCLK PLL	t_{SU}	—	0.716	1.391	1.657	1.921	1.821	1.826	ns
		t_H	—	-0.643	-1.243	-1.486	-1.720	-1.635	-1.655	ns

Table 1–53. EP3SL150 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.468	-0.959	-0.989	-1.072	-1.028	-1.683	ns
		t_H	—	0.539	1.102	1.157	1.265	1.208	1.851	ns
	GCLK PLL	t_{SU}	—	0.716	1.391	1.657	1.921	1.821	1.826	ns
		t_H	—	-0.643	-1.243	-1.486	-1.720	-1.635	-1.655	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.454	-0.932	-0.957	-1.039	-0.995	-1.651	ns
		t_H	—	0.526	1.075	1.125	1.233	1.176	1.819	ns
	GCLK PLL	t_{SU}	—	0.730	1.419	1.689	1.953	1.854	1.858	ns
		t_H	—	-0.657	-1.270	-1.517	-1.752	-1.667	-1.686	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.454	-0.932	-0.957	-1.039	-0.995	-1.651	ns
		t_H	—	0.526	1.075	1.125	1.233	1.176	1.819	ns
	GCLK PLL	t_{SU}	—	0.730	1.419	1.689	1.953	1.854	1.858	ns
		t_H	—	-0.657	-1.270	-1.517	-1.752	-1.667	-1.686	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.468	-0.959	-0.989	-1.072	-1.028	-1.683	ns
		t_H	—	0.539	1.102	1.157	1.265	1.208	1.851	ns
	GCLK PLL	t_{SU}	—	0.716	1.391	1.657	1.921	1.821	1.826	ns
		t_H	—	-0.643	-1.243	-1.486	-1.720	-1.635	-1.655	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.468	-0.959	-0.989	-1.072	-1.028	-1.683	ns
		t_H	—	0.539	1.102	1.157	1.265	1.208	1.851	ns
	GCLK PLL	t_{SU}	—	0.716	1.391	1.657	1.921	1.821	1.826	ns
		t_H	—	-0.643	-1.243	-1.486	-1.720	-1.635	-1.655	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.492	-1.010	-1.049	-1.131	-1.087	-1.743	ns
		t_H	—	0.562	1.150	1.212	1.320	1.264	1.906	ns
	GCLK PLL	t_{SU}	—	0.671	1.296	1.547	1.810	1.711	1.716	ns
		t_H	—	-0.599	-1.153	-1.379	-1.614	-1.530	-1.548	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.492	-1.010	-1.049	-1.131	-1.087	-1.743	ns
		t_H	—	0.562	1.150	1.212	1.320	1.264	1.906	ns
	GCLK PLL	t_{SU}	—	0.671	1.296	1.547	1.810	1.711	1.716	ns
		t_H	—	-0.599	-1.153	-1.379	-1.614	-1.530	-1.548	ns

Table 1–54 specifies EP3SL150 Column Pins Output Timing parameters for differential I/O standards.

Table 1–54. EP3SL150 Column Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.162	4.231	4.773	5.070	4.915	5.503	ns
		GCLK PLL	t_{CO}	—	1.037	2.002	2.267	2.225	2.209	2.133	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.090	4.084	4.600	4.895	4.742	5.330	ns
		GCLK PLL	t_{CO}	—	0.965	1.855	2.094	2.050	2.036	1.960	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.082	4.069	4.582	4.877	4.724	5.312	ns
		GCLK PLL	t_{CO}	—	0.957	1.840	2.076	2.032	2.018	1.942	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.082	4.069	4.582	4.877	4.724	5.312	ns
		GCLK PLL	t_{CO}	—	0.957	1.840	2.076	2.032	2.018	1.942	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.083	4.071	4.584	4.879	4.726	5.314	ns
		GCLK PLL	t_{CO}	—	0.958	1.842	2.078	2.034	2.020	1.944	ns

Table 1–54. EP3SL150 Column Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.082	4.068	4.581	4.876	4.723	5.311	ns
		GCLK PLL	t_{CO}	—	0.957	1.839	2.075	2.031	2.017	1.941	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.079	4.062	4.574	4.869	4.716	5.304	ns
		GCLK PLL	t_{CO}	—	0.954	1.833	2.068	2.024	2.010	1.934	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.078	4.060	4.571	4.866	4.713	5.301	ns
		GCLK PLL	t_{CO}	—	0.953	1.831	2.065	2.021	2.007	1.931	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.079	4.062	4.574	4.869	4.716	5.304	ns
		GCLK PLL	t_{CO}	—	0.954	1.833	2.068	2.024	2.010	1.934	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.074	4.052	4.562	4.857	4.704	5.292	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.056	2.012	1.998	1.922	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.071	4.047	4.556	4.851	4.698	5.286	ns
		GCLK PLL	t_{CO}	—	0.946	1.818	2.050	2.006	1.992	1.916	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.077	4.059	4.570	4.865	4.712	5.300	ns
		GCLK PLL	t_{CO}	—	0.952	1.830	2.064	2.020	2.006	1.930	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}		2.065	4.034	4.541	4.835	4.682	5.271	ns
		GCLK PLL	t_{CO}	—	0.940	1.805	2.035	1.990	1.976	1.901	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.072	4.049	4.558	4.853	4.700	5.288	ns
		GCLK PLL	t_{CO}	—	0.947	1.820	2.052	2.008	1.994	1.918	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.067	4.039	4.547	4.841	4.688	5.277	ns
		GCLK PLL	t_{CO}	—	0.942	1.810	2.041	1.996	1.982	1.907	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.071	4.046	4.555	4.850	4.697	5.285	ns
		GCLK PLL	t_{CO}	—	0.946	1.817	2.049	2.005	1.991	1.915	ns

Table 1–54. EP3SL150 Column Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.069	4.043	4.551	4.846	4.693	5.281	ns
		GCLK PLL	t_{CO}	—	0.944	1.814	2.045	2.001	1.987	1.911	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.068	4.041	4.549	4.844	4.691	5.279	ns
		GCLK PLL	t_{CO}	—	0.943	1.812	2.043	1.999	1.985	1.909	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.061	4.026	4.531	4.826	4.673	5.261	ns
		GCLK PLL	t_{CO}	—	0.936	1.797	2.025	1.981	1.967	1.891	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.087	4.079	4.594	4.889	4.736	5.324	ns
		GCLK PLL	t_{CO}	—	0.962	1.850	2.088	2.044	2.030	1.954	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.082	4.069	4.582	4.877	4.724	5.312	ns
		GCLK PLL	t_{CO}	—	0.957	1.840	2.076	2.032	2.018	1.942	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.079	4.063	4.575	4.870	4.717	5.305	ns
		GCLK PLL	t_{CO}	—	0.954	1.834	2.069	2.025	2.011	1.935	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.082	4.069	4.582	4.877	4.724	5.312	ns
		GCLK PLL	t_{CO}	—	0.957	1.840	2.076	2.032	2.018	1.942	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.080	4.065	4.577	4.872	4.719	5.307	ns
		GCLK PLL	t_{CO}	—	0.955	1.836	2.071	2.027	2.013	1.937	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.072	4.048	4.557	4.852	4.699	5.287	ns
		GCLK PLL	t_{CO}	—	0.947	1.819	2.051	2.007	1.993	1.917	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.074	4.053	4.563	4.858	4.705	5.293	ns
		GCLK PLL	t_{CO}	—	0.949	1.824	2.057	2.013	1.999	1.923	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.085	4.074	4.588	4.883	4.730	5.318	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.082	2.038	2.024	1.948	ns

Table 1–54. EP3SL150 Column Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.078	4.060	4.571	4.866	4.713	5.301	ns
		GCLK PLL	t_{CO}	—	0.953	1.831	2.065	2.021	2.007	1.931	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.080	4.064	4.576	4.871	4.718	5.306	ns
		GCLK PLL	t_{CO}	—	0.955	1.835	2.070	2.026	2.012	1.936	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.078	4.061	4.573	4.867	4.715	5.303	ns
		GCLK PLL	t_{CO}	—	0.953	1.832	2.067	2.022	2.009	1.933	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.075	4.054	4.564	4.859	4.706	5.294	ns
		GCLK PLL	t_{CO}	—	0.950	1.825	2.058	2.014	2.000	1.924	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.069	4.043	4.551	4.846	4.693	5.281	ns
		GCLK PLL	t_{CO}	—	0.944	1.814	2.045	2.001	1.987	1.911	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.072	4.049	4.558	4.853	4.700	5.288	ns
		GCLK PLL	t_{CO}	—	0.947	1.820	2.052	2.008	1.994	1.918	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.076	4.056	4.567	4.862	4.709	5.297	ns
		GCLK PLL	t_{CO}	—	0.951	1.827	2.061	2.017	2.003	1.927	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.075	4.054	4.564	4.859	4.706	5.294	ns
		GCLK PLL	t_{CO}	—	0.950	1.825	2.058	2.014	2.000	1.924	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.073	4.050	4.560	4.854	4.701	5.290	ns
		GCLK PLL	t_{CO}	—	0.948	1.821	2.054	2.009	1.995	1.920	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.071	4.047	4.556	4.851	4.698	5.286	ns
		GCLK PLL	t_{CO}	—	0.946	1.818	2.050	2.006	1.992	1.916	ns

Table 1–55 specifies EP3SL150 Row Pins Output Timing parameters for differential I/O standards.

Table 1–55. EP3SL150 Row Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	t_{CO}	—	2.118	4.143	4.676	4.964	4.814	5.370	ns
		GCLK PLL	t_{CO}	—	0.993	1.913	2.169	2.119	2.107	2.001	ns
LVDS_E_1R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
MINI-LVDS	-	GCLK	t_{CO}	—	2.118	4.143	4.676	4.964	4.814	5.370	ns
		GCLK PLL	t_{CO}	—	0.993	1.913	2.169	2.119	2.107	2.001	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
RSDS	-	GCLK	t_{CO}	—	2.118	4.143	4.676	4.964	4.814	5.370	ns
		GCLK PLL	t_{CO}	—	0.993	1.913	2.169	2.119	2.107	2.001	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.117	4.141	4.674	4.961	4.811	5.368	ns
		GCLK PLL	t_{CO}	—	0.992	1.911	2.167	2.116	2.104	1.999	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.054	4.014	4.523	4.809	4.661	5.217	ns
		GCLK PLL	t_{CO}	—	0.929	1.784	2.016	1.964	1.954	1.848	ns

Table 1–55. EP3SL150 Row Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.046	3.997	4.504	4.790	4.641	5.198	ns
		GCLK PLL	t_{CO}	—	0.921	1.767	1.997	1.945	1.934	1.829	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.045	3.994	4.501	4.786	4.638	5.195	ns
		GCLK PLL	t_{CO}	—	0.920	1.764	1.994	1.941	1.931	1.826	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.044	3.992	4.498	4.784	4.636	5.192	ns
		GCLK PLL	t_{CO}	—	0.919	1.762	1.991	1.939	1.929	1.823	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.043	3.990	4.496	4.781	4.633	5.190	ns
		GCLK PLL	t_{CO}	—	0.918	1.760	1.989	1.936	1.926	1.821	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.038	3.980	4.484	4.769	4.621	5.178	ns
		GCLK PLL	t_{CO}	—	0.913	1.750	1.977	1.924	1.914	1.809	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.038	3.980	4.484	4.769	4.621	5.178	ns
		GCLK PLL	t_{CO}	—	0.913	1.750	1.977	1.924	1.914	1.809	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.032	3.969	4.471	4.756	4.608	5.165	ns
		GCLK PLL	t_{CO}	—	0.907	1.739	1.964	1.911	1.901	1.796	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.034	3.972	4.475	4.760	4.612	5.169	ns
		GCLK PLL	t_{CO}	—	0.909	1.742	1.968	1.915	1.905	1.800	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.033	3.971	4.474	4.758	4.611	5.168	ns
		GCLK PLL	t_{CO}	—	0.908	1.741	1.967	1.913	1.904	1.799	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.031	3.967	4.469	4.754	4.606	5.163	ns
		GCLK PLL	t_{CO}	—	0.906	1.737	1.962	1.909	1.899	1.794	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.022	3.949	4.448	4.732	4.584	5.142	ns
		GCLK PLL	t_{CO}	—	0.897	1.719	1.941	1.887	1.877	1.773	ns

Table 1–55. EP3SL150 Row Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.054	4.013	4.522	4.808	4.659	5.216	ns
		GCLK PLL	t_{CO}	—	0.929	1.783	2.015	1.963	1.952	1.847	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.047	3.998	4.506	4.791	4.643	5.200	ns
		GCLK PLL	t_{CO}	—	0.922	1.768	1.999	1.946	1.936	1.831	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.043	3.990	4.496	4.781	4.633	5.190	ns
		GCLK PLL	t_{CO}	—	0.918	1.760	1.989	1.936	1.926	1.821	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.050	4.005	4.513	4.798	4.650	5.207	ns
		GCLK PLL	t_{CO}	—	0.925	1.775	2.006	1.953	1.943	1.838	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.043	3.991	4.497	4.782	4.634	5.191	ns
		GCLK PLL	t_{CO}	—	0.918	1.761	1.990	1.937	1.927	1.822	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.043	3.991	4.497	4.782	4.634	5.191	ns
		GCLK PLL	t_{CO}	—	0.918	1.761	1.990	1.937	1.927	1.822	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.042	3.989	4.495	4.780	4.632	5.189	ns
		GCLK PLL	t_{CO}	—	0.917	1.759	1.988	1.935	1.925	1.820	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.038	3.981	4.485	4.770	4.622	5.179	ns
		GCLK PLL	t_{CO}	—	0.913	1.751	1.978	1.925	1.915	1.810	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.033	3.971	4.474	4.758	4.611	5.168	ns
		GCLK PLL	t_{CO}	—	0.908	1.741	1.967	1.913	1.904	1.799	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.034	3.973	4.476	4.761	4.613	5.170	ns
		GCLK PLL	t_{CO}	—	0.909	1.743	1.969	1.916	1.906	1.801	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.042	3.988	4.494	4.779	4.631	5.188	ns
		GCLK PLL	t_{CO}	—	0.917	1.758	1.987	1.934	1.924	1.819	ns

Table 1–55. EP3SL150 Row Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.038	3.980	4.484	4.769	4.621	5.178	ns
		GCLK PLL	t_{CO}	—	0.913	1.750	1.977	1.924	1.914	1.809	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.034	3.973	4.476	4.761	4.613	5.170	ns
		GCLK PLL	t_{CO}	—	0.909	1.743	1.969	1.916	1.906	1.801	ns

Table 1–56 through Table 1–57 show EP3Sl150 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–56 specifies EP3SL150 Column Pin delay adders when using the Regional Clock.

Table 1–56. EP3SL150 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	—	0.158	0.322	0.348	0.375	0.359	0.492	ns
RCLK PLL input adder	—	0.011	0.022	0.0	-0.029	-0.013	-0.012	ns
RCLK output adder	—	-0.158	-0.321	-0.346	-0.375	-0.359	-0.491	ns
RCLK PLL output adder	—	0.498	1.065	1.31	1.315	1.188	1.7	ns

Table 1–57 specifies EP3SL150 Row Pin delay adders when using the Regional Clock.

Table 1–57. EP3SL150 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RCLK input adder	—	0.135	0.274	0.297	0.321	0.309	0.421	ns
RCLK PLL input adder	—	-0.007	-0.013	-0.039	-0.071	-0.054	-0.068	ns
RCLK output adder	—	-0.135	-0.273	-0.296	-0.319	-0.307	-0.419	ns
RCLK PLL output adder	—	0.007	0.013	0.038	0.071	0.054	0.067	ns

EP3SL200 I/O Timing Parameters

Table 1–58 through Table 1–61 show the maximum I/O timing parameters for EP3SL200 devices for single ended I/O standards.

Table 1–58 specifies EP3SL200 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–58. EP3SL200 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.699	-1.429	-1.526	-1.626	-1.575	-2.290	ns
		t_H	—	0.768	1.567	1.686	1.812	1.749	2.450	ns
	GCLK PLL	t_{SU}	—	0.460	0.872	1.063	1.314	1.221	1.199	ns
		t_H	—	-0.391	-0.734	-0.903	-1.128	-1.047	-1.039	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.699	-1.429	-1.526	-1.626	-1.575	-2.290	ns
		t_H	—	0.768	1.567	1.686	1.812	1.749	2.450	ns
	GCLK PLL	t_{SU}	—	0.460	0.872	1.063	1.314	1.221	1.199	ns
		t_H	—	-0.391	-0.734	-0.903	-1.128	-1.047	-1.039	ns
2.5 V	GCLK	t_{SU}	—	-0.704	-1.440	-1.538	-1.638	-1.587	-2.302	ns
		t_H	—	0.773	1.577	1.698	1.824	1.761	2.462	ns
	GCLK PLL	t_{SU}	—	0.455	0.861	1.051	1.302	1.209	1.187	ns
		t_H	—	-0.386	-0.724	-0.891	-1.116	-1.035	-1.027	ns

Table 1–58. EP3SL200 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	GCLK	t_{SU}	—	-0.714	-1.460	-1.562	-1.662	-1.611	-2.326	ns
		t_H	—	0.783	1.597	1.721	1.848	1.784	2.485	ns
	GCLK PLL	t_{SU}	—	0.445	0.841	1.027	1.278	1.185	1.163	ns
		t_H	—	-0.376	-0.704	-0.868	-1.092	-1.012	-1.004	ns
1.5 V	GCLK	t_{SU}	—	-0.694	-1.419	-1.515	-1.614	-1.563	-2.279	ns
		t_H	—	0.763	1.557	1.675	1.800	1.737	2.439	ns
	GCLK PLL	t_{SU}	—	0.465	0.882	1.074	1.326	1.233	1.210	ns
		t_H	—	-0.396	-0.744	-0.914	-1.140	-1.059	-1.050	ns
1.2 V	GCLK	t_{SU}	—	-0.637	-1.305	-1.381	-1.479	-1.428	-2.145	ns
		t_H	—	0.707	1.443	1.542	1.666	1.604	2.306	ns
	GCLK PLL	t_{SU}	—	0.522	0.996	1.208	1.461	1.368	1.344	ns
		t_H	—	-0.452	-0.858	-1.047	-1.274	-1.192	-1.183	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.577	-1.182	-1.238	-1.334	-1.284	-2.002	ns
		t_H	—	0.647	1.322	1.401	1.523	1.461	2.165	ns
	GCLK PLL	t_{SU}	—	0.582	1.119	1.351	1.606	1.512	1.487	ns
		t_H	—	-0.512	-0.979	-1.188	-1.417	-1.335	-1.324	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.577	-1.182	-1.238	-1.334	-1.284	-2.002	ns
		t_H	—	0.647	1.322	1.401	1.523	1.461	2.165	ns
	GCLK PLL	t_{SU}	—	0.582	1.119	1.351	1.606	1.512	1.487	ns
		t_H	—	-0.512	-0.979	-1.188	-1.417	-1.335	-1.324	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.553	-1.131	-1.178	-1.275	-1.225	-1.942	ns
	GCLK PLL	t_{SU}	—	0.606	1.170	1.411	1.665	1.571	2.110	ns
		t_H	—	-0.535	-1.027	-1.243	-1.472	-1.391	1.547	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.553	-1.131	-1.178	-1.275	-1.225	-1.379	ns
	GCLK PLL	t_{SU}	—	0.606	1.170	1.411	1.665	1.571	-1.942	ns
		t_H	—	-0.535	-1.027	-1.243	-1.472	-1.391	2.110	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.539	-1.104	-1.146	-1.242	-1.192	2.110	ns
	GCLK PLL	t_{SU}	—	0.620	1.197	1.443	1.698	1.604	1.547	ns
		t_H	—	-0.548	-1.054	-1.275	-1.504	-1.423	-1.379	ns

Table 1–58. EP3SL200 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.539	-1.104	-1.146	-1.242	-1.192	-1.910	ns
	GCLK PLL	t_{SU}	—	0.620	1.197	1.443	1.698	1.604	2.078	ns
		t_{H}	—	-0.548	-1.054	-1.275	-1.504	-1.423	1.579	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.553	-1.131	-1.178	-1.275	-1.225	1.579	ns
	GCLK PLL	t_{SU}	—	0.606	1.170	1.411	1.665	1.571	-1.411	ns
		t_{H}	—	-0.535	-1.027	-1.243	-1.472	-1.391	-1.910	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.553	-1.131	-1.178	-1.275	-1.225	2.110	ns
	GCLK PLL	t_{SU}	—	0.606	1.170	1.411	1.665	1.571	1.547	ns
		t_{H}	—	-0.535	-1.027	-1.243	-1.472	-1.391	-1.379	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.539	-1.104	-1.146	-1.242	-1.192	-1.942	ns
	GCLK PLL	t_{SU}	—	0.620	1.197	1.443	1.698	1.604	2.110	ns
		t_{H}	—	-0.548	-1.054	-1.275	-1.504	-1.423	1.547	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.539	-1.104	-1.146	-1.242	-1.192	-1.379	ns
	GCLK PLL	t_{SU}	—	0.620	1.197	1.443	1.698	1.604	-1.942	ns
		t_{H}	—	-0.548	-1.054	-1.275	-1.504	-1.423	2.110	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.532	-1.089	-1.130	-1.226	-1.176	1.547	ns
	GCLK PLL	t_{SU}	—	0.627	1.212	1.459	1.714	1.620	-1.379	ns
		t_{H}	—	-0.555	-1.068	-1.291	-1.520	-1.439	-1.910	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.532	-1.089	-1.130	-1.226	-1.176	2.078	ns
	GCLK PLL	t_{SU}	—	0.627	1.212	1.459	1.714	1.620	1.579	ns
		t_{H}	—	-0.555	-1.068	-1.291	-1.520	-1.439	-1.411	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.699	-1.429	-1.526	-1.626	-1.575	-1.910	ns
		t_{H}	—	0.768	1.567	1.686	1.812	1.749	2.078	ns
	GCLK PLL	t_{SU}	—	0.460	0.872	1.063	1.314	1.221	1.579	ns
		t_{H}	—	-0.391	-0.734	-0.903	-1.128	-1.047	-1.411	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.699	-1.429	-1.526	-1.626	-1.575	-1.910	ns
		t_{H}	—	0.768	1.567	1.686	1.812	1.749	2.078	ns
	GCLK PLL	t_{SU}	—	0.460	0.872	1.063	1.314	1.221	1.579	ns
		t_{H}	—	-0.391	-0.734	-0.903	-1.128	-1.047	-1.411	ns

Table 1–59 specifies EP3SL200 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–59. EP3SL200 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.643	-1.315	-1.394	-1.501	-1.457	-2.165	ns
		t_H	—	0.714	1.456	1.559	1.693	1.635	2.330	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.189	1.452	1.352	1.338	ns
		t_H	—	-0.444	-0.839	-1.024	-1.260	-1.174	-1.173	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.643	-1.315	-1.394	-1.501	-1.457	-2.165	ns
		t_H	—	0.714	1.456	1.559	1.693	1.635	2.330	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.189	1.452	1.352	1.338	ns
		t_H	—	-0.444	-0.839	-1.024	-1.260	-1.174	-1.173	ns
2.5 V	GCLK	t_{SU}	—	-0.648	-1.325	-1.405	-1.513	-1.469	-2.176	ns
		t_H	—	0.719	1.466	1.571	1.705	1.647	2.342	ns
	GCLK PLL	t_{SU}	—	0.510	0.970	1.178	1.440	1.340	1.327	ns
		t_H	—	-0.439	-0.829	-1.012	-1.248	-1.162	-1.161	ns
1.8 V	GCLK	t_{SU}	—	-0.663	-1.356	-1.442	-1.535	-1.488	-2.199	ns
		t_H	—	0.734	1.497	1.607	1.727	1.666	2.364	ns
	GCLK PLL	t_{SU}	—	0.500	0.950	1.154	1.416	1.317	1.303	ns
		t_H	—	-0.429	-0.809	-0.989	-1.224	-1.139	-1.138	ns
1.5 V	GCLK	t_{SU}	—	-0.642	-1.315	-1.394	-1.486	-1.440	-2.151	ns
		t_H	—	0.713	1.456	1.559	1.678	1.618	2.316	ns
	GCLK PLL	t_{SU}	—	0.521	0.991	1.202	1.465	1.365	1.351	ns
		t_H	—	-0.450	-0.850	-1.037	-1.273	-1.187	-1.186	ns
1.2 V	GCLK	t_{SU}	—	-0.585	-1.198	-1.258	-1.348	-1.303	-2.015	ns
		t_H	—	0.656	1.340	1.424	1.542	1.483	2.181	ns
	GCLK PLL	t_{SU}	—	0.578	1.108	1.338	1.603	1.502	1.487	ns
		t_H	—	-0.507	-0.966	-1.172	-1.409	-1.322	-1.321	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.517	-1.059	-1.096	-1.199	-1.157	-1.867	ns
		t_H	—	0.589	1.202	1.264	1.395	1.338	2.035	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.487	1.754	1.652	1.636	ns
		t_H	—	-0.569	-1.093	-1.319	-1.558	-1.471	-1.468	ns

Table 1–59. EP3SL200 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.517	-1.059	-1.096	-1.199	-1.157	-1.867	ns
		t_H	—	0.589	1.202	1.264	1.395	1.338	2.035	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.487	1.754	1.652	1.636	ns
		t_H	—	-0.569	-1.093	-1.319	-1.558	-1.471	-1.468	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.477	-0.975	-0.999	-1.086	-1.043	-1.756	ns
		t_H	—	0.550	1.123	1.170	1.287	1.229	1.927	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.597	1.865	1.762	1.746	ns
		t_H	—	-0.613	-1.183	-1.426	-1.664	-1.576	-1.575	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.477	-0.975	-0.999	-1.086	-1.043	-1.756	ns
		t_H	—	0.550	1.123	1.170	1.287	1.229	1.927	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.597	1.865	1.762	1.746	ns
		t_H	—	-0.613	-1.183	-1.426	-1.664	-1.576	-1.575	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.463	-0.947	-0.967	-1.054	-1.010	-1.724	ns
		t_H	—	0.536	1.096	1.139	1.255	1.197	1.896	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.629	1.897	1.795	1.778	ns
		t_H	—	-0.627	-1.210	-1.457	-1.696	-1.608	-1.606	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.463	-0.947	-0.967	-1.054	-1.010	-1.724	ns
		t_H	—	0.536	1.096	1.139	1.255	1.197	1.896	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.629	1.897	1.795	1.778	ns
		t_H	—	-0.627	-1.210	-1.457	-1.696	-1.608	-1.606	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.477	-0.975	-0.999	-1.086	-1.043	-1.756	ns
		t_H	—	0.550	1.123	1.170	1.287	1.229	1.927	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.597	1.865	1.762	1.746	ns
		t_H	—	-0.613	-1.183	-1.426	-1.664	-1.576	-1.575	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.477	-0.975	-0.999	-1.086	-1.043	-1.756	ns
		t_H	—	0.550	1.123	1.170	1.287	1.229	1.927	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.597	1.865	1.762	1.746	ns
		t_H	—	-0.613	-1.183	-1.426	-1.664	-1.576	-1.575	ns

Table 1–59. EP3SL200 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.463	-0.947	-0.967	-1.054	-1.010	-1.724	ns
		t_H	—	0.536	1.096	1.139	1.255	1.197	1.896	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.629	1.897	1.795	1.778	ns
		t_H	—	-0.627	-1.210	-1.457	-1.696	-1.608	-1.606	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.463	-0.947	-0.967	-1.054	-1.010	-1.724	ns
		t_H	—	0.536	1.096	1.139	1.255	1.197	1.896	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.629	1.897	1.795	1.778	ns
		t_H	—	-0.627	-1.210	-1.457	-1.696	-1.608	-1.606	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.456	-0.933	-0.951	-1.037	-0.994	-1.708	ns
		t_H	—	0.529	1.082	1.122	1.238	1.181	1.879	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.645	1.914	1.811	1.794	ns
		t_H	—	-0.634	-1.224	-1.474	-1.713	-1.624	-1.623	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.456	-0.933	-0.951	-1.037	-0.994	-1.708	ns
		t_H	—	0.529	1.082	1.122	1.238	1.181	1.879	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.645	1.914	1.811	1.794	ns
		t_H	—	-0.634	-1.224	-1.474	-1.713	-1.624	-1.623	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.643	-1.315	-1.394	-1.501	-1.457	-2.165	ns
		t_H	—	0.714	1.456	1.559	1.693	1.635	2.330	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.189	1.452	1.352	1.338	ns
		t_H	—	-0.444	-0.839	-1.024	-1.260	-1.174	-1.173	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.643	-1.315	-1.394	-1.501	-1.457	-2.165	ns
		t_H	—	0.714	1.456	1.559	1.693	1.635	2.330	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.189	1.452	1.352	1.338	ns
		t_H	—	-0.444	-0.839	-1.024	-1.260	-1.174	-1.173	ns

Table 1–60 specifies EP3SL200 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.610	4.481	5.015	5.295	4.956	5.583	ns
		GCLK PLL	t_{CO}	—	1.446	2.168	2.412	2.337	2.144	2.077	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.758	4.617	5.214	5.494	5.096	5.724	ns
		GCLK PLL	t_{CO}	—	1.594	2.304	2.611	2.536	2.284	2.218	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.818	4.696	5.269	5.549	5.183	5.810	ns
		GCLK PLL	t_{CO}	—	1.654	2.383	2.666	2.591	2.371	2.304	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	2.933	4.860	5.454	5.734	5.348	5.976	ns
		GCLK PLL	t_{CO}	—	1.769	2.547	2.851	2.776	2.536	2.470	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.758	4.617	5.213	5.493	5.096	5.724	ns
		GCLK PLL	t_{CO}	—	1.594	2.304	2.610	2.535	2.284	2.218	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.933	4.860	5.453	5.733	5.348	5.976	ns
		GCLK PLL	t_{CO}	—	1.769	2.547	2.850	2.775	2.536	2.470	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	2.988	4.936	5.518	5.798	5.427	6.054	ns
		GCLK PLL	t_{CO}	—	1.824	2.623	2.915	2.840	2.615	2.548	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	3.041	4.997	5.574	5.854	5.489	6.116	ns
		GCLK PLL	t_{CO}	—	1.877	2.684	2.971	2.896	2.677	2.610	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.696	4.642	5.283	5.563	5.125	5.752	ns
		GCLK PLL	t_{CO}	—	1.532	2.329	2.680	2.605	2.313	2.246	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.735	4.666	5.258	5.538	5.147	5.775	ns
		GCLK PLL	t_{CO}	—	1.571	2.353	2.655	2.580	2.335	2.269	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	12mA	GCLK	t_{CO}	—	2.983	5.011	5.658	5.938	5.502	6.130	ns
		GCLK PLL	t_{CO}	—	1.819	2.698	3.055	2.980	2.690	2.624	ns
2.5 V	16mA	GCLK	t_{CO}	—	3.016	5.070	5.755	6.035	5.564	6.192	ns
		GCLK PLL	t_{CO}	—	1.852	2.757	3.152	3.077	2.752	2.686	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.598	4.513	5.098	5.378	4.992	5.620	ns
		GCLK PLL	t_{CO}	—	1.434	2.200	2.495	2.420	2.180	2.114	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.660	4.630	5.327	5.607	5.111	5.738	ns
		GCLK PLL	t_{CO}	—	1.496	2.317	2.724	2.649	2.299	2.232	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.903	4.928	5.617	5.897	5.415	6.043	ns
		GCLK PLL	t_{CO}	—	1.739	2.615	3.014	2.939	2.603	2.537	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.730	4.675	5.299	5.579	5.155	5.783	ns
		GCLK PLL	t_{CO}	—	1.566	2.362	2.696	2.621	2.343	2.277	ns
1.8 V	10mA	GCLK	t_{CO}	—	2.992	5.037	5.710	5.990	5.527	6.155	ns
		GCLK PLL	t_{CO}	—	1.828	2.724	3.107	3.032	2.715	2.649	ns
1.8 V	12mA	GCLK	t_{CO}	—	3.063	5.183	5.930	6.210	5.679	6.307	ns
		GCLK PLL	t_{CO}	—	1.899	2.870	3.327	3.252	2.867	2.801	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.550	4.375	4.999	5.279	4.852	5.479	ns
		GCLK PLL	t_{CO}	—	1.386	2.062	2.396	2.321	2.042	1.974	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.818	4.835	5.476	5.756	5.326	5.953	ns
		GCLK PLL	t_{CO}	—	1.654	2.522	2.873	2.798	2.514	2.447	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.916	4.941	5.606	5.886	5.430	6.058	ns
		GCLK PLL	t_{CO}	—	1.752	2.628	3.003	2.928	2.618	2.552	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	8mA	GCLK	t_{CO}	—	2.841	4.797	5.449	5.729	5.284	5.912	ns
		GCLK PLL	t_{CO}	—	1.677	2.484	2.846	2.771	2.472	2.406	ns
1.5 V	10mA	GCLK	t_{CO}	—	3.007	5.084	5.804	6.084	5.574	6.202	ns
		GCLK PLL	t_{CO}	—	1.843	2.771	3.201	3.126	2.762	2.696	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.181	5.426	6.292	6.572	5.921	6.549	ns
		GCLK PLL	t_{CO}	—	2.017	3.113	3.689	3.614	3.109	3.043	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.826	4.895	5.704	5.984	5.362	5.990	ns
		GCLK PLL	t_{CO}	—	1.662	2.582	3.101	3.026	2.550	2.484	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.992	5.114	5.886	6.166	5.604	6.232	ns
		GCLK PLL	t_{CO}	—	1.828	2.801	3.283	3.208	2.792	2.726	ns
1.2 V	6mA	GCLK	t_{CO}	—	2.928	4.984	5.719	5.999	5.470	6.098	ns
		GCLK PLL	t_{CO}	—	1.764	2.671	3.116	3.041	2.658	2.592	ns
1.2 V	8mA	GCLK	t_{CO}	—	3.182	5.386	6.226	6.506	5.878	6.506	ns
		GCLK PLL	t_{CO}	—	2.018	3.073	3.623	3.548	3.066	3.000	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.308	4.013	4.495	4.775	4.476	5.104	ns
		GCLK PLL	t_{CO}	—	1.144	1.700	1.892	1.817	1.664	1.598	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.305	4.010	4.491	4.771	4.473	5.101	ns
		GCLK PLL	t_{CO}	—	1.141	1.697	1.888	1.813	1.661	1.595	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.308	4.018	4.500	4.780	4.481	5.109	ns
		GCLK PLL	t_{CO}	—	1.144	1.705	1.897	1.822	1.669	1.603	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.320	4.020	4.500	4.780	4.482	5.110	ns
		GCLK PLL	t_{CO}	—	1.156	1.707	1.897	1.822	1.670	1.604	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.315	4.027	4.512	4.792	4.490	5.118	ns
		GCLK PLL	t_{CO}	—	1.151	1.714	1.909	1.834	1.678	1.612	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.308	4.019	4.503	4.783	4.481	5.109	ns
		GCLK PLL	t_{CO}	—	1.144	1.706	1.900	1.825	1.669	1.603	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.312	4.028	4.515	4.795	4.491	5.119	ns
		GCLK PLL	t_{CO}	—	1.148	1.715	1.912	1.837	1.679	1.613	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.311	4.030	4.517	4.797	4.494	5.122	ns
		GCLK PLL	t_{CO}	—	1.147	1.717	1.914	1.839	1.682	1.616	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.309	4.028	4.515	4.795	4.492	5.120	ns
		GCLK PLL	t_{CO}	—	1.145	1.715	1.912	1.837	1.680	1.614	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.314	4.018	4.499	4.779	4.480	5.108	ns
		GCLK PLL	t_{CO}	—	1.150	1.705	1.896	1.821	1.668	1.602	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.330	4.053	4.540	4.820	4.517	5.145	ns
		GCLK PLL	t_{CO}	—	1.166	1.740	1.937	1.862	1.705	1.639	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.314	4.029	4.516	4.796	4.491	5.119	ns
		GCLK PLL	t_{CO}	—	1.150	1.716	1.913	1.838	1.679	1.613	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.313	4.030	4.518	4.798	4.493	5.121	ns
		GCLK PLL	t_{CO}	—	1.149	1.717	1.915	1.840	1.681	1.615	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.312	4.034	4.522	4.802	4.497	5.125	ns
		GCLK PLL	t_{CO}	—	1.148	1.721	1.919	1.844	1.685	1.619	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.320	4.048	4.538	4.818	4.512	5.140	ns
		GCLK PLL	t_{CO}	—	1.156	1.735	1.935	1.860	1.700	1.634	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.315	4.042	4.531	4.811	4.505	5.133	ns
		GCLK PLL	t_{CO}	—	1.151	1.729	1.928	1.853	1.693	1.627	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.316	4.025	4.509	4.789	4.488	5.116	ns
		GCLK PLL	t_{CO}	—	1.152	1.712	1.906	1.831	1.676	1.610	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.330	4.057	4.547	4.827	4.522	5.150	ns
		GCLK PLL	t_{CO}	—	1.166	1.744	1.944	1.869	1.710	1.644	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.311	4.009	4.490	4.770	4.471	5.099	ns
		GCLK PLL	t_{CO}	—	1.147	1.696	1.887	1.812	1.659	1.593	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.312	4.012	4.494	4.774	4.474	5.102	ns
		GCLK PLL	t_{CO}	—	1.148	1.699	1.891	1.816	1.662	1.596	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.314	4.020	4.502	4.782	4.482	5.110	ns
		GCLK PLL	t_{CO}	—	1.150	1.707	1.899	1.824	1.670	1.604	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.318	4.027	4.510	4.790	4.490	5.118	ns
		GCLK PLL	t_{CO}	—	1.154	1.714	1.907	1.832	1.678	1.612	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.320	4.030	4.513	4.793	4.493	5.121	ns
		GCLK PLL	t_{CO}	—	1.156	1.717	1.910	1.835	1.681	1.615	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.371	4.064	4.543	4.823	4.526	5.154	ns
		GCLK PLL	t_{CO}	—	1.207	1.751	1.940	1.865	1.714	1.648	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.317	4.018	4.501	4.781	4.480	5.108	ns
		GCLK PLL	t_{CO}	—	1.153	1.705	1.898	1.823	1.668	1.602	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.317	4.021	4.506	4.786	4.483	5.111	ns
		GCLK PLL	t_{CO}	—	1.153	1.708	1.903	1.828	1.671	1.605	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.314	4.016	4.499	4.779	4.478	5.106	ns
		GCLK PLL	t_{CO}	—	1.150	1.703	1.896	1.821	1.666	1.600	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.316	4.025	4.509	4.789	4.488	5.116	ns
		GCLK PLL	t_{CO}	—	1.152	1.712	1.906	1.831	1.676	1.610	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.325	4.039	4.525	4.805	4.502	5.130	ns
		GCLK PLL	t_{CO}	—	1.161	1.726	1.922	1.847	1.690	1.624	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.349	4.024	4.500	4.780	4.484	5.112	ns
		GCLK PLL	t_{CO}	—	1.185	1.711	1.897	1.822	1.672	1.606	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.328	4.037	4.525	4.805	4.500	5.128	ns
		GCLK PLL	t_{CO}	—	1.164	1.724	1.922	1.847	1.688	1.622	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.322	4.032	4.519	4.799	4.494	5.122	ns
		GCLK PLL	t_{CO}	—	1.158	1.719	1.916	1.841	1.682	1.616	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.332	4.050	4.540	4.820	4.513	5.141	ns
		GCLK PLL	t_{CO}	—	1.168	1.737	1.937	1.862	1.701	1.635	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.328	4.050	4.540	4.820	4.514	5.142	ns
		GCLK PLL	t_{CO}	—	1.164	1.737	1.937	1.862	1.702	1.636	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.328	4.049	4.538	4.818	4.512	5.140	ns
		GCLK PLL	t_{CO}	—	1.164	1.736	1.935	1.860	1.700	1.634	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.381	4.083	4.567	4.847	4.545	5.173	ns
		GCLK PLL	t_{CO}	—	1.217	1.770	1.964	1.889	1.733	1.667	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.306	5.357	6.036	6.316	5.858	6.485	ns
		GCLK PLL	t_{CO}	—	2.142	3.044	3.433	3.358	3.046	2.979	ns

Table 1–60. EP3SL200 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.306	5.357	6.036	6.316	5.858	6.485	ns
		GCLK PLL	t_{CO}	—	2.142	3.044	3.433	3.358	3.046	2.979	ns

Table 1–61 specifies EP3SL200 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–61. EP3SL200 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.700	4.589	5.154	5.448	5.083	5.701	ns
		GCLK PLL	t_{CO}	—	1.542	2.294	2.571	2.495	2.274	2.198	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.764	4.647	5.244	5.538	5.136	5.755	ns
		GCLK PLL	t_{CO}	—	1.606	2.352	2.661	2.585	2.327	2.252	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.895	4.804	5.390	5.684	5.298	5.916	ns
		GCLK PLL	t_{CO}	—	1.737	2.509	2.807	2.731	2.489	2.413	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.793	4.671	5.254	5.548	5.169	5.787	ns
		GCLK PLL	t_{CO}	—	1.635	2.376	2.671	2.595	2.360	2.284	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.935	4.854	5.459	5.753	5.354	5.973	ns
		GCLK PLL	t_{CO}	—	1.777	2.559	2.876	2.800	2.545	2.470	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.797	4.811	5.468	5.762	5.314	5.932	ns
		GCLK PLL	t_{CO}	—	1.639	2.516	2.885	2.809	2.505	2.429	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.791	4.742	5.346	5.640	5.237	5.855	ns
		GCLK PLL	t_{CO}	—	1.633	2.447	2.763	2.687	2.428	2.352	ns

Table 1–61. EP3SL200 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	12mA	GCLK	t_{CO}	—	2.996	5.022	5.680	5.974	5.533	6.151	ns
		GCLK PLL	t_{CO}	—	1.838	2.727	3.097	3.021	2.724	2.648	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.806	4.731	5.314	5.593	5.217	5.838	ns
		GCLK PLL	t_{CO}	—	1.643	2.425	2.718	2.642	2.412	2.336	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.837	4.866	5.578	5.857	5.346	5.968	ns
		GCLK PLL	t_{CO}	—	1.674	2.560	2.982	2.906	2.541	2.466	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.929	5.011	5.745	6.024	5.502	6.124	ns
		GCLK PLL	t_{CO}	—	1.766	2.705	3.149	3.073	2.697	2.622	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.814	4.786	5.418	5.697	5.265	5.886	ns
		GCLK PLL	t_{CO}	—	1.651	2.480	2.822	2.746	2.460	2.384	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.719	4.646	5.249	5.528	5.126	5.747	ns
		GCLK PLL	t_{CO}	—	1.556	2.340	2.653	2.577	2.321	2.245	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.844	4.889	5.558	5.837	5.378	5.999	ns
		GCLK PLL	t_{CO}	—	1.681	2.583	2.962	2.886	2.573	2.497	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.979	5.041	5.768	6.047	5.533	6.155	ns
		GCLK PLL	t_{CO}	—	1.816	2.735	3.172	3.096	2.728	2.653	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.866	4.867	5.543	5.822	5.353	5.975	ns
		GCLK PLL	t_{CO}	—	1.703	2.561	2.947	2.871	2.548	2.473	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.969	5.251	6.179	6.458	5.718	6.340	ns
		GCLK PLL	t_{CO}	—	1.806	2.945	3.583	3.507	2.913	2.838	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.097	5.319	6.170	6.449	5.798	6.420	ns
		GCLK PLL	t_{CO}	—	1.934	3.013	3.574	3.498	2.993	2.918	ns

Table 1–61. EP3SL200 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.289	3.992	4.475	4.769	4.469	5.088	ns
		GCLK PLL	t_{CO}	—	1.131	1.697	1.892	1.816	1.660	1.585	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.277	3.983	4.466	4.760	4.459	5.078	ns
		GCLK PLL	t_{CO}	—	1.119	1.688	1.883	1.807	1.650	1.575	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.282	3.984	4.466	4.760	4.460	5.079	ns
		GCLK PLL	t_{CO}	—	1.124	1.689	1.883	1.807	1.651	1.576	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.296	4.009	4.499	4.778	4.471	5.093	ns
		GCLK PLL	t_{CO}	—	1.133	1.703	1.903	1.827	1.666	1.591	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.284	3.997	4.486	4.765	4.458	5.080	ns
		GCLK PLL	t_{CO}	—	1.121	1.691	1.890	1.814	1.653	1.578	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.284	4.004	4.495	4.774	4.465	5.087	ns
		GCLK PLL	t_{CO}	—	1.121	1.698	1.899	1.823	1.660	1.585	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.276	3.999	4.489	4.768	4.460	5.082	ns
		GCLK PLL	t_{CO}	—	1.113	1.693	1.893	1.817	1.655	1.580	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.274	3.996	4.487	4.766	4.458	5.080	ns
		GCLK PLL	t_{CO}	—	1.111	1.690	1.891	1.815	1.653	1.578	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.279	3.988	4.476	4.755	4.449	5.071	ns
		GCLK PLL	t_{CO}	—	1.116	1.682	1.880	1.804	1.644	1.569	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.281	4.002	4.492	4.771	4.463	5.085	ns
		GCLK PLL	t_{CO}	—	1.118	1.696	1.896	1.820	1.658	1.583	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.296	4.012	4.505	4.784	4.473	5.095	ns
		GCLK PLL	t_{CO}	—	1.133	1.706	1.909	1.833	1.668	1.593	ns

Table 1–61. EP3SL200 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.285	4.007	4.501	4.780	4.468	5.090	ns
		GCLK PLL	t_{CO}	—	1.122	1.701	1.905	1.829	1.663	1.588	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.277	4.001	4.494	4.773	4.462	5.084	ns
		GCLK PLL	t_{CO}	—	1.114	1.695	1.898	1.822	1.657	1.582	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.291	3.990	4.475	4.754	4.450	5.072	ns
		GCLK PLL	t_{CO}	—	1.128	1.684	1.879	1.803	1.645	1.570	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.282	3.989	4.477	4.756	4.450	5.072	ns
		GCLK PLL	t_{CO}	—	1.119	1.683	1.881	1.805	1.645	1.570	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.276	3.988	4.475	4.754	4.448	5.070	ns
		GCLK PLL	t_{CO}	—	1.113	1.682	1.879	1.803	1.643	1.568	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.278	3.991	4.479	4.758	4.452	5.074	ns
		GCLK PLL	t_{CO}	—	1.115	1.685	1.883	1.807	1.647	1.572	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.277	3.994	4.483	4.762	4.455	5.077	ns
		GCLK PLL	t_{CO}	—	1.114	1.688	1.887	1.811	1.650	1.575	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.286	3.992	4.476	4.755	4.452	5.074	ns
		GCLK PLL	t_{CO}	—	1.123	1.686	1.880	1.804	1.647	1.572	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.297	3.998	4.487	4.766	4.458	5.080	ns
		GCLK PLL	t_{CO}	—	1.134	1.692	1.891	1.815	1.653	1.578	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.291	4.001	4.492	4.771	4.462	5.084	ns
		GCLK PLL	t_{CO}	—	1.128	1.695	1.896	1.820	1.657	1.582	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.283	3.992	4.482	4.761	4.453	5.075	ns
		GCLK PLL	t_{CO}	—	1.120	1.686	1.886	1.810	1.648	1.573	ns

Table 1–61. EP3SL200 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.300	4.014	4.511	4.790	4.475	5.097	ns
		GCLK PLL	t_{CO}	—	1.137	1.708	1.915	1.839	1.670	1.595	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.288	4.004	4.498	4.777	4.464	5.086	ns
		GCLK PLL	t_{CO}	—	1.125	1.698	1.902	1.826	1.659	1.584	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.291	4.016	4.512	4.791	4.477	5.099	ns
		GCLK PLL	t_{CO}	—	1.128	1.710	1.916	1.840	1.672	1.597	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.238	5.329	6.013	6.307	5.843	6.461	ns
		GCLK PLL	t_{CO}	—	2.080	3.034	3.430	3.354	3.034	2.958	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.238	5.329	6.013	6.307	5.843	6.461	ns
		GCLK PLL	t_{CO}	—	2.080	3.034	3.430	3.354	3.034	2.958	ns

Table 1–62 through Table 1–65 show the maximum I/O timing parameters for EP3SL200 devices for differential I/O standards.

Table 1–62 specifies EP3SL200 Column Pins Input Timing parameters for differential I/O standards.

Table 1–62. EP3SL200 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.534	-1.091	-1.133	-1.229	-1.179	-1.898	ns
		t_H	—	0.606	1.235	1.301	1.423	1.360	2.066	ns
	GCLK PLL	t_{SU}	—	0.630	1.216	1.464	1.721	1.625	1.607	ns
		t_H	—	-0.558	-1.072	-1.296	-1.527	-1.444	-1.439	ns

Table 1–62. EP3SL200 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.534	-1.091	-1.133	-1.229	-1.179	-1.898	ns
		t_H	—	0.606	1.235	1.301	1.423	1.360	2.066	ns
	GCLK PLL	t_{SU}	—	0.630	1.216	1.464	1.721	1.625	1.607	ns
		t_H	—	-0.558	-1.072	-1.296	-1.527	-1.444	-1.439	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.541	-1.106	-1.149	-1.245	-1.195	-1.914	ns
		t_H	—	0.613	1.249	1.317	1.439	1.376	2.082	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.448	1.705	1.609	1.591	ns
		t_H	—	-0.551	-1.058	-1.280	-1.511	-1.428	-1.423	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.541	-1.106	-1.149	-1.245	-1.195	-1.914	ns
		t_H	—	0.613	1.249	1.317	1.439	1.376	2.082	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.448	1.705	1.609	1.591	ns
		t_H	—	-0.551	-1.058	-1.280	-1.511	-1.428	-1.423	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.555	-1.133	-1.181	-1.278	-1.228	-1.946	ns
		t_H	—	0.626	1.276	1.349	1.471	1.408	2.114	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.416	1.672	1.576	1.559	ns
		t_H	—	-0.538	-1.031	-1.248	-1.479	-1.396	-1.391	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.555	-1.133	-1.181	-1.278	-1.228	-1.946	ns
		t_H	—	0.626	1.276	1.349	1.471	1.408	2.114	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.416	1.672	1.576	1.559	ns
		t_H	—	-0.538	-1.031	-1.248	-1.479	-1.396	-1.391	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.541	-1.106	-1.149	-1.245	-1.195	-1.914	ns
		t_H	—	0.613	1.249	1.317	1.439	1.376	2.082	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.448	1.705	1.609	1.591	ns
		t_H	—	-0.551	-1.058	-1.280	-1.511	-1.428	-1.423	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.541	-1.106	-1.149	-1.245	-1.195	-1.914	ns
		t_H	—	0.613	1.249	1.317	1.439	1.376	2.082	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.448	1.705	1.609	1.591	ns
		t_H	—	-0.551	-1.058	-1.280	-1.511	-1.428	-1.423	ns

Table 1–62. EP3SL200 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.555	-1.133	-1.181	-1.278	-1.228	-1.946	ns
		t_H	—	0.626	1.276	1.349	1.471	1.408	2.114	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.416	1.672	1.576	1.559	ns
		t_H	—	-0.538	-1.031	-1.248	-1.479	-1.396	-1.391	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.555	-1.133	-1.181	-1.278	-1.228	-1.946	ns
		t_H	—	0.626	1.276	1.349	1.471	1.408	2.114	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.416	1.672	1.576	1.559	ns
		t_H	—	-0.538	-1.031	-1.248	-1.479	-1.396	-1.391	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.579	-1.184	-1.241	-1.337	-1.287	-2.006	ns
		t_H	—	0.649	1.324	1.404	1.526	1.464	2.169	ns
	GCLK PLL	t_{SU}	—	0.585	1.123	1.356	1.613	1.517	1.499	ns
		t_H	—	-0.515	-0.983	-1.193	-1.424	-1.340	-1.336	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.579	-1.184	-1.241	-1.337	-1.287	-2.006	ns
		t_H	—	0.649	1.324	1.404	1.526	1.464	2.169	ns
	GCLK PLL	t_{SU}	—	0.585	1.123	1.356	1.613	1.517	1.499	ns
		t_H	—	-0.515	-0.983	-1.193	-1.424	-1.340	-1.336	ns

Table 1–63 specifies EP3SL200 Row Pins Input Timing parameters for differential I/O standards.

Table 1–63. EP3SL200 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.592	-1.209	-1.270	-1.366	-1.317	-2.024	ns
		t_H	—	0.663	1.351	1.437	1.559	1.497	2.191	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.366	1.631	1.531	1.517	ns
		t_H	—	-0.516	-0.987	-1.196	-1.432	-1.346	-1.347	ns

Table 1–63. EP3SL200 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
MINI-LVDS	GCLK	t_{SU}	—	-0.592	-1.209	-1.270	-1.366	-1.317	-2.024	ns
		t_H	—	0.663	1.351	1.437	1.559	1.497	2.191	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.366	1.631	1.531	1.517	ns
		t_H	—	-0.516	-0.987	-1.196	-1.432	-1.346	-1.347	ns
RSDS	GCLK	t_{SU}	—	-0.592	-1.209	-1.270	-1.366	-1.317	-2.024	ns
		t_H	—	0.663	1.351	1.437	1.559	1.497	2.191	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.366	1.631	1.531	1.517	ns
		t_H	—	-0.516	-0.987	-1.196	-1.432	-1.346	-1.347	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.516	-1.055	-1.092	-1.186	-1.138	-1.846	ns
		t_H	—	0.588	1.199	1.260	1.380	1.319	2.014	ns
	GCLK PLL	t_{SU}	—	0.706	1.372	1.643	1.912	1.810	1.794	ns
		t_H	—	-0.633	-1.223	-1.472	-1.711	-1.623	-1.623	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.516	-1.055	-1.092	-1.186	-1.138	-1.846	ns
		t_H	—	0.588	1.199	1.260	1.380	1.319	2.014	ns
	GCLK PLL	t_{SU}	—	0.706	1.372	1.643	1.912	1.810	1.794	ns
		t_H	—	-0.633	-1.223	-1.472	-1.711	-1.623	-1.623	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.523	-1.070	-1.108	-1.202	-1.154	-1.862	ns
		t_H	—	0.595	1.213	1.276	1.396	1.335	2.030	ns
	GCLK PLL	t_{SU}	—	0.699	1.358	1.627	1.895	1.794	1.778	ns
		t_H	—	-0.626	-1.209	-1.455	-1.694	-1.607	-1.606	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.523	-1.070	-1.108	-1.202	-1.154	-1.862	ns
		t_H	—	0.595	1.213	1.276	1.396	1.335	2.030	ns
	GCLK PLL	t_{SU}	—	0.699	1.358	1.627	1.895	1.794	1.778	ns
		t_H	—	-0.626	-1.209	-1.455	-1.694	-1.607	-1.606	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.537	-1.097	-1.140	-1.235	-1.187	-1.894	ns
		t_H	—	0.608	1.240	1.308	1.428	1.367	2.062	ns
	GCLK PLL	t_{SU}	—	0.685	1.330	1.595	1.863	1.761	1.746	ns
		t_H	—	-0.612	-1.182	-1.424	-1.662	-1.575	-1.575	ns

Table 1–63. EP3SL200 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.537	-1.097	-1.140	-1.235	-1.187	-1.894	ns
		t_H	—	0.608	1.240	1.308	1.428	1.367	2.062	ns
	GCLK PLL	t_{SU}	—	0.685	1.330	1.595	1.863	1.761	1.746	ns
		t_H	—	-0.612	-1.182	-1.424	-1.662	-1.575	-1.575	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.523	-1.070	-1.108	-1.202	-1.154	-1.862	ns
		t_H	—	0.595	1.213	1.276	1.396	1.335	2.030	ns
	GCLK PLL	t_{SU}	—	0.699	1.358	1.627	1.895	1.794	1.778	ns
		t_H	—	-0.626	-1.209	-1.455	-1.694	-1.607	-1.606	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.523	-1.070	-1.108	-1.202	-1.154	-1.862	ns
		t_H	—	0.595	1.213	1.276	1.396	1.335	2.030	ns
	GCLK PLL	t_{SU}	—	0.699	1.358	1.627	1.895	1.794	1.778	ns
		t_H	—	-0.626	-1.209	-1.455	-1.694	-1.607	-1.606	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.537	-1.097	-1.140	-1.235	-1.187	-1.894	ns
		t_H	—	0.608	1.240	1.308	1.428	1.367	2.062	ns
	GCLK PLL	t_{SU}	—	0.685	1.330	1.595	1.863	1.761	1.746	ns
		t_H	—	-0.612	-1.182	-1.424	-1.662	-1.575	-1.575	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.537	-1.097	-1.140	-1.235	-1.187	-1.894	ns
		t_H	—	0.608	1.240	1.308	1.428	1.367	2.062	ns
	GCLK PLL	t_{SU}	—	0.685	1.330	1.595	1.863	1.761	1.746	ns
		t_H	—	-0.612	-1.182	-1.424	-1.662	-1.575	-1.575	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.561	-1.148	-1.200	-1.294	-1.246	-1.954	ns
		t_H	—	0.631	1.288	1.363	1.483	1.423	2.117	ns
	GCLK PLL	t_{SU}	—	0.640	1.235	1.485	1.752	1.651	1.636	ns
		t_H	—	-0.568	-1.092	-1.317	-1.556	-1.470	-1.468	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.561	-1.148	-1.200	-1.294	-1.246	-1.954	ns
		t_H	—	0.631	1.288	1.363	1.483	1.423	2.117	ns
	GCLK PLL	t_{SU}	—	0.640	1.235	1.485	1.752	1.651	1.636	ns
		t_H	—	-0.568	-1.092	-1.317	-1.556	-1.470	-1.468	ns

Table 1–64 specifies EP3SL200 Column Pins Output Timing parameters for differential I/O standards.

Table 1–64. EP3SL200 Column Pins Output Timing Parameters (Part 1 of 4) (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.203	4.315	4.864	5.166	5.010	5.629	ns
		GCLK PLL	t_{CO}	—	1.038	2.005	2.265	2.214	2.203	2.122	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.131	4.168	4.691	4.991	4.837	5.456	ns
		GCLK PLL	t_{CO}	—	0.966	1.858	2.092	2.039	2.030	1.949	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.123	4.153	4.673	4.973	4.819	5.438	ns
		GCLK PLL	t_{CO}	—	0.958	1.843	2.074	2.021	2.012	1.931	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.123	4.153	4.673	4.973	4.819	5.438	ns
		GCLK PLL	t_{CO}	—	0.958	1.843	2.074	2.021	2.012	1.931	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.124	4.155	4.675	4.975	4.821	5.440	ns
		GCLK PLL	t_{CO}	—	0.959	1.845	2.076	2.023	2.014	1.933	ns

Table 1–64. EP3SL200 Column Pins Output Timing Parameters (Part 2 of 4) (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.123	4.152	4.672	4.972	4.818	5.437	ns
		GCLK PLL	t_{CO}	—	0.958	1.842	2.073	2.020	2.011	1.930	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.120	4.146	4.665	4.965	4.811	5.430	ns
		GCLK PLL	t_{CO}	—	0.955	1.836	2.066	2.013	2.004	1.923	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.119	4.144	4.662	4.962	4.808	5.427	ns
		GCLK PLL	t_{CO}	—	0.954	1.834	2.063	2.010	2.001	1.920	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.120	4.146	4.665	4.965	4.811	5.430	ns
		GCLK PLL	t_{CO}	—	0.955	1.836	2.066	2.013	2.004	1.923	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.115	4.136	4.653	4.953	4.799	5.418	ns
		GCLK PLL	t_{CO}	—	0.950	1.826	2.054	2.001	1.992	1.911	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.112	4.131	4.647	4.947	4.793	5.412	ns
		GCLK PLL	t_{CO}	—	0.947	1.821	2.048	1.995	1.986	1.905	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.118	4.143	4.661	4.961	4.807	5.426	ns
		GCLK PLL	t_{CO}	—	0.953	1.833	2.062	2.009	2.000	1.919	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.106	4.118	4.632	4.931	4.777	5.397	ns
		GCLK PLL	t_{CO}	—	0.941	1.808	2.033	1.979	1.970	1.890	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.113	4.133	4.649	4.949	4.795	5.414	ns
		GCLK PLL	t_{CO}	—	0.948	1.823	2.050	1.997	1.988	1.907	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.108	4.123	4.638	4.937	4.783	5.403	ns
		GCLK PLL	t_{CO}	—	0.943	1.813	2.039	1.985	1.976	1.896	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.112	4.130	4.646	4.946	4.792	5.411	ns
		GCLK PLL	t_{CO}	—	0.947	1.820	2.047	1.994	1.985	1.904	ns

Table 1–64. EP3SL200 Column Pins Output Timing Parameters (Part 3 of 4) (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.110	4.127	4.642	4.942	4.788	5.407	ns
		GCLK PLL	t_{CO}	—	0.945	1.817	2.043	1.990	1.981	1.900	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.109	4.125	4.640	4.940	4.786	5.405	ns
		GCLK PLL	t_{CO}	—	0.944	1.815	2.041	1.988	1.979	1.898	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.102	4.110	4.622	4.922	4.768	5.387	ns
		GCLK PLL	t_{CO}	—	0.937	1.800	2.023	1.970	1.961	1.880	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.128	4.163	4.685	4.985	4.831	5.450	ns
		GCLK PLL	t_{CO}	—	0.963	1.853	2.086	2.033	2.024	1.943	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.123	4.153	4.673	4.973	4.819	5.438	ns
		GCLK PLL	t_{CO}	—	0.958	1.843	2.074	2.021	2.012	1.931	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.120	4.147	4.666	4.966	4.812	5.431	ns
		GCLK PLL	t_{CO}	—	0.955	1.837	2.067	2.014	2.005	1.924	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.123	4.153	4.673	4.973	4.819	5.438	ns
		GCLK PLL	t_{CO}	—	0.958	1.843	2.074	2.021	2.012	1.931	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.121	4.149	4.668	4.968	4.814	5.433	ns
		GCLK PLL	t_{CO}	—	0.956	1.839	2.069	2.016	2.007	1.926	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.113	4.132	4.648	4.948	4.794	5.413	ns
		GCLK PLL	t_{CO}	—	0.948	1.822	2.049	1.996	1.987	1.906	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.115	4.137	4.654	4.954	4.800	5.419	ns
		GCLK PLL	t_{CO}	—	0.950	1.827	2.055	2.002	1.993	1.912	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.126	4.158	4.679	4.979	4.825	5.444	ns
		GCLK PLL	t_{CO}	—	0.961	1.848	2.080	2.027	2.018	1.937	ns

Table 1–64. EP3SL200 Column Pins Output Timing Parameters (Part 4 of 4) (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.119	4.144	4.662	4.962	4.808	5.427	ns
		GCLK PLL	t_{CO}	—	0.954	1.834	2.063	2.010	2.001	1.920	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.121	4.148	4.667	4.967	4.813	5.432	ns
		GCLK PLL	t_{CO}	—	0.956	1.838	2.068	2.015	2.006	1.925	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.119	4.145	4.664	4.963	4.810	5.429	ns
		GCLK PLL	t_{CO}	—	0.954	1.835	2.065	2.011	2.003	1.922	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.116	4.138	4.655	4.955	4.801	5.420	ns
		GCLK PLL	t_{CO}	—	0.951	1.828	2.056	2.003	1.994	1.913	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.110	4.127	4.642	4.942	4.788	5.407	ns
		GCLK PLL	t_{CO}	—	0.945	1.817	2.043	1.990	1.981	1.900	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.113	4.133	4.649	4.949	4.795	5.414	ns
		GCLK PLL	t_{CO}	—	0.948	1.823	2.050	1.997	1.988	1.907	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.117	4.140	4.658	4.958	4.804	5.423	ns
		GCLK PLL	t_{CO}	—	0.952	1.830	2.059	2.006	1.997	1.916	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.116	4.138	4.655	4.955	4.801	5.420	ns
		GCLK PLL	t_{CO}	—	0.951	1.828	2.056	2.003	1.994	1.913	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.114	4.134	4.651	4.950	4.796	5.416	ns
		GCLK PLL	t_{CO}	—	0.949	1.824	2.052	1.998	1.989	1.909	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.112	4.131	4.647	4.947	4.793	5.412	ns
		GCLK PLL	t_{CO}	—	0.947	1.821	2.048	1.995	1.986	1.905	ns

Table 1–65 specifies EP3SL200 Row Pins Output Timing parameters for differential I/O standards.

Table 1–65. EP3SL200 Row Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	t_{CO}	—	2.188	4.283	4.830	5.130	4.976	5.584	ns
		GCLK PLL	t_{CO}	—	1.024	1.975	2.232	2.180	2.170	2.082	ns
LVDS_E_1R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
		GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
		GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
MINI-LVDS	-	GCLK	t_{CO}	—	2.188	4.283	4.830	5.130	4.976	5.584	ns
		GCLK PLL	t_{CO}	—	1.024	1.975	2.232	2.180	2.170	2.082	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
		GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
		GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
RSDS	-	GCLK	t_{CO}	—	2.188	4.283	4.830	5.130	4.976	5.584	ns
		GCLK PLL	t_{CO}	—	1.024	1.975	2.232	2.180	2.170	2.082	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
		GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.187	4.281	4.828	5.127	4.973	5.582	ns
	-	GCLK PLL	t_{CO}	—	1.023	1.973	2.230	2.177	2.167	2.080	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.123	4.152	4.673	4.971	4.819	5.427	ns
		GCLK PLL	t_{CO}	—	0.960	1.846	2.079	2.025	2.017	1.929	ns

Table 1–65. EP3SL200 Row Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.115	4.135	4.654	4.952	4.799	5.408	ns
		GCLK PLL	t_{CO}	—	0.952	1.829	2.060	2.006	1.997	1.910	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.114	4.132	4.651	4.948	4.796	5.405	ns
		GCLK PLL	t_{CO}	—	0.951	1.826	2.057	2.002	1.994	1.907	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.113	4.130	4.648	4.946	4.794	5.402	ns
		GCLK PLL	t_{CO}	—	0.950	1.824	2.054	2.000	1.992	1.904	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.112	4.128	4.646	4.943	4.791	5.400	ns
		GCLK PLL	t_{CO}	—	0.949	1.822	2.052	1.997	1.989	1.902	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.107	4.118	4.634	4.931	4.779	5.388	ns
		GCLK PLL	t_{CO}	—	0.944	1.812	2.040	1.985	1.977	1.890	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.107	4.118	4.634	4.931	4.779	5.388	ns
		GCLK PLL	t_{CO}	—	0.944	1.812	2.040	1.985	1.977	1.890	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.101	4.107	4.621	4.918	4.766	5.375	ns
		GCLK PLL	t_{CO}	—	0.938	1.801	2.027	1.972	1.964	1.877	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.103	4.110	4.625	4.922	4.770	5.379	ns
		GCLK PLL	t_{CO}	—	0.940	1.804	2.031	1.976	1.968	1.881	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.102	4.109	4.624	4.920	4.769	5.378	ns
		GCLK PLL	t_{CO}	—	0.939	1.803	2.030	1.974	1.967	1.880	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.100	4.105	4.619	4.916	4.764	5.373	ns
		GCLK PLL	t_{CO}	—	0.937	1.799	2.025	1.970	1.962	1.875	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.091	4.087	4.598	4.894	4.742	5.352	ns
		GCLK PLL	t_{CO}	—	0.928	1.781	2.004	1.948	1.940	1.854	ns

Table 1–65. EP3SL200 Row Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.123	4.151	4.672	4.970	4.817	5.426	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.078	2.024	2.015	1.928	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.116	4.136	4.656	4.953	4.801	5.410	ns
		GCLK PLL	t_{CO}	—	0.953	1.830	2.062	2.007	1.999	1.912	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.112	4.128	4.646	4.943	4.791	5.400	ns
		GCLK PLL	t_{CO}	—	0.949	1.822	2.052	1.997	1.989	1.902	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.119	4.143	4.663	4.960	4.808	5.417	ns
		GCLK PLL	t_{CO}	—	0.956	1.837	2.069	2.014	2.006	1.919	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.112	4.129	4.647	4.944	4.792	5.401	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.053	1.998	1.990	1.903	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.112	4.129	4.647	4.944	4.792	5.401	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.053	1.998	1.990	1.903	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.111	4.127	4.645	4.942	4.790	5.399	ns
		GCLK PLL	t_{CO}	—	0.948	1.821	2.051	1.996	1.988	1.901	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.107	4.119	4.635	4.932	4.780	5.389	ns
		GCLK PLL	t_{CO}	—	0.944	1.813	2.041	1.986	1.978	1.891	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.102	4.109	4.624	4.920	4.769	5.378	ns
		GCLK PLL	t_{CO}	—	0.939	1.803	2.030	1.974	1.967	1.880	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.103	4.111	4.626	4.923	4.771	5.380	ns
		GCLK PLL	t_{CO}	—	0.940	1.805	2.032	1.977	1.969	1.882	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.111	4.126	4.644	4.941	4.789	5.398	ns
		GCLK PLL	t_{CO}	—	0.948	1.820	2.050	1.995	1.987	1.900	ns

Table 1–65. EP3SL200 Row Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.107	4.118	4.634	4.931	4.779	5.388	ns
		GCLK PLL	t_{CO}	—	0.944	1.812	2.040	1.985	1.977	1.890	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.103	4.111	4.626	4.923	4.771	5.380	ns
		GCLK PLL	t_{CO}	—	0.940	1.805	2.032	1.977	1.969	1.882	ns

Table 1–66 through Table 1–67 show EP3SL200 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–66 specifies EP3SL200 Column Pin delay adders when using the Regional Clock.

Table 1–66. EP3SL200 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.164	0.33	0.356	0.383	0.369	0.505	ns
RCLK PLL input adder	—	0.019	0.037	0.018	-0.015	0.004	0.009	ns
RCLK output adder	—	-0.16	-0.324	-0.352	-0.38	-0.365	-0.5	ns
RCLK PLL output adder	—	0.511	1.091	1.337	1.347	1.216	1.736	ns

Table 1–67 specifies EP3SL200 Row Pin delay adders when using the Regional Clock.

Table 1–67. EP3SL200 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.163	0.329	0.355	0.381	0.369	0.503	ns
RCLK PLL input adder	—	0.011	0.022	0.001	-0.031	-0.013	-0.014	ns
RCLK output adder	—	-0.163	-0.329	-0.355	-0.381	-0.369	-0.503	ns
RCLK PLL output adder	—	-0.011	-0.022	-0.001	0.031	0.013	0.014	ns

EP3SL340 I/O Timing Parameters

Table 1–68 through Table 1–71 show the maximum I/O timing parameters for EP3SL340 devices for single ended I/O standards.

Table 1–68 specifies EP3SL340 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–68. EP3SL340 Column Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}=0. 9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.899	-1.836	-1.966	-2.100	-2.029	-2.902	ns
		t_H	—	0.968	1.974	2.126	2.286	2.203	3.062	ns
	GCLK PLL	t_{SU}	—	0.421	0.793	1.005	1.283	1.176	1.141	ns
		t_H	—	-0.352	-0.655	-0.845	-1.097	-1.002	-0.981	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.899	-1.836	-1.966	-2.100	-2.029	-2.902	ns
		t_H	—	0.968	1.974	2.126	2.286	2.203	3.062	ns
	GCLK PLL	t_{SU}	—	0.421	0.793	1.005	1.283	1.176	1.141	ns
		t_H	—	-0.352	-0.655	-0.845	-1.097	-1.002	-0.981	ns

Table 1–68. EP3SL340 Column Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}=0.9V	
2.5 V	GCLK	t_{SU}	—	-0.904	-1.847	-1.978	-2.112	-2.041	-2.914	ns
		t_H	—	0.973	1.984	2.138	2.298	2.215	3.074	ns
	GCLK PLL	t_{SU}	—	0.416	0.782	0.993	1.271	1.164	1.129	ns
		t_H	—	-0.347	-0.645	-0.833	-1.085	-0.990	-0.969	ns
1.8 V	GCLK	t_{SU}	—	-0.914	-1.867	-2.002	-2.136	-2.065	-2.938	ns
		t_H	—	0.983	2.004	2.161	2.322	2.238	3.097	ns
	GCLK PLL	t_{SU}	—	0.406	0.762	0.969	1.247	1.140	1.105	ns
		t_H	—	-0.337	-0.625	-0.810	-1.061	-0.967	-0.946	ns
1.5 V	GCLK	t_{SU}	—	-0.894	-1.826	-1.955	-2.088	-2.017	-2.891	ns
		t_H	—	0.963	1.964	2.115	2.274	2.191	3.051	ns
	GCLK PLL	t_{SU}	—	0.426	0.803	1.016	1.295	1.188	1.152	ns
		t_H	—	-0.357	-0.665	-0.856	-1.109	-1.014	-0.992	ns
1.2 V	GCLK	t_{SU}	—	-0.837	-1.712	-1.821	-1.953	-1.882	-2.757	ns
		t_H	—	0.907	1.850	1.982	2.140	2.058	2.918	ns
	GCLK PLL	t_{SU}	—	0.483	0.917	1.150	1.430	1.323	1.286	ns
		t_H	—	-0.413	-0.779	-0.989	-1.243	-1.147	-1.125	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.777	-1.589	-1.678	-1.808	-1.738	-2.614	ns
		t_H	—	0.847	1.729	1.841	1.997	1.915	2.777	ns
	GCLK PLL	t_{SU}	—	0.543	1.040	1.293	1.575	1.467	1.429	ns
		t_H	—	-0.473	-0.900	-1.130	-1.386	-1.290	-1.266	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.777	-1.589	-1.678	-1.808	-1.738	-2.614	ns
		t_H	—	0.847	1.729	1.841	1.997	1.915	2.777	ns
	GCLK PLL	t_{SU}	—	0.543	1.040	1.293	1.575	1.467	1.429	ns
		t_H	—	-0.473	-0.900	-1.130	-1.386	-1.290	-1.266	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.753	-1.538	-1.618	-1.749	-1.679	-2.554	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	2.722	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	1.489	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.753	-1.538	-1.618	-1.749	-1.679	-1.321	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	-2.554	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	2.722	ns

Table 1–68. EP3SL340 Column Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}=0.9V	
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.739	-1.511	-1.586	-1.716	-1.646	2.722	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	1.489	ns
		t_{H}	—	-0.509	-0.975	-1.217	-1.473	-1.378	-1.321	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.739	-1.511	-1.586	-1.716	-1.646	-2.522	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	2.690	ns
		t_{H}	—	-0.509	-0.975	-1.217	-1.473	-1.378	1.521	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.753	-1.538	-1.618	-1.749	-1.679	1.521	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	-1.353	ns
		t_{H}	—	-0.496	-0.948	-1.185	-1.441	-1.346	-2.522	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.753	-1.538	-1.618	-1.749	-1.679	2.722	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	1.489	ns
		t_{H}	—	-0.496	-0.948	-1.185	-1.441	-1.346	-1.321	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.739	-1.511	-1.586	-1.716	-1.646	-2.554	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	2.722	ns
		t_{H}	—	-0.509	-0.975	-1.217	-1.473	-1.378	1.489	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.739	-1.511	-1.586	-1.716	-1.646	-1.321	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	-2.554	ns
		t_{H}	—	-0.509	-0.975	-1.217	-1.473	-1.378	2.722	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.732	-1.496	-1.570	-1.700	-1.630	1.489	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.401	1.683	1.575	-1.321	ns
		t_{H}	—	-0.516	-0.989	-1.233	-1.489	-1.394	-2.522	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.732	-1.496	-1.570	-1.700	-1.630	2.690	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.401	1.683	1.575	1.521	ns
		t_{H}	—	-0.516	-0.989	-1.233	-1.489	-1.394	-1.353	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.899	-1.836	-1.966	-2.100	-2.029	-2.522	ns
		t_{H}	—	0.968	1.974	2.126	2.286	2.203	2.690	ns
	GCLK PLL	t_{SU}	—	0.421	0.793	1.005	1.283	1.176	1.521	ns
		t_{H}	—	-0.352	-0.655	-0.845	-1.097	-1.002	-1.353	ns

Table 1–68. EP3SL340 Column Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}=0.9V	
3.0-V PCI-X	GCLK	t_{SU}	—	-0.899	-1.836	-1.966	-2.100	-2.029	-2.522	ns
		t_H	—	0.968	1.974	2.126	2.286	2.203	2.690	ns
	GCLK PLL	t_{SU}	—	0.421	0.793	1.005	1.283	1.176	1.521	ns
		t_H	—	-0.352	-0.655	-0.845	-1.097	-1.002	-1.353	ns

Table 1–69 specifies EP3SL340 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–69. EP3SL340 Row Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.833	-1.702	-1.813	-1.935	-1.873	-2.727	ns
		t_H	—	0.904	1.843	1.978	2.127	2.051	2.892	ns
	GCLK PLL	t_{SU}	—	0.503	0.953	1.188	1.467	1.368	1.334	ns
		t_H	—	-0.432	-0.812	-1.023	-1.275	-1.190	-1.169	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.833	-1.702	-1.813	-1.935	-1.873	-2.727	ns
		t_H	—	0.904	1.843	1.978	2.127	2.051	2.892	ns
	GCLK PLL	t_{SU}	—	0.503	0.953	1.188	1.467	1.368	1.334	ns
		t_H	—	-0.432	-0.812	-1.023	-1.275	-1.190	-1.169	ns
2.5 V	GCLK	t_{SU}	—	-0.838	-1.712	-1.824	-1.947	-1.885	-2.738	ns
		t_H	—	0.909	1.853	1.990	2.139	2.063	2.904	ns
	GCLK PLL	t_{SU}	—	0.498	0.943	1.177	1.455	1.356	1.323	ns
		t_H	—	-0.427	-0.802	-1.011	-1.263	-1.178	-1.157	ns
1.8 V	GCLK	t_{SU}	—	-0.848	-1.732	-1.848	-1.971	-1.908	-2.762	ns
		t_H	—	0.919	1.873	2.013	2.163	2.086	2.927	ns
	GCLK PLL	t_{SU}	—	0.488	0.923	1.153	1.431	1.333	1.299	ns
		t_H	—	-0.417	-0.782	-0.988	-1.239	-1.155	-1.134	ns

Table 1–69. EP3SL340 Row Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	GCLK	t_{SU}	—	-0.827	-1.691	-1.800	-1.922	-1.860	-2.714	ns
		t_H	—	0.898	1.832	1.965	2.114	2.038	2.879	ns
	GCLK PLL	t_{SU}	—	0.509	0.964	1.201	1.480	1.381	1.347	ns
		t_H	—	-0.438	-0.823	-1.036	-1.288	-1.203	-1.182	ns
1.2 V	GCLK	t_{SU}	—	-0.770	-1.574	-1.664	-1.784	-1.723	-2.578	ns
		t_H	—	0.841	1.716	1.830	1.978	1.903	2.744	ns
	GCLK PLL	t_{SU}	—	0.566	1.081	1.337	1.618	1.518	1.483	ns
		t_H	—	-0.495	-0.939	-1.171	-1.424	-1.338	-1.317	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.707	-1.446	-1.515	-1.633	-1.573	-2.429	ns
		t_H	—	0.779	1.589	1.683	1.829	1.754	2.597	ns
	GCLK PLL	t_{SU}	—	0.629	1.209	1.486	1.769	1.668	1.632	ns
		t_H	—	-0.557	-1.066	-1.318	-1.573	-1.487	-1.464	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.707	-1.446	-1.515	-1.633	-1.573	-2.429	ns
		t_H	—	0.779	1.589	1.683	1.829	1.754	2.597	ns
	GCLK PLL	t_{SU}	—	0.629	1.209	1.486	1.769	1.668	1.632	ns
		t_H	—	-0.557	-1.066	-1.318	-1.573	-1.487	-1.464	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.662	-1.351	-1.405	-1.522	-1.463	-2.319	ns
		t_H	—	0.735	1.499	1.576	1.723	1.649	2.490	ns
	GCLK PLL	t_{SU}	—	0.674	1.304	1.596	1.880	1.778	1.742	ns
		t_H	—	-0.601	-1.156	-1.425	-1.679	-1.592	-1.571	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.662	-1.351	-1.405	-1.522	-1.463	-2.319	ns
		t_H	—	0.735	1.499	1.576	1.723	1.649	2.490	ns
	GCLK PLL	t_{SU}	—	0.674	1.304	1.596	1.880	1.778	1.742	ns
		t_H		-0.601	-1.156	-1.425	-1.679	-1.592	-1.571	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.648	-1.323	-1.373	-1.490	-1.430	-2.287	ns
		t_H	—	0.721	1.472	1.545	1.691	1.617	2.459	ns
	GCLK PLL	t_{SU}	—	0.688	1.332	1.628	1.912	1.811	1.774	ns
		t_H	—	-0.615	-1.183	-1.456	-1.711	-1.624	-1.602	ns

Table 1–69. EP3SL340 Row Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.648	-1.323	-1.373	-1.490	-1.430	-2.287	ns
		t_H	—	0.721	1.472	1.545	1.691	1.617	2.459	ns
	GCLK PLL	t_{SU}	—	0.688	1.332	1.628	1.912	1.811	1.774	ns
		t_H	—	-0.615	-1.183	-1.456	-1.711	-1.624	-1.602	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.662	-1.351	-1.405	-1.522	-1.463	-2.319	ns
		t_H	—	0.735	1.499	1.576	1.723	1.649	2.490	ns
	GCLK PLL	t_{SU}	—	0.674	1.304	1.596	1.880	1.778	1.742	ns
		t_H	—	-0.601	-1.156	-1.425	-1.679	-1.592	-1.571	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.662	-1.351	-1.405	-1.522	-1.463	-2.319	ns
		t_H	—	0.735	1.499	1.576	1.723	1.649	2.490	ns
	GCLK PLL	t_{SU}	—	0.674	1.304	1.596	1.880	1.778	1.742	ns
		t_H	—	-0.601	-1.156	-1.425	-1.679	-1.592	-1.571	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.648	-1.323	-1.373	-1.490	-1.430	-2.287	ns
		t_H	—	0.721	1.472	1.545	1.691	1.617	2.459	ns
	GCLK PLL	t_{SU}	—	0.688	1.332	1.628	1.912	1.811	1.774	ns
		t_H	—	-0.615	-1.183	-1.456	-1.711	-1.624	-1.602	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.648	-1.323	-1.373	-1.490	-1.430	-2.287	ns
		t_H	—	0.721	1.472	1.545	1.691	1.617	2.459	ns
	GCLK PLL	t_{SU}	—	0.688	1.332	1.628	1.912	1.811	1.774	ns
		t_H	—	-0.615	-1.183	-1.456	-1.711	-1.624	-1.602	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.641	-1.309	-1.357	-1.473	-1.414	-2.271	ns
		t_H	—	0.714	1.458	1.528	1.674	1.601	2.442	ns
	GCLK PLL	t_{SU}	—	0.695	1.346	1.644	1.929	1.827	1.790	ns
		t_H	—	-0.622	-1.197	-1.473	-1.728	-1.640	-1.619	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.641	-1.309	-1.357	-1.473	-1.414	-2.271	ns
		t_H	—	0.714	1.458	1.528	1.674	1.601	2.442	ns
	GCLK PLL	t_{SU}	—	0.695	1.346	1.644	1.929	1.827	1.790	ns
		t_H	—	-0.622	-1.197	-1.473	-1.728	-1.640	-1.619	ns

Table 1–69. EP3SL340 Row Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI	GCLK	t_{SU}	—	-0.833	-1.702	-1.813	-1.935	-1.873	-2.727	ns
		t_H	—	0.904	1.843	1.978	2.127	2.051	2.892	ns
	GCLK PLL	t_{SU}	—	0.503	0.953	1.188	1.467	1.368	1.334	ns
		t_H	—	-0.432	-0.812	-1.023	-1.275	-1.190	-1.169	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.833	-1.702	-1.813	-1.935	-1.873	-2.727	ns
		t_H	—	0.904	1.843	1.978	2.127	2.051	2.892	ns
	GCLK PLL	t_{SU}	—	0.503	0.953	1.188	1.467	1.368	1.334	ns
		t_H	—	-0.432	-0.812	-1.023	-1.275	-1.190	-1.169	ns

Table 1–70 specifies EP3SL340 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.812	4.890	5.457	5.770	5.411	6.197	ns
		GCLK PLL	t_{CO}	—	1.492	2.263	2.488	2.359	2.209	2.120	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.960	5.026	5.656	5.969	5.551	6.338	ns
		GCLK PLL	t_{CO}	—	1.640	2.399	2.687	2.558	2.349	2.270	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	3.020	5.105	5.711	6.024	5.638	6.424	ns
		GCLK PLL	t_{CO}	—	1.700	2.478	2.742	2.613	2.436	2.347	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	3.135	5.269	5.896	6.209	5.803	6.590	ns
		GCLK PLL	t_{CO}	—	1.815	2.642	2.927	2.798	2.601	2.515	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.960	5.026	5.655	5.968	5.551	6.338	ns
		GCLK PLL	t_{CO}	—	1.640	2.399	2.686	2.557	2.349	2.270	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	3.135	5.269	5.895	6.208	5.803	6.590	ns
		GCLK PLL	t_{CO}	—	1.815	2.642	2.926	2.797	2.601	2.515	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	3.190	5.345	5.960	6.273	5.882	6.668	ns
		GCLK PLL	t_{CO}	—	1.870	2.718	2.991	2.862	2.680	2.591	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	3.243	5.406	6.016	6.329	5.944	6.730	ns
		GCLK PLL	t_{CO}	—	1.923	2.779	3.047	2.918	2.742	2.658	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.898	5.051	5.725	6.038	5.580	6.366	ns
		GCLK PLL	t_{CO}	—	1.578	2.424	2.756	2.627	2.378	2.289	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.937	5.075	5.700	6.013	5.602	6.389	ns
		GCLK PLL	t_{CO}	—	1.617	2.448	2.731	2.602	2.400	2.312	ns
2.5 V	12mA	GCLK	t_{CO}	—	3.185	5.420	6.100	6.413	5.957	6.744	ns
		GCLK PLL	t_{CO}	—	1.865	2.793	3.131	3.002	2.755	2.667	ns
2.5 V	16mA	GCLK	t_{CO}	—	3.218	5.479	6.197	6.510	6.019	6.806	ns
		GCLK PLL	t_{CO}	—	1.898	2.852	3.228	3.099	2.817	2.733	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.800	4.922	5.540	5.853	5.447	6.234	ns
		GCLK PLL	t_{CO}	—	1.480	2.295	2.571	2.442	2.245	2.157	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.862	5.039	5.769	6.082	5.566	6.352	ns
		GCLK PLL	t_{CO}	—	1.542	2.412	2.800	2.671	2.364	2.275	ns
1.8 V	6mA	GCLK	t_{CO}	—	3.105	5.337	6.059	6.372	5.870	6.657	ns
		GCLK PLL	t_{CO}	—	1.785	2.710	3.090	2.961	2.668	2.580	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.932	5.084	5.741	6.054	5.610	6.397	ns
		GCLK PLL	t_{CO}	—	1.612	2.457	2.772	2.643	2.408	2.320	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	10mA	GCLK	t_{CO}	—	3.194	5.446	6.152	6.465	5.982	6.769	ns
		GCLK PLL	t_{CO}	—	1.874	2.819	3.183	3.054	2.780	2.697	ns
1.8 V	12mA	GCLK	t_{CO}	—	3.265	5.592	6.372	6.685	6.134	6.921	ns
		GCLK PLL	t_{CO}	—	1.945	2.965	3.403	3.274	2.932	2.844	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.752	4.784	5.441	5.754	5.307	6.093	ns
		GCLK PLL	t_{CO}	—	1.432	2.157	2.472	2.343	2.105	2.036	ns
1.5 V	4mA	GCLK	t_{CO}	—	3.020	5.244	5.918	6.231	5.781	6.567	ns
		GCLK PLL	t_{CO}	—	1.700	2.617	2.949	2.820	2.579	2.490	ns
1.5 V	6mA	GCLK	t_{CO}	—	3.118	5.350	6.048	6.361	5.885	6.672	ns
		GCLK PLL	t_{CO}	—	1.798	2.723	3.079	2.950	2.683	2.595	ns
1.5 V	8mA	GCLK	t_{CO}	—	3.043	5.206	5.891	6.204	5.739	6.526	ns
		GCLK PLL	t_{CO}	—	1.723	2.579	2.922	2.793	2.537	2.449	ns
1.5 V	10mA	GCLK	t_{CO}	—	3.209	5.493	6.246	6.559	6.029	6.816	ns
		GCLK PLL	t_{CO}	—	1.889	2.866	3.277	3.148	2.827	2.743	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.383	5.835	6.734	7.047	6.376	7.163	ns
		GCLK PLL	t_{CO}	—	2.063	3.208	3.765	3.636	3.174	3.086	ns
1.2 V	2mA	GCLK	t_{CO}	—	3.028	5.304	6.146	6.459	5.817	6.604	ns
		GCLK PLL	t_{CO}	—	1.708	2.677	3.177	3.048	2.615	2.527	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.194	5.523	6.328	6.641	6.059	6.846	ns
		GCLK PLL	t_{CO}	—	1.874	2.896	3.359	3.230	2.857	2.769	ns
1.2 V	6mA	GCLK	t_{CO}	—	3.130	5.393	6.161	6.474	5.925	6.712	ns
		GCLK PLL	t_{CO}	—	1.810	2.766	3.192	3.063	2.723	2.635	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2 V	8mA	GCLK	t_{CO}	—	3.384	5.795	6.668	6.981	6.333	7.120	ns
		GCLK PLL	t_{CO}	—	2.064	3.168	3.699	3.570	3.131	3.043	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.510	4.422	4.937	5.250	4.931	5.718	ns
		GCLK PLL	t_{CO}	—	1.190	1.795	1.968	1.841	1.729	1.648	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.507	4.419	4.933	5.246	4.928	5.715	ns
		GCLK PLL	t_{CO}	—	1.187	1.792	1.964	1.836	1.726	1.643	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.510	4.427	4.942	5.255	4.936	5.723	ns
		GCLK PLL	t_{CO}	—	1.190	1.800	1.973	1.844	1.734	1.646	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.522	4.429	4.942	5.255	4.937	5.724	ns
		GCLK PLL	t_{CO}	—	1.202	1.802	1.973	1.844	1.735	1.647	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.517	4.436	4.954	5.267	4.945	5.732	ns
		GCLK PLL	t_{CO}	—	1.197	1.809	1.985	1.856	1.743	1.655	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.510	4.428	4.945	5.258	4.936	5.723	ns
		GCLK PLL	t_{CO}	—	1.190	1.801	1.976	1.847	1.734	1.646	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.514	4.437	4.957	5.270	4.946	5.733	ns
		GCLK PLL	t_{CO}	—	1.194	1.810	1.988	1.859	1.744	1.659	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.513	4.439	4.959	5.272	4.949	5.736	ns
		GCLK PLL	t_{CO}	—	1.193	1.812	1.990	1.861	1.747	1.659	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.511	4.437	4.957	5.270	4.947	5.734	ns
		GCLK PLL	t_{CO}	—	1.191	1.810	1.988	1.859	1.745	1.657	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.516	4.427	4.941	5.254	4.935	5.722	ns
		GCLK PLL	t_{CO}	—	1.196	1.800	1.972	1.843	1.733	1.645	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.532	4.462	4.982	5.295	4.972	5.759	ns
		GCLK PLL	t_{CO}	—	1.212	1.835	2.013	1.884	1.770	1.682	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.516	4.438	4.958	5.271	4.946	5.733	ns
		GCLK PLL	t_{CO}	—	1.196	1.811	1.989	1.860	1.744	1.656	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.515	4.439	4.960	5.273	4.948	5.735	ns
		GCLK PLL	t_{CO}	—	1.195	1.812	1.991	1.862	1.746	1.658	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.514	4.443	4.964	5.277	4.952	5.739	ns
		GCLK PLL	t_{CO}	—	1.194	1.816	1.995	1.866	1.750	1.662	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.522	4.457	4.980	5.293	4.967	5.754	ns
		GCLK PLL	t_{CO}	—	1.202	1.830	2.011	1.882	1.765	1.677	ns
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.517	4.451	4.973	5.286	4.960	5.747	ns
		GCLK PLL	t_{CO}	—	1.197	1.824	2.004	1.875	1.758	1.670	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.518	4.434	4.951	5.264	4.943	5.730	ns
		GCLK PLL	t_{CO}	—	1.198	1.807	1.982	1.853	1.741	1.653	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.532	4.466	4.989	5.302	4.977	5.764	ns
		GCLK PLL	t_{CO}	—	1.212	1.839	2.020	1.891	1.775	1.687	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.513	4.418	4.932	5.245	4.926	5.713	ns
		GCLK PLL	t_{CO}	—	1.193	1.791	1.963	1.834	1.724	1.636	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.514	4.421	4.936	5.249	4.929	5.716	ns
		GCLK PLL	t_{CO}	—	1.194	1.794	1.967	1.843	1.727	1.646	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.516	4.429	4.944	5.257	4.937	5.724	ns
		GCLK PLL	t_{CO}	—	1.196	1.802	1.975	1.846	1.735	1.647	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.520	4.436	4.952	5.265	4.945	5.732	ns
		GCLK PLL	t_{CO}	—	1.200	1.809	1.983	1.854	1.743	1.655	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.522	4.439	4.955	5.268	4.948	5.735	ns
		GCLK PLL	t_{CO}	—	1.202	1.812	1.986	1.857	1.746	1.658	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.573	4.473	4.985	5.298	4.981	5.768	ns
		GCLK PLL	t_{CO}	—	1.253	1.846	2.016	1.887	1.779	1.691	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.519	4.427	4.943	5.256	4.935	5.722	ns
		GCLK PLL	t_{CO}	—	1.199	1.800	1.974	1.845	1.733	1.645	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.519	4.430	4.948	5.261	4.938	5.725	ns
		GCLK PLL	t_{CO}	—	1.199	1.803	1.979	1.854	1.736	1.655	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.516	4.425	4.941	5.254	4.933	5.720	ns
		GCLK PLL	t_{CO}	—	1.196	1.798	1.972	1.843	1.731	1.645	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.518	4.434	4.951	5.264	4.943	5.730	ns
		GCLK PLL	t_{CO}	—	1.198	1.807	1.982	1.853	1.741	1.653	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.527	4.448	4.967	5.280	4.957	5.744	ns
		GCLK PLL	t_{CO}	—	1.207	1.821	1.998	1.869	1.755	1.667	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.551	4.433	4.942	5.255	4.939	5.726	ns
		GCLK PLL	t_{CO}	—	1.231	1.806	1.973	1.844	1.737	1.649	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.530	4.446	4.967	5.280	4.955	5.742	ns
		GCLK PLL	t_{CO}	—	1.210	1.819	1.998	1.869	1.753	1.665	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.524	4.441	4.961	5.274	4.949	5.736	ns
		GCLK PLL	t_{CO}	—	1.204	1.814	1.992	1.863	1.747	1.659	ns

Table 1–70. EP3SL340 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.534	4.459	4.982	5.295	4.968	5.755	ns
		GCLK PLL	t_{CO}	—	1.214	1.832	2.013	1.884	1.766	1.678	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.530	4.459	4.982	5.295	4.969	5.756	ns
		GCLK PLL	t_{CO}	—	1.210	1.832	2.013	1.884	1.767	1.679	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.530	4.458	4.980	5.293	4.967	5.754	ns
		GCLK PLL	t_{CO}	—	1.210	1.831	2.011	1.882	1.765	1.677	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.583	4.492	5.009	5.322	5.000	5.787	ns
		GCLK PLL	t_{CO}	—	1.263	1.865	2.040	1.911	1.798	1.710	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.508	5.766	6.478	6.791	6.313	7.099	ns
		GCLK PLL	t_{CO}	—	2.188	3.139	3.509	3.380	3.111	3.024	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.508	5.766	6.478	6.791	6.313	7.099	ns
		GCLK PLL	t_{CO}	—	2.188	3.139	3.509	3.380	3.111	3.024	ns

Table 1–71 specifies EP3SL340 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–71. EP3SL340 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.890	4.976	5.573	5.882	5.499	6.269	ns
		GCLK PLL	t_{CO}	—	1.554	2.321	2.572	2.480	2.258	2.202	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.954	5.034	5.663	5.972	5.552	6.323	ns
		GCLK PLL	t_{CO}	—	1.618	2.379	2.662	2.570	2.311	2.256	ns

Table 1–71. EP3SL340 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	3.085	5.191	5.809	6.118	5.714	6.484	ns
		GCLK PLL	t_{CO}	—	1.749	2.536	2.808	2.716	2.473	2.417	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.983	5.058	5.673	5.982	5.585	6.355	ns
		GCLK PLL	t_{CO}	—	1.647	2.403	2.672	2.580	2.344	2.288	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	3.125	5.241	5.878	6.187	5.770	6.541	ns
		GCLK PLL	t_{CO}	—	1.789	2.586	2.877	2.785	2.529	2.474	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.987	5.198	5.887	6.196	5.730	6.500	ns
		GCLK PLL	t_{CO}	—	1.651	2.543	2.886	2.794	2.489	2.433	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.981	5.129	5.765	6.074	5.653	6.423	ns
		GCLK PLL	t_{CO}	—	1.645	2.474	2.764	2.672	2.412	2.356	ns
2.5 V	12mA	GCLK	t_{CO}	—	3.186	5.409	6.099	6.408	5.949	6.719	ns
		GCLK PLL	t_{CO}	—	1.850	2.754	3.098	3.006	2.708	2.652	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.991	5.107	5.720	6.029	5.637	6.407	ns
		GCLK PLL	t_{CO}	—	1.655	2.452	2.719	2.627	2.396	2.340	ns
1.8 V	4mA	GCLK	t_{CO}	—	3.022	5.242	5.984	6.293	5.766	6.537	ns
		GCLK PLL	t_{CO}	—	1.686	2.587	2.983	2.891	2.525	2.470	ns
1.8 V	6mA	GCLK	t_{CO}	—	3.114	5.387	6.151	6.460	5.922	6.693	ns
		GCLK PLL	t_{CO}	—	1.778	2.732	3.150	3.058	2.681	2.626	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.999	5.162	5.824	6.133	5.685	6.455	ns
		GCLK PLL	t_{CO}	—	1.663	2.507	2.823	2.731	2.444	2.388	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.904	5.022	5.655	5.964	5.546	6.316	ns
		GCLK PLL	t_{CO}	—	1.568	2.367	2.654	2.562	2.305	2.249	ns

Table 1–71. EP3SL340 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	4mA	GCLK	t_{CO}	—	3.029	5.265	5.964	6.273	5.798	6.568	ns
		GCLK PLL	t_{CO}	—	1.693	2.610	2.963	2.871	2.557	2.501	ns
1.5 V	6mA	GCLK	t_{CO}	—	3.164	5.417	6.174	6.483	5.953	6.724	ns
		GCLK PLL	t_{CO}	—	1.828	2.762	3.173	3.081	2.712	2.657	ns
1.5 V	8mA	GCLK	t_{CO}	—	3.051	5.243	5.949	6.258	5.773	6.544	ns
		GCLK PLL	t_{CO}	—	1.715	2.588	2.948	2.856	2.532	2.477	ns
1.2 V	2mA	GCLK	t_{CO}	—	3.154	5.627	6.585	6.894	6.138	6.909	ns
		GCLK PLL	t_{CO}	—	1.818	2.972	3.584	3.492	2.897	2.842	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.282	5.695	6.576	6.885	6.218	6.989	ns
		GCLK PLL	t_{CO}	—	1.946	3.040	3.575	3.483	2.977	2.922	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.479	4.379	4.894	5.203	4.885	5.656	ns
		GCLK PLL	t_{CO}	—	1.143	1.724	1.893	1.801	1.644	1.589	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.467	4.370	4.885	5.194	4.875	5.646	ns
		GCLK PLL	t_{CO}	—	1.131	1.715	1.884	1.792	1.634	1.579	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.472	4.371	4.885	5.194	4.876	5.647	ns
		GCLK PLL	t_{CO}	—	1.136	1.716	1.884	1.792	1.635	1.580	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.481	4.385	4.905	5.214	4.891	5.662	ns
		GCLK PLL	t_{CO}	—	1.145	1.730	1.904	1.812	1.650	1.595	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.469	4.373	4.892	5.201	4.878	5.649	ns
		GCLK PLL	t_{CO}	—	1.133	1.718	1.891	1.799	1.637	1.582	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.469	4.380	4.901	5.210	4.885	5.656	ns
		GCLK PLL	t_{CO}	—	1.133	1.725	1.900	1.808	1.644	1.589	ns

Table 1–71. EP3SL340 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.461	4.375	4.895	5.204	4.880	5.651	ns
		GCLK PLL	t_{CO}	—	1.125	1.720	1.894	1.802	1.639	1.584	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.459	4.372	4.893	5.202	4.878	5.649	ns
		GCLK PLL	t_{CO}	—	1.123	1.717	1.892	1.800	1.637	1.582	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.464	4.364	4.882	5.191	4.869	5.640	ns
		GCLK PLL	t_{CO}	—	1.128	1.709	1.881	1.789	1.628	1.573	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.466	4.378	4.898	5.207	4.883	5.654	ns
		GCLK PLL	t_{CO}	—	1.130	1.723	1.897	1.805	1.642	1.587	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.481	4.388	4.911	5.220	4.893	5.664	ns
		GCLK PLL	t_{CO}	—	1.145	1.733	1.910	1.818	1.652	1.597	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.470	4.383	4.907	5.216	4.888	5.659	ns
		GCLK PLL	t_{CO}	—	1.134	1.728	1.906	1.814	1.647	1.592	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.462	4.377	4.900	5.209	4.882	5.653	ns
		GCLK PLL	t_{CO}	—	1.126	1.722	1.899	1.807	1.641	1.586	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.476	4.366	4.881	5.190	4.870	5.641	ns
		GCLK PLL	t_{CO}	—	1.140	1.711	1.880	1.788	1.629	1.574	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.467	4.365	4.883	5.192	4.870	5.641	ns
		GCLK PLL	t_{CO}	—	1.131	1.710	1.882	1.790	1.629	1.574	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.461	4.364	4.881	5.190	4.868	5.639	ns
		GCLK PLL	t_{CO}	—	1.125	1.709	1.880	1.788	1.627	1.572	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.463	4.367	4.885	5.194	4.872	5.643	ns
		GCLK PLL	t_{CO}	—	1.127	1.712	1.884	1.792	1.631	1.576	ns

Table 1–71. EP3SL340 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.462	4.370	4.889	5.198	4.875	5.646	ns
		GCLK PLL	t_{CO}	—	1.126	1.715	1.888	1.796	1.634	1.579	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.471	4.368	4.882	5.191	4.872	5.643	ns
		GCLK PLL	t_{CO}	—	1.135	1.713	1.881	1.789	1.631	1.576	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.482	4.374	4.893	5.202	4.878	5.649	ns
		GCLK PLL	t_{CO}	—	1.146	1.719	1.892	1.800	1.637	1.582	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.476	4.377	4.898	5.207	4.882	5.653	ns
		GCLK PLL	t_{CO}	—	1.140	1.722	1.897	1.805	1.641	1.586	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.468	4.368	4.888	5.197	4.873	5.644	ns
		GCLK PLL	t_{CO}	—	1.132	1.713	1.887	1.795	1.632	1.577	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.485	4.390	4.917	5.226	4.895	5.666	ns
		GCLK PLL	t_{CO}	—	1.149	1.735	1.916	1.824	1.654	1.599	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.473	4.380	4.904	5.213	4.884	5.655	ns
		GCLK PLL	t_{CO}	—	1.137	1.725	1.903	1.811	1.643	1.588	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.476	4.392	4.918	5.227	4.897	5.668	ns
		GCLK PLL	t_{CO}	—	1.140	1.737	1.917	1.825	1.656	1.601	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.428	5.716	6.432	6.741	6.259	7.029	ns
		GCLK PLL	t_{CO}	—	2.092	3.061	3.431	3.339	3.018	2.962	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.428	5.716	6.432	6.741	6.259	7.029	ns
		GCLK PLL	t_{CO}	—	2.092	3.061	3.431	3.339	3.018	2.962	ns

Table 1–72 through Table 1–75 show the maximum I/O timing parameters for EP3SL340 devices for differential I/O standards.

Table 1–72 specifies EP3SL340 Column Pins Input Timing parameters for differential I/O standards.

Table 1–72. EP3SL340 Column Pins Input Timing Parameters (Part 1 of 2)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.744	-1.518	-1.594	-1.732	-1.661	-2.542	ns
		t_H	—	0.816	1.662	1.762	1.926	1.842	2.710	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.401	1.683	1.575	1.537	ns
		t_H	—	-0.516	-0.989	-1.233	-1.489	-1.394	-1.369	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.744	-1.518	-1.594	-1.732	-1.661	-2.542	ns
		t_H	—	0.816	1.662	1.762	1.926	1.842	2.710	ns
	GCLK PLL	t_{SU}	—	0.588	1.133	1.401	1.683	1.575	1.537	ns
		t_H	—	-0.516	-0.989	-1.233	-1.489	-1.394	-1.369	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.751	-1.533	-1.610	-1.748	-1.677	-2.558	ns
		t_H	—	0.823	1.676	1.778	1.942	1.858	2.726	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	1.521	ns
		t_H	—	-0.509	-0.975	-1.217	-1.473	-1.378	-1.353	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.751	-1.533	-1.610	-1.748	-1.677	-2.558	ns
		t_H	—	0.823	1.676	1.778	1.942	1.858	2.726	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	1.521	ns
		t_H	—	-0.509	-0.975	-1.217	-1.473	-1.378	-1.353	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.765	-1.560	-1.642	-1.781	-1.710	-2.590	ns
		t_H	—	0.836	1.703	1.810	1.974	1.890	2.758	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	1.489	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	-1.321	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.765	-1.560	-1.642	-1.781	-1.710	-2.590	ns
		t_H	—	0.836	1.703	1.810	1.974	1.890	2.758	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	1.489	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	-1.321	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.751	-1.533	-1.610	-1.748	-1.677	-2.558	ns
		t_H	—	0.823	1.676	1.778	1.942	1.858	2.726	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	1.521	ns
		t_H	—	-0.509	-0.975	-1.217	-1.473	-1.378	-1.353	ns

Table 1–72. EP3SL340 Column Pins Input Timing Parameters (Part 2 of 2)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.751	-1.533	-1.610	-1.748	-1.677	-2.558	ns
		t_H	—	0.823	1.676	1.778	1.942	1.858	2.726	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.385	1.667	1.559	1.521	ns
		t_H	—	-0.509	-0.975	-1.217	-1.473	-1.378	-1.353	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.765	-1.560	-1.642	-1.781	-1.710	-2.590	ns
		t_H	—	0.836	1.703	1.810	1.974	1.890	2.758	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	1.489	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	-1.321	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.765	-1.560	-1.642	-1.781	-1.710	-2.590	ns
		t_H	—	0.836	1.703	1.810	1.974	1.890	2.758	ns
	GCLK PLL	t_{SU}	—	0.567	1.091	1.353	1.634	1.526	1.489	ns
		t_H	—	-0.496	-0.948	-1.185	-1.441	-1.346	-1.321	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.789	-1.611	-1.702	-1.840	-1.769	-2.650	ns
		t_H	—	0.859	1.751	1.865	2.029	1.946	2.813	ns
	GCLK PLL	t_{SU}	—	0.543	1.040	1.293	1.575	1.467	1.429	ns
		t_H	—	-0.473	-0.900	-1.130	-1.386	-1.290	-1.266	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.789	-1.611	-1.702	-1.840	-1.769	-2.650	ns
		t_H	—	0.859	1.751	1.865	2.029	1.946	2.813	ns
	GCLK PLL	t_{SU}	—	0.543	1.040	1.293	1.575	1.467	1.429	ns
		t_H	—	-0.473	-0.900	-1.130	-1.386	-1.290	-1.266	ns

Table 1–73 specifies EP3SL340 Row Pins Input Timing parameters for differential I/O standards.

Table 1–73. EP3SL340 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.781	-1.593	-1.687	-1.817	-1.751	-2.610	ns
		t_H	—	0.852	1.735	1.854	2.010	1.931	2.777	ns
	GCLK PLL	t_{SU}	—	0.569	1.090	1.349	1.646	1.529	1.511	ns
		t_H	—	-0.497	-0.944	-1.179	-1.447	-1.344	-1.341	ns
MINI-LVDS	GCLK	t_{SU}	—	-0.781	-1.593	-1.687	-1.817	-1.751	-2.610	ns
		t_H	—	0.852	1.735	1.854	2.010	1.931	2.777	ns
	GCLK PLL	t_{SU}	—	0.569	1.090	1.349	1.646	1.529	1.511	ns
		t_H	—	-0.497	-0.944	-1.179	-1.447	-1.344	-1.341	ns
RSDS	GCLK	t_{SU}	—	-0.781	-1.593	-1.687	-1.817	-1.751	-2.610	ns
		t_H	—	0.852	1.735	1.854	2.010	1.931	2.777	ns
	GCLK PLL	t_{SU}	—	0.569	1.090	1.349	1.646	1.529	1.511	ns
		t_H	—	-0.497	-0.944	-1.179	-1.447	-1.344	-1.341	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.705	-1.439	-1.509	-1.637	-1.572	-2.432	ns
		t_H	—	0.777	1.583	1.677	1.831	1.753	2.600	ns
	GCLK PLL	t_{SU}	—	0.687	1.329	1.626	1.927	1.808	1.788	ns
		t_H	—	-0.614	-1.180	-1.455	-1.726	-1.621	-1.617	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.705	-1.439	-1.509	-1.637	-1.572	-2.432	ns
		t_H	—	0.777	1.583	1.677	1.831	1.753	2.600	ns
	GCLK PLL	t_{SU}	—	0.687	1.329	1.626	1.927	1.808	1.788	ns
		t_H	—	-0.614	-1.180	-1.455	-1.726	-1.621	-1.617	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.712	-1.454	-1.525	-1.653	-1.588	-2.448	ns
		t_H	—	0.784	1.597	1.693	1.847	1.769	2.616	ns
	GCLK PLL	t_{SU}	—	0.680	1.315	1.610	1.910	1.792	1.772	ns
		t_H	—	-0.607	-1.166	-1.438	-1.709	-1.605	-1.600	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.712	-1.454	-1.525	-1.653	-1.588	-2.448	ns
		t_H	—	0.784	1.597	1.693	1.847	1.769	2.616	ns
	GCLK PLL	t_{SU}	—	0.680	1.315	1.610	1.910	1.792	1.772	ns
		t_H	—	-0.607	-1.166	-1.438	-1.709	-1.605	-1.600	ns

Table 1–73. EP3SL340 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.726	-1.481	-1.557	-1.686	-1.621	-2.480	ns
		t_H	—	0.797	1.624	1.725	1.879	1.801	2.648	ns
	GCLK PLL	t_{SU}	—	0.666	1.287	1.578	1.878	1.759	1.740	ns
		t_H	—	-0.593	-1.139	-1.407	-1.677	-1.573	-1.569	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.726	-1.481	-1.557	-1.686	-1.621	-2.480	ns
		t_H	—	0.797	1.624	1.725	1.879	1.801	2.648	ns
	GCLK PLL	t_{SU}	—	0.666	1.287	1.578	1.878	1.759	1.740	ns
		t_H	—	-0.593	-1.139	-1.407	-1.677	-1.573	-1.569	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.712	-1.454	-1.525	-1.653	-1.588	-2.448	ns
		t_H	—	0.784	1.597	1.693	1.847	1.769	2.616	ns
	GCLK PLL	t_{SU}	—	0.680	1.315	1.610	1.910	1.792	1.772	ns
		t_H	—	-0.607	-1.166	-1.438	-1.709	-1.605	-1.600	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.712	-1.454	-1.525	-1.653	-1.588	-2.448	ns
		t_H	—	0.784	1.597	1.693	1.847	1.769	2.616	ns
	GCLK PLL	t_{SU}	—	0.680	1.315	1.610	1.910	1.792	1.772	ns
		t_H	—	-0.607	-1.166	-1.438	-1.709	-1.605	-1.600	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.726	-1.481	-1.557	-1.686	-1.621	-2.480	ns
		t_H	—	0.797	1.624	1.725	1.879	1.801	2.648	ns
	GCLK PLL	t_{SU}	—	0.666	1.287	1.578	1.878	1.759	1.740	ns
		t_H	—	-0.593	-1.139	-1.407	-1.677	-1.573	-1.569	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.726	-1.481	-1.557	-1.686	-1.621	-2.480	ns
		t_H	—	0.797	1.624	1.725	1.879	1.801	2.648	ns
	GCLK PLL	t_{SU}	—	0.666	1.287	1.578	1.878	1.759	1.740	ns
		t_H	—	-0.593	-1.139	-1.407	-1.677	-1.573	-1.569	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.750	-1.532	-1.617	-1.745	-1.680	-2.540	ns
		t_H	—	0.820	1.672	1.780	1.934	1.857	2.703	ns
	GCLK PLL	t_{SU}	—	0.621	1.192	1.468	1.767	1.649	1.630	ns
		t_H	—	-0.549	-1.049	-1.300	-1.571	-1.468	-1.462	ns

Table 1–73. EP3SL340 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.750	-1.532	-1.617	-1.745	-1.680	-2.540	ns
		t_H	—	0.820	1.672	1.780	1.934	1.857	2.703	ns
	GCLK PLL	t_{SU}	—	0.621	1.192	1.468	1.767	1.649	1.630	ns
		t_H	—	-0.549	-1.049	-1.300	-1.571	-1.468	-1.462	ns

Table 1–74 specifies EP3SL340 Column Pins Output Timing parameters for differential I/O standards.

Table 1–74. EP3SL340 Column Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.412	4.737	5.323	5.664	5.487	6.268	ns
		GCLK PLL	t_{CO}	—	1.078	2.084	2.323	2.245	2.247	2.185	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.340	4.590	5.150	5.489	5.314	6.095	ns
		GCLK PLL	t_{CO}	—	1.006	1.937	2.150	2.070	2.074	2.012	ns

Table 1–74. EP3SL340 Column Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.332	4.575	5.132	5.471	5.296	6.077	ns
		GCLK PLL	t_{CO}	—	0.998	1.922	2.132	2.052	2.056	1.994	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.332	4.575	5.132	5.471	5.296	6.077	ns
		GCLK PLL	t_{CO}	—	0.998	1.922	2.132	2.052	2.056	1.994	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.333	4.577	5.134	5.473	5.298	6.079	ns
		GCLK PLL	t_{CO}	—	0.999	1.924	2.134	2.054	2.058	1.996	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.332	4.574	5.131	5.470	5.295	6.076	ns
		GCLK PLL	t_{CO}	—	0.998	1.921	2.131	2.051	2.055	1.993	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.329	4.568	5.124	5.463	5.288	6.069	ns
		GCLK PLL	t_{CO}	—	0.995	1.915	2.124	2.044	2.048	1.986	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.328	4.566	5.121	5.460	5.285	6.066	ns
		GCLK PLL	t_{CO}	—	0.994	1.913	2.121	2.041	2.045	1.983	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.329	4.568	5.124	5.463	5.288	6.069	ns
		GCLK PLL	t_{CO}	—	0.995	1.915	2.124	2.044	2.048	1.986	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.324	4.558	5.112	5.451	5.276	6.057	ns
		GCLK PLL	t_{CO}	—	0.990	1.905	2.112	2.032	2.036	1.974	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.321	4.553	5.106	5.445	5.270	6.051	ns
		GCLK PLL	t_{CO}	—	0.987	1.900	2.106	2.026	2.030	1.968	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.327	4.565	5.120	5.459	5.284	6.065	ns
		GCLK PLL	t_{CO}	—	0.993	1.912	2.120	2.040	2.044	1.982	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.315	4.540	5.091	5.429	5.254	6.036	ns
		GCLK PLL	t_{CO}	—	0.981	1.887	2.091	2.010	2.014	1.953	ns

Table 1–74. EP3SL340 Column Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.322	4.555	5.108	5.447	5.272	6.053	ns
		GCLK PLL	t_{CO}	—	0.988	1.902	2.108	2.028	2.032	1.970	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.317	4.545	5.097	5.435	5.260	6.042	ns
		GCLK PLL	t_{CO}	—	0.983	1.892	2.097	2.016	2.020	1.959	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.321	4.552	5.105	5.444	5.269	6.050	ns
		GCLK PLL	t_{CO}	—	0.987	1.899	2.105	2.025	2.029	1.967	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.319	4.549	5.101	5.440	5.265	6.046	ns
		GCLK PLL	t_{CO}	—	0.985	1.896	2.101	2.021	2.025	1.963	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.318	4.547	5.099	5.438	5.263	6.044	ns
		GCLK PLL	t_{CO}	—	0.984	1.894	2.099	2.019	2.023	1.961	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.311	4.532	5.081	5.420	5.245	6.026	ns
		GCLK PLL	t_{CO}	—	0.977	1.879	2.081	2.001	2.005	1.943	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.337	4.585	5.144	5.483	5.308	6.089	ns
		GCLK PLL	t_{CO}	—	1.003	1.932	2.144	2.064	2.068	2.006	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.332	4.575	5.132	5.471	5.296	6.077	ns
		GCLK PLL	t_{CO}	—	0.998	1.922	2.132	2.052	2.056	1.994	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.329	4.569	5.125	5.464	5.289	6.070	ns
		GCLK PLL	t_{CO}	—	0.995	1.916	2.125	2.045	2.049	1.987	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.332	4.575	5.132	5.471	5.296	6.077	ns
		GCLK PLL	t_{CO}	—	0.998	1.922	2.132	2.052	2.056	1.994	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.330	4.571	5.127	5.466	5.291	6.072	ns
		GCLK PLL	t_{CO}	—	0.996	1.918	2.127	2.047	2.051	1.989	ns

Table 1–74. EP3SL340 Column Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.322	4.554	5.107	5.446	5.271	6.052	ns
		GCLK PLL	t_{CO}	—	0.988	1.901	2.107	2.027	2.031	1.969	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.324	4.559	5.113	5.452	5.277	6.058	ns
		GCLK PLL	t_{CO}	—	0.990	1.906	2.113	2.033	2.037	1.975	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.335	4.580	5.138	5.477	5.302	6.083	ns
		GCLK PLL	t_{CO}	—	1.001	1.927	2.138	2.058	2.062	2.000	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.328	4.566	5.121	5.460	5.285	6.066	ns
		GCLK PLL	t_{CO}	—	0.994	1.913	2.121	2.041	2.045	1.983	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.330	4.570	5.126	5.465	5.290	6.071	ns
		GCLK PLL	t_{CO}	—	0.996	1.917	2.126	2.046	2.050	1.988	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.328	4.567	5.123	5.461	5.287	6.068	ns
		GCLK PLL	t_{CO}	—	0.994	1.914	2.123	2.042	2.047	1.985	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.325	4.560	5.114	5.453	5.278	6.059	ns
		GCLK PLL	t_{CO}	—	0.991	1.907	2.114	2.034	2.038	1.976	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.319	4.549	5.101	5.440	5.265	6.046	ns
		GCLK PLL	t_{CO}	—	0.985	1.896	2.101	2.021	2.025	1.963	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.322	4.555	5.108	5.447	5.272	6.053	ns
		GCLK PLL	t_{CO}	—	0.988	1.902	2.108	2.028	2.032	1.970	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.326	4.562	5.117	5.456	5.281	6.062	ns
		GCLK PLL	t_{CO}	—	0.992	1.909	2.117	2.037	2.041	1.979	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.325	4.560	5.114	5.453	5.278	6.059	ns
		GCLK PLL	t_{CO}	—	0.991	1.907	2.114	2.034	2.038	1.976	ns

Table 1–74. EP3SL340 Column Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.323	4.556	5.110	5.448	5.273	6.055	ns
		GCLK PLL	t_{CO}	—	0.989	1.903	2.110	2.029	2.033	1.972	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.321	4.553	5.106	5.445	5.270	6.051	ns
		GCLK PLL	t_{CO}	—	0.987	1.900	2.106	2.026	2.030	1.968	ns

Table 1–75 specifies EP3SL340 Row Pins Output Timing parameters for differential I/O standards.

Table 1–75. EP3SL340 Row Pins output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	tco	—	2.380	4.673	5.252	5.586	5.414	6.177	ns
		GCLK PLL	tco	—	1.049	2.025	2.258	2.174	2.180	2.098	ns
LVDS_E_1R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns
LVDS_E_3R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns
MINI-LVDS	-	GCLK	tco	—	2.380	4.673	5.252	5.586	5.414	6.177	ns
		GCLK PLL	tco	—	1.049	2.025	2.258	2.174	2.180	2.098	ns
MINI-LVDS_E_1R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns
MINI-LVDS_E_3R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns

Table 1–75. EP3SL340 Row Pins output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RSDS	-	GCLK	tco	—	2.380	4.673	5.252	5.586	5.414	6.177	ns
		GCLK PLL	tco	—	1.049	2.025	2.258	2.174	2.180	2.098	ns
RSDS_E_1R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns
RSDS_E_3R	-	GCLK	tco	—	2.379	4.671	5.250	5.583	5.411	6.175	ns
		GCLK PLL	tco	—	1.048	2.023	2.256	2.171	2.177	2.096	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	tco	—	2.310	4.532	5.086	5.418	5.248	6.008	ns
		GCLK PLL	tco	—	0.985	1.896	2.105	2.019	2.027	1.945	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	tco	—	2.302	4.515	5.067	5.399	5.228	5.989	ns
		GCLK PLL	tco	—	0.977	1.879	2.086	2.000	2.007	1.926	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	tco	—	2.301	4.512	5.064	5.395	5.225	5.986	ns
		GCLK PLL	tco	—	0.976	1.876	2.083	1.996	2.004	1.923	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	tco	—	2.300	4.510	5.061	5.393	5.223	5.983	ns
		GCLK PLL	tco	—	0.975	1.874	2.080	1.994	2.002	1.920	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	tco	—	2.299	4.508	5.059	5.390	5.220	5.981	ns
		GCLK PLL	tco	—	0.974	1.872	2.078	1.991	1.999	1.918	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	tco	—	2.294	4.498	5.047	5.378	5.208	5.969	ns
		GCLK PLL	tco	—	0.969	1.862	2.066	1.979	1.987	1.906	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	tco	—	2.294	4.498	5.047	5.378	5.208	5.969	ns
		GCLK PLL	tco	—	0.969	1.862	2.066	1.979	1.987	1.906	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	tco	—	2.288	4.487	5.034	5.365	5.195	5.956	ns
		GCLK PLL	tco	—	0.963	1.851	2.053	1.966	1.974	1.893	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	tco	—	2.290	4.490	5.038	5.369	5.199	5.960	ns
		GCLK PLL	tco	—	0.965	1.854	2.057	1.970	1.978	1.897	ns

Table 1–75. EP3SL340 Row Pins output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	tco	—	2.289	4.489	5.037	5.367	5.198	5.959	ns
		GCLK PLL	tco	—	0.964	1.853	2.056	1.968	1.977	1.896	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	tco	—	2.287	4.485	5.032	5.363	5.193	5.954	ns
		GCLK PLL	tco	—	0.962	1.849	2.051	1.964	1.972	1.891	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	tco	—	2.278	4.467	5.011	5.341	5.171	5.933	ns
		GCLK PLL	tco	—	0.953	1.831	2.030	1.942	1.950	1.870	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	tco	—	2.310	4.531	5.085	5.417	5.246	6.007	ns
		GCLK PLL	tco	—	0.985	1.895	2.104	2.018	2.025	1.944	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	tco	—	2.303	4.516	5.069	5.400	5.230	5.991	ns
		GCLK PLL	tco	—	0.978	1.880	2.088	2.001	2.009	1.928	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	tco	—	2.299	4.508	5.059	5.390	5.220	5.981	ns
		GCLK PLL	tco	—	0.974	1.872	2.078	1.991	1.999	1.918	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	tco	—	2.306	4.523	5.076	5.407	5.237	5.998	ns
		GCLK PLL	tco	—	0.981	1.887	2.095	2.008	2.016	1.935	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	tco	—	2.299	4.509	5.060	5.391	5.221	5.982	ns
		GCLK PLL	tco	—	0.974	1.873	2.079	1.992	2.000	1.919	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	tco	—	2.299	4.509	5.060	5.391	5.221	5.982	ns
		GCLK PLL	tco	—	0.974	1.873	2.079	1.992	2.000	1.919	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	tco	—	2.298	4.507	5.058	5.389	5.219	5.980	ns
		GCLK PLL	tco	—	0.973	1.871	2.077	1.990	1.998	1.917	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	tco	—	2.294	4.499	5.048	5.379	5.209	5.970	ns
		GCLK PLL	tco	—	0.969	1.863	2.067	1.980	1.988	1.907	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	tco	—	2.289	4.489	5.037	5.367	5.198	5.959	ns
		GCLK PLL	tco	—	0.964	1.853	2.056	1.968	1.977	1.896	ns

Table 1–75. EP3SL340 Row Pins output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	tco	—	2.290	4.491	5.039	5.370	5.200	5.961	ns
		GCLK PLL	tco	—	0.965	1.855	2.058	1.971	1.979	1.898	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	tco	—	2.298	4.506	5.057	5.388	5.218	5.979	ns
		GCLK PLL	tco	—	0.973	1.870	2.076	1.989	1.997	1.916	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	tco	—	2.294	4.498	5.047	5.378	5.208	5.969	ns
		GCLK PLL	tco	—	0.969	1.862	2.066	1.979	1.987	1.906	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	tco	—	2.290	4.491	5.039	5.370	5.200	5.961	ns
		GCLK PLL	tco	—	0.965	1.855	2.058	1.971	1.979	1.898	ns

Table 1–76 through Table 1–77 show EP3SL340 regional (RCLK) clock adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–76 specifies EP3SL340 Column Pin delay adders when using the Regional Clock.

Table 1–76. EP3SL340 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.204	0.416	0.448	0.479	0.46	0.637	ns
RCLK PLL input adder	—	0.011	0.022	-0.009	-0.051	-0.029	-0.028	ns
RCLK output adder	—	-0.217	-0.44	-0.477	-0.512	-0.492	-0.675	ns
RCLK PLL output adder	—	-0.027	-0.054	-0.022	0.046	-0.006	0.024	ns

Table 1–77 specifies EP3SL340 Row Pin delay adders when using the Regional Clock.

Table 1–77. EP3SL340 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.22	0.444	0.48	0.515	0.501	0.679	ns
RCLK PLL input adder	—	0.014	0.03	-0.001	-0.043	-0.021	-0.019	ns
RCLK output adder	—	-0.22	-0.444	-0.48	-0.515	-0.501	-0.692	ns
RCLK PLL output adder	—	-0.014	-0.03	0.001	0.043	0.021	0.019	ns

EP3SE50 I/O Timing Parameters

Table 1–78 through Table 1–81 show the maximum I/O timing parameters for EP3SE50 devices for single ended I/O standards.

Table 1–78 specifies EP3SE50 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–78. EP3SE50 Column Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.534	-1.093	-1.164	-1.236	-1.199	-1.769	ns
		t_H	—	0.603	1.231	1.324	1.422	1.373	1.929	ns
	GCLK PLL	t_{SU}	—	0.436	0.820	0.975	1.178	1.110	1.066	ns
		t_H	—	-0.367	-0.682	-0.815	-0.992	-0.936	-0.906	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.534	-1.093	-1.164	-1.236	-1.199	-1.769	ns
		t_H	—	0.603	1.231	1.324	1.422	1.373	1.929	ns
	GCLK PLL	t_{SU}	—	0.436	0.820	0.975	1.178	1.110	1.066	ns
		t_H	—	-0.367	-0.682	-0.815	-0.992	-0.936	-0.906	ns

Table 1–78. EP3SE50 Column Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	GCLK	t_{SU}	—	-0.539	-1.104	-1.176	-1.248	-1.211	-1.781	ns
		t_H	—	0.608	1.241	1.336	1.434	1.385	1.941	ns
	GCLK PLL	t_{SU}	—	0.431	0.809	0.963	1.166	1.098	1.054	ns
		t_H	—	-0.362	-0.672	-0.803	-0.980	-0.924	-0.894	ns
1.8 V	GCLK	t_{SU}	—	-0.549	-1.124	-1.200	-1.272	-1.235	-1.805	ns
		t_H	—	0.618	1.261	1.359	1.458	1.408	1.964	ns
	GCLK PLL	t_{SU}	—	0.421	0.789	0.939	1.142	1.074	1.030	ns
		t_H	—	-0.352	-0.652	-0.780	-0.956	-0.901	-0.871	ns
1.5 V	GCLK	t_{SU}	—	-0.529	-1.083	-1.153	-1.224	-1.187	-1.758	ns
		t_H	—	0.598	1.221	1.313	1.410	1.361	1.918	ns
	GCLK PLL	t_{SU}	—	0.441	0.830	0.986	1.190	1.122	1.077	ns
		t_H	—	-0.372	-0.692	-0.826	-1.004	-0.948	-0.917	ns
1.2 V	GCLK	t_{SU}	—	-0.472	-0.969	-1.019	-1.089	-1.052	-1.624	ns
		t_H	—	0.542	1.107	1.180	1.276	1.228	1.785	ns
	GCLK PLL	t_{SU}	—	0.498	0.944	1.120	1.325	1.257	1.211	ns
		t_H	—	-0.428	-0.806	-0.959	-1.138	-1.081	-1.050	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.412	-0.846	-0.876	-0.944	-0.908	-1.481	ns
		t_H	—	0.482	0.986	1.039	1.133	1.085	1.644	ns
	GCLK PLL	t_{SU}	—	0.558	1.067	1.263	1.470	1.401	1.354	ns
		t_H	—	-0.488	-0.927	-1.100	-1.281	-1.224	-1.191	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.412	-0.846	-0.876	-0.944	-0.908	-1.481	ns
		t_H	—	0.482	0.986	1.039	1.133	1.085	1.644	ns
	GCLK PLL	t_{SU}	—	0.558	1.067	1.263	1.470	1.401	1.354	ns
		t_H	—	-0.488	-0.927	-1.100	-1.281	-1.224	-1.191	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.388	-0.795	-0.816	-0.885	-0.849	-1.421	ns
	GCLK PLL	t_H	—	0.582	1.118	1.323	1.529	1.460	1.589	ns
		t_{SU}	—	-0.511	-0.975	-1.155	-1.336	-1.280	1.414	ns
SSTL-18 CLASS II	GCLK	t_H	—	-0.388	-0.795	-0.816	-0.885	-0.849	-1.246	ns
	GCLK PLL	t_{SU}	—	0.582	1.118	1.323	1.529	1.460	-1.421	ns
		t_H	—	-0.511	-0.975	-1.155	-1.336	-1.280	1.589	ns

Table 1–78. EP3SE50 Column Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.374	-0.768	-0.784	-0.852	-0.816	1.589	ns
	GCLK PLL	t_{SU}	—	0.596	1.145	1.355	1.562	1.493	1.414	ns
		t_{H}	—	-0.524	-1.002	-1.187	-1.368	-1.312	-1.246	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.374	-0.768	-0.784	-0.852	-0.816	-1.389	ns
	GCLK PLL	t_{SU}	—	0.596	1.145	1.355	1.562	1.493	1.557	ns
		t_{H}	—	-0.524	-1.002	-1.187	-1.368	-1.312	1.446	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.388	-0.795	-0.816	-0.885	-0.849	1.446	ns
	GCLK PLL	t_{SU}	—	0.582	1.118	1.323	1.529	1.460	-1.278	ns
		t_{H}	—	-0.511	-0.975	-1.155	-1.336	-1.280	-1.389	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.388	-0.795	-0.816	-0.885	-0.849	1.589	ns
	GCLK PLL	t_{SU}	—	0.582	1.118	1.323	1.529	1.460	1.414	ns
		t_{H}	—	-0.511	-0.975	-1.155	-1.336	-1.280	-1.246	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.374	-0.768	-0.784	-0.852	-0.816	-1.421	ns
	GCLK PLL	t_{SU}	—	0.596	1.145	1.355	1.562	1.493	1.589	ns
		t_{H}	—	-0.524	-1.002	-1.187	-1.368	-1.312	1.414	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.374	-0.768	-0.784	-0.852	-0.816	-1.246	ns
	GCLK PLL	t_{SU}	—	0.596	1.145	1.355	1.562	1.493	-1.421	ns
		t_{H}	—	-0.524	-1.002	-1.187	-1.368	-1.312	1.589	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.367	-0.753	-0.768	-0.836	-0.800	1.414	ns
	GCLK PLL	t_{SU}	—	0.603	1.160	1.371	1.578	1.509	-1.246	ns
		t_{H}	—	-0.531	-1.016	-1.203	-1.384	-1.328	-1.389	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.367	-0.753	-0.768	-0.836	-0.800	1.557	ns
	GCLK PLL	t_{SU}	—	0.603	1.160	1.371	1.578	1.509	1.446	ns
		t_{H}	—	-0.531	-1.016	-1.203	-1.384	-1.328	-1.278	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.534	-1.093	-1.164	-1.236	-1.199	-1.389	ns
		t_{H}	—	0.603	1.231	1.324	1.422	1.373	1.557	ns
	GCLK PLL	t_{SU}	—	0.436	0.820	0.975	1.178	1.110	1.446	ns
		t_{H}	—	-0.367	-0.682	-0.815	-0.992	-0.936	-1.278	ns

Table 1–78. EP3SE50 Column Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI-X	GCLK	t_{SU}	—	-0.534	-1.093	-1.164	-1.236	-1.199	-1.389	ns
		t_H	—	0.603	1.231	1.324	1.422	1.373	1.557	ns
	GCLK PLL	t_{SU}	—	0.436	0.820	0.975	1.178	1.110	1.446	ns
		t_H	—	-0.367	-0.682	-0.815	-0.992	-0.936	-1.278	ns

Table 1–79 specifies EP3SE50 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–79. EP3SE50 Row Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.451	-0.926	-0.975	-1.030	-1.002	-1.543	ns
		t_H	—	0.522	1.067	1.140	1.222	1.180	1.708	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.155	1.374	1.299	1.281	ns
		t_H	—	-0.444	-0.839	-0.990	-1.182	-1.121	-1.116	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.451	-0.926	-0.975	-1.030	-1.002	-1.543	ns
		t_H	—	0.522	1.067	1.140	1.222	1.180	1.708	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.155	1.374	1.299	1.281	ns
		t_H	—	-0.444	-0.839	-0.990	-1.182	-1.121	-1.116	ns
2.5 V	GCLK	t_{SU}	—	-0.456	-0.936	-0.986	-1.042	-1.014	-1.554	ns
		t_H	—	0.527	1.077	1.152	1.234	1.192	1.720	ns
	GCLK PLL	t_{SU}	—	0.510	0.970	1.144	1.362	1.287	1.270	ns
		t_H	—	-0.439	-0.829	-0.978	-1.170	-1.109	-1.104	ns
1.8 V	GCLK	t_{SU}	—	-0.467	-0.959	-1.013	-1.069	-1.040	-1.581	ns
		t_H	—	0.538	1.100	1.178	1.261	1.218	1.746	ns
	GCLK PLL	t_{SU}	—	0.500	0.950	1.120	1.338	1.264	1.246	ns
		t_H	—	-0.429	-0.809	-0.955	-1.146	-1.086	-1.081	ns

Table 1–79. EP3SE50 Row Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	GCLK	t_{SU}	—	-0.446	-0.918	-0.965	-1.020	-0.992	-1.533	ns
		t_H	—	0.517	1.059	1.130	1.212	1.170	1.698	ns
	GCLK PLL	t_{SU}	—	0.521	0.991	1.168	1.387	1.312	1.294	ns
		t_H	—	-0.450	-0.850	-1.003	-1.195	-1.134	-1.129	ns
1.2 V	GCLK	t_{SU}	—	-0.389	-0.801	-0.829	-0.882	-0.855	-1.397	ns
		t_H	—	0.460	0.943	0.995	1.076	1.035	1.563	ns
	GCLK PLL	t_{SU}	—	0.578	1.108	1.304	1.525	1.449	1.430	ns
		t_H	—	-0.507	-0.966	-1.138	-1.331	-1.269	-1.264	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.325	-0.670	-0.677	-0.728	-0.702	-1.245	ns
		t_H	—	0.397	0.813	0.845	0.924	0.883	1.413	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.453	1.676	1.599	1.579	ns
		t_H	—	-0.569	-1.093	-1.285	-1.480	-1.418	-1.411	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.325	-0.670	-0.677	-0.728	-0.702	-1.245	ns
		t_H	—	0.397	0.813	0.845	0.924	0.883	1.413	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.453	1.676	1.599	1.579	ns
		t_H	—	-0.569	-1.093	-1.285	-1.480	-1.418	-1.411	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.281	-0.578	-0.570	-0.620	-0.595	-1.138	ns
		t_H	—	0.354	0.726	0.741	0.821	0.781	1.309	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.281	-0.578	-0.570	-0.620	-0.595	-1.138	ns
		t_H	—	0.354	0.726	0.741	0.821	0.781	1.309	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.267	-0.550	-0.538	-0.588	-0.562	-1.106	ns
		t_H	—	0.340	0.699	0.710	0.789	0.749	1.278	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns

Table 1–79. EP3SE50 Row Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.267	-0.550	-0.538	-0.588	-0.562	-1.106	ns
		t_H	—	0.340	0.699	0.710	0.789	0.749	1.278	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.281	-0.578	-0.570	-0.620	-0.595	-1.138	ns
		t_H	—	0.354	0.726	0.741	0.821	0.781	1.309	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.281	-0.578	-0.570	-0.620	-0.595	-1.138	ns
		t_H	—	0.354	0.726	0.741	0.821	0.781	1.309	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.267	-0.550	-0.538	-0.588	-0.562	-1.106	ns
		t_H	—	0.340	0.699	0.710	0.789	0.749	1.278	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.267	-0.550	-0.538	-0.588	-0.562	-1.106	ns
		t_H	—	0.340	0.699	0.710	0.789	0.749	1.278	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.260	-0.536	-0.522	-0.571	-0.546	-1.090	ns
		t_H	—	0.333	0.685	0.693	0.772	0.733	1.261	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.611	1.836	1.758	1.737	ns
		t_H	—	-0.634	-1.224	-1.440	-1.635	-1.571	-1.566	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.260	-0.536	-0.522	-0.571	-0.546	-1.090	ns
		t_H	—	0.333	0.685	0.693	0.772	0.733	1.261	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.611	1.836	1.758	1.737	ns
		t_H	—	-0.634	-1.224	-1.440	-1.635	-1.571	-1.566	ns

Table 1–79. EP3SE50 Row Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI	GCLK	t_{SU}	—	-0.451	-0.926	-0.975	-1.030	-1.002	-1.543	ns
		t_H	—	0.522	1.067	1.140	1.222	1.180	1.708	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.155	1.374	1.299	1.281	ns
		t_H	—	-0.444	-0.839	-0.990	-1.182	-1.121	-1.116	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.451	-0.926	-0.975	-1.030	-1.002	-1.543	ns
		t_H	—	0.522	1.067	1.140	1.222	1.180	1.708	ns
	GCLK PLL	t_{SU}	—	0.515	0.980	1.155	1.374	1.299	1.281	ns
		t_H	—	-0.444	-0.839	-0.990	-1.182	-1.121	-1.116	ns

Table 1–80 specifies EP3SE50 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.432	4.115	4.620	4.869	4.546	5.015	ns
		GCLK PLL	t_{CO}	—	1.477	2.235	2.518	2.493	2.273	2.231	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.580	4.256	4.819	5.068	4.693	5.178	ns
		GCLK PLL	t_{CO}	—	1.625	2.371	2.717	2.692	2.413	2.372	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.640	4.330	4.874	5.123	4.773	5.250	ns
		GCLK PLL	t_{CO}	—	1.685	2.450	2.772	2.747	2.500	2.458	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	2.755	4.494	5.059	5.310	4.938	5.423	ns
		GCLK PLL	t_{CO}	—	1.800	2.614	2.957	2.932	2.665	2.624	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.580	4.256	4.818	5.067	4.693	5.178	ns
		GCLK PLL	t_{CO}	—	1.625	2.371	2.716	2.691	2.413	2.372	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.755	4.494	5.059	5.310	4.938	5.423	ns
		GCLK PLL	t_{CO}	—	1.800	2.614	2.956	2.931	2.665	2.624	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	2.810	4.570	5.123	5.372	5.017	5.499	ns
		GCLK PLL	t_{CO}	—	1.855	2.690	3.021	2.996	2.744	2.702	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	2.863	4.631	5.182	5.433	5.082	5.566	ns
		GCLK PLL	t_{CO}	—	1.908	2.751	3.077	3.052	2.806	2.764	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.518	4.276	4.888	5.137	4.715	5.184	ns
		GCLK PLL	t_{CO}	—	1.563	2.396	2.786	2.761	2.442	2.400	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.557	4.300	4.863	5.112	4.737	5.209	ns
		GCLK PLL	t_{CO}	—	1.602	2.420	2.761	2.736	2.464	2.423	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.805	4.645	5.263	5.512	5.092	5.572	ns
		GCLK PLL	t_{CO}	—	1.850	2.765	3.161	3.136	2.819	2.778	ns
2.5 V	16mA	GCLK	t_{CO}	—	2.838	4.704	5.360	5.609	5.156	5.641	ns
		GCLK PLL	t_{CO}	—	1.883	2.824	3.258	3.233	2.881	2.840	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.420	4.147	4.703	4.952	4.582	5.052	ns
		GCLK PLL	t_{CO}	—	1.465	2.267	2.601	2.576	2.309	2.268	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.483	4.264	4.932	5.181	4.701	5.170	ns
		GCLK PLL	t_{CO}	—	1.527	2.384	2.830	2.805	2.428	2.386	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.725	4.562	5.222	5.471	5.005	5.481	ns
		GCLK PLL	t_{CO}	—	1.770	2.682	3.120	3.095	2.732	2.691	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.552	4.309	4.904	5.153	4.745	5.227	ns
		GCLK PLL	t_{CO}	—	1.597	2.429	2.802	2.777	2.472	2.431	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	10mA	GCLK	t_{CO}	—	2.814	4.671	5.315	5.566	5.120	5.605	ns
		GCLK PLL	t_{CO}	—	1.859	2.791	3.213	3.188	2.844	2.803	ns
1.8 V	12mA	GCLK	t_{CO}	—	2.885	4.817	5.535	5.784	5.269	5.748	ns
		GCLK PLL	t_{CO}	—	1.930	2.937	3.433	3.408	2.996	2.955	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.372	4.024	4.604	4.853	4.460	4.944	ns
		GCLK PLL	t_{CO}	—	1.417	2.129	2.502	2.477	2.169	2.127	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.640	4.469	5.081	5.330	4.916	5.385	ns
		GCLK PLL	t_{CO}	—	1.685	2.589	2.979	2.954	2.643	2.601	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.738	4.575	5.211	5.460	5.020	5.490	ns
		GCLK PLL	t_{CO}	—	1.783	2.695	3.109	3.084	2.747	2.706	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.663	4.431	5.054	5.303	4.874	5.353	ns
		GCLK PLL	t_{CO}	—	1.708	2.551	2.952	2.927	2.601	2.560	ns
1.5 V	10mA	GCLK	t_{CO}	—	2.829	4.718	5.409	5.658	5.166	5.651	ns
		GCLK PLL	t_{CO}	—	1.874	2.838	3.307	3.282	2.891	2.850	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.003	5.060	5.897	6.146	5.511	5.981	ns
		GCLK PLL	t_{CO}	—	2.048	3.180	3.795	3.770	3.238	3.197	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.648	4.529	5.309	5.558	4.952	5.422	ns
		GCLK PLL	t_{CO}	—	1.693	2.649	3.207	3.182	2.679	2.638	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.814	4.748	5.491	5.740	5.194	5.664	ns
		GCLK PLL	t_{CO}	—	1.859	2.868	3.389	3.364	2.921	2.880	ns
1.2 V	6mA	GCLK	t_{CO}	—	2.750	4.618	5.324	5.573	5.060	5.530	ns
		GCLK PLL	t_{CO}	—	1.795	2.738	3.222	3.197	2.787	2.746	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2 V	8mA	GCLK	t_{CO}	—	3.004	5.020	5.831	6.080	5.468	5.938	ns
		GCLK PLL	t_{CO}	—	2.049	3.140	3.729	3.704	3.195	3.154	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.130	3.647	4.107	4.358	4.071	4.556	ns
		GCLK PLL	t_{CO}	—	1.175	1.767	1.998	1.973	1.793	1.752	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.127	3.644	4.102	4.353	4.066	4.551	ns
		GCLK PLL	t_{CO}	—	1.172	1.764	1.994	1.969	1.790	1.749	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.130	3.652	4.105	4.354	4.071	4.551	ns
		GCLK PLL	t_{CO}	—	1.175	1.772	2.003	1.978	1.798	1.757	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.142	3.654	4.106	4.357	4.072	4.554	ns
		GCLK PLL	t_{CO}	—	1.187	1.774	2.003	1.978	1.799	1.758	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.137	3.661	4.118	4.369	4.080	4.563	ns
		GCLK PLL	t_{CO}	—	1.182	1.781	2.015	1.990	1.807	1.766	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.130	3.653	4.108	4.358	4.071	4.553	ns
		GCLK PLL	t_{CO}	—	1.175	1.773	2.006	1.981	1.798	1.757	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.134	3.662	4.123	4.374	4.082	4.567	ns
		GCLK PLL	t_{CO}	—	1.179	1.782	2.018	1.993	1.808	1.767	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.133	3.664	4.122	4.371	4.084	4.565	ns
		GCLK PLL	t_{CO}	—	1.178	1.784	2.020	1.995	1.811	1.770	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.131	3.662	4.120	4.369	4.082	4.562	ns
		GCLK PLL	t_{CO}	—	1.176	1.782	2.018	1.993	1.809	1.768	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.136	3.652	4.104	4.353	4.070	4.547	ns
		GCLK PLL	t_{CO}	—	1.181	1.772	2.002	1.977	1.797	1.756	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.152	3.687	4.145	4.394	4.107	4.577	ns
		GCLK PLL	t_{CO}	—	1.197	1.807	2.043	2.018	1.834	1.793	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.136	3.663	4.121	4.370	4.081	4.561	ns
		GCLK PLL	t_{CO}	—	1.181	1.783	2.019	1.994	1.808	1.767	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.135	3.664	4.125	4.376	4.083	4.566	ns
		GCLK PLL	t_{CO}	—	1.180	1.784	2.021	1.996	1.810	1.769	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.134	3.668	4.127	4.376	4.087	4.565	ns
		GCLK PLL	t_{CO}	—	1.179	1.788	2.025	2.000	1.814	1.773	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.142	3.682	4.143	4.393	4.102	4.582	ns
		GCLK PLL	t_{CO}	—	1.187	1.802	2.041	2.016	1.829	1.788	ns
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.137	3.676	4.136	4.385	4.095	4.574	ns
		GCLK PLL	t_{CO}	—	1.182	1.796	2.034	2.009	1.822	1.781	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.138	3.659	4.114	4.363	4.078	4.554	ns
		GCLK PLL	t_{CO}	—	1.183	1.779	2.012	1.987	1.805	1.764	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.152	3.691	4.152	4.401	4.112	4.582	ns
		GCLK PLL	t_{CO}	—	1.197	1.811	2.050	2.025	1.839	1.798	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.133	3.643	4.097	4.348	4.061	4.544	ns
		GCLK PLL	t_{CO}	—	1.178	1.763	1.993	1.968	1.788	1.747	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.134	3.646	4.109	4.360	4.069	4.554	ns
		GCLK PLL	t_{CO}	—	1.179	1.766	1.997	1.972	1.791	1.750	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.136	3.654	4.107	4.358	4.072	4.553	ns
		GCLK PLL	t_{CO}	—	1.181	1.774	2.005	1.980	1.799	1.758	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.140	3.661	4.115	4.364	4.080	4.556	ns
		GCLK PLL	t_{CO}	—	1.185	1.781	2.013	1.988	1.807	1.766	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.142	3.664	4.118	4.369	4.083	4.563	ns
		GCLK PLL	t_{CO}	—	1.187	1.784	2.016	1.991	1.810	1.769	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.193	3.698	4.148	4.397	4.116	4.586	ns
		GCLK PLL	t_{CO}	—	1.238	1.818	2.046	2.021	1.843	1.802	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.139	3.652	4.106	4.357	4.070	4.551	ns
		GCLK PLL	t_{CO}	—	1.184	1.772	2.004	1.979	1.797	1.756	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.139	3.655	4.120	4.371	4.078	4.563	ns
		GCLK PLL	t_{CO}	—	1.184	1.775	2.009	1.984	1.800	1.759	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.136	3.650	4.109	4.360	4.068	4.553	ns
		GCLK PLL	t_{CO}	—	1.181	1.770	2.002	1.977	1.795	1.754	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.138	3.659	4.114	4.363	4.078	4.554	ns
		GCLK PLL	t_{CO}	—	1.183	1.779	2.012	1.987	1.805	1.764	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.147	3.673	4.130	4.380	4.092	4.571	ns
		GCLK PLL	t_{CO}	—	1.192	1.793	2.028	2.003	1.819	1.778	ns
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.171	3.658	4.105	4.354	4.074	4.544	ns
		GCLK PLL	t_{CO}	—	1.216	1.778	2.003	1.978	1.801	1.760	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.150	3.671	4.134	4.385	4.090	4.571	ns
		GCLK PLL	t_{CO}	—	1.195	1.791	2.028	2.003	1.817	1.776	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.144	3.666	4.128	4.379	4.084	4.567	ns
		GCLK PLL	t_{CO}	—	1.189	1.786	2.022	1.997	1.811	1.770	ns

Table 1–80. EP3SE50 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.154	3.684	4.147	4.398	4.103	4.584	ns
		GCLK PLL	t_{CO}	—	1.199	1.804	2.043	2.018	1.830	1.789	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.150	3.684	4.145	4.394	4.104	4.579	ns
		GCLK PLL	t_{CO}	—	1.195	1.804	2.043	2.018	1.831	1.790	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.150	3.683	4.143	4.392	4.102	4.576	ns
		GCLK PLL	t_{CO}	—	1.195	1.803	2.041	2.016	1.829	1.788	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.203	3.717	4.172	4.421	4.135	4.605	ns
		GCLK PLL	t_{CO}	—	1.248	1.837	2.070	2.045	1.862	1.821	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.128	4.991	5.641	5.892	5.448	5.932	ns
		GCLK PLL	t_{CO}	—	2.173	3.111	3.539	3.514	3.175	3.133	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.128	4.991	5.641	5.892	5.448	5.932	ns
		GCLK PLL	t_{CO}	—	2.173	3.111	3.539	3.514	3.175	3.133	ns

Table 1–81 specifies EP3SE50 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–81. EP3SE50 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.508	4.200	4.735	4.977	4.628	5.079	ns
		GCLK PLL	t_{CO}	—	1.542	2.294	2.605	2.573	2.327	2.255	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.572	4.258	4.825	5.067	4.681	5.133	ns
		GCLK PLL	t_{CO}	—	1.606	2.352	2.695	2.663	2.380	2.309	ns

Table 1–81. EP3SE50 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.703	4.415	4.971	5.213	4.843	5.294	ns
		GCLK PLL	t_{CO}	—	1.737	2.509	2.841	2.809	2.542	2.470	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.601	4.282	4.835	5.077	4.714	5.165	ns
		GCLK PLL	t_{CO}	—	1.635	2.376	2.705	2.673	2.413	2.341	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.743	4.465	5.040	5.282	4.899	5.351	ns
		GCLK PLL	t_{CO}	—	1.777	2.559	2.910	2.878	2.598	2.527	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.605	4.422	5.049	5.291	4.859	5.310	ns
		GCLK PLL	t_{CO}	—	1.639	2.516	2.919	2.887	2.558	2.486	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.599	4.353	4.927	5.169	4.782	5.233	ns
		GCLK PLL	t_{CO}	—	1.633	2.447	2.797	2.765	2.481	2.409	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.804	4.633	5.261	5.503	5.078	5.529	ns
		GCLK PLL	t_{CO}	—	1.838	2.727	3.131	3.099	2.777	2.705	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.610	4.334	4.885	5.127	4.769	5.220	ns
		GCLK PLL	t_{CO}	—	1.643	2.425	2.752	2.720	2.465	2.393	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.641	4.469	5.149	5.391	4.898	5.350	ns
		GCLK PLL	t_{CO}	—	1.674	2.560	3.016	2.984	2.594	2.523	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.733	4.614	5.316	5.558	5.054	5.506	ns
		GCLK PLL	t_{CO}	—	1.766	2.705	3.183	3.151	2.750	2.679	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.618	4.389	4.989	5.231	4.817	5.268	ns
		GCLK PLL	t_{CO}	—	1.651	2.480	2.856	2.824	2.513	2.441	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.523	4.249	4.820	5.062	4.678	5.129	ns
		GCLK PLL	t_{CO}	—	1.556	2.340	2.687	2.655	2.374	2.302	ns

Table 1–81. EP3SE50 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5 V	4mA	GCLK	t_{CO}	—	2.648	4.492	5.129	5.371	4.930	5.381	ns
		GCLK PLL	t_{CO}	—	1.681	2.583	2.996	2.964	2.626	2.554	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.783	4.644	5.339	5.581	5.085	5.537	ns
		GCLK PLL	t_{CO}	—	1.816	2.735	3.206	3.174	2.781	2.710	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.670	4.470	5.114	5.356	4.905	5.357	ns
		GCLK PLL	t_{CO}	—	1.703	2.561	2.981	2.949	2.601	2.530	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.773	4.854	5.750	5.992	5.270	5.722	ns
		GCLK PLL	t_{CO}	—	1.806	2.945	3.617	3.585	2.966	2.895	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.901	4.922	5.741	5.983	5.350	5.802	ns
		GCLK PLL	t_{CO}	—	1.934	3.013	3.608	3.576	3.046	2.975	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.097	3.603	4.056	4.298	4.014	4.466	ns
		GCLK PLL	t_{CO}	—	1.131	1.697	1.926	1.894	1.713	1.642	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.085	3.594	4.047	4.289	4.004	4.456	ns
		GCLK PLL	t_{CO}	—	1.119	1.688	1.917	1.885	1.703	1.632	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.090	3.595	4.047	4.289	4.005	4.457	ns
		GCLK PLL	t_{CO}	—	1.124	1.689	1.917	1.885	1.704	1.633	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.100	3.612	4.070	4.312	4.023	4.475	ns
		GCLK PLL	t_{CO}	—	1.133	1.703	1.937	1.905	1.719	1.648	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.088	3.600	4.057	4.299	4.010	4.462	ns
		GCLK PLL	t_{CO}	—	1.121	1.691	1.924	1.892	1.706	1.635	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.088	3.607	4.066	4.308	4.017	4.469	ns
		GCLK PLL	t_{CO}	—	1.121	1.698	1.933	1.901	1.713	1.642	ns

Table 1–81. EP3SE50 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.080	3.602	4.060	4.302	4.012	4.464	ns
		GCLK PLL	t_{CO}	—	1.113	1.693	1.927	1.895	1.708	1.637	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.078	3.599	4.058	4.300	4.010	4.462	ns
		GCLK PLL	t_{CO}	—	1.111	1.690	1.925	1.893	1.706	1.635	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.083	3.591	4.047	4.289	4.001	4.453	ns
		GCLK PLL	t_{CO}	—	1.116	1.682	1.914	1.882	1.697	1.626	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.085	3.605	4.063	4.305	4.015	4.467	ns
		GCLK PLL	t_{CO}	—	1.118	1.696	1.930	1.898	1.711	1.640	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.100	3.615	4.076	4.318	4.025	4.477	ns
		GCLK PLL	t_{CO}	—	1.133	1.706	1.943	1.911	1.721	1.650	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.089	3.610	4.072	4.314	4.020	4.472	ns
		GCLK PLL	t_{CO}	—	1.122	1.701	1.939	1.907	1.716	1.645	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.081	3.604	4.065	4.307	4.014	4.466	ns
		GCLK PLL	t_{CO}	—	1.114	1.695	1.932	1.900	1.710	1.639	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.095	3.593	4.046	4.288	4.002	4.454	ns
		GCLK PLL	t_{CO}	—	1.128	1.684	1.913	1.881	1.698	1.627	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.086	3.592	4.048	4.290	4.002	4.454	ns
		GCLK PLL	t_{CO}	—	1.119	1.683	1.915	1.883	1.698	1.627	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.080	3.591	4.046	4.288	4.000	4.452	ns
		GCLK PLL	t_{CO}	—	1.113	1.682	1.913	1.881	1.696	1.625	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.082	3.594	4.050	4.292	4.004	4.456	ns
		GCLK PLL	t_{CO}	—	1.115	1.685	1.917	1.885	1.700	1.629	ns

Table 1–81. EP3SE50 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.081	3.597	4.054	4.296	4.007	4.459	ns
		GCLK PLL	t_{CO}	—	1.114	1.688	1.921	1.889	1.703	1.632	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.090	3.595	4.047	4.289	4.004	4.456	ns
		GCLK PLL	t_{CO}	—	1.123	1.686	1.914	1.882	1.700	1.629	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.101	3.601	4.058	4.300	4.010	4.462	ns
		GCLK PLL	t_{CO}	—	1.134	1.692	1.925	1.893	1.706	1.635	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.095	3.604	4.063	4.305	4.014	4.466	ns
		GCLK PLL	t_{CO}	—	1.128	1.695	1.930	1.898	1.710	1.639	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.087	3.595	4.053	4.295	4.005	4.457	ns
		GCLK PLL	t_{CO}	—	1.120	1.686	1.920	1.888	1.701	1.630	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.104	3.617	4.082	4.324	4.027	4.479	ns
		GCLK PLL	t_{CO}	—	1.137	1.708	1.949	1.917	1.723	1.652	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.092	3.607	4.069	4.311	4.016	4.468	ns
		GCLK PLL	t_{CO}	—	1.125	1.698	1.936	1.904	1.712	1.641	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.095	3.619	4.083	4.325	4.029	4.481	ns
		GCLK PLL	t_{CO}	—	1.128	1.710	1.950	1.918	1.725	1.654	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.046	4.940	5.594	5.836	5.388	5.839	ns
		GCLK PLL	t_{CO}	—	2.080	3.034	3.464	3.432	3.087	3.015	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.046	4.940	5.594	5.836	5.388	5.839	ns
		GCLK PLL	t_{CO}	—	2.080	3.034	3.464	3.432	3.087	3.015	ns

Table 1–82 through Table 1–85 show the maximum I/O timing parameters for EP3SE50 devices for differential I/O standards.

Table 1–82 specifies EP3SE50 Column Pins Input Timing parameters for differential I/O standards.

Table 1–82. EP3SE50 Column Pins Input Timing Parameters (Part 1 of 2)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.364	-0.747	-0.761	-0.828	-0.793	-1.364	ns
		t_H	—	0.436	0.891	0.929	1.022	0.974	1.532	ns
	GCLK PLL	t_{SU}	—	0.604	1.162	1.373	1.581	1.512	1.465	ns
		t_H	—	-0.532	-1.018	-1.205	-1.387	-1.331	-1.297	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.364	-0.747	-0.761	-0.828	-0.793	-1.364	ns
		t_H	—	0.436	0.891	0.929	1.022	0.974	1.532	ns
	GCLK PLL	t_{SU}	—	0.604	1.162	1.373	1.581	1.512	1.465	ns
		t_H	—	-0.532	-1.018	-1.205	-1.387	-1.331	-1.297	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.371	-0.762	-0.777	-0.844	-0.809	-1.380	ns
		t_H	—	0.443	0.905	0.945	1.038	0.990	1.548	ns
	GCLK PLL	t_{SU}	—	0.597	1.147	1.357	1.565	1.496	1.449	ns
		t_H	—	-0.525	-1.004	-1.189	-1.371	-1.315	-1.281	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.371	-0.762	-0.777	-0.844	-0.809	-1.380	ns
		t_H	—	0.443	0.905	0.945	1.038	0.990	1.548	ns
	GCLK PLL	t_{SU}	—	0.597	1.147	1.357	1.565	1.496	1.449	ns
		t_H	—	-0.525	-1.004	-1.189	-1.371	-1.315	-1.281	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.385	-0.789	-0.809	-0.877	-0.842	-1.412	ns
		t_H	—	0.456	0.932	0.977	1.070	1.022	1.580	ns
	GCLK PLL	t_{SU}	—	0.583	1.120	1.325	1.532	1.463	1.417	ns
		t_H	—	-0.512	-0.977	-1.157	-1.339	-1.283	-1.249	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.385	-0.789	-0.809	-0.877	-0.842	-1.412	ns
		t_H	—	0.456	0.932	0.977	1.070	1.022	1.580	ns
	GCLK PLL	t_{SU}	—	0.583	1.120	1.325	1.532	1.463	1.417	ns
		t_H	—	-0.512	-0.977	-1.157	-1.339	-1.283	-1.249	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.371	-0.762	-0.777	-0.844	-0.809	-1.380	ns
		t_H	—	0.443	0.905	0.945	1.038	0.990	1.548	ns
	GCLK PLL	t_{SU}	—	0.597	1.147	1.357	1.565	1.496	1.449	ns
		t_H		-0.525	-1.004	-1.189	-1.371	-1.315	-1.281	ns

Table 1–82. EP3SE50 Column Pins Input Timing Parameters (Part 2 of 2)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.371	-0.762	-0.777	-0.844	-0.809	-1.380	ns
		t_H	—	0.443	0.905	0.945	1.038	0.990	1.548	ns
	GCLK PLL	t_{SU}	—	0.597	1.147	1.357	1.565	1.496	1.449	ns
		t_H	—	-0.525	-1.004	-1.189	-1.371	-1.315	-1.281	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.385	-0.789	-0.809	-0.877	-0.842	-1.412	ns
		t_H	—	0.456	0.932	0.977	1.070	1.022	1.580	ns
	GCLK PLL	t_{SU}	—	0.583	1.120	1.325	1.532	1.463	1.417	ns
		t_H	—	-0.512	-0.977	-1.157	-1.339	-1.283	-1.249	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.385	-0.789	-0.809	-0.877	-0.842	-1.412	ns
		t_H	—	0.456	0.932	0.977	1.070	1.022	1.580	ns
	GCLK PLL	t_{SU}	—	0.583	1.120	1.325	1.532	1.463	1.417	ns
		t_H	—	-0.512	-0.977	-1.157	-1.339	-1.283	-1.249	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.409	-0.840	-0.869	-0.936	-0.901	-1.472	ns
		t_H	—	0.479	0.980	1.032	1.125	1.078	1.635	ns
	GCLK PLL	t_{SU}	—	0.559	1.069	1.265	1.473	1.404	1.357	ns
		t_H	—	-0.489	-0.929	-1.102	-1.284	-1.227	-1.194	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.409	-0.840	-0.869	-0.936	-0.901	-1.472	ns
		t_H	—	0.479	0.980	1.032	1.125	1.078	1.635	ns
	GCLK PLL	t_{SU}	—	0.559	1.069	1.265	1.473	1.404	1.357	ns
		t_H	—	-0.489	-0.929	-1.102	-1.284	-1.227	-1.194	ns

Table 1–83 specifies EP3SE50 Row Pins Input Timing parameters for differential I/O standards.

Table 1–83. EP3SE50 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.395	-0.809	-0.837	-0.899	-0.866	-1.407	ns
		t_H	—	0.466	0.951	1.004	1.092	1.046	1.574	ns
	GCLK PLL	t_{SU}	—	0.589	1.134	1.334	1.555	1.479	1.460	ns
		t_H	—	-0.517	-0.988	-1.164	-1.356	-1.294	-1.290	ns
MINI-LVDS	GCLK	t_{SU}	—	-0.395	-0.809	-0.837	-0.899	-0.866	-1.407	ns
		t_H	—	0.466	0.951	1.004	1.092	1.046	1.574	ns
	GCLK PLL	t_{SU}	—	0.589	1.134	1.334	1.555	1.479	1.460	ns
		t_H	—	-0.517	-0.988	-1.164	-1.356	-1.294	-1.290	ns
RSDS	GCLK	t_{SU}	—	-0.395	-0.809	-0.837	-0.899	-0.866	-1.407	ns
		t_H	—	0.466	0.951	1.004	1.092	1.046	1.574	ns
	GCLK PLL	t_{SU}	—	0.589	1.134	1.334	1.555	1.479	1.460	ns
		t_H	—	-0.517	-0.988	-1.164	-1.356	-1.294	-1.290	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.319	-0.655	-0.659	-0.719	-0.687	-1.229	ns
		t_H	—	0.391	0.799	0.827	0.913	0.868	1.397	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.611	1.836	1.758	1.737	ns
		t_H	—	-0.634	-1.224	-1.440	-1.635	-1.571	-1.566	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.319	-0.655	-0.659	-0.719	-0.687	-1.229	ns
		t_H	—	0.391	0.799	0.827	0.913	0.868	1.397	ns
	GCLK PLL	t_{SU}	—	0.707	1.373	1.611	1.836	1.758	1.737	ns
		t_H	—	-0.634	-1.224	-1.440	-1.635	-1.571	-1.566	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.326	-0.670	-0.675	-0.735	-0.703	-1.245	ns
		t_H	—	0.398	0.813	0.843	0.929	0.884	1.413	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.326	-0.670	-0.675	-0.735	-0.703	-1.245	ns
		t_H	—	0.398	0.813	0.843	0.929	0.884	1.413	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns

Table 1–83. EP3SE50 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.340	-0.697	-0.707	-0.768	-0.736	-1.277	ns
		t_H	—	0.411	0.840	0.875	0.961	0.916	1.445	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.340	-0.697	-0.707	-0.768	-0.736	-1.277	ns
		t_H	—	0.411	0.840	0.875	0.961	0.916	1.445	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.326	-0.670	-0.675	-0.735	-0.703	-1.245	ns
		t_H	—	0.398	0.813	0.843	0.929	0.884	1.413	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.326	-0.670	-0.675	-0.735	-0.703	-1.245	ns
		t_H	—	0.398	0.813	0.843	0.929	0.884	1.413	ns
	GCLK PLL	t_{SU}	—	0.700	1.359	1.595	1.819	1.742	1.721	ns
		t_H	—	-0.627	-1.210	-1.423	-1.618	-1.555	-1.549	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.340	-0.697	-0.707	-0.768	-0.736	-1.277	ns
		t_H	—	0.411	0.840	0.875	0.961	0.916	1.445	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.340	-0.697	-0.707	-0.768	-0.736	-1.277	ns
		t_H	—	0.411	0.840	0.875	0.961	0.916	1.445	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.563	1.787	1.709	1.689	ns
		t_H	—	-0.613	-1.183	-1.392	-1.586	-1.523	-1.518	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.364	-0.748	-0.767	-0.827	-0.795	-1.337	ns
		t_H	—	0.434	0.888	0.930	1.016	0.972	1.500	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.453	1.676	1.599	1.579	ns
		t_H	—	-0.569	-1.093	-1.285	-1.480	-1.418	-1.411	ns

Table 1–83. EP3SE50 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.364	-0.748	-0.767	-0.827	-0.795	-1.337	ns
		t_H	—	0.434	0.888	0.930	1.016	0.972	1.500	ns
	GCLK PLL	t_{SU}	—	0.641	1.236	1.453	1.676	1.599	1.579	ns
		t_H	—	-0.569	-1.093	-1.285	-1.480	-1.418	-1.411	ns

Table 1–84 specifies EP3SE50 Column Pins Output Timing parameters for differential I/O standards.

Table 1–84. EP3SE50 Column Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.024	3.948	4.469	4.740	4.599	5.061	ns
		GCLK PLL	t_{CO}	—	1.061	2.050	2.349	2.344	2.308	2.252	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.952	3.801	4.296	4.565	4.426	4.888	ns
		GCLK PLL	t_{CO}	—	0.989	1.903	2.176	2.169	2.135	2.079	ns

Table 1–84. EP3SE50 Column Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.944	3.786	4.278	4.547	4.408	4.870	ns
		GCLK PLL	t_{CO}	—	0.981	1.888	2.158	2.151	2.117	2.061	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.944	3.786	4.278	4.547	4.408	4.870	ns
		GCLK PLL	t_{CO}	—	0.981	1.888	2.158	2.151	2.117	2.061	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.945	3.788	4.280	4.549	4.410	4.872	ns
		GCLK PLL	t_{CO}	—	0.982	1.890	2.160	2.153	2.119	2.063	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.944	3.785	4.277	4.546	4.407	4.869	ns
		GCLK PLL	t_{CO}	—	0.981	1.887	2.157	2.150	2.116	2.060	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.941	3.779	4.270	4.539	4.400	4.862	ns
		GCLK PLL	t_{CO}	—	0.978	1.881	2.150	2.143	2.109	2.053	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.940	3.777	4.267	4.536	4.397	4.859	ns
		GCLK PLL	t_{CO}	—	0.977	1.879	2.147	2.140	2.106	2.050	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.941	3.779	4.270	4.539	4.400	4.862	ns
		GCLK PLL	t_{CO}	—	0.978	1.881	2.150	2.143	2.109	2.053	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.936	3.769	4.258	4.527	4.388	4.850	ns
		GCLK PLL	t_{CO}	—	0.973	1.871	2.138	2.131	2.097	2.041	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.933	3.764	4.252	4.521	4.382	4.844	ns
		GCLK PLL	t_{CO}	—	0.970	1.866	2.132	2.125	2.091	2.035	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.939	3.776	4.266	4.535	4.396	4.858	ns
		GCLK PLL	t_{CO}	—	0.976	1.878	2.146	2.139	2.105	2.049	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.927	3.751	4.237	4.505	4.366	4.829	ns
		GCLK PLL	t_{CO}	—	0.964	1.853	2.117	2.109	2.075	2.020	ns

Table 1–84. EP3SE50 Column Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.934	3.766	4.254	4.523	4.384	4.846	ns
		GCLK PLL	t_{CO}	—	0.971	1.868	2.134	2.127	2.093	2.037	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.929	3.756	4.243	4.511	4.372	4.835	ns
		GCLK PLL	t_{CO}	—	0.966	1.858	2.123	2.115	2.081	2.026	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.933	3.763	4.251	4.520	4.381	4.843	ns
		GCLK PLL	t_{CO}	—	0.970	1.865	2.131	2.124	2.090	2.034	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.931	3.760	4.247	4.516	4.377	4.839	ns
		GCLK PLL	t_{CO}	—	0.968	1.862	2.127	2.120	2.086	2.030	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.930	3.758	4.245	4.514	4.375	4.837	ns
		GCLK PLL	t_{CO}	—	0.967	1.860	2.125	2.118	2.084	2.028	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.923	3.743	4.227	4.496	4.357	4.819	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.107	2.100	2.066	2.010	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.949	3.796	4.290	4.559	4.420	4.882	ns
		GCLK PLL	t_{CO}	—	0.986	1.898	2.170	2.163	2.129	2.073	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.944	3.786	4.278	4.547	4.408	4.870	ns
		GCLK PLL	t_{CO}	—	0.981	1.888	2.158	2.151	2.117	2.061	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.941	3.780	4.271	4.540	4.401	4.863	ns
		GCLK PLL	t_{CO}	—	0.978	1.882	2.151	2.144	2.110	2.054	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.944	3.786	4.278	4.547	4.408	4.870	ns
		GCLK PLL	t_{CO}	—	0.981	1.888	2.158	2.151	2.117	2.061	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.942	3.782	4.273	4.542	4.403	4.865	ns
		GCLK PLL	t_{CO}	—	0.979	1.884	2.153	2.146	2.112	2.056	ns

Table 1–84. EP3SE50 Column Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.934	3.765	4.253	4.522	4.383	4.845	ns
		GCLK PLL	t_{CO}	—	0.971	1.867	2.133	2.126	2.092	2.036	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.936	3.770	4.259	4.528	4.389	4.851	ns
		GCLK PLL	t_{CO}	—	0.973	1.872	2.139	2.132	2.098	2.042	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.947	3.791	4.284	4.553	4.414	4.876	ns
		GCLK PLL	t_{CO}	—	0.984	1.893	2.164	2.157	2.123	2.067	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.940	3.777	4.267	4.536	4.397	4.859	ns
		GCLK PLL	t_{CO}	—	0.977	1.879	2.147	2.140	2.106	2.050	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.942	3.781	4.272	4.541	4.402	4.864	ns
		GCLK PLL	t_{CO}	—	0.979	1.883	2.152	2.145	2.111	2.055	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.940	3.778	4.269	4.537	4.399	4.861	ns
		GCLK PLL	t_{CO}	—	0.977	1.880	2.149	2.141	2.108	2.052	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.937	3.771	4.260	4.529	4.390	4.852	ns
		GCLK PLL	t_{CO}	—	0.974	1.873	2.140	2.133	2.099	2.043	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.931	3.760	4.247	4.516	4.377	4.839	ns
		GCLK PLL	t_{CO}	—	0.968	1.862	2.127	2.120	2.086	2.030	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.934	3.766	4.254	4.523	4.384	4.846	ns
		GCLK PLL	t_{CO}	—	0.971	1.868	2.134	2.127	2.093	2.037	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.938	3.773	4.263	4.532	4.393	4.855	ns
		GCLK PLL	t_{CO}	—	0.975	1.875	2.143	2.136	2.102	2.046	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.937	3.771	4.260	4.529	4.390	4.852	ns
		GCLK PLL	t_{CO}	—	0.974	1.873	2.140	2.133	2.099	2.043	ns

Table 1–84. EP3SE50 Column Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.935	3.767	4.256	4.524	4.385	4.848	ns
		GCLK PLL	t_{CO}	—	0.972	1.869	2.136	2.128	2.094	2.039	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.933	3.764	4.252	4.521	4.382	4.844	ns
		GCLK PLL	t_{CO}	—	0.970	1.866	2.132	2.125	2.091	2.035	ns

Table 1–85 specifies EP3SE50 Row Pins Output Timing parameters for differential I/O standards.

Table 1–85. EP3SE50 Row Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	t_{CO}	—	1.990	3.883	4.396	4.661	4.524	4.967	ns
		GCLK PLL	t_{CO}	—	1.023	1.972	2.263	2.253	2.219	2.137	ns
LVDS_E_1R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns
MINI-LVDS	-	GCLK	t_{CO}	—	1.990	3.883	4.396	4.661	4.524	4.967	ns
		GCLK PLL	t_{CO}	—	1.023	1.972	2.263	2.253	2.219	2.137	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns

Table 1–85. EP3SE50 Row Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
RSDS	-	GCLK	t_{CO}	—	1.990	3.883	4.396	4.661	4.524	4.967	ns
		GCLK PLL	t_{CO}	—	1.023	1.972	2.263	2.253	2.219	2.137	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	1.989	3.881	4.394	4.658	4.521	4.965	ns
		GCLK PLL	t_{CO}	—	1.022	1.970	2.261	2.250	2.216	2.135	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.926	3.754	4.243	4.506	4.371	4.814	ns
		GCLK PLL	t_{CO}	—	0.959	1.843	2.110	2.098	2.066	1.984	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.918	3.737	4.224	4.487	4.351	4.795	ns
		GCLK PLL	t_{CO}	—	0.951	1.826	2.091	2.079	2.046	1.965	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.917	3.734	4.221	4.483	4.348	4.792	ns
		GCLK PLL	t_{CO}	—	0.950	1.823	2.088	2.075	2.043	1.962	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.916	3.732	4.218	4.481	4.346	4.789	ns
		GCLK PLL	t_{CO}	—	0.949	1.821	2.085	2.073	2.041	1.959	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.915	3.730	4.216	4.478	4.343	4.787	ns
		GCLK PLL	t_{CO}	—	0.948	1.819	2.083	2.070	2.038	1.957	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.910	3.720	4.204	4.466	4.331	4.775	ns
		GCLK PLL	t_{CO}	—	0.943	1.809	2.071	2.058	2.026	1.945	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	1.910	3.720	4.204	4.466	4.331	4.775	ns
		GCLK PLL	t_{CO}	—	0.943	1.809	2.071	2.058	2.026	1.945	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	1.904	3.709	4.191	4.453	4.318	4.762	ns
		GCLK PLL	t_{CO}	—	0.937	1.798	2.058	2.045	2.013	1.932	ns

Table 1–85. EP3SE50 Row Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	1.906	3.712	4.195	4.457	4.322	4.766	ns
		GCLK PLL	t_{CO}	—	0.939	1.801	2.062	2.049	2.017	1.936	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	1.905	3.711	4.194	4.455	4.321	4.765	ns
		GCLK PLL	t_{CO}	—	0.938	1.800	2.061	2.047	2.016	1.935	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	1.903	3.707	4.189	4.451	4.316	4.760	ns
		GCLK PLL	t_{CO}	—	0.936	1.796	2.056	2.043	2.011	1.930	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	1.894	3.689	4.168	4.429	4.294	4.739	ns
		GCLK PLL	t_{CO}	—	0.927	1.778	2.035	2.021	1.989	1.909	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.926	3.753	4.242	4.505	4.369	4.813	ns
		GCLK PLL	t_{CO}	—	0.959	1.842	2.109	2.097	2.064	1.983	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.919	3.738	4.226	4.488	4.353	4.797	ns
		GCLK PLL	t_{CO}	—	0.952	1.827	2.093	2.080	2.048	1.967	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.915	3.730	4.216	4.478	4.343	4.787	ns
		GCLK PLL	t_{CO}	—	0.948	1.819	2.083	2.070	2.038	1.957	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	1.922	3.745	4.233	4.495	4.360	4.804	ns
		GCLK PLL	t_{CO}	—	0.955	1.834	2.100	2.087	2.055	1.974	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	1.915	3.731	4.217	4.479	4.344	4.788	ns
		GCLK PLL	t_{CO}	—	0.948	1.820	2.084	2.071	2.039	1.958	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.915	3.731	4.217	4.479	4.344	4.788	ns
		GCLK PLL	t_{CO}	—	0.948	1.820	2.084	2.071	2.039	1.958	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	1.914	3.729	4.215	4.477	4.342	4.786	ns
		GCLK PLL	t_{CO}	—	0.947	1.818	2.082	2.069	2.037	1.956	ns

Table 1–85. EP3SE50 Row Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.910	3.721	4.205	4.467	4.332	4.776	ns
		GCLK PLL	t_{CO}	—	0.943	1.810	2.072	2.059	2.027	1.946	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	1.905	3.711	4.194	4.455	4.321	4.765	ns
		GCLK PLL	t_{CO}	—	0.938	1.800	2.061	2.047	2.016	1.935	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.906	3.713	4.196	4.458	4.323	4.767	ns
		GCLK PLL	t_{CO}	—	0.939	1.802	2.063	2.050	2.018	1.937	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	1.914	3.728	4.214	4.476	4.341	4.785	ns
		GCLK PLL	t_{CO}	—	0.947	1.817	2.081	2.068	2.036	1.955	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	1.910	3.720	4.204	4.466	4.331	4.775	ns
		GCLK PLL	t_{CO}	—	0.943	1.809	2.071	2.058	2.026	1.945	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	1.906	3.713	4.196	4.458	4.323	4.767	ns
		GCLK PLL	t_{CO}	—	0.939	1.802	2.063	2.050	2.018	1.937	ns

Table 1–86 through Table 1–87 show EP3SE50 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–86 specifies EP3SE50 Column Pin delay adders when using the Regional Clock in Stratix III devices.

Table 1–86. EP3SE50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.096	0.194	0.209	0.225	0.218	0.302	ns
RCLK PLL input adder	—	0.006	0.014	-0.001	-0.019	-0.006	-0.006	ns

Table 1–86. EP3SE50 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK output adder	—	-0.085	-0.169	-0.183	-0.198	-0.192	-0.271	ns
RCLK PLL output adder	—	0.454	0.968	1.187	1.164	1.051	1.532	ns

Table 1–87 specifies EP3SE50 Row Pin delay adders when using the Regional Clock in Stratix III devices.

Table 1–87. EP3SE50 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.083	0.167	0.18	0.195	0.188	0.259	ns
RCLK PLL input adder	—	-0.005	-0.01	-0.025	-0.045	-0.034	-0.043	ns
RCLK output adder	—	-0.083	-0.167	-0.18	-0.195	-0.188	-0.259	ns
RCLK PLL output adder	—	0.005	0.01	0.025	0.045	0.034	0.043	ns

EP3SE110 I/O Timing Parameters

Table 1–88 through Table 1–91 show the maximum I/O timing parameters for EP3SE110 for single ended I/O standards.

Table 1–88 specifies EP3SE110 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–88. EP3SE110 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.652	-1.335	-1.423	-1.525	-1.469	-2.158	ns
		t_H	—	0.721	1.473	1.583	1.711	1.643	2.318	ns
	GCLK PLL	t_{SU}	—	0.463	0.876	1.063	1.307	1.216	1.196	ns
		t_H	—	-0.394	-0.738	-0.903	-1.121	-1.042	-1.036	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.652	-1.335	-1.423	-1.525	-1.469	-2.158	ns
		t_H	—	0.721	1.473	1.583	1.711	1.643	2.318	ns
	GCLK PLL	t_{SU}	—	0.463	0.876	1.063	1.307	1.216	1.196	ns
		t_H	—	-0.394	-0.738	-0.903	-1.121	-1.042	-1.036	ns
2.5 V	GCLK	t_{SU}	—	-0.657	-1.346	-1.435	-1.537	-1.481	-2.170	ns
		t_H	—	0.726	1.483	1.595	1.723	1.655	2.330	ns
	GCLK PLL	t_{SU}	—	0.458	0.865	1.051	1.295	1.204	1.184	ns
		t_H	—	-0.389	-0.728	-0.891	-1.109	-1.030	-1.024	ns
1.8 V	GCLK	t_{SU}	—	-0.667	-1.366	-1.459	-1.561	-1.505	-2.194	ns
		t_H	—	0.736	1.503	1.618	1.747	1.678	2.353	ns
	GCLK PLL	t_{SU}	—	0.448	0.845	1.027	1.271	1.180	1.160	ns
		t_H	—	-0.379	-0.708	-0.868	-1.085	-1.007	-1.001	ns
1.5 V	GCLK	t_{SU}	—	-0.647	-1.325	-1.412	-1.513	-1.457	-2.147	ns
		t_H	—	0.716	1.463	1.572	1.699	1.631	2.307	ns
	GCLK PLL	t_{SU}	—	0.468	0.886	1.074	1.319	1.228	1.207	ns
		t_H	—	-0.399	-0.748	-0.914	-1.133	-1.054	-1.047	ns
1.2 V	GCLK	t_{SU}	—	-0.590	-1.211	-1.278	-1.378	-1.322	-2.013	ns
		t_H	—	0.660	1.349	1.439	1.565	1.498	2.174	ns
	GCLK PLL	t_{SU}	—	0.525	1.000	1.208	1.454	1.363	1.341	ns
		t_H	—	-0.455	-0.862	-1.047	-1.267	-1.187	-1.180	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.530	-1.088	-1.135	-1.233	-1.178	-1.870	ns
		t_H	—	0.600	1.228	1.298	1.422	1.355	2.033	ns
	GCLK PLL	t_{SU}	—	0.585	1.123	1.351	1.599	1.507	1.484	ns
		t_H	—	-0.515	-0.983	-1.188	-1.410	-1.330	-1.321	ns

Table 1–88. EP3SE110 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.530	-1.088	-1.135	-1.233	-1.178	-1.870	ns
		t_H	—	0.600	1.228	1.298	1.422	1.355	2.033	ns
	GCLK PLL	t_{SU}	—	0.585	1.123	1.351	1.599	1.507	1.484	ns
		t_H	—	-0.515	-0.983	-1.188	-1.410	-1.330	-1.321	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.174	-1.119	-1.810	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.411	1.658	1.566	1.978	ns
		t_H	—	-0.538	-1.031	-1.243	-1.465	-1.386	1.544	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.174	-1.119	-1.376	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.411	1.658	1.566	-1.810	ns
		t_H	—	-0.538	-1.031	-1.243	-1.465	-1.386	1.978	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.141	-1.086	1.978	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.443	1.691	1.599	1.544	ns
		t_H	—	-0.551	-1.058	-1.275	-1.497	-1.418	-1.376	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.141	-1.086	-1.778	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.443	1.691	1.599	1.946	ns
		t_H	—	-0.551	-1.058	-1.275	-1.497	-1.418	1.576	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.174	-1.119	1.576	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.411	1.658	1.566	-1.408	ns
		t_H	—	-0.538	-1.031	-1.243	-1.465	-1.386	-1.778	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.174	-1.119	1.978	ns
	GCLK PLL	t_{SU}	—	0.609	1.174	1.411	1.658	1.566	1.544	ns
		t_H	—	-0.538	-1.031	-1.243	-1.465	-1.386	-1.376	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.141	-1.086	-1.810	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.443	1.691	1.599	1.978	ns
		t_H	—	-0.551	-1.058	-1.275	-1.497	-1.418	1.544	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.141	-1.086	-1.376	ns
	GCLK PLL	t_{SU}	—	0.623	1.201	1.443	1.691	1.599	-1.810	ns
		t_H	—	-0.551	-1.058	-1.275	-1.497	-1.418	1.978	ns

Table 1–88. EP3SE110 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.485	-0.995	-1.027	-1.125	-1.070	1.544	ns
	GCLK PLL	t_{SU}	—	0.630	1.216	1.459	1.707	1.615	-1.376	ns
		t_{H}	—	-0.558	-1.072	-1.291	-1.513	-1.434	-1.778	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.485	-0.995	-1.027	-1.125	-1.070	1.946	ns
	GCLK PLL	t_{SU}	—	0.630	1.216	1.459	1.707	1.615	1.576	ns
		t_{H}	—	-0.558	-1.072	-1.291	-1.513	-1.434	-1.408	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.652	-1.335	-1.423	-1.525	-1.469	-1.778	ns
		t_{H}	—	0.721	1.473	1.583	1.711	1.643	1.946	ns
	GCLK PLL	t_{SU}	—	0.463	0.876	1.063	1.307	1.216	1.576	ns
		t_{H}	—	-0.394	-0.738	-0.903	-1.121	-1.042	-1.408	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.652	-1.335	-1.423	-1.525	-1.469	-1.778	ns
		t_{H}	—	0.721	1.473	1.583	1.711	1.643	1.946	ns
	GCLK PLL	t_{SU}	—	0.463	0.876	1.063	1.307	1.216	1.576	ns
		t_{H}	—	-0.394	-0.738	-0.903	-1.121	-1.042	-1.408	ns

Table 1–89 specifies EP3SE110 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–89. EP3SE110 Row Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.582	-1.195	-1.264	-1.341	-1.301	-1.958	ns
		t_{H}	—	0.653	1.336	1.429	1.533	1.479	2.123	ns
	GCLK PLL	t_{SU}	—	0.546	1.044	1.252	1.515	1.417	1.423	ns
		t_{H}	—	-0.475	-0.903	-1.087	-1.323	-1.239	-1.258	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.582	-1.195	-1.264	-1.341	-1.301	-1.958	ns
		t_{H}	—	0.653	1.336	1.429	1.533	1.479	2.123	ns
	GCLK PLL	t_{SU}	—	0.546	1.044	1.252	1.515	1.417	1.423	ns
		t_{H}	—	-0.475	-0.903	-1.087	-1.323	-1.239	-1.258	ns

Table 1–89. EP3SE110 Row Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	GCLK	t_{SU}	—	-0.587	-1.205	-1.275	-1.353	-1.313	-1.969	ns
		t_H	—	0.658	1.346	1.441	1.545	1.491	2.135	ns
	GCLK PLL	t_{SU}	—	0.541	1.034	1.241	1.503	1.405	1.412	ns
		t_H	—	-0.470	-0.893	-1.075	-1.311	-1.227	-1.246	ns
1.8 V	GCLK	t_{SU}	—	-0.597	-1.225	-1.299	-1.377	-1.336	-1.993	ns
		t_H	—	0.668	1.366	1.464	1.569	1.514	2.158	ns
	GCLK PLL	t_{SU}	—	0.531	1.014	1.217	1.479	1.382	1.388	ns
		t_H	—	-0.460	-0.873	-1.052	-1.287	-1.204	-1.223	ns
1.5 V	GCLK	t_{SU}	—	-0.576	-1.184	-1.251	-1.328	-1.288	-1.945	ns
		t_H	—	0.647	1.325	1.416	1.520	1.466	2.110	ns
	GCLK PLL	t_{SU}	—	0.552	1.055	1.265	1.528	1.430	1.436	ns
		t_H	—	-0.481	-0.914	-1.100	-1.336	-1.252	-1.271	ns
1.2 V	GCLK	t_{SU}	—	-0.519	-1.067	-1.115	-1.190	-1.151	-1.809	ns
		t_H	—	0.590	1.209	1.281	1.384	1.331	1.975	ns
	GCLK PLL	t_{SU}	—	0.609	1.172	1.401	1.666	1.567	1.572	ns
		t_H	—	-0.538	-1.030	-1.235	-1.472	-1.387	-1.406	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.456	-0.939	-0.966	-1.039	-1.001	-1.660	ns
		t_H	—	0.528	1.082	1.134	1.235	1.182	1.828	ns
	GCLK PLL	t_{SU}	—	0.672	1.300	1.550	1.817	1.717	1.721	ns
		t_H	—	-0.600	-1.157	-1.382	-1.621	-1.536	-1.553	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.456	-0.939	-0.966	-1.039	-1.001	-1.660	ns
		t_H	—	0.528	1.082	1.134	1.235	1.182	1.828	ns
	GCLK PLL	t_{SU}	—	0.672	1.300	1.550	1.817	1.717	1.721	ns
		t_H	—	-0.600	-1.157	-1.382	-1.621	-1.536	-1.553	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.411	-0.844	-0.856	-0.928	-0.891	-1.550	ns
		t_H	—	0.484	0.992	1.027	1.129	1.077	1.721	ns
	GCLK PLL	t_{SU}	—	0.717	1.395	1.660	1.928	1.827	1.831	ns
		t_H	—	-0.644	-1.247	-1.489	-1.727	-1.641	-1.660	ns

Table 1–89. EP3SE110 Row Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.411	-0.844	-0.856	-0.928	-0.891	-1.550	ns
		t_H	—	0.484	0.992	1.027	1.129	1.077	1.721	ns
	GCLK PLL	t_{SU}	—	0.717	1.395	1.660	1.928	1.827	1.831	ns
		t_H	—	-0.644	-1.247	-1.489	-1.727	-1.641	-1.660	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.397	-0.816	-0.824	-0.896	-0.858	-1.518	ns
		t_H	—	0.470	0.965	0.996	1.097	1.045	1.690	ns
	GCLK PLL	t_{SU}	—	0.731	1.423	1.692	1.960	1.860	1.863	ns
		t_H	—	-0.658	-1.274	-1.520	-1.759	-1.673	-1.691	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.397	-0.816	-0.824	-0.896	-0.858	-1.518	ns
		t_H	—	0.470	0.965	0.996	1.097	1.045	1.690	ns
	GCLK PLL	t_{SU}	—	0.731	1.423	1.692	1.960	1.860	1.863	ns
		t_H	—	-0.658	-1.274	-1.520	-1.759	-1.673	-1.691	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.411	-0.844	-0.856	-0.928	-0.891	-1.550	ns
		t_H	—	0.484	0.992	1.027	1.129	1.077	1.721	ns
	GCLK PLL	t_{SU}	—	0.717	1.395	1.660	1.928	1.827	1.831	ns
		t_H	—	-0.644	-1.247	-1.489	-1.727	-1.641	-1.660	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.411	-0.844	-0.856	-0.928	-0.891	-1.550	ns
		t_H	—	0.484	0.992	1.027	1.129	1.077	1.721	ns
	GCLK PLL	t_{SU}	—	0.717	1.395	1.660	1.928	1.827	1.831	ns
		t_H	—	-0.644	-1.247	-1.489	-1.727	-1.641	-1.660	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.397	-0.816	-0.824	-0.896	-0.858	-1.518	ns
		t_H	—	0.470	0.965	0.996	1.097	1.045	1.690	ns
	GCLK PLL	t_{SU}	—	0.731	1.423	1.692	1.960	1.860	1.863	ns
		t_H	—	-0.658	-1.274	-1.520	-1.759	-1.673	-1.691	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.397	-0.816	-0.824	-0.896	-0.858	-1.518	ns
		t_H	—	0.470	0.965	0.996	1.097	1.045	1.690	ns
	GCLK PLL	t_{SU}	—	0.731	1.423	1.692	1.960	1.860	1.863	ns
		t_H	—	-0.658	-1.274	-1.520	-1.759	-1.673	-1.691	ns

Table 1–89. EP3SE110 Row Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.390	-0.802	-0.808	-0.879	-0.842	-1.502	ns
		t_H	—	0.463	0.951	0.979	1.080	1.029	1.673	ns
	GCLK PLL	t_{SU}	—	0.738	1.437	1.708	1.977	1.876	1.879	ns
		t_H	—	-0.665	-1.288	-1.537	-1.776	-1.689	-1.708	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.390	-0.802	-0.808	-0.879	-0.842	-1.502	ns
		t_H	—	0.463	0.951	0.979	1.080	1.029	1.673	ns
	GCLK PLL	t_{SU}	—	0.738	1.437	1.708	1.977	1.876	1.879	ns
		t_H	—	-0.665	-1.288	-1.537	-1.776	-1.689	-1.708	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.582	-1.195	-1.264	-1.341	-1.301	-1.958	ns
		t_H	—	0.653	1.336	1.429	1.533	1.479	2.123	ns
	GCLK PLL	t_{SU}	—	0.546	1.044	1.252	1.515	1.417	1.423	ns
		t_H	—	-0.475	-0.903	-1.087	-1.323	-1.239	-1.258	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.582	-1.195	-1.264	-1.341	-1.301	-1.958	ns
		t_H	—	0.653	1.336	1.429	1.533	1.479	2.123	ns
	GCLK PLL	t_{SU}	—	0.546	1.044	1.252	1.515	1.417	1.423	ns
		t_H	—	-0.475	-0.903	-1.087	-1.323	-1.239	-1.258	ns

Table 1–90 specifies EP3SE110 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.547	4.352	4.875	5.145	4.810	5.388	ns
		GCLK PLL	t_{CO}	—	1.451	2.180	2.431	2.367	2.169	2.105	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.695	4.500	5.074	5.344	4.965	5.563	ns
		GCLK PLL	t_{CO}	—	1.599	2.316	2.630	2.566	2.309	2.246	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.755	4.568	5.129	5.399	5.038	5.635	ns
		GCLK PLL	t_{CO}	—	1.659	2.395	2.685	2.621	2.396	2.332	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	2.870	4.735	5.320	5.596	5.210	5.808	ns
		GCLK PLL	t_{CO}	—	1.774	2.559	2.870	2.806	2.561	2.498	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.695	4.500	5.073	5.343	4.965	5.563	ns
		GCLK PLL	t_{CO}	—	1.599	2.316	2.629	2.565	2.309	2.246	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.870	4.735	5.320	5.596	5.210	5.808	ns
		GCLK PLL	t_{CO}	—	1.774	2.559	2.869	2.805	2.561	2.498	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	2.925	4.808	5.380	5.656	5.287	5.884	ns
		GCLK PLL	t_{CO}	—	1.829	2.635	2.934	2.870	2.640	2.576	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	2.978	4.874	5.443	5.719	5.354	5.951	ns
		GCLK PLL	t_{CO}	—	1.882	2.696	2.990	2.926	2.702	2.638	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.633	4.513	5.143	5.413	4.979	5.557	ns
		GCLK PLL	t_{CO}	—	1.537	2.341	2.699	2.635	2.338	2.274	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.672	4.537	5.118	5.388	5.001	5.594	ns
		GCLK PLL	t_{CO}	—	1.576	2.365	2.674	2.610	2.360	2.297	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.920	4.882	5.522	5.798	5.359	5.957	ns
		GCLK PLL	t_{CO}	—	1.824	2.710	3.074	3.010	2.715	2.652	ns
2.5 V	16mA	GCLK	t_{CO}	—	2.953	4.946	5.617	5.893	5.428	6.026	ns
		GCLK PLL	t_{CO}	—	1.857	2.769	3.171	3.107	2.777	2.714	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.535	4.384	4.958	5.228	4.846	5.425	ns
		GCLK PLL	t_{CO}	—	1.439	2.212	2.514	2.450	2.205	2.142	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	4mA	GCLK	t_{CO}	—	2.602	4.501	5.187	5.457	4.965	5.543	ns
		GCLK PLL	t_{CO}	—	1.501	2.329	2.743	2.679	2.324	2.260	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.840	4.799	5.477	5.747	5.269	5.866	ns
		GCLK PLL	t_{CO}	—	1.744	2.627	3.033	2.969	2.628	2.565	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.667	4.548	5.159	5.434	5.014	5.612	ns
		GCLK PLL	t_{CO}	—	1.571	2.374	2.715	2.651	2.368	2.305	ns
1.8 V	10mA	GCLK	t_{CO}	—	2.929	4.911	5.576	5.852	5.392	5.990	ns
		GCLK PLL	t_{CO}	—	1.833	2.736	3.126	3.062	2.740	2.677	ns
1.8 V	12mA	GCLK	t_{CO}	—	3.000	5.054	5.790	6.060	5.535	6.133	ns
		GCLK PLL	t_{CO}	—	1.904	2.882	3.346	3.282	2.892	2.829	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.487	4.268	4.859	5.129	4.732	5.329	ns
		GCLK PLL	t_{CO}	—	1.391	2.074	2.415	2.351	2.065	2.001	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.755	4.706	5.336	5.606	5.180	5.766	ns
		GCLK PLL	t_{CO}	—	1.659	2.534	2.892	2.828	2.539	2.475	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.853	4.812	5.466	5.736	5.284	5.874	ns
		GCLK PLL	t_{CO}	—	1.757	2.640	3.022	2.958	2.643	2.580	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.778	4.670	5.309	5.579	5.140	5.738	ns
		GCLK PLL	t_{CO}	—	1.682	2.496	2.865	2.801	2.497	2.434	ns
1.5 V	10mA	GCLK	t_{CO}	—	2.944	4.960	5.664	5.939	5.438	6.036	ns
		GCLK PLL	t_{CO}	—	1.848	2.783	3.220	3.156	2.787	2.724	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.118	5.297	6.152	6.422	5.775	6.354	ns
		GCLK PLL	t_{CO}	—	2.022	3.125	3.708	3.644	3.134	3.071	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2 V	2mA	GCLK	t_{CO}	—	2.763	4.766	5.564	5.834	5.216	5.795	ns
		GCLK PLL	t_{CO}	—	1.667	2.594	3.120	3.056	2.575	2.512	ns
1.2 V	4mA	GCLK	t_{CO}	—	2.929	4.985	5.746	6.016	5.458	6.037	ns
		GCLK PLL	t_{CO}	—	1.833	2.813	3.302	3.238	2.817	2.754	ns
1.2 V	6mA	GCLK	t_{CO}	—	2.865	4.855	5.579	5.849	5.324	5.912	ns
		GCLK PLL	t_{CO}	—	1.769	2.683	3.135	3.071	2.683	2.620	ns
1.2 V	8mA	GCLK	t_{CO}	—	3.119	5.257	6.086	6.356	5.732	6.312	ns
		GCLK PLL	t_{CO}	—	2.023	3.085	3.642	3.578	3.091	3.028	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.245	3.891	4.368	4.644	4.343	4.941	ns
		GCLK PLL	t_{CO}	—	1.149	1.712	1.911	1.847	1.689	1.626	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.242	3.886	4.363	4.639	4.338	4.936	ns
		GCLK PLL	t_{CO}	—	1.146	1.709	1.907	1.843	1.686	1.623	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.245	3.889	4.363	4.639	4.338	4.936	ns
		GCLK PLL	t_{CO}	—	1.149	1.717	1.916	1.852	1.694	1.631	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.257	3.891	4.367	4.643	4.341	4.939	ns
		GCLK PLL	t_{CO}	—	1.161	1.719	1.916	1.852	1.695	1.632	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.252	3.898	4.379	4.655	4.350	4.948	ns
		GCLK PLL	t_{CO}	—	1.156	1.726	1.928	1.864	1.703	1.640	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.245	3.890	4.368	4.644	4.340	4.938	ns
		GCLK PLL	t_{CO}	—	1.149	1.718	1.919	1.855	1.694	1.631	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.249	3.901	4.384	4.660	4.354	4.952	ns
		GCLK PLL	t_{CO}	—	1.153	1.727	1.931	1.867	1.704	1.641	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.248	3.901	4.381	4.657	4.352	4.950	ns
		GCLK PLL	t_{CO}	—	1.152	1.729	1.933	1.869	1.707	1.644	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.246	3.899	4.379	4.655	4.349	4.947	ns
		GCLK PLL	t_{CO}	—	1.150	1.727	1.931	1.867	1.705	1.642	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.251	3.889	4.362	4.638	4.334	4.932	ns
		GCLK PLL	t_{CO}	—	1.155	1.717	1.915	1.851	1.693	1.630	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.267	3.924	4.400	4.670	4.371	4.957	ns
		GCLK PLL	t_{CO}	—	1.171	1.752	1.956	1.892	1.730	1.667	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.251	3.900	4.379	4.655	4.348	4.946	ns
		GCLK PLL	t_{CO}	—	1.155	1.728	1.932	1.868	1.704	1.641	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.250	3.901	4.386	4.662	4.353	4.951	ns
		GCLK PLL	t_{CO}	—	1.154	1.729	1.934	1.870	1.706	1.643	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.249	3.905	4.384	4.660	4.352	4.950	ns
		GCLK PLL	t_{CO}	—	1.153	1.733	1.938	1.874	1.710	1.647	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.257	3.919	4.403	4.679	4.369	4.967	ns
		GCLK PLL	t_{CO}	—	1.161	1.747	1.954	1.890	1.725	1.662	ns
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.252	3.913	4.394	4.670	4.361	4.959	ns
		GCLK PLL	t_{CO}	—	1.156	1.741	1.947	1.883	1.718	1.655	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.253	3.896	4.371	4.647	4.342	4.939	ns
		GCLK PLL	t_{CO}	—	1.157	1.724	1.925	1.861	1.701	1.638	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.267	3.928	4.407	4.677	4.376	4.960	ns
		GCLK PLL	t_{CO}	—	1.171	1.756	1.963	1.899	1.735	1.672	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.248	3.880	4.358	4.634	4.331	4.929	ns
		GCLK PLL	t_{CO}	—	1.152	1.708	1.906	1.842	1.684	1.621	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.249	3.889	4.370	4.646	4.341	4.939	ns
		GCLK PLL	t_{CO}	—	1.153	1.711	1.910	1.846	1.687	1.624	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.251	3.891	4.368	4.644	4.340	4.938	ns
		GCLK PLL	t_{CO}	—	1.155	1.719	1.918	1.854	1.695	1.632	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.255	3.898	4.371	4.647	4.344	4.941	ns
		GCLK PLL	t_{CO}	—	1.159	1.726	1.926	1.862	1.703	1.640	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.257	3.901	4.379	4.655	4.350	4.948	ns
		GCLK PLL	t_{CO}	—	1.161	1.729	1.929	1.865	1.706	1.643	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.308	3.935	4.403	4.673	4.380	4.959	ns
		GCLK PLL	t_{CO}	—	1.212	1.763	1.959	1.895	1.739	1.676	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.254	3.889	4.367	4.643	4.338	4.936	ns
		GCLK PLL	t_{CO}	—	1.158	1.717	1.917	1.853	1.693	1.630	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.254	3.897	4.381	4.657	4.350	4.948	ns
		GCLK PLL	t_{CO}	—	1.158	1.720	1.922	1.858	1.696	1.633	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.251	3.888	4.370	4.646	4.340	4.938	ns
		GCLK PLL	t_{CO}	—	1.155	1.715	1.915	1.851	1.691	1.628	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.253	3.896	4.371	4.647	4.342	4.939	ns
		GCLK PLL	t_{CO}	—	1.157	1.724	1.925	1.861	1.701	1.638	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.262	3.910	4.390	4.666	4.358	4.956	ns
		GCLK PLL	t_{CO}	—	1.166	1.738	1.941	1.877	1.715	1.652	ns

Table 1–90. EP3SE110 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.286	3.895	4.360	4.630	4.338	4.922	ns
		GCLK PLL	t_{CO}	—	1.190	1.723	1.916	1.852	1.697	1.634	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.265	3.908	4.395	4.671	4.358	4.956	ns
		GCLK PLL	t_{CO}	—	1.169	1.736	1.941	1.877	1.713	1.650	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.259	3.903	4.389	4.665	4.354	4.952	ns
		GCLK PLL	t_{CO}	—	1.163	1.731	1.935	1.871	1.707	1.644	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.269	3.921	4.408	4.684	4.371	4.969	ns
		GCLK PLL	t_{CO}	—	1.173	1.749	1.956	1.892	1.726	1.663	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.265	3.921	4.402	4.678	4.368	4.964	ns
		GCLK PLL	t_{CO}	—	1.169	1.749	1.956	1.892	1.727	1.664	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.265	3.920	4.399	4.675	4.366	4.961	ns
		GCLK PLL	t_{CO}	—	1.169	1.748	1.954	1.890	1.725	1.662	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.318	3.954	4.427	4.697	4.399	4.978	ns
		GCLK PLL	t_{CO}	—	1.222	1.782	1.983	1.919	1.758	1.695	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.243	5.232	5.902	6.178	5.720	6.317	ns
		GCLK PLL	t_{CO}	—	2.147	3.056	3.452	3.388	3.071	3.007	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.243	5.232	5.902	6.178	5.720	6.317	ns
		GCLK PLL	t_{CO}	—	2.147	3.056	3.452	3.388	3.071	3.007	ns

Table 1–91 specifies EP3SE110 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–91. EP3SE110 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.639	4.469	5.024	5.288	4.927	5.494	ns
		GCLK PLL	t_{CO}	—	1.511	2.230	2.508	2.432	2.209	2.113	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.703	4.527	5.114	5.378	4.980	5.548	ns
		GCLK PLL	t_{CO}	—	1.575	2.288	2.598	2.522	2.262	2.167	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.834	4.684	5.260	5.524	5.142	5.709	ns
		GCLK PLL	t_{CO}	—	1.706	2.445	2.744	2.668	2.424	2.328	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.732	4.551	5.124	5.388	5.013	5.580	ns
		GCLK PLL	t_{CO}	—	1.604	2.312	2.608	2.532	2.295	2.199	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	2.874	4.734	5.329	5.593	5.198	5.766	ns
		GCLK PLL	t_{CO}	—	1.746	2.495	2.813	2.737	2.480	2.385	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.736	4.691	5.338	5.602	5.158	5.725	ns
		GCLK PLL	t_{CO}	—	1.608	2.452	2.822	2.746	2.440	2.344	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.730	4.622	5.216	5.480	5.081	5.648	ns
		GCLK PLL	t_{CO}	—	1.602	2.383	2.700	2.624	2.363	2.267	ns
2.5 V	12mA	GCLK	t_{CO}	—	2.935	4.902	5.550	5.814	5.377	5.944	ns
		GCLK PLL	t_{CO}	—	1.807	2.663	3.034	2.958	2.659	2.563	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.740	4.600	5.171	5.435	5.065	5.632	ns
		GCLK PLL	t_{CO}	—	1.612	2.361	2.655	2.579	2.347	2.251	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.771	4.735	5.435	5.699	5.194	5.762	ns
		GCLK PLL	t_{CO}	—	1.643	2.496	2.919	2.843	2.476	2.381	ns

Table 1–91. EP3SE110 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	6mA	GCLK	t_{CO}	—	2.863	4.880	5.602	5.866	5.350	5.918	ns
		GCLK PLL	t_{CO}	—	1.735	2.641	3.086	3.010	2.632	2.537	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.748	4.655	5.275	5.539	5.113	5.680	ns
		GCLK PLL	t_{CO}	—	1.620	2.416	2.759	2.683	2.395	2.299	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.653	4.515	5.106	5.370	4.974	5.541	ns
		GCLK PLL	t_{CO}	—	1.525	2.276	2.590	2.514	2.256	2.160	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.778	4.758	5.415	5.679	5.226	5.793	ns
		GCLK PLL	t_{CO}	—	1.650	2.519	2.899	2.823	2.508	2.412	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.913	4.910	5.625	5.889	5.381	5.949	ns
		GCLK PLL	t_{CO}	—	1.785	2.671	3.109	3.033	2.663	2.568	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.800	4.736	5.400	5.664	5.201	5.769	ns
		GCLK PLL	t_{CO}	—	1.672	2.497	2.884	2.808	2.483	2.388	ns
1.2 V	2mA	GCLK	t_{CO}	—	2.903	5.120	6.036	6.300	5.566	6.134	ns
		GCLK PLL	t_{CO}	—	1.775	2.881	3.520	3.444	2.848	2.753	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.031	5.188	6.027	6.291	5.646	6.214	ns
		GCLK PLL	t_{CO}	—	1.903	2.949	3.511	3.435	2.928	2.833	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.228	3.872	4.345	4.609	4.313	4.881	ns
		GCLK PLL	t_{CO}	—	1.100	1.633	1.829	1.753	1.595	1.500	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.216	3.863	4.336	4.600	4.303	4.871	ns
		GCLK PLL	t_{CO}	—	1.088	1.624	1.820	1.744	1.585	1.490	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.221	3.864	4.336	4.600	4.304	4.872	ns
		GCLK PLL	t_{CO}	—	1.093	1.625	1.820	1.744	1.586	1.491	ns

Table 1–91. EP3SE110 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.230	3.878	4.356	4.620	4.319	4.887	ns
		GCLK PLL	t_{CO}	—	1.102	1.639	1.840	1.764	1.601	1.506	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.218	3.866	4.343	4.607	4.306	4.874	ns
		GCLK PLL	t_{CO}	—	1.090	1.627	1.827	1.751	1.588	1.493	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.218	3.873	4.352	4.616	4.313	4.881	ns
		GCLK PLL	t_{CO}	—	1.090	1.634	1.836	1.760	1.595	1.500	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.210	3.868	4.346	4.610	4.308	4.876	ns
		GCLK PLL	t_{CO}	—	1.082	1.629	1.830	1.754	1.590	1.495	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.208	3.865	4.344	4.608	4.306	4.874	ns
		GCLK PLL	t_{CO}	—	1.080	1.626	1.828	1.752	1.588	1.493	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.213	3.857	4.333	4.597	4.297	4.865	ns
		GCLK PLL	t_{CO}	—	1.085	1.618	1.817	1.741	1.579	1.484	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.215	3.871	4.349	4.613	4.311	4.879	ns
		GCLK PLL	t_{CO}	—	1.087	1.632	1.833	1.757	1.593	1.498	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.230	3.881	4.362	4.626	4.321	4.889	ns
		GCLK PLL	t_{CO}	—	1.102	1.642	1.846	1.770	1.603	1.508	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.219	3.876	4.358	4.622	4.316	4.884	ns
		GCLK PLL	t_{CO}	—	1.091	1.637	1.842	1.766	1.598	1.503	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.211	3.870	4.351	4.615	4.310	4.878	ns
		GCLK PLL	t_{CO}	—	1.083	1.631	1.835	1.759	1.592	1.497	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.225	3.859	4.332	4.596	4.298	4.866	ns
		GCLK PLL	t_{CO}	—	1.097	1.620	1.816	1.740	1.580	1.485	ns

Table 1–91. EP3SE110 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.216	3.858	4.334	4.598	4.298	4.866	ns
		GCLK PLL	t_{CO}	—	1.088	1.619	1.818	1.742	1.580	1.485	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.210	3.857	4.332	4.596	4.296	4.864	ns
		GCLK PLL	t_{CO}	—	1.082	1.618	1.816	1.740	1.578	1.483	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.212	3.860	4.336	4.600	4.300	4.868	ns
		GCLK PLL	t_{CO}	—	1.084	1.621	1.820	1.744	1.582	1.487	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.211	3.863	4.340	4.604	4.303	4.871	ns
		GCLK PLL	t_{CO}	—	1.083	1.624	1.824	1.748	1.585	1.490	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.220	3.861	4.333	4.597	4.300	4.868	ns
		GCLK PLL	t_{CO}	—	1.092	1.622	1.817	1.741	1.582	1.487	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.231	3.867	4.344	4.608	4.306	4.874	ns
		GCLK PLL	t_{CO}	—	1.103	1.628	1.828	1.752	1.588	1.493	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.225	3.870	4.349	4.613	4.310	4.878	ns
		GCLK PLL	t_{CO}	—	1.097	1.631	1.833	1.757	1.592	1.497	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.217	3.861	4.339	4.603	4.301	4.869	ns
		GCLK PLL	t_{CO}	—	1.089	1.622	1.823	1.747	1.583	1.488	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.234	3.883	4.368	4.632	4.323	4.891	ns
		GCLK PLL	t_{CO}	—	1.106	1.644	1.852	1.776	1.605	1.510	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.222	3.873	4.355	4.619	4.312	4.880	ns
		GCLK PLL	t_{CO}	—	1.094	1.634	1.839	1.763	1.594	1.499	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.225	3.885	4.369	4.633	4.325	4.893	ns
		GCLK PLL	t_{CO}	—	1.097	1.646	1.853	1.777	1.607	1.512	ns

Table 1–91. EP3SE110 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI	-	GCLK	t_{CO}	—	3.177	5.209	5.883	6.147	5.687	6.254	ns
		GCLK PLL	t_{CO}	—	2.049	2.970	3.367	3.291	2.969	2.873	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.177	5.209	5.883	6.147	5.687	6.254	ns
		GCLK PLL	t_{CO}	—	2.049	2.970	3.367	3.291	2.969	2.873	ns

Table 1–92 through Table 1–95 show the maximum I/O timing parameters for EP3SE110 devices for differential I/O standards.

Table 1–92 specifies EP3SE110 Column Pins Input Timing parameters for differential I/O standards.

Table 1–92. EP3SE110 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.485	-0.995	-1.027	-1.117	-1.070	-1.753	ns
		t_H	—	0.557	1.139	1.195	1.311	1.251	1.921	ns
	GCLK PLL	t_{SU}	—	0.639	1.233	1.478	1.729	1.636	1.617	ns
		t_H	—	-0.567	-1.089	-1.310	-1.535	-1.455	-1.449	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.485	-0.995	-1.027	-1.117	-1.070	-1.753	ns
		t_H	—	0.557	1.139	1.195	1.311	1.251	1.921	ns
	GCLK PLL	t_{SU}	—	0.639	1.233	1.478	1.729	1.636	1.617	ns
		t_H	—	-0.567	-1.089	-1.310	-1.535	-1.455	-1.449	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.133	-1.086	-1.769	ns
		t_H	—	0.564	1.153	1.211	1.327	1.267	1.937	ns
	GCLK PLL	t_{SU}	—	0.632	1.218	1.462	1.713	1.620	1.601	ns
		t_H	—	-0.560	-1.075	-1.294	-1.519	-1.439	-1.433	ns

Table 1–92. EP3SE110 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.133	-1.086	-1.769	ns
		t_H	—	0.564	1.153	1.211	1.327	1.267	1.937	ns
	GCLK PLL	t_{SU}	—	0.632	1.218	1.462	1.713	1.620	1.601	ns
		t_H	—	-0.560	-1.075	-1.294	-1.519	-1.439	-1.433	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.166	-1.119	-1.801	ns
		t_H	—	0.577	1.180	1.243	1.359	1.299	1.969	ns
	GCLK PLL	t_{SU}	—	0.618	1.191	1.430	1.680	1.587	1.569	ns
		t_H	—	-0.547	-1.048	-1.262	-1.487	-1.407	-1.401	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.166	-1.119	-1.801	ns
		t_H	—	0.577	1.180	1.243	1.359	1.299	1.969	ns
	GCLK PLL	t_{SU}	—	0.618	1.191	1.430	1.680	1.587	1.569	ns
		t_H	—	-0.547	-1.048	-1.262	-1.487	-1.407	-1.401	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.133	-1.086	-1.769	ns
		t_H	—	0.564	1.153	1.211	1.327	1.267	1.937	ns
	GCLK PLL	t_{SU}	—	0.632	1.218	1.462	1.713	1.620	1.601	ns
		t_H	—	-0.560	-1.075	-1.294	-1.519	-1.439	-1.433	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.492	-1.010	-1.043	-1.133	-1.086	-1.769	ns
		t_H	—	0.564	1.153	1.211	1.327	1.267	1.937	ns
	GCLK PLL	t_{SU}	—	0.632	1.218	1.462	1.713	1.620	1.601	ns
		t_H	—	-0.560	-1.075	-1.294	-1.519	-1.439	-1.433	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.166	-1.119	-1.801	ns
		t_H	—	0.577	1.180	1.243	1.359	1.299	1.969	ns
	GCLK PLL	t_{SU}	—	0.618	1.191	1.430	1.680	1.587	1.569	ns
		t_H	—	-0.547	-1.048	-1.262	-1.487	-1.407	-1.401	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.506	-1.037	-1.075	-1.166	-1.119	-1.801	ns
		t_H	—	0.577	1.180	1.243	1.359	1.299	1.969	ns
	GCLK PLL	t_{SU}	—	0.618	1.191	1.430	1.680	1.587	1.569	ns
		t_H	—	-0.547	-1.048	-1.262	-1.487	-1.407	-1.401	ns

Table 1–92. EP3SE110 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.530	-1.088	-1.135	-1.225	-1.178	-1.861	ns
		t_H	—	0.600	1.228	1.298	1.414	1.355	2.024	ns
	GCLK PLL	t_{SU}	—	0.594	1.140	1.370	1.621	1.528	1.509	ns
		t_H	—	-0.524	-1.000	-1.207	-1.432	-1.351	-1.346	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.530	-1.088	-1.135	-1.225	-1.178	-1.861	ns
		t_H	—	0.600	1.228	1.298	1.414	1.355	2.024	ns
	GCLK PLL	t_{SU}	—	0.594	1.140	1.370	1.621	1.528	1.509	ns
		t_H	—	-0.524	-1.000	-1.207	-1.432	-1.351	-1.346	ns

Table 1–93 specifies EP3SE110 Row Pins Input Timing parameters for differential I/O standards

Table 1–93. EP3SE110 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.526	-1.077	-1.126	-1.210	-1.165	-1.822	ns
		t_H	—	0.597	1.219	1.293	1.403	1.345	1.989	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.425	1.689	1.590	1.594	ns
		t_H	—	-0.546	-1.046	-1.255	-1.490	-1.405	-1.424	ns
MINI-LVDS	GCLK	t_{SU}	—	-0.526	-1.077	-1.126	-1.210	-1.165	-1.822	ns
		t_H	—	0.597	1.219	1.293	1.403	1.345	1.989	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.425	1.689	1.590	1.594	ns
		t_H	—	-0.546	-1.046	-1.255	-1.490	-1.405	-1.424	ns
RSDS	GCLK	t_{SU}	—	-0.526	-1.077	-1.126	-1.210	-1.165	-1.822	ns
		t_H	—	0.597	1.219	1.293	1.403	1.345	1.989	ns
	GCLK PLL	t_{SU}	—	0.618	1.192	1.425	1.689	1.590	1.594	ns
		t_H	—	-0.546	-1.046	-1.255	-1.490	-1.405	-1.424	ns

Table 1–93. EP3SE110 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.450	-0.923	-0.948	-1.030	-0.986	-1.644	ns
		t_H	—	0.522	1.067	1.116	1.224	1.167	1.812	ns
	GCLK PLL	t_{SU}	—	0.736	1.431	1.702	1.970	1.869	1.871	ns
		t_H	—	-0.663	-1.282	-1.531	-1.769	-1.682	-1.700	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.450	-0.923	-0.948	-1.030	-0.986	-1.644	ns
		t_H	—	0.522	1.067	1.116	1.224	1.167	1.812	ns
	GCLK PLL	t_{SU}	—	0.736	1.431	1.702	1.970	1.869	1.871	ns
		t_H	—	-0.663	-1.282	-1.531	-1.769	-1.682	-1.700	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.457	-0.938	-0.964	-1.046	-1.002	-1.660	ns
		t_H	—	0.529	1.081	1.132	1.240	1.183	1.828	ns
	GCLK PLL	t_{SU}	—	0.729	1.417	1.686	1.953	1.853	1.855	ns
		t_H	—	-0.656	-1.268	-1.514	-1.752	-1.666	-1.683	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.457	-0.938	-0.964	-1.046	-1.002	-1.660	ns
		t_H	—	0.529	1.081	1.132	1.240	1.183	1.828	ns
	GCLK PLL	t_{SU}	—	0.729	1.417	1.686	1.953	1.853	1.855	ns
		t_H	—	-0.656	-1.268	-1.514	-1.752	-1.666	-1.683	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.471	-0.965	-0.996	-1.079	-1.035	-1.692	ns
		t_H	—	0.542	1.108	1.164	1.272	1.215	1.860	ns
	GCLK PLL	t_{SU}	—	0.715	1.389	1.654	1.921	1.820	1.823	ns
		t_H	—	-0.642	-1.241	-1.483	-1.720	-1.634	-1.652	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.471	-0.965	-0.996	-1.079	-1.035	-1.692	ns
		t_H	—	0.542	1.108	1.164	1.272	1.215	1.860	ns
	GCLK PLL	t_{SU}	—	0.715	1.389	1.654	1.921	1.820	1.823	ns
		t_H	—	-0.642	-1.241	-1.483	-1.720	-1.634	-1.652	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.457	-0.938	-0.964	-1.046	-1.002	-1.660	ns
		t_H	—	0.529	1.081	1.132	1.240	1.183	1.828	ns
	GCLK PLL	t_{SU}	—	0.729	1.417	1.686	1.953	1.853	1.855	ns
		t_H	—	-0.656	-1.268	-1.514	-1.752	-1.666	-1.683	ns

Table 1–93. EP3SE110 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.457	-0.938	-0.964	-1.046	-1.002	-1.660	ns
		t_H	—	0.529	1.081	1.132	1.240	1.183	1.828	ns
	GCLK PLL	t_{SU}	—	0.729	1.417	1.686	1.953	1.853	1.855	ns
		t_H	—	-0.656	-1.268	-1.514	-1.752	-1.666	-1.683	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.471	-0.965	-0.996	-1.079	-1.035	-1.692	ns
		t_H	—	0.542	1.108	1.164	1.272	1.215	1.860	ns
	GCLK PLL	t_{SU}	—	0.715	1.389	1.654	1.921	1.820	1.823	ns
		t_H	—	-0.642	-1.241	-1.483	-1.720	-1.634	-1.652	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.471	-0.965	-0.996	-1.079	-1.035	-1.692	ns
		t_H	—	0.542	1.108	1.164	1.272	1.215	1.860	ns
	GCLK PLL	t_{SU}	—	0.715	1.389	1.654	1.921	1.820	1.823	ns
		t_H	—	-0.642	-1.241	-1.483	-1.720	-1.634	-1.652	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.495	-1.016	-1.056	-1.138	-1.094	-1.752	ns
		t_H	—	0.565	1.156	1.219	1.327	1.271	1.915	ns
	GCLK PLL	t_{SU}	—	0.670	1.294	1.544	1.810	1.710	1.713	ns
		t_H	—	-0.598	-1.151	-1.376	-1.614	-1.529	-1.545	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.495	-1.016	-1.056	-1.138	-1.094	-1.752	ns
		t_H	—	0.565	1.156	1.219	1.327	1.271	1.915	ns
	GCLK PLL	t_{SU}	—	0.670	1.294	1.544	1.810	1.710	1.713	ns
		t_H	—	-0.598	-1.151	-1.376	-1.614	-1.529	-1.545	ns

Table 1–94 specifies EP3SE110 Column Pins Output Timing parameters for differential I/O standards.

Table 1–94. EP3SE110 Column Pins output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns

Table 1–94. EP3SE110 Column Pins output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_3R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.166	4.241	4.784	5.082	4.927	5.516	ns
		GCLK PLL	t_{CO}	—	1.040	2.007	2.273	2.231	2.216	2.141	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.094	4.094	4.611	4.907	4.754	5.343	ns
		GCLK PLL	t_{CO}	—	0.968	1.860	2.100	2.056	2.043	1.968	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.086	4.079	4.593	4.889	4.736	5.325	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.082	2.038	2.025	1.950	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.086	4.079	4.593	4.889	4.736	5.325	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.082	2.038	2.025	1.950	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.087	4.081	4.595	4.891	4.738	5.327	ns
		GCLK PLL	t_{CO}	—	0.961	1.847	2.084	2.040	2.027	1.952	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.086	4.078	4.592	4.888	4.735	5.324	ns
		GCLK PLL	t_{CO}	—	0.960	1.844	2.081	2.037	2.024	1.949	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.083	4.072	4.585	4.881	4.728	5.317	ns
		GCLK PLL	t_{CO}	—	0.957	1.838	2.074	2.030	2.017	1.942	ns

Table 1–94. EP3SE110 Column Pins output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.082	4.070	4.582	4.878	4.725	5.314	ns
		GCLK PLL	t_{CO}	—	0.956	1.836	2.071	2.027	2.014	1.939	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.083	4.072	4.585	4.881	4.728	5.317	ns
		GCLK PLL	t_{CO}	—	0.957	1.838	2.074	2.030	2.017	1.942	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.078	4.062	4.573	4.869	4.716	5.305	ns
		GCLK PLL	t_{CO}	—	0.952	1.828	2.062	2.018	2.005	1.930	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.075	4.057	4.567	4.863	4.710	5.299	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.056	2.012	1.999	1.924	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.081	4.069	4.581	4.877	4.724	5.313	ns
		GCLK PLL	t_{CO}	—	0.955	1.835	2.070	2.026	2.013	1.938	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.069	4.044	4.552	4.847	4.694	5.284	ns
		GCLK PLL	t_{CO}	—	0.943	1.810	2.041	1.996	1.983	1.909	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.076	4.059	4.569	4.865	4.712	5.301	ns
		GCLK PLL	t_{CO}	—	0.950	1.825	2.058	2.014	2.001	1.926	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.071	4.049	4.558	4.853	4.700	5.290	ns
		GCLK PLL	t_{CO}	—	0.945	1.815	2.047	2.002	1.989	1.915	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.075	4.056	4.566	4.862	4.709	5.298	ns
		GCLK PLL	t_{CO}	—	0.949	1.822	2.055	2.011	1.998	1.923	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.073	4.053	4.562	4.858	4.705	5.294	ns
		GCLK PLL	t_{CO}	—	0.947	1.819	2.051	2.007	1.994	1.919	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.072	4.051	4.560	4.856	4.703	5.292	ns
		GCLK PLL	t_{CO}	—	0.946	1.817	2.049	2.005	1.992	1.917	ns

Table 1–94. EP3SE110 Column Pins output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.065	4.036	4.542	4.838	4.685	5.274	ns
		GCLK PLL	t_{CO}	—	0.939	1.802	2.031	1.987	1.974	1.899	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.091	4.089	4.605	4.901	4.748	5.337	ns
		GCLK PLL	t_{CO}	—	0.965	1.855	2.094	2.050	2.037	1.962	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.086	4.079	4.593	4.889	4.736	5.325	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.082	2.038	2.025	1.950	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.083	4.073	4.586	4.882	4.729	5.318	ns
		GCLK PLL	t_{CO}	—	0.957	1.839	2.075	2.031	2.018	1.943	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.086	4.079	4.593	4.889	4.736	5.325	ns
		GCLK PLL	t_{CO}	—	0.960	1.845	2.082	2.038	2.025	1.950	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.084	4.075	4.588	4.884	4.731	5.320	ns
		GCLK PLL	t_{CO}	—	0.958	1.841	2.077	2.033	2.020	1.945	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.076	4.058	4.568	4.864	4.711	5.300	ns
		GCLK PLL	t_{CO}	—	0.950	1.824	2.057	2.013	2.000	1.925	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.078	4.063	4.574	4.870	4.717	5.306	ns
		GCLK PLL	t_{CO}	—	0.952	1.829	2.063	2.019	2.006	1.931	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.089	4.084	4.599	4.895	4.742	5.331	ns
		GCLK PLL	t_{CO}	—	0.963	1.850	2.088	2.044	2.031	1.956	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.082	4.070	4.582	4.878	4.725	5.314	ns
		GCLK PLL	t_{CO}	—	0.956	1.836	2.071	2.027	2.014	1.939	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.084	4.074	4.587	4.883	4.730	5.319	ns
		GCLK PLL	t_{CO}	—	0.958	1.840	2.076	2.032	2.019	1.944	ns

Table 1–94. EP3SE110 Column Pins output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.082	4.071	4.584	4.879	4.727	5.316	ns
		GCLK PLL	t_{CO}	—	0.956	1.837	2.073	2.028	2.016	1.941	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.079	4.064	4.575	4.871	4.718	5.307	ns
		GCLK PLL	t_{CO}	—	0.953	1.830	2.064	2.020	2.007	1.932	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.073	4.053	4.562	4.858	4.705	5.294	ns
		GCLK PLL	t_{CO}	—	0.947	1.819	2.051	2.007	1.994	1.919	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.076	4.059	4.569	4.865	4.712	5.301	ns
		GCLK PLL	t_{CO}	—	0.950	1.825	2.058	2.014	2.001	1.926	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.080	4.066	4.578	4.874	4.721	5.310	ns
		GCLK PLL	t_{CO}	—	0.954	1.832	2.067	2.023	2.010	1.935	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.079	4.064	4.575	4.871	4.718	5.307	ns
		GCLK PLL	t_{CO}	—	0.953	1.830	2.064	2.020	2.007	1.932	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.077	4.060	4.571	4.866	4.713	5.303	ns
		GCLK PLL	t_{CO}	—	0.951	1.826	2.060	2.015	2.002	1.928	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.075	4.057	4.567	4.863	4.710	5.299	ns
		GCLK PLL	t_{CO}	—	0.949	1.823	2.056	2.012	1.999	1.924	ns

Table 1–95 specifies EP3SE110 Row Pins Output Timing parameters for differential I/O standards.

Table 1–95. EP3SE110 Row Pins Output Timing Parameters (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	tco	—	2.121	4.149	4.683	4.971	4.821	5.379	ns
		GCLK PLL	tco	—	0.994	1.915	2.172	2.120	2.109	2.003	ns
LVDS_E_1R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
LVDS_E_3R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
MINI-LVDS	-	GCLK	tco	—	2.121	4.149	4.683	4.971	4.821	5.379	ns
		GCLK PLL	tco	—	0.994	1.915	2.172	2.120	2.109	2.003	ns
MINI-LVDS_E_1R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
MINI-LVDS_E_3R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
RSDS	-	GCLK	tco	—	2.121	4.149	4.683	4.971	4.821	5.379	ns
		GCLK PLL	tco	—	0.994	1.915	2.172	2.120	2.109	2.003	ns
RSDS_E_1R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
RSDS_E_3R	-	GCLK	tco	—	2.120	4.147	4.681	4.968	4.818	5.377	ns
		GCLK PLL	tco	—	0.993	1.913	2.170	2.117	2.106	2.001	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	tco	—	2.057	4.020	4.530	4.816	4.668	5.226	ns
		GCLK PLL	tco	—	0.930	1.786	2.019	1.965	1.956	1.850	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	tco	—	2.049	4.003	4.511	4.797	4.648	5.207	ns
		GCLK PLL	tco	—	0.922	1.769	2.000	1.946	1.936	1.831	ns

Table 1–95. EP3SE110 Row Pins Output Timing Parameters (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	tco	—	2.048	4.000	4.508	4.793	4.645	5.204	ns
		GCLK PLL	tco	—	0.921	1.766	1.997	1.942	1.933	1.828	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	tco	—	2.047	3.998	4.505	4.791	4.643	5.201	ns
		GCLK PLL	tco	—	0.920	1.764	1.994	1.940	1.931	1.825	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	tco	—	2.046	3.996	4.503	4.788	4.640	5.199	ns
		GCLK PLL	tco	—	0.919	1.762	1.992	1.937	1.928	1.823	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	tco	—	2.041	3.986	4.491	4.776	4.628	5.187	ns
		GCLK PLL	tco	—	0.914	1.752	1.980	1.925	1.916	1.811	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	tco	—	2.041	3.986	4.491	4.776	4.628	5.187	ns
		GCLK PLL	tco	—	0.914	1.752	1.980	1.925	1.916	1.811	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	tco	—	2.035	3.975	4.478	4.763	4.615	5.174	ns
		GCLK PLL	tco	—	0.908	1.741	1.967	1.912	1.903	1.798	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	tco	—	2.037	3.978	4.482	4.767	4.619	5.178	ns
		GCLK PLL	tco	—	0.910	1.744	1.971	1.916	1.907	1.802	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	tco	—	2.036	3.977	4.481	4.765	4.618	5.177	ns
		GCLK PLL	tco	—	0.909	1.743	1.970	1.914	1.906	1.801	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	tco	—	2.034	3.973	4.476	4.761	4.613	5.172	ns
		GCLK PLL	tco	—	0.907	1.739	1.965	1.910	1.901	1.796	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	tco	—	2.025	3.955	4.455	4.739	4.591	5.151	ns
		GCLK PLL	tco	—	0.898	1.721	1.944	1.888	1.879	1.775	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	tco	—	2.057	4.019	4.529	4.815	4.666	5.225	ns
		GCLK PLL	tco	—	0.930	1.785	2.018	1.964	1.954	1.849	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	tco	—	2.050	4.004	4.513	4.798	4.650	5.209	ns
		GCLK PLL	tco	—	0.923	1.770	2.002	1.947	1.938	1.833	ns

Table 1–95. EP3SE110 Row Pins Output Timing Parameters (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	tco	—	2.046	3.996	4.503	4.788	4.640	5.199	ns
		GCLK PLL	tco	—	0.919	1.762	1.992	1.937	1.928	1.823	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	tco	—	2.053	4.011	4.520	4.805	4.657	5.216	ns
		GCLK PLL	tco	—	0.926	1.777	2.009	1.954	1.945	1.840	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	tco	—	2.046	3.997	4.504	4.789	4.641	5.200	ns
		GCLK PLL	tco	—	0.919	1.763	1.993	1.938	1.929	1.824	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	tco	—	2.046	3.997	4.504	4.789	4.641	5.200	ns
		GCLK PLL	tco	—	0.919	1.763	1.993	1.938	1.929	1.824	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	tco	—	2.045	3.995	4.502	4.787	4.639	5.198	ns
		GCLK PLL	tco	—	0.918	1.761	1.991	1.936	1.927	1.822	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	tco	—	2.041	3.987	4.492	4.777	4.629	5.188	ns
		GCLK PLL	tco	—	0.914	1.753	1.981	1.926	1.917	1.812	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	tco	—	2.036	3.977	4.481	4.765	4.618	5.177	ns
		GCLK PLL	tco	—	0.909	1.743	1.970	1.914	1.906	1.801	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	tco	—	2.037	3.979	4.483	4.768	4.620	5.179	ns
		GCLK PLL	tco	—	0.910	1.745	1.972	1.917	1.908	1.803	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	tco	—	2.045	3.994	4.501	4.786	4.638	5.197	ns
		GCLK PLL	tco	—	0.918	1.760	1.990	1.935	1.926	1.821	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	tco	—	2.041	3.986	4.491	4.776	4.628	5.187	ns
		GCLK PLL	tco	—	0.914	1.752	1.980	1.925	1.916	1.811	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	tco	—	2.037	3.979	4.483	4.768	4.620	5.179	ns
		GCLK PLL	tco	—	0.910	1.745	1.972	1.917	1.908	1.803	ns

Table 1–96 through Table 1–97 show EP3SE110 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–96 specifies EP3SE110 Column Pin delay adders when using the Regional Clock

Table 1–96. EP3SE110 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.149	0.302	0.325	0.37	0.348	0.486	ns
RCLK PLL input adder	—	0.025	0.05	0.03	-0.001	0.019	0.022	ns
RCLK output adder	—	-0.13	-0.263	-0.282	-0.317	-0.304	-0.436	ns
RCLK PLL output adder	—	0.439	0.942	1.168	1.154	1.035	1.511	ns

Table 1–97 specifies EP3SE110 Row Pin delay adders when using the Regional Clock.EP3SE260 I/O Timing Parameters.

Table 1–97. EP3SE110 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.134	0.274	0.295	0.319	0.306	0.418	ns
RCLK PLL input adder	—	-0.007	-0.014	-0.039	-0.073	-0.055	-0.068	ns
RCLK output adder	—	-0.134	-0.274	-0.295	-0.319	-0.306	-0.418	ns
RCLK PLL output adder	—	0.007	0.014	0.039	0.073	0.055	0.068	ns

Table 1–98 through Table 1–102 show the maximum I/O timing parameters for EP3SE260 devices for single ended I/O standards.

Table 1–98 specifies EP3SE260 Column Pins Input Timing parameters for single-ended I/O standards.

Table 1–98. EP3SE260 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.780	-1.595	-1.703	-1.820	-1.761	-2.540	ns
		t_H	—	0.849	1.733	1.863	2.006	1.935	2.700	ns
	GCLK PLL	t_{SU}	—	0.435	0.820	1.018	1.276	1.179	1.147	ns
		t_H	—	-0.366	-0.682	-0.858	-1.090	-1.005	-0.987	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.780	-1.595	-1.703	-1.820	-1.761	-2.540	ns
		t_H	—	0.849	1.733	1.863	2.006	1.935	2.700	ns
	GCLK PLL	t_{SU}	—	0.435	0.820	1.018	1.276	1.179	1.147	ns
		t_H	—	-0.366	-0.682	-0.858	-1.090	-1.005	-0.987	ns
2.5 V	GCLK	t_{SU}	—	-0.785	-1.606	-1.715	-1.832	-1.773	-2.552	ns
		t_H	—	0.854	1.743	1.875	2.018	1.947	2.712	ns
	GCLK PLL	t_{SU}	—	0.430	0.809	1.006	1.264	1.167	1.135	ns
		t_H	—	-0.361	-0.672	-0.846	-1.078	-0.993	-0.975	ns
1.8 V	GCLK	t_{SU}	—	-0.795	-1.626	-1.739	-1.856	-1.797	-2.576	ns
		t_H	—	0.864	1.763	1.898	2.042	1.970	2.735	ns
	GCLK PLL	t_{SU}	—	0.420	0.789	0.982	1.240	1.143	1.111	ns
		t_H	—	-0.351	-0.652	-0.823	-1.054	-0.970	-0.952	ns
1.5 V	GCLK	t_{SU}	—	-0.775	-1.585	-1.692	-1.808	-1.749	-2.529	ns
		t_H	—	0.844	1.723	1.852	1.994	1.923	2.689	ns
	GCLK PLL	t_{SU}	—	0.440	0.830	1.029	1.288	1.191	1.158	ns
		t_H	—	-0.371	-0.692	-0.869	-1.102	-1.017	-0.998	ns
1.2 V	GCLK	t_{SU}	—	-0.718	-1.471	-1.558	-1.673	-1.614	-2.395	ns
		t_H	—	0.788	1.609	1.719	1.860	1.790	2.556	ns
	GCLK PLL	t_{SU}	—	0.497	0.944	1.163	1.423	1.326	1.292	ns
		t_H	—	-0.427	-0.806	-1.002	-1.236	-1.150	-1.131	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.658	-1.348	-1.415	-1.528	-1.470	-2.252	ns
		t_H	—	0.728	1.488	1.578	1.717	1.647	2.415	ns
	GCLK PLL	t_{SU}	—	0.557	1.067	1.306	1.568	1.470	1.435	ns
		t_H	—	-0.487	-0.927	-1.143	-1.379	-1.293	-1.272	ns

Table 1–98. EP3SE260 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.658	-1.348	-1.415	-1.528	-1.470	-2.252	ns
		t_H	—	0.728	1.488	1.578	1.717	1.647	2.415	ns
	GCLK PLL	t_{SU}	—	0.557	1.067	1.306	1.568	1.470	1.435	ns
		t_H	—	-0.487	-0.927	-1.143	-1.379	-1.293	-1.272	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.634	-1.297	-1.355	-1.469	-1.411	-2.192	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.366	1.627	1.529	2.360	ns
		t_H	—	-0.510	-0.975	-1.198	-1.434	-1.349	1.495	ns
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.634	-1.297	-1.355	-1.469	-1.411	-1.327	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.366	1.627	1.529	-2.192	ns
		t_H	—	-0.510	-0.975	-1.198	-1.434	-1.349	2.360	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.620	-1.270	-1.323	-1.436	-1.378	2.360	ns
	GCLK PLL	t_{SU}	—	0.595	1.145	1.398	1.660	1.562	1.495	ns
		t_H	—	-0.523	-1.002	-1.230	-1.466	-1.381	-1.327	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.620	-1.270	-1.323	-1.436	-1.378	-2.160	ns
	GCLK PLL	t_{SU}	—	0.595	1.145	1.398	1.660	1.562	2.328	ns
		t_H	—	-0.523	-1.002	-1.230	-1.466	-1.381	1.527	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.634	-1.297	-1.355	-1.469	-1.411	1.527	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.366	1.627	1.529	-1.359	ns
		t_H	—	-0.510	-0.975	-1.198	-1.434	-1.349	-2.160	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.634	-1.297	-1.355	-1.469	-1.411	2.360	ns
	GCLK PLL	t_{SU}	—	0.581	1.118	1.366	1.627	1.529	1.495	ns
		t_H	—	-0.510	-0.975	-1.198	-1.434	-1.349	-1.327	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.620	-1.270	-1.323	-1.436	-1.378	-2.192	ns
	GCLK PLL	t_{SU}	—	0.595	1.145	1.398	1.660	1.562	2.360	ns
		t_H	—	-0.523	-1.002	-1.230	-1.466	-1.381	1.495	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.620	-1.270	-1.323	-1.436	-1.378	-1.327	ns
	GCLK PLL	t_{SU}	—	0.595	1.145	1.398	1.660	1.562	-2.192	ns
		t_H	—	-0.523	-1.002	-1.230	-1.466	-1.381	2.360	ns

Table 1–98. EP3SE260 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.613	-1.255	-1.307	-1.420	-1.362	1.495	ns
	GCLK PLL	t_{SU}	—	0.602	1.160	1.414	1.676	1.578	-1.327	ns
		t_{H}	—	-0.530	-1.016	-1.246	-1.482	-1.397	-2.160	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.613	-1.255	-1.307	-1.420	-1.362	2.328	ns
	GCLK PLL	t_{SU}	—	0.602	1.160	1.414	1.676	1.578	1.527	ns
		t_{H}	—	-0.530	-1.016	-1.246	-1.482	-1.397	-1.359	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.780	-1.595	-1.703	-1.820	-1.761	-2.160	ns
		t_{H}	—	0.849	1.733	1.863	2.006	1.935	2.328	ns
	GCLK PLL	t_{SU}	—	0.435	0.820	1.018	1.276	1.179	1.527	ns
		t_{H}	—	-0.366	-0.682	-0.858	-1.090	-1.005	-1.359	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.780	-1.595	-1.703	-1.820	-1.761	-2.160	ns
		t_{H}	—	0.849	1.733	1.863	2.006	1.935	2.328	ns
	GCLK PLL	t_{SU}	—	0.435	0.820	1.018	1.276	1.179	1.527	ns
		t_{H}	—	-0.366	-0.682	-0.858	-1.090	-1.005	-1.359	ns

Table 1–99 specifies EP3SE260 Row Pins Input Timing parameters for single-ended I/O standards.

Table 1–99. EP3SE260 Row Pins Input Timing Parameters (Part 1 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	GCLK	t_{SU}	—	-0.712	-1.455	-1.547	-1.654	-1.603	-2.380	ns
		t_{H}	—	0.783	1.596	1.712	1.846	1.781	2.545	ns
	GCLK PLL	t_{SU}	—	0.465	0.882	1.088	1.352	1.252	1.317	ns
		t_{H}	—	-0.396	-0.744	-0.928	-1.166	-1.078	-1.152	ns
3.0-V LVCMOS	GCLK	t_{SU}	—	-0.712	-1.455	-1.547	-1.654	-1.603	-2.380	ns
		t_{H}	—	0.783	1.596	1.712	1.846	1.781	2.545	ns
	GCLK PLL	t_{SU}	—	0.465	0.882	1.088	1.352	1.252	1.317	ns
		t_{H}	—	-0.396	-0.744	-0.928	-1.166	-1.078	-1.152	ns

Table 1–99. EP3SE260 Row Pins Input Timing Parameters (Part 2 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
2.5 V	GCLK	t_{SU}	—	-0.717	-1.465	-1.558	-1.666	-1.615	-2.391	ns
		t_H	—	0.788	1.606	1.724	1.858	1.793	2.557	ns
	GCLK PLL	t_{SU}	—	0.460	0.871	1.076	1.340	1.240	1.306	ns
		t_H	—	-0.391	-0.734	-0.916	-1.154	-1.066	-1.140	ns
1.8 V	GCLK	t_{SU}	—	-0.730	-1.492	-1.589	-1.690	-1.638	-2.415	ns
		t_H	—	0.801	1.633	1.754	1.882	1.816	2.580	ns
	GCLK PLL	t_{SU}	—	0.450	0.851	1.052	1.316	1.216	1.318	ns
		t_H	—	-0.381	-0.714	-0.893	-1.130	-1.043	-1.153	ns
1.5 V	GCLK	t_{SU}	—	-0.709	-1.451	-1.541	-1.641	-1.590	-2.367	ns
		t_H	—	0.780	1.592	1.706	1.833	1.768	2.532	ns
	GCLK PLL	t_{SU}	—	0.470	0.892	1.099	1.364	1.264	1.366	ns
		t_H	—	-0.401	-0.754	-0.939	-1.178	-1.090	-1.201	ns
1.2 V	GCLK	t_{SU}	—	-0.652	-1.334	-1.405	-1.503	-1.453	-2.231	ns
		t_H	—	0.723	1.476	1.571	1.697	1.633	2.397	ns
	GCLK PLL	t_{SU}	—	0.527	1.006	1.233	1.499	1.399	1.502	ns
		t_H	—	-0.457	-0.868	-1.072	-1.312	-1.223	-1.336	ns
SSTL-2 CLASS I	GCLK	t_{SU}	—	-0.586	-1.199	-1.249	-1.352	-1.303	-2.082	ns
		t_H	—	0.658	1.342	1.417	1.548	1.484	2.250	ns
	GCLK PLL	t_{SU}	—	0.587	1.129	1.376	1.644	1.543	1.615	ns
		t_H	—	-0.517	-0.989	-1.213	-1.455	-1.366	-1.447	ns
SSTL-2 CLASS II	GCLK	t_{SU}	—	-0.586	-1.199	-1.249	-1.352	-1.303	-2.082	ns
		t_H	—	0.658	1.342	1.417	1.548	1.484	2.250	ns
	GCLK PLL	t_{SU}	—	0.587	1.129	1.376	1.644	1.543	1.615	ns
		t_H	—	-0.517	-0.989	-1.213	-1.455	-1.366	-1.447	ns
SSTL-18 CLASS I	GCLK	t_{SU}	—	-0.544	-1.111	-1.146	-1.241	-1.193	-1.972	ns
		t_H	—	0.617	1.259	1.317	1.442	1.379	2.143	ns
	GCLK PLL	t_{SU}	—	0.611	1.180	1.436	1.703	1.602	1.761	ns
		t_H	—	-0.540	-1.037	-1.268	-1.510	-1.422	-1.590	ns

Table 1–99. EP3SE260 Row Pins Input Timing Parameters (Part 3 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS II	GCLK	t_{SU}	—	-0.544	-1.111	-1.146	-1.241	-1.193	-1.972	ns
		t_H	—	0.617	1.259	1.317	1.442	1.379	2.143	ns
	GCLK PLL	t_{SU}	—	0.611	1.180	1.436	1.703	1.602	1.761	ns
		t_H	—	-0.540	-1.037	-1.268	-1.510	-1.422	-1.590	ns
SSTL-15 CLASS I	GCLK	t_{SU}	—	-0.530	-1.083	-1.114	-1.209	-1.160	-1.940	ns
		t_H	—	0.603	1.232	1.286	1.410	1.347	2.112	ns
	GCLK PLL	t_{SU}	—	0.625	1.207	1.468	1.736	1.635	1.793	ns
		t_H	—	-0.553	-1.064	-1.300	-1.542	-1.454	-1.621	ns
SSTL-15 CLASS II	GCLK	t_{SU}	—	-0.530	-1.083	-1.114	-1.209	-1.160	-1.940	ns
		t_H	—	0.603	1.232	1.286	1.410	1.347	2.112	ns
	GCLK PLL	t_{SU}	—	0.625	1.207	1.468	1.736	1.635	1.793	ns
		t_H	—	-0.553	-1.064	-1.300	-1.542	-1.454	-1.621	ns
1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.544	-1.111	-1.146	-1.241	-1.193	-1.972	ns
		t_H	—	0.617	1.259	1.317	1.442	1.379	2.143	ns
	GCLK PLL	t_{SU}	—	0.611	1.180	1.436	1.703	1.602	1.761	ns
		t_H	—	-0.540	-1.037	-1.268	-1.510	-1.422	-1.590	ns
1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.544	-1.111	-1.146	-1.241	-1.193	-1.972	ns
		t_H	—	0.617	1.259	1.317	1.442	1.379	2.143	ns
	GCLK PLL	t_{SU}	—	0.611	1.180	1.436	1.703	1.602	1.761	ns
		t_H	—	-0.540	-1.037	-1.268	-1.510	-1.422	-1.590	ns
1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.530	-1.083	-1.114	-1.209	-1.160	-1.940	ns
		t_H	—	0.603	1.232	1.286	1.410	1.347	2.112	ns
	GCLK PLL	t_{SU}	—	0.625	1.207	1.468	1.736	1.635	1.793	ns
		t_H	—	-0.553	-1.064	-1.300	-1.542	-1.454	-1.621	ns
1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.530	-1.083	-1.114	-1.209	-1.160	-1.940	ns
		t_H	—	0.603	1.232	1.286	1.410	1.347	2.112	ns
	GCLK PLL	t_{SU}	—	0.625	1.207	1.468	1.736	1.635	1.793	ns
		t_H	—	-0.553	-1.064	-1.300	-1.542	-1.454	-1.621	ns

Table 1–99. EP3SE260 Row Pins Input Timing Parameters (Part 4 of 4)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.523	-1.069	-1.098	-1.192	-1.144	-1.924	ns
		t_H	—	0.596	1.218	1.269	1.393	1.331	2.095	ns
	GCLK PLL	t_{SU}	—	0.632	1.222	1.484	1.752	1.651	1.809	ns
		t_H	—	-0.560	-1.078	-1.316	-1.558	-1.470	-1.638	ns
1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.523	-1.069	-1.098	-1.192	-1.144	-1.924	ns
		t_H	—	0.596	1.218	1.269	1.393	1.331	2.095	ns
	GCLK PLL	t_{SU}	—	0.632	1.222	1.484	1.752	1.651	1.809	ns
		t_H	—	-0.560	-1.078	-1.316	-1.558	-1.470	-1.638	ns
3.0-V PCI	GCLK	t_{SU}	—	-0.712	-1.455	-1.547	-1.654	-1.603	-2.380	ns
		t_H	—	0.783	1.596	1.712	1.846	1.781	2.545	ns
	GCLK PLL	t_{SU}	—	0.465	0.882	1.088	1.352	1.252	1.317	ns
		t_H	—	-0.396	-0.744	-0.928	-1.166	-1.078	-1.152	ns
3.0-V PCI-X	GCLK	t_{SU}	—	-0.712	-1.455	-1.547	-1.654	-1.603	-2.380	ns
		t_H	—	0.783	1.596	1.712	1.846	1.781	2.545	ns
	GCLK PLL	t_{SU}	—	0.465	0.882	1.088	1.352	1.252	1.317	ns
		t_H	—	-0.396	-0.744	-0.928	-1.166	-1.078	-1.152	ns

Table 1–100 specifies EP3SE260 Column Pins Output Timing parameters for single-ended I/O standards.

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.689	4.639	5.185	5.479	5.133	5.838	ns
		GCLK PLL	t_{CO}	—	1.469	2.220	2.457	2.376	2.186	2.123	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.837	4.775	5.384	5.678	5.273	5.979	ns
		GCLK PLL	t_{CO}	—	1.617	2.356	2.656	2.575	2.326	2.264	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.897	4.854	5.439	5.733	5.360	6.065	ns
		GCLK PLL	t_{CO}	—	1.677	2.435	2.711	2.630	2.413	2.350	ns
3.0-V LVTTL	16mA	GCLK	t_{CO}	—	3.012	5.018	5.624	5.918	5.525	6.231	ns
		GCLK PLL	t_{CO}	—	1.792	2.599	2.896	2.815	2.578	2.516	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.837	4.775	5.383	5.677	5.273	5.979	ns
		GCLK PLL	t_{CO}	—	1.617	2.356	2.655	2.574	2.326	2.264	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	3.012	5.018	5.623	5.917	5.525	6.231	ns
		GCLK PLL	t_{CO}	—	1.792	2.599	2.895	2.814	2.578	2.516	ns
3.0-V LVCMOS	12mA	GCLK	t_{CO}	—	3.067	5.094	5.688	5.982	5.604	6.309	ns
		GCLK PLL	t_{CO}	—	1.847	2.675	2.960	2.879	2.657	2.594	ns
3.0-V LVCMOS	16mA	GCLK	t_{CO}	—	3.120	5.155	5.744	6.038	5.666	6.371	ns
		GCLK PLL	t_{CO}	—	1.900	2.736	3.016	2.935	2.719	2.656	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.775	4.800	5.453	5.747	5.302	6.007	ns
		GCLK PLL	t_{CO}	—	1.555	2.381	2.725	2.644	2.355	2.292	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.814	4.824	5.428	5.722	5.324	6.030	ns
		GCLK PLL	t_{CO}	—	1.594	2.405	2.700	2.619	2.377	2.315	ns
2.5 V	12mA	GCLK	t_{CO}	—	3.062	5.169	5.828	6.122	5.679	6.385	ns
		GCLK PLL	t_{CO}	—	1.842	2.750	3.100	3.019	2.732	2.670	ns
2.5 V	16mA	GCLK	t_{CO}	—	3.095	5.228	5.925	6.219	5.741	6.447	ns
		GCLK PLL	t_{CO}	—	1.875	2.809	3.197	3.116	2.794	2.732	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.677	4.671	5.268	5.562	5.169	5.875	ns
		GCLK PLL	t_{CO}	—	1.457	2.252	2.540	2.459	2.222	2.160	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	4mA	GCLK	t_{CO}	—	2.739	4.788	5.497	5.791	5.288	5.993	ns
		GCLK PLL	t_{CO}	—	1.519	2.369	2.769	2.688	2.341	2.278	ns
1.8 V	6mA	GCLK	t_{CO}	—	2.982	5.086	5.787	6.081	5.592	6.298	ns
		GCLK PLL	t_{CO}	—	1.762	2.667	3.059	2.978	2.645	2.583	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.809	4.833	5.469	5.763	5.332	6.038	ns
		GCLK PLL	t_{CO}	—	1.589	2.414	2.741	2.660	2.385	2.323	ns
1.8 V	10mA	GCLK	t_{CO}	—	3.071	5.195	5.880	6.174	5.704	6.410	ns
		GCLK PLL	t_{CO}	—	1.851	2.776	3.152	3.071	2.757	2.695	ns
1.8 V	12mA	GCLK	t_{CO}	—	3.142	5.341	6.100	6.394	5.856	6.562	ns
		GCLK PLL	t_{CO}	—	1.922	2.922	3.372	3.291	2.909	2.847	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.629	4.533	5.169	5.463	5.029	5.734	ns
		GCLK PLL	t_{CO}	—	1.409	2.114	2.441	2.360	2.083	2.030	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.897	4.993	5.646	5.940	5.503	6.208	ns
		GCLK PLL	t_{CO}	—	1.677	2.574	2.918	2.837	2.556	2.493	ns
1.5 V	6mA	GCLK	t_{CO}	—	2.995	5.099	5.776	6.070	5.607	6.313	ns
		GCLK PLL	t_{CO}	—	1.775	2.680	3.048	2.967	2.660	2.598	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.920	4.955	5.619	5.913	5.461	6.167	ns
		GCLK PLL	t_{CO}	—	1.700	2.536	2.891	2.810	2.514	2.452	ns
1.5 V	10mA	GCLK	t_{CO}	—	3.086	5.242	5.974	6.268	5.751	6.457	ns
		GCLK PLL	t_{CO}	—	1.866	2.823	3.246	3.165	2.804	2.742	ns
1.5 V	12mA	GCLK	t_{CO}	—	3.260	5.584	6.462	6.756	6.098	6.804	ns
		GCLK PLL	t_{CO}	—	2.040	3.165	3.734	3.653	3.151	3.089	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.2 V	2mA	GCLK	t_{CO}	—	2.905	5.053	5.874	6.168	5.539	6.245	ns
		GCLK PLL	t_{CO}	—	1.685	2.634	3.146	3.065	2.592	2.530	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.071	5.272	6.056	6.350	5.781	6.487	ns
		GCLK PLL	t_{CO}	—	1.851	2.853	3.328	3.247	2.834	2.772	ns
1.2 V	6mA	GCLK	t_{CO}	—	3.007	5.142	5.889	6.183	5.647	6.353	ns
		GCLK PLL	t_{CO}	—	1.787	2.723	3.161	3.080	2.700	2.638	ns
1.2 V	8mA	GCLK	t_{CO}	—	3.261	5.544	6.396	6.690	6.055	6.761	ns
		GCLK PLL	t_{CO}	—	2.041	3.125	3.668	3.587	3.108	3.046	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.387	4.171	4.665	4.959	4.653	5.359	ns
		GCLK PLL	t_{CO}	—	1.167	1.752	1.937	1.856	1.706	1.644	ns
SSTL-2 CLASS I	10mA	GCLK	t_{CO}	—	2.384	4.168	4.661	4.955	4.650	5.356	ns
		GCLK PLL	t_{CO}	—	1.164	1.749	1.933	1.852	1.703	1.641	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.387	4.176	4.670	4.964	4.658	5.364	ns
		GCLK PLL	t_{CO}	—	1.167	1.757	1.942	1.861	1.711	1.649	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.399	4.178	4.670	4.964	4.659	5.365	ns
		GCLK PLL	t_{CO}	—	1.179	1.759	1.942	1.861	1.712	1.650	ns
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.394	4.185	4.682	4.976	4.667	5.373	ns
		GCLK PLL	t_{CO}	—	1.174	1.766	1.954	1.873	1.720	1.658	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.387	4.177	4.673	4.967	4.658	5.364	ns
		GCLK PLL	t_{CO}	—	1.167	1.758	1.945	1.864	1.711	1.649	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.391	4.186	4.685	4.979	4.668	5.374	ns
		GCLK PLL	t_{CO}	—	1.171	1.767	1.957	1.876	1.721	1.659	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.390	4.188	4.687	4.981	4.671	5.377	ns
		GCLK PLL	t_{CO}	—	1.170	1.769	1.959	1.878	1.724	1.662	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.388	4.186	4.685	4.979	4.669	5.375	ns
		GCLK PLL	t_{CO}	—	1.168	1.767	1.957	1.876	1.722	1.660	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.393	4.176	4.669	4.963	4.657	5.363	ns
		GCLK PLL	t_{CO}	—	1.173	1.757	1.941	1.860	1.710	1.648	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.409	4.211	4.710	5.004	4.694	5.400	ns
		GCLK PLL	t_{CO}	—	1.189	1.792	1.982	1.901	1.747	1.685	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.393	4.187	4.686	4.980	4.668	5.374	ns
		GCLK PLL	t_{CO}	—	1.173	1.768	1.958	1.877	1.721	1.659	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.392	4.188	4.688	4.982	4.670	5.376	ns
		GCLK PLL	t_{CO}	—	1.172	1.769	1.960	1.879	1.723	1.661	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.391	4.192	4.692	4.986	4.674	5.380	ns
		GCLK PLL	t_{CO}	—	1.171	1.773	1.964	1.883	1.727	1.665	ns
SSTL-15 CLASS I	10mA	GCLK	t_{CO}	—	2.399	4.206	4.708	5.002	4.689	5.395	ns
		GCLK PLL	t_{CO}	—	1.179	1.787	1.980	1.899	1.742	1.680	ns
SSTL-15 CLASS I	12mA	GCLK	t_{CO}	—	2.394	4.200	4.701	4.995	4.682	5.388	ns
		GCLK PLL	t_{CO}	—	1.174	1.781	1.973	1.892	1.735	1.673	ns
SSTL-15 CLASS II	8mA	GCLK	t_{CO}	—	2.395	4.183	4.679	4.973	4.665	5.371	ns
		GCLK PLL	t_{CO}	—	1.175	1.764	1.951	1.870	1.718	1.656	ns
SSTL-15 CLASS II	16mA	GCLK	t_{CO}	—	2.409	4.215	4.717	5.011	4.699	5.405	ns
		GCLK PLL	t_{CO}	—	1.189	1.796	1.989	1.908	1.752	1.690	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.390	4.167	4.660	4.954	4.648	5.354	ns
		GCLK PLL	t_{CO}	—	1.170	1.748	1.932	1.851	1.701	1.639	ns
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.391	4.170	4.664	4.958	4.651	5.357	ns
		GCLK PLL	t_{CO}	—	1.171	1.751	1.936	1.855	1.704	1.642	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.393	4.178	4.672	4.966	4.659	5.365	ns
		GCLK PLL	t_{CO}	—	1.173	1.759	1.944	1.863	1.712	1.650	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.397	4.185	4.680	4.974	4.667	5.373	ns
		GCLK PLL	t_{CO}	—	1.177	1.766	1.952	1.871	1.720	1.658	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.399	4.188	4.683	4.977	4.670	5.376	ns
		GCLK PLL	t_{CO}	—	1.179	1.769	1.955	1.874	1.723	1.661	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.450	4.222	4.713	5.007	4.703	5.409	ns
		GCLK PLL	t_{CO}	—	1.230	1.803	1.985	1.904	1.756	1.694	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.396	4.176	4.671	4.965	4.657	5.363	ns
		GCLK PLL	t_{CO}	—	1.176	1.757	1.943	1.862	1.710	1.648	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.396	4.179	4.676	4.970	4.660	5.366	ns
		GCLK PLL	t_{CO}	—	1.176	1.760	1.948	1.867	1.713	1.651	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.393	4.174	4.669	4.963	4.655	5.361	ns
		GCLK PLL	t_{CO}	—	1.173	1.755	1.941	1.860	1.708	1.646	ns
1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.395	4.183	4.679	4.973	4.665	5.371	ns
		GCLK PLL	t_{CO}	—	1.175	1.764	1.951	1.870	1.718	1.656	ns
1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.404	4.197	4.695	4.989	4.679	5.385	ns
		GCLK PLL	t_{CO}	—	1.184	1.778	1.967	1.886	1.732	1.670	ns

Table 1–100. EP3SE260 Column Pins Output Timing Parameters (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.428	4.182	4.670	4.964	4.661	5.367	ns
		GCLK PLL	t_{CO}	—	1.208	1.763	1.942	1.861	1.714	1.652	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.407	4.195	4.695	4.989	4.677	5.383	ns
		GCLK PLL	t_{CO}	—	1.187	1.776	1.967	1.886	1.730	1.668	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.401	4.190	4.689	4.983	4.671	5.377	ns
		GCLK PLL	t_{CO}	—	1.181	1.771	1.961	1.880	1.724	1.662	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.411	4.208	4.710	5.004	4.690	5.396	ns
		GCLK PLL	t_{CO}	—	1.191	1.789	1.982	1.901	1.743	1.681	ns
1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.407	4.208	4.710	5.004	4.691	5.397	ns
		GCLK PLL	t_{CO}	—	1.187	1.789	1.982	1.901	1.744	1.682	ns
1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.407	4.207	4.708	5.002	4.689	5.395	ns
		GCLK PLL	t_{CO}	—	1.187	1.788	1.980	1.899	1.742	1.680	ns
1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.460	4.241	4.737	5.031	4.722	5.428	ns
		GCLK PLL	t_{CO}	—	1.240	1.822	2.009	1.928	1.775	1.713	ns
3.0-V PCI	-	GCLK	t_{CO}	—	3.385	5.515	6.206	6.500	6.035	6.740	ns
		GCLK PLL	t_{CO}	—	2.165	3.096	3.478	3.397	3.088	3.025	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.385	5.515	6.206	6.500	6.035	6.740	ns
		GCLK PLL	t_{CO}	—	2.165	3.096	3.478	3.397	3.088	3.025	ns

Table 1–101 specifies EP3SE260 Row Pins Output Timing parameters for single-ended I/O standards.

Table 1–101. EP3SE260 Row Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V LVTTL	4mA	GCLK	t_{CO}	—	2.769	4.729	5.307	5.601	5.229	5.916	ns
		GCLK PLL	t_{CO}	—	1.559	2.327	2.595	2.510	2.293	2.219	ns
3.0-V LVTTL	8mA	GCLK	t_{CO}	—	2.833	4.787	5.397	5.691	5.282	5.970	ns
		GCLK PLL	t_{CO}	—	1.623	2.385	2.685	2.600	2.346	2.273	ns
3.0-V LVTTL	12mA	GCLK	t_{CO}	—	2.964	4.944	5.543	5.837	5.444	6.131	ns
		GCLK PLL	t_{CO}	—	1.754	2.542	2.831	2.746	2.508	2.434	ns
3.0-V LVCMOS	4mA	GCLK	t_{CO}	—	2.862	4.811	5.407	5.701	5.315	6.002	ns
		GCLK PLL	t_{CO}	—	1.652	2.409	2.695	2.610	2.379	2.305	ns
3.0-V LVCMOS	8mA	GCLK	t_{CO}	—	3.004	4.994	5.612	5.906	5.500	6.188	ns
		GCLK PLL	t_{CO}	—	1.794	2.592	2.900	2.815	2.564	2.491	ns
2.5 V	4mA	GCLK	t_{CO}	—	2.866	4.951	5.621	5.915	5.460	6.147	ns
		GCLK PLL	t_{CO}	—	1.656	2.549	2.909	2.824	2.524	2.450	ns
2.5 V	8mA	GCLK	t_{CO}	—	2.860	4.882	5.499	5.793	5.383	6.070	ns
		GCLK PLL	t_{CO}	—	1.650	2.480	2.787	2.702	2.447	2.373	ns
2.5 V	12mA	GCLK	t_{CO}	—	3.065	5.162	5.833	6.127	5.679	6.366	ns
		GCLK PLL	t_{CO}	—	1.855	2.760	3.121	3.036	2.743	2.669	ns
1.8 V	2mA	GCLK	t_{CO}	—	2.873	4.867	5.461	5.748	5.367	6.054	ns
		GCLK PLL	t_{CO}	—	1.660	2.458	2.742	2.657	2.431	2.321	ns
1.8 V	4mA	GCLK	t_{CO}	—	2.904	5.002	5.725	6.012	5.496	6.184	ns
		GCLK PLL	t_{CO}	—	1.691	2.593	3.006	2.921	2.560	2.451	ns

Table 1–101. EP3SE260 Row Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8 V	6mA	GCLK	t_{CO}	—	2.996	5.147	5.892	6.179	5.652	6.340	ns
		GCLK PLL	t_{CO}	—	1.783	2.738	3.173	3.088	2.716	2.607	ns
1.8 V	8mA	GCLK	t_{CO}	—	2.881	4.922	5.565	5.852	5.415	6.102	ns
		GCLK PLL	t_{CO}	—	1.668	2.513	2.846	2.761	2.479	2.369	ns
1.5 V	2mA	GCLK	t_{CO}	—	2.786	4.782	5.396	5.683	5.276	5.963	ns
		GCLK PLL	t_{CO}	—	1.573	2.373	2.677	2.592	2.340	2.230	ns
1.5 V	4mA	GCLK	t_{CO}	—	2.911	5.025	5.705	5.992	5.528	6.215	ns
		GCLK PLL	t_{CO}	—	1.698	2.616	2.986	2.901	2.592	2.482	ns
1.5 V	6mA	GCLK	t_{CO}	—	3.046	5.177	5.915	6.202	5.683	6.371	ns
		GCLK PLL	t_{CO}	—	1.833	2.768	3.196	3.111	2.747	2.638	ns
1.5 V	8mA	GCLK	t_{CO}	—	2.933	5.003	5.690	5.977	5.503	6.191	ns
		GCLK PLL	t_{CO}	—	1.720	2.594	2.971	2.886	2.567	2.458	ns
1.2 V	2mA	GCLK	t_{CO}	—	3.036	5.387	6.326	6.613	5.868	6.556	ns
		GCLK PLL	t_{CO}	—	1.823	2.978	3.607	3.522	2.932	2.823	ns
1.2 V	4mA	GCLK	t_{CO}	—	3.164	5.455	6.317	6.604	5.948	6.636	ns
		GCLK PLL	t_{CO}	—	1.951	3.046	3.598	3.513	3.012	2.903	ns
SSTL-2 CLASS I	8mA	GCLK	t_{CO}	—	2.358	4.132	4.628	4.922	4.615	5.303	ns
		GCLK PLL	t_{CO}	—	1.148	1.730	1.916	1.831	1.679	1.606	ns
SSTL-2 CLASS I	12mA	GCLK	t_{CO}	—	2.346	4.123	4.619	4.913	4.605	5.293	ns
		GCLK PLL	t_{CO}	—	1.136	1.721	1.907	1.822	1.669	1.596	ns
SSTL-2 CLASS II	16mA	GCLK	t_{CO}	—	2.351	4.124	4.619	4.913	4.606	5.294	ns
		GCLK PLL	t_{CO}	—	1.141	1.722	1.907	1.822	1.670	1.597	ns

Table 1–101. EP3SE260 Row Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
SSTL-18 CLASS I	4mA	GCLK	t_{CO}	—	2.363	4.145	4.646	4.933	4.621	5.309	ns
		GCLK PLL	t_{CO}	—	1.150	1.736	1.927	1.842	1.685	1.576	ns
SSTL-18 CLASS I	6mA	GCLK	t_{CO}	—	2.351	4.133	4.633	4.920	4.608	5.296	ns
		GCLK PLL	t_{CO}	—	1.138	1.724	1.914	1.829	1.672	1.563	ns
SSTL-18 CLASS I	8mA	GCLK	t_{CO}	—	2.351	4.140	4.642	4.929	4.615	5.303	ns
		GCLK PLL	t_{CO}	—	1.138	1.731	1.923	1.838	1.679	1.570	ns
SSTL-18 CLASS I	10mA	GCLK	t_{CO}	—	2.343	4.135	4.636	4.923	4.610	5.298	ns
		GCLK PLL	t_{CO}	—	1.130	1.726	1.917	1.832	1.674	1.565	ns
SSTL-18 CLASS I	12mA	GCLK	t_{CO}	—	2.341	4.132	4.634	4.921	4.608	5.296	ns
		GCLK PLL	t_{CO}	—	1.128	1.723	1.915	1.830	1.672	1.563	ns
SSTL-18 CLASS II	8mA	GCLK	t_{CO}	—	2.346	4.124	4.623	4.910	4.599	5.287	ns
		GCLK PLL	t_{CO}	—	1.133	1.715	1.904	1.819	1.663	1.554	ns
SSTL-18 CLASS II	16mA	GCLK	t_{CO}	—	2.348	4.138	4.639	4.926	4.613	5.301	ns
		GCLK PLL	t_{CO}	—	1.135	1.729	1.920	1.835	1.677	1.568	ns
SSTL-15 CLASS I	4mA	GCLK	t_{CO}	—	2.363	4.148	4.652	4.939	4.623	5.311	ns
		GCLK PLL	t_{CO}	—	1.150	1.739	1.933	1.848	1.687	1.578	ns
SSTL-15 CLASS I	6mA	GCLK	t_{CO}	—	2.352	4.143	4.648	4.935	4.618	5.306	ns
		GCLK PLL	t_{CO}	—	1.139	1.734	1.929	1.844	1.682	1.573	ns
SSTL-15 CLASS I	8mA	GCLK	t_{CO}	—	2.344	4.137	4.641	4.928	4.612	5.300	ns
		GCLK PLL	t_{CO}	—	1.131	1.728	1.922	1.837	1.676	1.567	ns
1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.358	4.126	4.622	4.909	4.600	5.288	ns
		GCLK PLL	t_{CO}	—	1.145	1.717	1.903	1.818	1.664	1.555	ns

Table 1–101. EP3SE260 Row Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.349	4.125	4.624	4.911	4.600	5.288	ns
		GCLK PLL	t_{CO}	—	1.136	1.716	1.905	1.820	1.664	1.555	ns
1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.343	4.124	4.622	4.909	4.598	5.286	ns
		GCLK PLL	t_{CO}	—	1.130	1.715	1.903	1.818	1.662	1.553	ns
1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.345	4.127	4.626	4.913	4.602	5.290	ns
		GCLK PLL	t_{CO}	—	1.132	1.718	1.907	1.822	1.666	1.557	ns
1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.344	4.130	4.630	4.917	4.605	5.293	ns
		GCLK PLL	t_{CO}	—	1.131	1.721	1.911	1.826	1.669	1.560	ns
1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.353	4.128	4.623	4.910	4.602	5.290	ns
		GCLK PLL	t_{CO}	—	1.140	1.719	1.904	1.819	1.666	1.557	ns
1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.364	4.134	4.634	4.921	4.608	5.296	ns
		GCLK PLL	t_{CO}	—	1.151	1.725	1.915	1.830	1.672	1.563	ns
1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.358	4.137	4.639	4.926	4.612	5.300	ns
		GCLK PLL	t_{CO}	—	1.145	1.728	1.920	1.835	1.676	1.567	ns
1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.350	4.128	4.629	4.916	4.603	5.291	ns
		GCLK PLL	t_{CO}	—	1.137	1.719	1.910	1.825	1.667	1.558	ns
1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.367	4.150	4.658	4.945	4.625	5.313	ns
		GCLK PLL	t_{CO}	—	1.154	1.741	1.939	1.854	1.689	1.580	ns
1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.355	4.140	4.645	4.932	4.614	5.302	ns
		GCLK PLL	t_{CO}	—	1.142	1.731	1.926	1.841	1.678	1.569	ns
1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.358	4.152	4.659	4.946	4.627	5.315	ns
		GCLK PLL	t_{CO}	—	1.145	1.743	1.940	1.855	1.691	1.582	ns

Table 1–101. EP3SE260 Row Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
3.0-V PCI	-	GCLK	t_{CO}	—	3.307	5.469	6.166	6.460	5.989	6.676	ns
		GCLK PLL	t_{CO}	—	2.097	3.067	3.454	3.369	3.053	2.979	ns
3.0-V PCI-X	-	GCLK	t_{CO}	—	3.307	5.469	6.166	6.460	5.989	6.676	ns
		GCLK PLL	t_{CO}	—	2.097	3.067	3.454	3.369	3.053	2.979	ns

Table 1–102 through Table 1–107 show the maximum I/O timing parameters for EP3SE260 devices for differential I/O standards.

Table 1–102 specifies EP3SE260 Column Pins Input Timing parameters for differential I/O standards.

Table 1–102. EP3SE260 Column Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.618	-1.262	-1.317	-1.431	-1.372	-2.155	ns
		t_H	—	0.690	1.406	1.485	1.625	1.553	2.323	ns
	GCLK PLL	t_{SU}	—	0.604	1.163	1.417	1.680	1.582	1.549	ns
		t_H	—	-0.532	-1.019	-1.249	-1.486	-1.401	-1.381	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.618	-1.262	-1.317	-1.431	-1.372	-2.155	ns
		t_H	—	0.690	1.406	1.485	1.625	1.553	2.323	ns
	GCLK PLL	t_{SU}	—	0.604	1.163	1.417	1.680	1.582	1.549	ns
		t_H	—	-0.532	-1.019	-1.249	-1.486	-1.401	-1.381	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.625	-1.277	-1.333	-1.447	-1.388	-2.171	ns
		t_H	—	0.697	1.420	1.501	1.641	1.569	2.339	ns
	GCLK PLL	t_{SU}	—	0.597	1.148	1.401	1.664	1.566	1.533	ns
		t_H	—	-0.525	-1.005	-1.233	-1.470	-1.385	-1.365	ns

Table 1–102. EP3SE260 Column Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.625	-1.277	-1.333	-1.447	-1.388	-2.171	ns
		t_H	—	0.697	1.420	1.501	1.641	1.569	2.339	ns
	GCLK PLL	t_{SU}	—	0.597	1.148	1.401	1.664	1.566	1.533	ns
		t_H	—	-0.525	-1.005	-1.233	-1.470	-1.385	-1.365	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.639	-1.304	-1.365	-1.480	-1.421	-2.203	ns
		t_H	—	0.710	1.447	1.533	1.673	1.601	2.371	ns
	GCLK PLL	t_{SU}	—	0.583	1.121	1.369	1.631	1.533	1.501	ns
		t_H	—	-0.512	-0.978	-1.201	-1.438	-1.353	-1.333	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.639	-1.304	-1.365	-1.480	-1.421	-2.203	ns
		t_H	—	0.710	1.447	1.533	1.673	1.601	2.371	ns
	GCLK PLL	t_{SU}	—	0.583	1.121	1.369	1.631	1.533	1.501	ns
		t_H	—	-0.512	-0.978	-1.201	-1.438	-1.353	-1.333	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.625	-1.277	-1.333	-1.447	-1.388	-2.171	ns
		t_H	—	0.697	1.420	1.501	1.641	1.569	2.339	ns
	GCLK PLL	t_{SU}	—	0.597	1.148	1.401	1.664	1.566	1.533	ns
		t_H	—	-0.525	-1.005	-1.233	-1.470	-1.385	-1.365	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.625	-1.277	-1.333	-1.447	-1.388	-2.171	ns
		t_H	—	0.697	1.420	1.501	1.641	1.569	2.339	ns
	GCLK PLL	t_{SU}	—	0.597	1.148	1.401	1.664	1.566	1.533	ns
		t_H	—	-0.525	-1.005	-1.233	-1.470	-1.385	-1.365	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.639	-1.304	-1.365	-1.480	-1.421	-2.203	ns
		t_H	—	0.710	1.447	1.533	1.673	1.601	2.371	ns
	GCLK PLL	t_{SU}	—	0.583	1.121	1.369	1.631	1.533	1.501	ns
		t_H	—	-0.512	-0.978	-1.201	-1.438	-1.353	-1.333	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.639	-1.304	-1.365	-1.480	-1.421	-2.203	ns
		t_H	—	0.710	1.447	1.533	1.673	1.601	2.371	ns
	GCLK PLL	t_{SU}	—	0.583	1.121	1.369	1.631	1.533	1.501	ns
		t_H	—	-0.512	-0.978	-1.201	-1.438	-1.353	-1.333	ns

Table 1–102. EP3SE260 Column Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.663	-1.355	-1.425	-1.539	-1.480	-2.263	ns
		t_H	—	0.733	1.495	1.588	1.728	1.657	2.426	ns
	GCLK PLL	t_{SU}	—	0.559	1.070	1.309	1.572	1.474	1.441	ns
		t_H	—	-0.489	-0.930	-1.146	-1.383	-1.297	-1.278	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.663	-1.355	-1.425	-1.539	-1.480	-2.263	ns
		t_H	—	0.733	1.495	1.588	1.728	1.657	2.426	ns
	GCLK PLL	t_{SU}	—	0.559	1.070	1.309	1.572	1.474	1.441	ns
		t_H	—	-0.489	-0.930	-1.146	-1.383	-1.297	-1.278	ns

Table 1–103 specifies EP3SE260 Row Pins Input Timing parameters for differential I/O standards.

Table 1–103. EP3SE260 Row Pins Input Timing Parameters (Part 1 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	GCLK	t_{SU}	—	-0.664	-1.354	-1.428	-1.536	-1.480	-2.245	ns
		t_H	—	0.735	1.496	1.595	1.729	1.660	2.412	ns
	GCLK PLL	t_{SU}	—	0.575	1.106	1.348	1.622	1.517	1.498	ns
		t_H	—	-0.503	-0.960	-1.178	-1.423	-1.332	-1.328	ns
MINI-LVDS	GCLK	t_{SU}	—	-0.664	-1.354	-1.428	-1.536	-1.480	-2.245	ns
		t_H	—	0.735	1.496	1.595	1.729	1.660	2.412	ns
	GCLK PLL	t_{SU}	—	0.575	1.106	1.348	1.622	1.517	1.498	ns
		t_H	—	-0.503	-0.960	-1.178	-1.423	-1.332	-1.328	ns
RSDS	GCLK	t_{SU}	—	-0.664	-1.354	-1.428	-1.536	-1.480	-2.245	ns
		t_H	—	0.735	1.496	1.595	1.729	1.660	2.412	ns
	GCLK PLL	t_{SU}	—	0.575	1.106	1.348	1.622	1.517	1.498	ns
		t_H	—	-0.503	-0.960	-1.178	-1.423	-1.332	-1.328	ns

Table 1–103. EP3SE260 Row Pins Input Timing Parameters (Part 2 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	GCLK	t_{SU}	—	-0.588	-1.200	-1.250	-1.356	-1.301	-2.067	ns
		t_H	—	0.660	1.344	1.418	1.550	1.482	2.235	ns
	GCLK PLL	t_{SU}	—	0.693	1.345	1.625	1.903	1.796	1.775	ns
		t_H	—	-0.620	-1.196	-1.454	-1.702	-1.609	-1.604	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	GCLK	t_{SU}	—	-0.588	-1.200	-1.250	-1.356	-1.301	-2.067	ns
		t_H	—	0.660	1.344	1.418	1.550	1.482	2.235	ns
	GCLK PLL	t_{SU}	—	0.693	1.345	1.625	1.903	1.796	1.775	ns
		t_H	—	-0.620	-1.196	-1.454	-1.702	-1.609	-1.604	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	GCLK	t_{SU}	—	-0.595	-1.215	-1.266	-1.372	-1.317	-2.083	ns
		t_H	—	0.667	1.358	1.434	1.566	1.498	2.251	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.609	1.886	1.780	1.759	ns
		t_H	—	-0.613	-1.182	-1.437	-1.685	-1.593	-1.587	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	GCLK	t_{SU}	—	-0.595	-1.215	-1.266	-1.372	-1.317	-2.083	ns
		t_H	—	0.667	1.358	1.434	1.566	1.498	2.251	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.609	1.886	1.780	1.759	ns
		t_H	—	-0.613	-1.182	-1.437	-1.685	-1.593	-1.587	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	GCLK	t_{SU}	—	-0.609	-1.242	-1.298	-1.405	-1.350	-2.115	ns
		t_H	—	0.680	1.385	1.466	1.598	1.530	2.283	ns
	GCLK PLL	t_{SU}	—	0.672	1.303	1.577	1.854	1.747	1.727	ns
		t_H	—	-0.599	-1.155	-1.406	-1.653	-1.561	-1.556	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	GCLK	t_{SU}	—	-0.609	-1.242	-1.298	-1.405	-1.350	-2.115	ns
		t_H	—	0.680	1.385	1.466	1.598	1.530	2.283	ns
	GCLK PLL	t_{SU}	—	0.672	1.303	1.577	1.854	1.747	1.727	ns
		t_H	—	-0.599	-1.155	-1.406	-1.653	-1.561	-1.556	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.595	-1.215	-1.266	-1.372	-1.317	-2.083	ns
		t_H	—	0.667	1.358	1.434	1.566	1.498	2.251	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.609	1.886	1.780	1.759	ns
		t_H	—	-0.613	-1.182	-1.437	-1.685	-1.593	-1.587	ns

Table 1–103. EP3SE260 Row Pins Input Timing Parameters (Part 3 of 3)

IO Standard	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
			Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.595	-1.215	-1.266	-1.372	-1.317	-2.083	ns
		t_H	—	0.667	1.358	1.434	1.566	1.498	2.251	ns
	GCLK PLL	t_{SU}	—	0.686	1.331	1.609	1.886	1.780	1.759	ns
		t_H	—	-0.613	-1.182	-1.437	-1.685	-1.593	-1.587	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	GCLK	t_{SU}	—	-0.609	-1.242	-1.298	-1.405	-1.350	-2.115	ns
		t_H	—	0.680	1.385	1.466	1.598	1.530	2.283	ns
	GCLK PLL	t_{SU}	—	0.672	1.303	1.577	1.854	1.747	1.727	ns
		t_H	—	-0.599	-1.155	-1.406	-1.653	-1.561	-1.556	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	GCLK	t_{SU}	—	-0.609	-1.242	-1.298	-1.405	-1.350	-2.115	ns
		t_H	—	0.680	1.385	1.466	1.598	1.530	2.283	ns
	GCLK PLL	t_{SU}	—	0.672	1.303	1.577	1.854	1.747	1.727	ns
		t_H	—	-0.599	-1.155	-1.406	-1.653	-1.561	-1.556	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	GCLK	t_{SU}	—	-0.633	-1.293	-1.358	-1.464	-1.409	-2.175	ns
		t_H	—	0.703	1.433	1.521	1.653	1.586	2.338	ns
	GCLK PLL	t_{SU}	—	0.627	1.208	1.467	1.743	1.637	1.617	ns
		t_H	—	-0.555	-1.065	-1.299	-1.547	-1.456	-1.449	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	GCLK	t_{SU}	—	-0.633	-1.293	-1.358	-1.464	-1.409	-2.175	ns
		t_H	—	0.703	1.433	1.521	1.653	1.586	2.338	ns
	GCLK PLL	t_{SU}	—	0.627	1.208	1.467	1.743	1.637	1.617	ns
		t_H	—	-0.555	-1.065	-1.299	-1.547	-1.456	-1.449	ns

Table 1–104 specifies EP3SE260 Column Pins Output Timing parameters for differential I/O standards.

Table 1–104. EP3SE260 Column Pins Output Timing Parameters (Part 1 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_1R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns

Table 1–104. EP3SE260 Column Pins Output Timing Parameters (Part 2 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS_E_3R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.283	4.480	5.042	5.360	5.195	5.877	ns
		GCLK PLL	t_{CO}	—	1.062	2.056	2.309	2.251	2.243	2.176	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.211	4.333	4.869	5.185	5.022	5.704	ns
		GCLK PLL	t_{CO}	—	0.990	1.909	2.136	2.076	2.070	2.003	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.203	4.318	4.851	5.167	5.004	5.686	ns
		GCLK PLL	t_{CO}	—	0.982	1.894	2.118	2.058	2.052	1.985	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.203	4.318	4.851	5.167	5.004	5.686	ns
		GCLK PLL	t_{CO}	—	0.982	1.894	2.118	2.058	2.052	1.985	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.204	4.320	4.853	5.169	5.006	5.688	ns
		GCLK PLL	t_{CO}	—	0.983	1.896	2.120	2.060	2.054	1.987	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.203	4.317	4.850	5.166	5.003	5.685	ns
		GCLK PLL	t_{CO}	—	0.982	1.893	2.117	2.057	2.051	1.984	ns
DIFFERENTIAL 1.2-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.200	4.311	4.843	5.159	4.996	5.678	ns
		GCLK PLL	t_{CO}	—	0.979	1.887	2.110	2.050	2.044	1.977	ns

Table 1–104. EP3SE260 Column Pins Output Timing Parameters (Part 3 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.199	4.309	4.840	5.156	4.993	5.675	ns
		GCLK PLL	t_{CO}	—	0.978	1.885	2.107	2.047	2.041	1.974	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.200	4.311	4.843	5.159	4.996	5.678	ns
		GCLK PLL	t_{CO}	—	0.979	1.887	2.110	2.050	2.044	1.977	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.195	4.301	4.831	5.147	4.984	5.666	ns
		GCLK PLL	t_{CO}	—	0.974	1.877	2.098	2.038	2.032	1.965	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.192	4.296	4.825	5.141	4.978	5.660	ns
		GCLK PLL	t_{CO}	—	0.971	1.872	2.092	2.032	2.026	1.959	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.198	4.308	4.839	5.155	4.992	5.674	ns
		GCLK PLL	t_{CO}	—	0.977	1.884	2.106	2.046	2.040	1.973	ns
DIFFERENTIAL 1.5-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.186	4.283	4.810	5.125	4.962	5.645	ns
		GCLK PLL	t_{CO}	—	0.965	1.859	2.077	2.016	2.010	1.944	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.193	4.298	4.827	5.143	4.980	5.662	ns
		GCLK PLL	t_{CO}	—	0.972	1.874	2.094	2.034	2.028	1.961	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.188	4.288	4.816	5.131	4.968	5.651	ns
		GCLK PLL	t_{CO}	—	0.967	1.864	2.083	2.022	2.016	1.950	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.192	4.295	4.824	5.140	4.977	5.659	ns
		GCLK PLL	t_{CO}	—	0.971	1.871	2.091	2.031	2.025	1.958	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.190	4.292	4.820	5.136	4.973	5.655	ns
		GCLK PLL	t_{CO}	—	0.969	1.868	2.087	2.027	2.021	1.954	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.189	4.290	4.818	5.134	4.971	5.653	ns
		GCLK PLL	t_{CO}	—	0.968	1.866	2.085	2.025	2.019	1.952	ns

Table 1–104. EP3SE260 Column Pins Output Timing Parameters (Part 4 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.182	4.275	4.800	5.116	4.953	5.635	ns
		GCLK PLL	t_{CO}	—	0.961	1.851	2.067	2.007	2.001	1.934	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.208	4.328	4.863	5.179	5.016	5.698	ns
		GCLK PLL	t_{CO}	—	0.987	1.904	2.130	2.070	2.064	1.997	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.203	4.318	4.851	5.167	5.004	5.686	ns
		GCLK PLL	t_{CO}	—	0.982	1.894	2.118	2.058	2.052	1.985	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.200	4.312	4.844	5.160	4.997	5.679	ns
		GCLK PLL	t_{CO}	—	0.979	1.888	2.111	2.051	2.045	1.978	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.203	4.318	4.851	5.167	5.004	5.686	ns
		GCLK PLL	t_{CO}	—	0.982	1.894	2.118	2.058	2.052	1.985	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.201	4.314	4.846	5.162	4.999	5.681	ns
		GCLK PLL	t_{CO}	—	0.980	1.890	2.113	2.053	2.047	1.980	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.193	4.297	4.826	5.142	4.979	5.661	ns
		GCLK PLL	t_{CO}	—	0.972	1.873	2.093	2.033	2.027	1.960	ns
DIFFERENTIAL 1.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.195	4.302	4.832	5.148	4.985	5.667	ns
		GCLK PLL	t_{CO}	—	0.974	1.878	2.099	2.039	2.033	1.966	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.206	4.323	4.857	5.173	5.010	5.692	ns
		GCLK PLL	t_{CO}	—	0.985	1.899	2.124	2.064	2.058	1.991	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.199	4.309	4.840	5.156	4.993	5.675	ns
		GCLK PLL	t_{CO}	—	0.978	1.885	2.107	2.047	2.041	1.974	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.201	4.313	4.845	5.161	4.998	5.680	ns
		GCLK PLL	t_{CO}	—	0.980	1.889	2.112	2.052	2.046	1.979	ns

Table 1–104. EP3SE260 Column Pins Output Timing Parameters (Part 5 of 5)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.199	4.310	4.842	5.157	4.995	5.677	ns
		GCLK PLL	t_{CO}	—	0.978	1.886	2.109	2.048	2.043	1.976	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.196	4.303	4.833	5.149	4.986	5.668	ns
		GCLK PLL	t_{CO}	—	0.975	1.879	2.100	2.040	2.034	1.967	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.190	4.292	4.820	5.136	4.973	5.655	ns
		GCLK PLL	t_{CO}	—	0.969	1.868	2.087	2.027	2.021	1.954	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.193	4.298	4.827	5.143	4.980	5.662	ns
		GCLK PLL	t_{CO}	—	0.972	1.874	2.094	2.034	2.028	1.961	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.197	4.305	4.836	5.152	4.989	5.671	ns
		GCLK PLL	t_{CO}	—	0.976	1.881	2.103	2.043	2.037	1.970	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.196	4.303	4.833	5.149	4.986	5.668	ns
		GCLK PLL	t_{CO}	—	0.975	1.879	2.100	2.040	2.034	1.967	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.194	4.299	4.829	5.144	4.981	5.664	ns
		GCLK PLL	t_{CO}	—	0.973	1.875	2.096	2.035	2.029	1.963	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.192	4.296	4.825	5.141	4.978	5.660	ns
		GCLK PLL	t_{CO}	—	0.971	1.872	2.092	2.032	2.026	1.959	ns

Table 1–105 specifies EP3SE260 Row Pins Output Timing parameters for differential I/O standards

Table 1–105. EP3SE260 Row Pins Output Timing Parameters (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
LVDS	-	GCLK	t_{CO}	—	2.259	4.429	4.987	5.300	5.139	5.805	ns
		GCLK PLL	t_{CO}	—	1.038	2.003	2.250	2.189	2.183	2.101	ns
LVDS_E_1R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
LVDS_E_3R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
MINI-LVDS	-	GCLK	t_{CO}	—	2.259	4.429	4.987	5.300	5.139	5.805	ns
		GCLK PLL	t_{CO}	—	1.038	2.003	2.250	2.189	2.183	2.101	ns
MINI-LVDS_E_1R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
MINI-LVDS_E_3R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
RSDS	-	GCLK	t_{CO}	—	2.259	4.429	4.987	5.300	5.139	5.805	ns
		GCLK PLL	t_{CO}	—	1.038	2.003	2.250	2.189	2.183	2.101	ns
RSDS_E_1R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
RSDS_E_3R	-	GCLK	t_{CO}	—	2.258	4.427	4.985	5.297	5.136	5.803	ns
		GCLK PLL	t_{CO}	—	1.037	2.001	2.248	2.186	2.180	2.099	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.189	4.287	4.820	5.129	4.971	5.633	ns
		GCLK PLL	t_{CO}	—	0.974	1.874	2.097	2.034	2.030	1.948	ns

Table 1–105. EP3SE260 Row Pins Output Timing Parameters (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.2-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.181	4.270	4.801	5.110	4.951	5.614	ns
		GCLK PLL	t_{CO}	—	0.966	1.857	2.078	2.015	2.010	1.929	ns
DIFFERENTIAL 1.2-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.180	4.267	4.798	5.106	4.948	5.612	ns
		GCLK PLL	t_{CO}	—	0.965	1.854	2.075	2.011	2.007	1.926	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.179	4.265	4.795	5.104	4.946	5.608	ns
		GCLK PLL	t_{CO}	—	0.964	1.852	2.072	2.009	2.005	1.923	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.178	4.263	4.793	5.101	4.943	5.606	ns
		GCLK PLL	t_{CO}	—	0.963	1.850	2.070	2.006	2.002	1.921	ns
DIFFERENTIAL 1.5-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.173	4.253	4.781	5.089	4.931	5.594	ns
		GCLK PLL	t_{CO}	—	0.958	1.840	2.058	1.994	1.990	1.909	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	4mA	GCLK	t_{CO}	—	2.173	4.253	4.781	5.089	4.931	5.594	ns
		GCLK PLL	t_{CO}	—	0.958	1.840	2.058	1.994	1.990	1.909	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	6mA	GCLK	t_{CO}	—	2.167	4.242	4.768	5.076	4.918	5.581	ns
		GCLK PLL	t_{CO}	—	0.952	1.829	2.045	1.981	1.977	1.896	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	8mA	GCLK	t_{CO}	—	2.169	4.245	4.772	5.080	4.922	5.585	ns
		GCLK PLL	t_{CO}	—	0.954	1.832	2.049	1.985	1.981	1.900	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	10mA	GCLK	t_{CO}	—	2.168	4.244	4.771	5.078	4.921	5.584	ns
		GCLK PLL	t_{CO}	—	0.953	1.831	2.048	1.983	1.980	1.899	ns
DIFFERENTIAL 1.8-V HSTL CLASS I	12mA	GCLK	t_{CO}	—	2.166	4.240	4.766	5.074	4.916	5.579	ns
		GCLK PLL	t_{CO}	—	0.951	1.827	2.043	1.979	1.975	1.894	ns
DIFFERENTIAL 1.8-V HSTL CLASS II	16mA	GCLK	t_{CO}	—	2.157	4.222	4.745	5.053	4.894	5.561	ns
		GCLK PLL	t_{CO}	—	0.942	1.809	2.022	1.957	1.953	1.873	ns

Table 1–105. EP3SE260 Row Pins Output Timing Parameters (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 1.5-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.189	4.286	4.819	5.128	4.969	5.632	ns
		GCLK PLL	t_{CO}	—	0.974	1.873	2.096	2.033	2.028	1.947	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.182	4.271	4.803	5.111	4.953	5.616	ns
		GCLK PLL	t_{CO}	—	0.967	1.858	2.080	2.016	2.012	1.931	ns
DIFFERENTIAL 1.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.178	4.263	4.793	5.101	4.943	5.606	ns
		GCLK PLL	t_{CO}	—	0.963	1.850	2.070	2.006	2.002	1.921	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	4mA	GCLK	t_{CO}	—	2.185	4.278	4.810	5.118	4.960	5.623	ns
		GCLK PLL	t_{CO}	—	0.970	1.865	2.087	2.023	2.019	1.938	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	6mA	GCLK	t_{CO}	—	2.178	4.264	4.794	5.102	4.944	5.607	ns
		GCLK PLL	t_{CO}	—	0.963	1.851	2.071	2.007	2.003	1.922	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.178	4.264	4.794	5.102	4.944	5.607	ns
		GCLK PLL	t_{CO}	—	0.963	1.851	2.071	2.007	2.003	1.922	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	10mA	GCLK	t_{CO}	—	2.177	4.262	4.792	5.100	4.942	5.605	ns
		GCLK PLL	t_{CO}	—	0.962	1.849	2.069	2.005	2.001	1.920	ns
DIFFERENTIAL 1.8-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.173	4.254	4.782	5.090	4.932	5.595	ns
		GCLK PLL	t_{CO}	—	0.958	1.841	2.059	1.995	1.991	1.910	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	8mA	GCLK	t_{CO}	—	2.168	4.244	4.771	5.078	4.921	5.584	ns
		GCLK PLL	t_{CO}	—	0.953	1.831	2.048	1.983	1.980	1.899	ns
DIFFERENTIAL 1.8-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.169	4.246	4.773	5.081	4.923	5.588	ns
		GCLK PLL	t_{CO}	—	0.954	1.833	2.050	1.986	1.982	1.901	ns
DIFFERENTIAL 2.5-V SSTL CLASS I	8mA	GCLK	t_{CO}	—	2.177	4.261	4.791	5.099	4.941	5.604	ns
		GCLK PLL	t_{CO}	—	0.962	1.848	2.068	2.004	2.000	1.919	ns

Table 1–105. EP3SE260 Row Pins Output Timing Parameters (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	Fast Model		-2	-3	-4	-4L		Units
				Industrial	Commercial	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 1.1V	V_{CCL}= 0.9V	
DIFFERENTIAL 2.5-V SSTL CLASS I	12mA	GCLK	t_{CO}	—	2.173	4.253	4.781	5.089	4.931	5.594	ns
		GCLK PLL	t_{CO}	—	0.958	1.840	2.058	1.994	1.990	1.909	ns
DIFFERENTIAL 2.5-V SSTL CLASS II	16mA	GCLK	t_{CO}	—	2.169	4.246	4.773	5.081	4.923	5.586	ns
		GCLK PLL	t_{CO}	—	0.954	1.833	2.050	1.986	1.982	1.901	ns

Table 1–107 through Table 1–107 show EP3SE260 regional clock (RCLK) adder values that should be added to GCLK values. These adder values are used to determine I/O timing when I/O pin is driven using regional clock. This applies for all I/O standards supported by Stratix III.

Table 1–106 specifies EP3SE260 Column Pin delay adders when using the Regional Clock.

Table 1–106. EP3SE260 Column Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
RCLK input adder	—	0.176	0.36	0.385	0.416	0.401	0.555	ns
RCLK PLL input adder	—	0.022	0.042	0.019	-0.012	0.006	0.014	ns
RCLK output adder	—	-0.174	-0.352	-0.379	-0.453	-0.432	-0.597	ns
RCLK PLL output adder	—	0.408	0.878	1.1	1.078	0.966	1.465	ns

Table 1–107 specifies EP3SE260 Row Pin delay adders when using the Regional Clock in Stratix III devices.

Table 1–107. EP3SE260 Row Pin Delay Adders for Regional Clock

Parameter	Fast Model		-2	-3	-4	-4L
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V
RCLK input adder	—	0.182	0.369	0.4	0.429	0.414
RCLK PLL input adder	—	0.013	0.026	0.001	-0.035	-0.017
RCLK output adder	—	-0.182	-0.369	-0.4	-0.429	-0.414
RCLK PLL output adder	—	-0.013	-0.026	-0.001	0.035	0.017

Dedicated Clock Pin Timing

Table 1–109 to Table 1–150 show clock pin timing for Stratix III devices when the clock is driven by global clock, regional clock, periphery clock and a PLL.

Table 1–108 describes Stratix III clock timing parameters.

Table 1–108. Stratix III Clock Timing Parameters

Symbol	Parameter
t_{CIN}	Delay from clock pad to I/O input register
t_{COUT}	Delay from clock pad to I/O output register
t_{PLLCIN}	Delay from PLL `inclk` pad to I/O input register
$t_{PLLCOUT}$	Delay from PLL `inclk` pad to I/O output register

EP3SL70 Clock Timing Parameters

Table 1–109 through Table 1–110 show the global clock timing specifications for EP3SL70 devices.

Table 1–109. EP3SL70 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.274	2.509	2.796	3.051	2.900	3.685	ns
tcout	—	1.274	2.509	2.796	3.051	2.900	3.685	ns
tpllcin	—	0.276	0.540	0.591	0.558	0.524	0.758	ns
tpllcout	—	0.276	0.540	0.591	0.558	0.524	0.758	ns

Table 1–110. EP3SL70 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.204	2.366	2.625	2.859	2.743	3.226	ns
tcout	—	1.077	2.109	2.326	2.510	2.420	2.927	ns
tpllcin	—	0.205	0.399	0.416	0.366	0.360	0.293	ns
tpllcout	—	0.078	0.142	0.117	0.017	0.037	-0.006	ns

Table 1–111 through Table 1–112 show the regional clock timing parameters for EP3SL70 devices.

Table 1–111. EP3SL70 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.176	2.314	2.587	2.808	2.694	3.375	ns
tcout	—	1.176	2.314	2.587	2.808	2.694	3.375	ns
tpllcin	—	0.281	0.550	0.602	0.570	0.535	0.773	ns
tpllcout	—	0.281	0.550	0.602	0.570	0.535	0.773	ns

Table 1–112. EP3SL70 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.115	2.189	2.432	2.648	2.541	2.943	ns
tcout	—	0.988	1.932	2.133	2.299	2.218	2.644	ns
tpllcin	—	0.210	0.409	0.432	0.378	0.371	0.308	ns
tpllcout	—	0.083	0.152	0.133	0.029	0.048	0.009	ns

Table 1–113 through Table 1–114 show the periphery clock timing parameters for EP3SL70 devices.

Table 1–113. EP3SL70 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.894	1.736	1.969	2.153	2.042	2.465	ns
tcout	—	0.894	1.736	1.969	2.153	2.042	2.465	ns
tpllcin	—	0.284	0.604	0.599	0.579	0.613	0.767	ns
tpllcout	—	0.284	0.604	0.599	0.579	0.613	0.767	ns

Table 1–114. EP3SL70 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.826	1.602	1.805	1.968	1.889	2.015	ns
tcout	—	0.699	1.345	1.506	1.619	1.566	1.716	ns
tpllcin	—	0.214	0.461	0.424	0.387	0.456	0.308	ns
tpllcout	—	0.087	0.204	0.125	0.038	0.133	0.009	ns

EP3SL150 Clock Timing Parameters

Table 1–115 through Table 1–116 show the global clock timing parameters for EP3SL150 devices.

Table 1–115. EP3SL150 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.391	2.747	3.048	3.317	3.170	4.045	ns
tcout	—	1.391	2.747	3.048	3.317	3.170	4.045	ns
tpllcin	—	0.256	0.499	0.525	0.450	0.447	0.649	ns
tpllcout	—	0.256	0.499	0.525	0.450	0.447	0.649	ns

Table 1–116. EP3SL150 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.309	2.578	2.855	3.101	2.978	3.563	ns
tcout	—	1.182	2.321	2.556	2.752	2.655	3.264	ns
tpllcin	—	0.174	0.334	0.330	0.235	0.252	0.166	ns
tpllcout	—	0.047	0.077	0.031	-0.114	-0.071	-0.133	ns

Table 1–117 through Table 1–118 show the regional clock timing parameters for EP3SL150 devices.

Table 1–117. EP3SL150 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.238	2.438	2.732	2.956	2.851	3.595	ns
tcout	—	1.238	2.438	2.732	2.956	2.851	3.595	ns
tpllcin	—	0.250	0.489	0.513	0.438	0.435	0.632	ns
tpllcout	—	0.250	0.489	0.513	0.438	0.435	0.632	ns

Table 1–118. EP3SL150 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.177	2.313	2.565	2.788	2.676	3.155	ns
tcout	—	1.050	2.056	2.266	2.439	2.353	2.856	ns
tpllcin	—	0.169	0.322	0.318	0.222	0.237	0.155	ns
tpllcout	—	0.042	0.065	0.019	-0.127	-0.086	-0.144	ns

Table 1–119 through Table 1–120 show the periphery clock timing parameters for EP3SL150 devices.

Table 1–119. EP3SL150 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.928	1.812	2.060	2.241	2.152	2.589	ns
tcout	—	0.928	1.812	2.060	2.241	2.152	2.589	ns
tpllcin	—	0.263	0.515	0.539	0.469	0.461	0.673	ns
tpllcout	—	0.263	0.515	0.539	0.469	0.461	0.673	ns

Table 1–120. EP3SL150 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.786	1.518	1.702	1.852	1.789	1.893	ns
tcout	—	0.659	1.261	1.403	1.503	1.466	1.594	ns
tpllcin	—	0.180	0.346	0.344	0.252	0.268	0.190	ns
tpllcout	—	0.053	0.089	0.045	-0.097	-0.055	-0.109	ns

EP3SL200 Clock Timing Parameters

Table 1–121 through Table 1–122 show the global clock timing parameters for EP3SL200 devices.

Table 1–121. EP3SL200 Global Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.442	2.850	3.164	3.442	3.302	4.211	ns
tcout	—	1.442	2.850	3.164	3.442	3.302	4.211	ns
tpllcin	—	0.268	0.526	0.548	0.475	0.479	0.686	ns
tpllcout	—	0.268	0.526	0.548	0.475	0.479	0.686	ns

Table 1–122. EP3SL200 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1 V	V_{CCL}=1.1 V	V_{CCL}=1.1 V	V_{CCL}=1.1 V	V_{CCL}=0.9 V	
tcin	—	1.378	2.721	3.016	3.271	3.145	3.784	ns
tcout	—	1.251	2.464	2.717	2.922	2.822	3.485	ns
tpllcin	—	0.207	0.401	0.399	0.299	0.320	0.257	ns
tpllcout	—	0.080	0.144	0.100	-0.050	-0.003	-0.042	ns

Table 1–123 through Table 1–124 show the regional clock timing parameters for EP3SL200

Table 1–123. EP3SL200 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.280	2.525	2.812	3.062	2.936	3.709	ns
tcout	—	1.280	2.525	2.812	3.062	2.936	3.709	ns
tpllcin	—	0.263	0.515	0.535	0.460	0.465	0.671	ns
tpllcout	—	0.263	0.515	0.535	0.460	0.465	0.671	ns

Table 1–124. EP3SL200 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.218	2.395	2.662	2.889	2.778	3.283	ns
tcout	—	1.091	2.138	2.363	2.540	2.455	2.984	ns
tpllcin	—	0.202	0.392	0.392	0.292	0.305	0.248	ns
tpllcout	—	0.075	0.135	0.093	-0.057	-0.018	-0.051	ns

Table 1–125 through Table 1–126 show the periphery clock timing parameters for EP3SL200 devices.

Table 1–125. EP3SL200 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.975	1.906	2.154	2.357	2.255	2.716	ns
tcout	—	0.975	1.906	2.154	2.357	2.255	2.716	ns
tpllcin	—	0.271	0.531	0.553	0.477	0.482	0.691	ns
tpllcout	—	0.271	0.531	0.553	0.477	0.482	0.691	ns

Table 1–126. EP3SL200 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.810	1.564	1.770	1.922	1.845	1.978	ns
tcout	—	0.683	1.307	1.471	1.573	1.522	1.679	ns
tpllcin	—	0.209	0.406	0.407	0.309	0.320	0.269	ns
tpllcout	—	0.082	0.149	0.108	-0.040	-0.003	-0.030	ns

EP3SL340 Clock Timing Parameters

Table 1–127 through Table 1–128 show the global clock timing parameters for EP3S340 devices.

Table 1–127. EP3SL340 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.646	3.267	3.580	3.890	3.771	4.793	ns
tcout	—	1.646	3.267	3.580	3.890	3.771	4.793	ns
tpllcin	—	0.303	0.597	0.570	0.461	0.518	0.687	ns
tpllcout	—	0.303	0.597	0.570	0.461	0.518	0.687	ns

Table 1–128. EP3SL340 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.570	3.111	3.422	3.710	3.563	4.370	ns
tcout	—	1.443	2.854	3.123	3.361	3.240	4.071	ns
tpllcin	—	0.224	0.439	0.405	0.271	0.304	0.268	ns
tpllcout	—	0.097	0.182	0.106	-0.078	-0.019	-0.031	ns

Table 1–129 through Table 1–130 show the regional clock timing parameters for EP3S340 devices.

Table 1–129. EP3SL340 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.430	2.828	3.117	3.378	3.228	4.123	ns
tcout	—	1.430	2.828	3.101	3.373	3.228	4.123	ns
tpllcin	—	0.278	0.547	0.553	0.441	0.499	0.667	ns
tpllcout	—	0.278	0.547	0.553	0.441	0.499	0.667	ns

Table 1–130. EP3SL340 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.352	2.669	2.941	3.190	3.063	3.689	ns
tcout	—	1.225	2.412	2.642	2.841	2.740	3.390	ns
tpllcin	—	0.219	0.426	0.386	0.257	0.286	0.244	ns
tpllcout	—	0.092	0.169	0.087	-0.092	-0.037	-0.055	ns

Table 1–131 through Table 1–132 show the periphery clock timing parameters for EP3SL340 devices.

Table 1–131. EP3SL340 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.052	2.062	2.325	2.769	2.430	3.218	ns
tcout	—	1.052	2.062	2.325	2.542	2.430	2.931	ns
tpllcin	—	0.308	0.606	0.571	0.464	0.523	0.695	ns
tpllcout	—	0.308	0.606	0.571	0.464	0.523	0.695	ns

Table 1–132. EP3SL340 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.838	1.624	1.820	1.969	1.896	2.053	ns
tcout	—	0.711	1.367	1.521	1.620	1.573	1.754	ns
tpllcin	—	0.231	0.448	0.403	0.268	0.302	0.276	ns
tpllcout	—	0.104	0.191	0.104	-0.081	-0.021	-0.023	ns

EP3SE50 Clock Timing Parameters

Table 1–133 through Table 1–134 show the global clock timing parameters for EP3SE50 devices.

Table 1–133. EP3SE50 Column Pin Global Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.260	2.480	2.763	3.013	2.889	3.635	ns
tcout	—	1.260	2.480	2.763	3.013	2.889	3.635	ns
tpllcin	—	0.284	0.557	0.615	0.582	0.564	1.053	ns
tpllcout	—	0.284	0.557	0.615	0.582	0.564	0.785	ns

Table 1–134. EP3SE50 Row Pin Global Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.175	2.308	2.579	2.800	2.688	3.156	ns
tcout	—	1.048	2.051	2.280	2.451	2.365	2.857	ns
tpllcin	—	0.199	0.385	0.432	0.376	0.369	0.299	ns
tpllcout	—	0.072	0.128	0.133	0.027	0.046	0.000	ns

Table 1–135 through Table 1–136 show the regional clock timing parameters for EP3SE50 devices.

Table 1–135. EP3SE50 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.169	2.300	2.571	2.800	2.682	3.355	ns
tcout	—	1.169	2.300	2.571	2.800	2.682	3.355	ns
tpllcin	—	0.288	0.566	0.627	0.595	0.574	1.067	ns
tpllcout	—	0.288	0.566	0.627	0.595	0.574	0.799	ns

Table 1–136. EP3SE50 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.096	2.148	2.405	2.609	2.503	2.900	ns
tcout	—	0.969	1.891	2.106	2.260	2.180	2.601	ns
tpllcin	—	0.202	0.391	0.440	0.383	0.375	0.317	ns
tpllcout	—	0.075	0.134	0.141	0.034	0.052	0.018	ns

Table 1–137 through Table 1–138 show the periphery clock timing parameters for EP3SE50 devices.

Table 1–137. EP3SE50 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.897	1.744	1.977	2.160	2.065	2.480	ns
tcout	—	0.897	1.744	1.977	2.160	2.065	2.480	ns
tpllcin	—	0.291	0.619	0.617	0.601	0.658	0.792	ns
tpllcout	—	0.291	0.619	0.617	0.601	0.658	0.792	ns

Table 1–138. EP3SE50 Row Pin Periphery Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L	-4L	Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.820	1.587	1.802	1.957	1.878	2.007	ns
tcout	—	0.693	1.330	1.503	1.608	1.555	1.708	ns
tpllcin	—	0.208	0.452	0.435	0.391	0.459	0.313	ns
tpllcout	—	0.081	0.195	0.136	0.042	0.136	0.014	ns

EP3SE110 Clock Timing Parameters

Table 1–139 through Table 1–140 show the global clock timing parameters for EP3SE110 devices.

Table 1–139. EP3SE110 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.390	2.745	3.050	3.318	3.179	4.048	ns
tcout	—	1.390	2.745	3.050	3.318	3.179	4.048	ns
tpllcin	—	0.253	0.493	0.520	0.446	0.447	0.647	ns
tpllcout	—	0.253	0.493	0.520	0.446	0.447	0.647	ns

Table 1–140. EP3SE110 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.310	2.581	2.867	3.108	2.985	3.573	ns
tcout	—	1.183	2.324	2.568	2.759	2.662	3.274	ns
tpllcin	—	0.173	0.332	0.335	0.236	0.253	0.168	ns
tpllcout	—	0.046	0.075	0.036	-0.113	-0.070	-0.131	ns

Table 1–141 through Table 1–142 show the regional clock timing parameters for EP3SE110 devices.

Table 1–141. EP3SE110 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.247	2.458	2.742	2.984	2.826	3.607	ns
tcout	—	1.247	2.458	2.742	2.984	2.826	3.607	ns
tpllcin	—	0.248	0.483	0.508	0.433	0.434	0.631	ns
tpllcout	—	0.248	0.483	0.508	0.433	0.434	0.631	ns

Table 1–142. EP3SE110 Row Pin Regional Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.176	2.312	2.576	2.796	2.683	3.164	ns
tcout	—	1.049	2.055	2.277	2.447	2.360	2.865	ns
tpllcin	—	0.167	0.319	0.323	0.223	0.239	0.153	ns
tpllcout	—	0.040	0.062	0.024	-0.126	-0.084	-0.146	ns

Table 1–143 through Table 1–144 show the periphery clock timing parameters for EP3SE110 devices.

Table 1–143. EP3SE110 Column Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.943	1.841	2.086	2.281	2.157	2.623	ns
tcout	—	0.943	1.841	2.086	2.281	2.157	2.623	ns
tpllcin	—	0.261	0.508	0.536	0.463	0.463	0.670	ns
tpllcout	—	0.261	0.508	0.536	0.463	0.463	0.670	ns

Table 1–144. EP3SE110 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.778	1.500	1.694	1.835	1.761	1.885	ns
tcout	—	0.651	1.243	1.395	1.486	1.438	1.586	ns
tpllcin	—	0.180	0.346	0.349	0.251	0.267	0.193	ns
tpllcout	—	0.053	0.089	0.050	-0.098	-0.056	-0.106	ns

EP3SE260 Clock Timing Parameters

Table 1–145 through Table 1–146 show the global clock timing parameters for EP3SE260 devices.

Table 1–145. EP3SE260 Column Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.520	3.009	3.337	3.627	3.479	4.442	ns
tcout	—	1.520	3.009	3.337	3.627	3.479	4.442	ns
tpllcin	—	0.289	0.568	0.582	0.495	0.506	0.722	ns
tpllcout	—	0.289	0.568	0.582	0.495	0.506	0.722	ns

Table 1–146. EP3SE260 Row Pin Global Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.455	2.878	3.188	3.454	3.320	4.021	ns
tcout	—	1.328	2.621	2.889	3.105	2.997	3.722	ns
tpllcin	—	0.225	0.438	0.436	0.327	0.349	0.294	ns
tpllcout	—	0.098	0.181	0.137	-0.022	0.026	-0.005	ns

Table 1–147 through Table 1–148 show the regional clock timing parameters for EP3SE260 devices.

Table 1–147. EP3SE260 Column Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.341	2.646	2.943	3.202	3.070	3.876	ns
tcout	—	1.341	2.646	2.943	3.202	3.070	3.876	ns
tpllcin	—	0.283	0.555	0.568	0.479	0.489	0.700	ns
tpllcout	—	0.283	0.555	0.568	0.479	0.489	0.700	ns

Table 1–148. EP3SE260 Row Pin Regional Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.277	2.515	2.792	3.030	2.909	3.462	ns
tcout	—	1.150	2.258	2.493	2.681	2.586	3.163	ns
tpllcin	—	0.218	0.425	0.421	0.308	0.333	0.277	ns
tpllcout	—	0.091	0.168	0.122	-0.041	0.010	-0.022	ns

Table 1–149 through Table 1–150 show the periphery clock timing parameters for EP3SE260 devices.

Table 1–149. EP3SE260 Column Pin Periphery Clock timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	1.010	1.977	2.235	2.441	2.337	2.808	ns
tcout	—	1.010	1.977	2.235	2.441	2.337	2.808	ns
tpllcin	—	0.292	0.574	0.589	0.503	0.513	0.726	ns
tpllcout	—	0.292	0.574	0.589	0.503	0.513	0.726	ns

Table 1–150. EP3SE260 Row Pin Periphery Clock Timing Specifications

Parameter	Fast Model		-2	-3	-4	-4L		Units
	Industrial	Commercial	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=1.1V	V_{CCL}=0.9V	
tcin	—	0.823	1.592	1.800	1.958	1.877	2.017	ns
tcout	—	0.696	1.335	1.501	1.609	1.554	1.718	ns
tpllcin	—	0.228	0.445	0.441	0.329	0.354	0.304	ns
tpllcout	—	0.101	0.188	0.142	-0.020	0.031	0.005	ns

Glossary

Table 1–151 shows the glossary for this chapter.

Table 1–151. Glossary Table

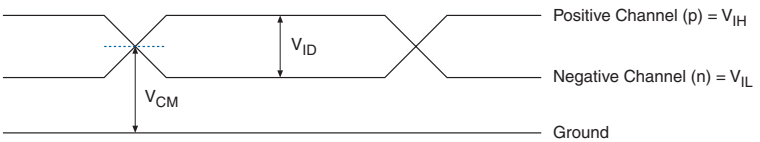
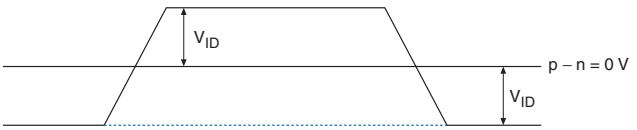
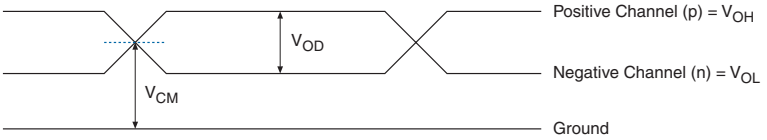
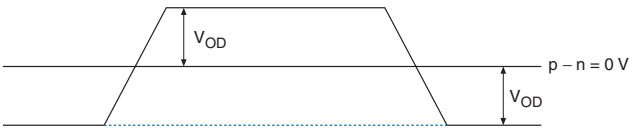
Letter	Subject	Definitions
A	—	—
B	—	—
C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—

Table 1–151. Glossary Table

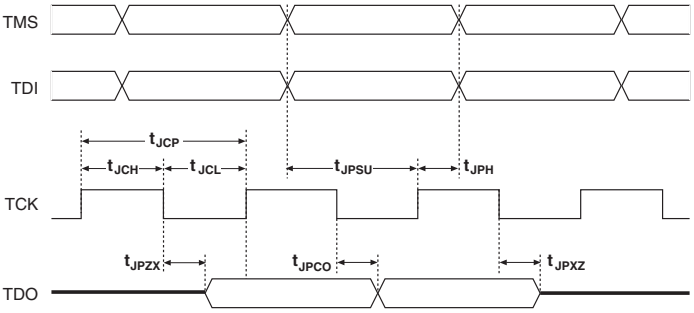
Letter	Subject	Definitions
F	f_{HSCLK}	HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency.
	f_{HSDR}	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G	—	—
H	—	—
I	—	—
J	J	HIGH-SPEED I/O Block: Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications are in the following figure: 
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—

Table 1–151. Glossary Table

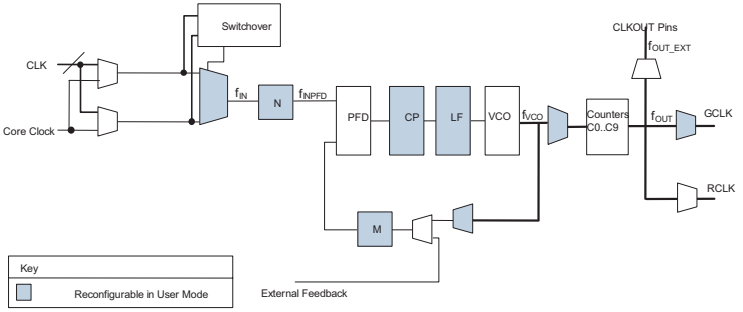
Letter	Subject	Definitions
P	PLL Specifications	The block diagram shown in the following figure highlights the PLL Specification parameters: *Diagram of PLL Specifications* 
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Stratix III device).

Table 1–151. Glossary Table

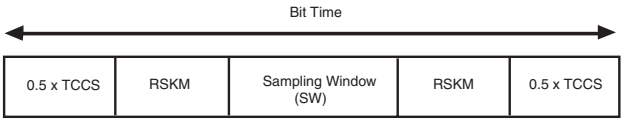
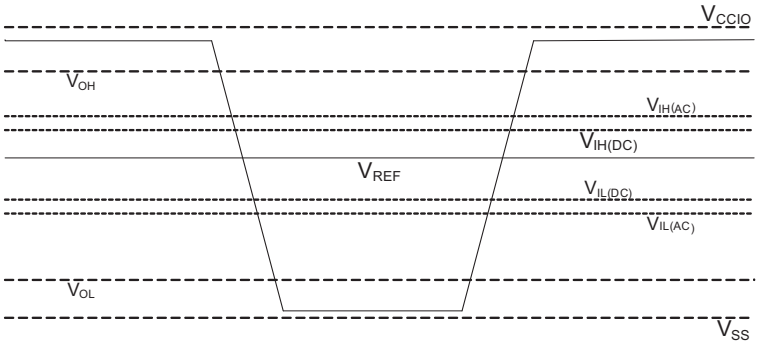
Letter	Subject	Definitions
S	SW (sampling window)	The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window (the following figure): *Timing Diagram* 
	Single-ended Voltage Referenced I/O Standard	The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the AC value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing (The following figure): *Single-Ended Voltage Referenced I/O Standard* 

Table 1–151. Glossary Table

Letter	Subject	Definitions
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **S** in this table)
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock. Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal High-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on PLL clock input
	t_{OUTPJ_IO}	Period jitter on general purpose I/O driven by a PLL
	t_{OUTPJ_DC}	Period jitter on dedicated clock output driven by a PLL
	t_{RISE}	Signal Low-to-high transition time (20-80%)
U	—	—
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential Input Voltage: Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
W	W	HIGH-SPEED I/O BLOCK: Clock Boost Factor
X	—	—

Table 1–151. Glossary Table		
Letter	**Subject**	**Definitions**
Y	—	—
Z	—	—
	—	—

Document Revision History

Table 1–152 shows the revision history for this document.

Table 1–152. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
May 2007 v1.3	Added new contact information table to the About this Handbook section.	—
May 2007 v1.2	Updated Table 1–37 through Table 1–150.	Update
March 2007 v1.1	Added I/O Timing section	—
November 2006 v1.0	Initial Release	—