Cyclone III Device Handbook, Volume 1

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About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® III family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.

Visual Cue	Meaning
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section 1. Device Core

This section provides a complete overview of all features relating to the Cyclone® III device family, which is the most architecturally advanced, high-performance, low-power FPGA in the market place. This section includes the following chapters:

- Chapter 1, Cyclone III Device Family Overview
- Chapter 2, Logic Elements and Logic Array Blocks in Cyclone III Devices
- Chapter 3, MultiTrack Interconnect in Cyclone III Devices
- Chapter 4, Memory Blocks in Cyclone III Devices
- Chapter 5, Embedded Multipliers in Cyclone III Devices
- Chapter 6, Clock Networks and PLLs in Cyclone III Devices

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

1. Cyclone III Device Family Overview

CIII51001-1.1

Cyclone III: Lowest System-Cost FPGAs

The Cyclone® III FPGA family offered by Altera is a cost-optimized, memory-rich FPGA family. Cyclone III FPGAs are built on TSMC's 65-nm low-power (LP) process technology with additional silicon optimizations and software features to minimize power consumption. With this third generation in the Cyclone series, Altera broadens the number of high volume, cost-sensitive applications that can benefit from FPGAs.

This chapter contains the following sections:

- "Cyclone III Device Features" on page 1–1
- "Cyclone III Device Architecture" on page 1–4
- "Reference and Ordering Information" on page 1–9
- "Reference and Ordering Information" on page 1–9

Cyclone III Device Features

Cyclone III devices are designed to offer low-power consumption and increased system integration at reduced cost.

Reduced Cost

Cyclone III devices deliver the lowest device and system costs based on the following facts:

- Staggered I/O ring to lower die area
- Wide range of low cost packages
- Support for low-cost serial flash and commodity parallel flash devices for configuration

Lowest-Power 65-nm FPGA

Cyclone III devices are the lowest-power 65-nm FPGAs designed via TSMC's 65-nm low power process and Altera's power aware design flow. Cyclone III devices support hot-socketing operation; therefore, unused I/O banks can be powered down when the devices to which they are connected are turned off. Benefits of the Cyclone III device's low-power operation include:

- Extended battery life for portable and handheld applications
- Enabled operation in thermally challenged environments
- Eliminated or reduced cooling system costs

Increased System Integration

Cyclone III devices provide increased system integration by offering the following features:

- Density is up to 119,088 logic elements (LEs) and memory is up to 3.8 Mbits. Refer to Table 1–1 on page 1–2.
- High memory to logic ratio for embedded DSP applications
- Highest multiplier-to-logic ratio in the industry at every density; 260 MHz multiplier performance
- High I/O count, low- and mid-range density devices for user I/O constrained applications
- Up to four phase-locked loops (PLLs) provide robust clock management and synthesis for device clocks, external system clocks, and I/O interfaces
  - Up to five outputs per PLL
  - Cascadable to save I/Os, ease PCB routing, and reduce the number of external reference clocks needed
  - Dynamically reconfigurable to change phase shift, frequency multiplication/division, and input frequency in-system without reconfiguring the device

- Support for high-speed external memory interfaces including DDR, DDR2, SDR SDRAM, and QDRII SRAM at up to 400 Mbps
  - Auto-calibrating physical layer (PHY) feature accelerates timing closure process and eliminates variations over process, voltage and temperature (PVT) for DDR, DDR2, SDRAM, and QDRII SRAM interfaces
- Up to 534 user I/O pins arranged in 8 I/O banks that support a wide range of industry I/O standards
  - Up to 875 Mbps receive and 840 Mbps transmit LVDS communications
  - LVDS, RSDS®, mini-LVDS and PPDS® transmission without the use of external resistors
  - Supported I/O standards include LVTTL, LVCMOS, SSTL, HSTL, PCI, PCI-X, LVPECL, LVDS, mini-LVDS, RSDS, and PPDS; PCI Express and Serial Rapid I/O are supported using external PHY devices
- Multi-value on-chip termination (OCT) support with calibration feature to eliminate variations over PVT
- Adjustable I/O slew rates to improve signal integrity
- Support for low-cost Altera® serial flash and commodity parallel flash configuration devices from Intel
- Remote system upgrade feature without requiring an external controller
- Dedicated Cyclic Redundancy Code (CRC) checker circuitry to detect single event upset (SEU) conditions
- Nios® II embedded processors for Cyclone III devices offer low cost and custom-fit embedded processing solutions
- Broad portfolio of pre-built and verified intellectual property cores from Altera and Altera Megafunction Partners Program (AMPP℠) partners

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Table 1–1 displays Cyclone III device family features.

Table 1–1. Cyclone III FPGA Device Family Features

Feature	EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Logic Elements	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
Memory (Kbits)	414	414	504	594	1,134	2,340	2,745	3,888
Multipliers	23	23	56	66	126	156	244	288
PLLs	2	2	4	4	4	4	4	4
Global Clock Networks	10	10	20	20	20	20	20	20

All Cyclone III devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. This allows designers to optimize density and cost as the design evolves.

Table 1–2 lists the Cyclone III device package options and user I/O pin counts. The highest I/O count in the family is delivered by the EP3C40.

Table 1–2. Cyclone III FPGA Package Options and I/O Pin Counts Notes (1), (2), (3)

Device	144-pin Plastic Enhanced Quad Flat Pack (EQFP) (5)	240-pin Plastic Quad Flat Pack (PQFP)	256-pin FineLine Ball-Grid Array (FBGA)	256-pin Ultra FineLine Ball-Grid Array (UBGA)(6)	324-pin FineLine Ball-Grid Array (FBGA)	484-pin FineLine Ball-Grid Array (FBGA)	484-pin Ultra FineLine Ball-Grid Array (UBGA)(6)	780-pin FineLine Ball-Grid Array (FBGA)
EP3C5	94	—	182	182	—	—	—	—
EP3C10	94	—	182	182	—	—	—	—
EP3C16	84	160	168	168	—	346	346	—
EP3C25	82	148	156	156	215	—	—	—
EP3C40	—	128	—	—	195	331	331	535 (4)
EP3C55	—	—	—	—	—	327	327	377
EP3C80	—	—	—	—	—	295	295	429
EP3C120	—	—	—	—	—	283	—	531

Notes to Table 1–2:

(1) For more information about Device Packaging Specifications, refer to the support section of the Altera website. (**http://www.altera.com/support/devices/packaging/specifications/pkg-pin/spe-index.html**).

(2) The numbers are the maximum I/O counts (including clock input pins) supported by the device-package combination and can be affected by the configuration scheme selected for the device.

(3) All the packages available in lead-free and leaded options.

(4) The EP3C40 device in the F780 package supports restricted vertical migration. Maximum user I/O is restricted to 510 I/Os if you enable migration to the EP3C120 and are using voltage referenced I/O standards. If you are not using voltage referenced I/O standards the maximum number of I/Os can be increased.

(5) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity and not for thermal purposes.

(6) All the UBGA packages will be supported starting in Quartus II v7.1 SP1 except for the UBGA packages of EP3C16 which will be supported starting in Quartus II v7.2

Table 1–3 lists the Cyclone III FPGA package sizes.

Table 1–3. Cyclone III FPGA Package Sizes

Dimensions	144-pin EQFP	240-pin PQFP	256-pin FBGA	256-pin UBGA	324-pin FBGA	484-pin FBGA	484-pin UBGA	780-pin FBGA
Pitch (mm)	0.5	0.5	1.0	0.8	1.0	1.0	0.8	1.0
Nominal Area (mm^2)	484	1197	289	196	361	529	361	841
Length \ Width (mm \ mm)	22 \ 22	34.6 \ 34.6	17 \ 17	14 \ 14	19 \ 19	23 \ 23	19 \ 19	29 \ 29
Height (mm)	1.60	4.10	1.55	2.20	2.20	2.60	2.20	2.60

Cyclone III devices are available in up to three speed grades: –6, –7, and –8 (–6 is the fastest). Table 1–4 shows Cyclone III device speed grade offerings.

Table 1–4. Cyclone III Devices Speed Grades

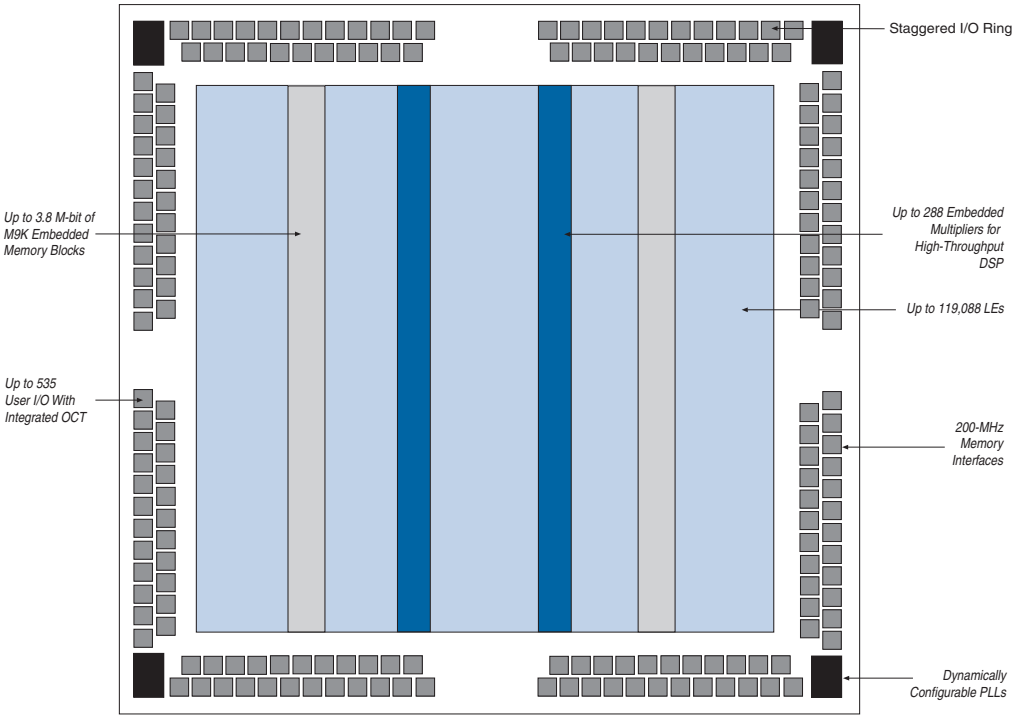
Device	144-pin EQFP	240-pin PQFP	256-pin FBGA	256-pin UBGA	324-pin FBGA	484-pin FBGA	484-pin UBGA	780-pin FBGA
EP3C5	–7, –8	—	–6, –7, –8	–6, –7, –8	—	—	—	—
EP3C10	–7, –8	—	–6, –7, –8	–6, –7, –8	—	—	—	—
EP3C16	–7, –8	–8	–6, –7, –8	–6, –7, –8	—	–6, –7, –8	–6, –7, –8	—
EP3C25	–7, –8	–8	–6, –7, –8	–6, –7, –8	–6, –7, –8	—	—	—
EP3C40	—	–8	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C55	—	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C80	—	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8
EP3C120	—	—	—	—	—	–7, –8	—	–7, –8

Cyclone III Device Architecture

Cyclone III FPGAs include a customer-defined feature set optimized for cost-sensitive applications and offer a wide range of density, memory, embedded multiplier, I/O, and packaging options. Cyclone III FPGAs support numerous external memory interfaces and I/O protocols common in high-volume applications.

Figure 1–1 shows a floor plan view of the Cyclone III device architecture.

Figure 1–1. Cyclone III Device Architecture Overview *Note (1)*



Note to Figure 1–1:
(1) EP3C5 and EP3C10 have only 2 PLLs

LEs and LABs

The logic array block (LAB) consists of 16 logic elements (LEs) and a LAB-wide control block. An LE is the smallest unit of logic in the Cyclone III device architecture. Each LE has four inputs, a 4-input look-up-table (LUT), a register, and output logic. The 4-input LUT is a function generator that can implement any function of four variables.

For more information, refer to the *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook.*

MultiTrack Interconnect

In the Cyclone III device architecture, interconnections between LEs, LABs, M9K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure which is a fabric of routing wires. The MultiTrack interconnect structure consists of performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus® II software automatically optimizes designs by placing the critical path on the fastest interconnects.

For more information, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Memory Blocks

Each Cyclone III FPGA M9K memory block provides up to 9 kbits of on-chip memory capable of operation at up to 260 MHz. The embedded memory structure consists of columns of M9K memory blocks that can be configured as RAM, first-in first-out (FIFO) buffers, or ROM. Cyclone III memory blocks are optimized for applications such as high throughput packet processing, high definition (HD) line buffers for video processing functions, and embedded processor program and data storage. The Quartus II software allows you to take advantage of M9K memory blocks by instantiating memory using a dedicated megafunction wizard, or by inferring memory directly from VHDL or Verilog source code.

Table 1–5. Cyclone III Memory Modes

Port Mode	Port Width Configuration
Single Port	x1, x2, x4, x8, x9, x16, x18, x32 and x36
Simple Dual Port	x1, x2, x4, x8, x9, x16, x18, x32 and x36
True Dual Port	x1, x2, x4, x8, x9, x16 and x18

For more information, refer to the *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*.

Embedded Multipliers and Digital Signal Processing Support

Cyclone III devices offer up to 288 embedded multiplier blocks and support the following modes: one individual 18 × 18-bit multiplier per block, or two individual 9 × 9-bit multipliers per block. The Quartus II software includes megafunctions that are used to control the mode of operation of the embedded multiplier blocks based on user parameter settings. Multipliers can also be inferred directly from VHDL or Verilog source code.

In addition to embedded multipliers, Cyclone III FPGAs include a combination of on-chip resources and external interfaces that make them ideal to increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. Cyclone III FPGAs can be used alone or as DSP device co-processors to improve price-to-performance ratios of DSP systems.

Cyclone III FPGA DSP system design support includes the following features:

- DSP IP cores, which include:
  - Common DSP processing functions, such as finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
  - Suites of common video and image processing functions
- Complete reference designs for end-market applications
- DSP Builder interface tool between The MathWorks Simulink and MATLAB design environment, and Quartus II software
- DSP development kits

For more information, refer to the *Embedded Multipliers* chapter in volume 1 of the *Cyclone III Device Handbook*.

I/O Features

All Cyclone III devices contain eight I/O banks. All I/O banks support the single-ended and differential I/O standards listed in Table 1–6.

Table 1–6. Cyclone III FPGA I/O Standards Support *Note (1)*

Type	I/O Standard
Single-Ended I/O	• LVTTL • LVCMOS • SSTL • HSTL • PCI • PCI-X
Differential I/O	• SSTL • HSTL • LVPECL • LVDS • mini-LVDS • RSDS • PPDS

Note to Table 1–6:
(1) PCI Express and Serial Rapid I/O can be supported using an external PHY device.

The Cyclone III device I/O also supports programmable bus hold, programmable pull-up and pull-down resistors, programmable slew rate control to optimize signal integrity, and hot socketing. Cyclone III devices support calibrated on-chip series termination (OCT) or driver impedance matching (Rs) for single-ended I/O standards with one OCT calibration block per side.

For more information, refer to the *Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Clock Networks and PLLs

Cyclone III FPGAs include up to 20 global clock networks. Global clock signals can be driven from dedicated clock pins, dual-purpose clock pins, user logic, and PLLs. Cyclone III FPGAs include up to four PLLs with five outputs per PLL to provide robust clock management and synthesis. PLLs can be used for device clock management, external system clock management, and I/O interfaces.

Cyclone III PLLs can be dynamically reconfigured to enable auto-calibration of external memory interfaces while the device is in operation. This feature also enables support of multiple input source frequencies and corresponding multiplication, division, and phase shift requirements. PLLs in Cyclone III devices may be cascaded to generate up to ten internal clocks and two external clocks on output pins from a single external clock source.

For PLL specifications and information, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* and the *Clock Networks and PLLs* chapters in the *Cyclone III Device Handbook*.

High-Speed Differential Interfaces

Cyclone III FPGAs support high-speed differential interfaces, such as LVDS, mini-LVDS, RSDS, and PPDS. These high-speed I/O standards in Cyclone III FPGAs are ideal for low-cost applications by providing high data throughput using a relatively small number of I/O pins. All device I/O banks contain LVDS receivers that operate at up to 875 Mbps data rates. Dedicated differential output drivers on the left and right I/O banks can transmit at up to 840 Mbps data rates without the need for any external resistors to save board space and simplify PCB routing. Top and bottom I/O banks support differential transmit functionality with the addition of an external resistor network at up to 640 Mbps data rates.

For more information, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Auto-Calibrating External Memory Interfaces

Cyclone III devices support common memory types including DDR, DDR2, SDR SDRAM, and QDRII SRAM. The DDR2 SDRAM memory interfaces support data rates of up to 400 Mbps. Memory interfaces are supported on all sides of the Cyclone III FPGA. The Cyclone III FPGA contains features such as on-chip termination, DDR output registers, and 8- to 36-bit programmable `DQ` group widths to enable rapid and robust implementation of different memory standards.

An auto-calibrating megafunction is available in the Quartus II software for DDR and QDR memory interface PHYs. The megafunction is optimized to take advantage of the Cyclone III I/O structure, simplify timing closure requirements, and take advantage of the Cyclone III PLL dynamic reconfiguration feature to calibrate over process, voltage and temperature changes.

For more information, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

Quartus II Software Support

The Quartus II software is the number one design software for performance and productivity. It is the industry's only complete design solution for CPLDs, FPGAs, and structured ASICs. The Quartus II software includes an integrated development environment to accelerate system-level design and seamless integration with leading third-party software tools and flows. Cyclone III FPGAs are supported by both the subscription and free Quartus II Web Edition software.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

Nios II—World's Most Versatile Embedded Processor

Cyclone III devices support the Nios® II embedded processor, which allows you to implement custom-fit embedded processing solutions. Cyclone III devices can also expand the peripheral set, memory, I/O, or performance of embedded processors. Single or multiple Nios II embedded processors can be designed into a Cyclone III device to provide additional co-processing power, or even replace existing embedded processors in your system. Using Cyclone III and Nios II together allows for low-cost, high-performance embedded processing solutions, which in turn allows you to extend your product's life cycle and improve time-to-market over standard product solutions.

Configuration

Cyclone III devices use SRAM cells to store configuration data. Configuration data is downloaded to Cyclone III devices each time the device powers up. Low-cost configuration options include Altera EPCS family serial flash devices, as well as parallel flash configuration options using commodity Intel devices. These options provide flexibility for general-purpose applications and the ability to

meet specific configuration and wake up time requirements of applications, such as the 100 ms requirement in many automotive applications. Wake up time can be adjusted by choosing a configuration option and selecting a fast or standard power-on-reset time.

For more information, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

Remote System Upgrades

Cyclone III devices offer remote system upgrades without an external controller. Remote system upgrade capability in Cyclone III devices allows deployment of system upgrades from a remote location. Soft logic (either the Nios II embedded processor or user logic) implemented in a Cyclone III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This feature supports serial and parallel flash configuration topologies.

For more information, refer to the *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*.

Hot Socketing and Power-On-Reset

Cyclone III devices feature hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of external devices. You can insert or remove a board populated with one or more Cyclone III devices during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot socketing feature allows you to use FPGAs on printed circuit boards (PCBs) that also contain a mixture of 3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.2 V devices. The Cyclone III device's hot socketing feature eliminates power-up sequence requirements for other devices on the board for proper FPGA operation.

For more information, refer to the *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*.

SEU Mitigation

Cyclone III devices offer built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory (CRAM) cells. This feature allows all CRAM contents to be read and verified to match a configuration-computed CRC value. The Quartus II software activates the Cyclone III built-in 32-bit CRC checker.

For more information, refer to the *SEU Mitigation* chapter in volume 1 of the *Cyclone III Device Handbook*.

JTAG Boundary Scan Testing

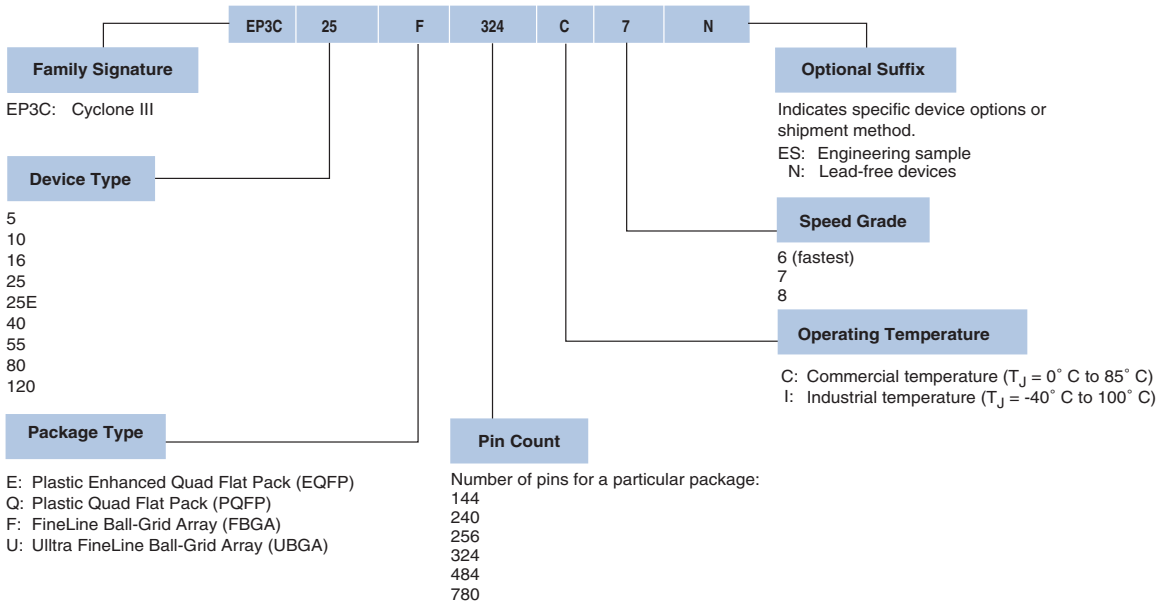
Cyclone III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the Cyclone III device can force signals onto pins or capture data from pins or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Cyclone III device in-circuit reconfiguration (ICR).

For more information, refer to *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

Reference and Ordering Information

Figure 1–2 describes the ordering codes for Cyclone III devices.

Figure 1–2. Cyclone III Device Packaging Ordering Information



Referenced Documents

This chapter references the following documents:

- *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Clock Networks and PLLs* chapter in volume 1 of the *Cyclone III Device Handbook*
- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Quartus II Handbook*
- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*
- *SEU Mitigation* chapter in volume 1 of the *Cyclone III Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 1–7 shows the revision history for this document.

Table 1–7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Removed the text "Spansion" in "Increased System Integration" and "Configuration" sections. • Removed trademark symbol from "MultiTrack" in "MultiTrack Interconnect". • Removed registered trademark symbol from "Simulink" and "MATLAB" from "Embedded Multipliers and Digital Signal Processing Support" section. • Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release.	—

2. Logic Elements and Logic Array Blocks in Cyclone III Devices

CIII51002-1.1

Introduction

This chapter contains feature definitions for logic elements (LEs) and logic array blocks (LABs). It provides details on how an LE works, how LABs contain groups of LEs, and how LABs interface with the other blocks in Cyclone® III devices.

This chapter contains the following sections:

- "Logic Elements" on page 2–1
- "LE Operating Modes" on page 2–4
- "Logic Array Blocks" on page 2–6
- "LAB Control Signals" on page 2–7

Overview

The logic array consists of LABs, with 16 LEs in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone III devices range from 5,136 to 119,088 LEs.

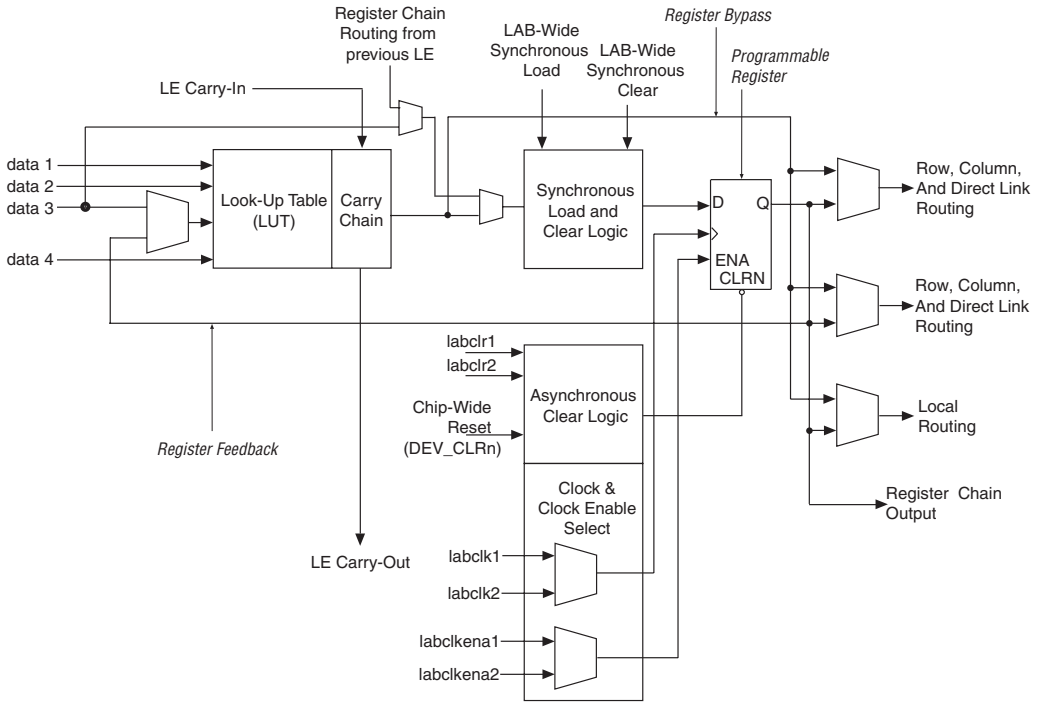
Logic Elements

The smallest unit of logic in the Cyclone III architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE features:

- A four-input look-up table (LUT), which can implement any function of four variables
- A programmable register
- A carry chain connection
- A register chain connection
- The ability to drive all types of interconnects: local, row, column, register chain, and direct link interconnects
- Support for register packing
- Support for register feedback

Figure 2–1 shows a Cyclone III LE.

Figure 2–1. Cyclone III LE



LE Features

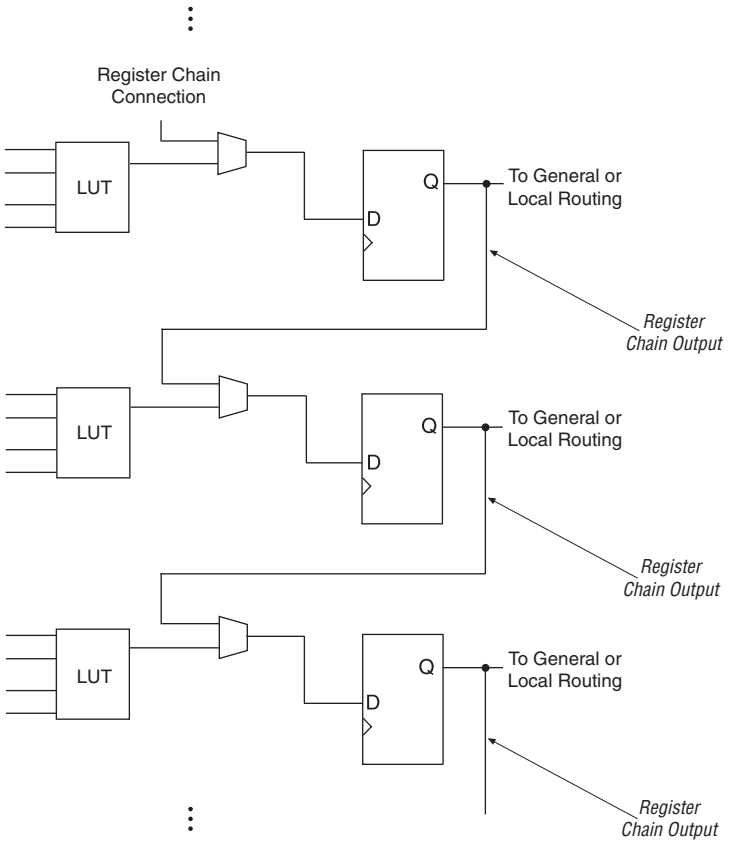
You can configure each LE's programmable register for D, T, JK, or SR flip-flop operation. Each register has data, clock, clock enable, and clear inputs. Signals that use the global clock network, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. When using register packing, the LAB-wide synchronous load control signal is not available. Refer to "LAB Control Signals" on page 2–7 for more information about the synchronous load control signal.

Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT, providing another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

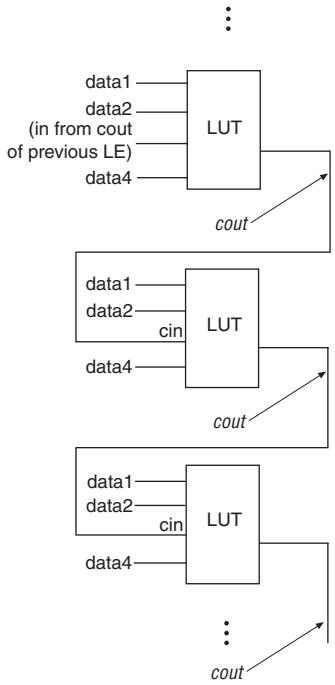
In addition to the three general routing outputs, the LEs within a LAB have register chain outputs. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows the LUTs to be used for combinational functions and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. Figure 2–2 shows a register cascading among LEs in Cyclone III devices.

Figure 2–2. LE Register Cascade



The LUT carry chain may connect to other LUTs from different LEs. The LE carry chain feature is achieved by connecting an LE carry-out to the next LE carry-in. LE carry chains can span more than 16 LEs by using the LAB carry-in and LAB carry-out. Figure 2–3 shows LE carry chains.

Figure 2–3. LE Carry Chains



LE Operating Modes

The Cyclone III LE operates in normal or arithmetic mode.

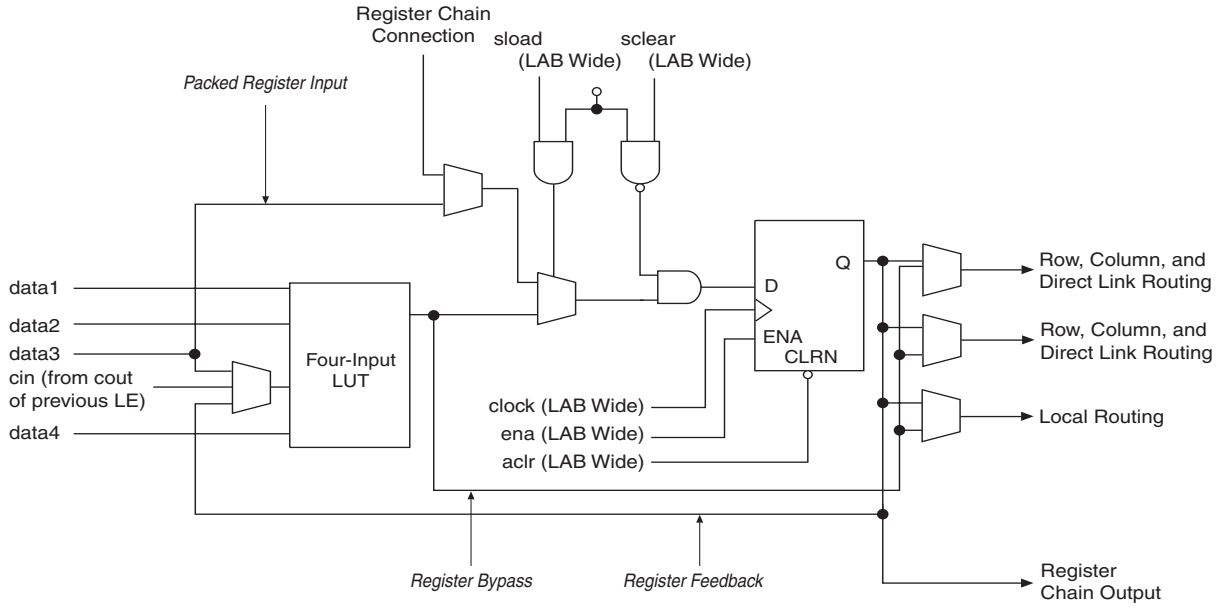
LE operating modes use LE resources differently. In each mode, there are six available inputs to the LE. These inputs include the four data inputs from the LAB local interconnect, the LE carry-in from the previous carry-chain LE, and the register chain connection. Each input is directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

In conjunction with parameterized functions such as the library of parameterized modules (LPM) functions, the Quartus® II software chooses the appropriate mode for common functions, such as counters, adders, subtractors, and arithmetic functions, automatically. If required, you can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (Figure 2–4). The Quartus II Compiler automatically selects the carry-in (`cin`) or the `data3` signal as one of the inputs to the LUT. LEs in normal mode support packed registers and register feedback.

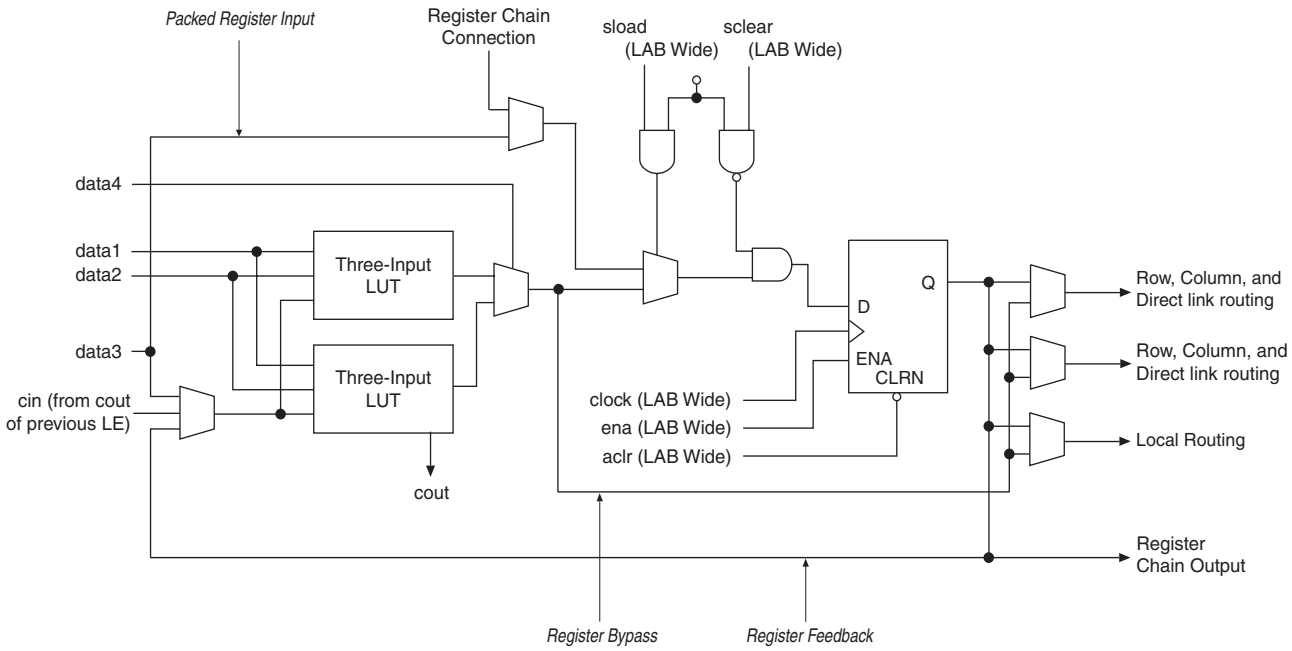
Figure 2–4. LE in Normal Mode



Arithmetic Mode

The arithmetic mode is ideal for implementing adders, counters, accumulators, and comparators. An LE in arithmetic mode implements a 2-bit full adder and basic carry chain (Figure 2–5). LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output. Register feedback and register packing are supported when LEs are used in arithmetic mode.

Figure 2–5. LE in Arithmetic Mode



The Quartus II Compiler automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions, such as LPM functions, take advantage of carry chains for the appropriate functions automatically.

The Quartus II Compiler creates carry chains longer than 16 LEs by automatically linking LABs in the same column. For enhanced fitting, a long carry chain runs vertically, which allows fast horizontal connections to M9K memory blocks or embedded multipliers through direct link interconnects. For example, if a design has a long carry chain in a LAB column next to a column of M9K memory blocks, any LE output can feed an adjacent M9K memory block through the direct link interconnect. If the carry chains ran horizontally, any LAB not next to the column of M9K memory blocks would use other row or column interconnects to drive a M9K memory block. A carry chain continues as far as a full column.

Logic Array Blocks

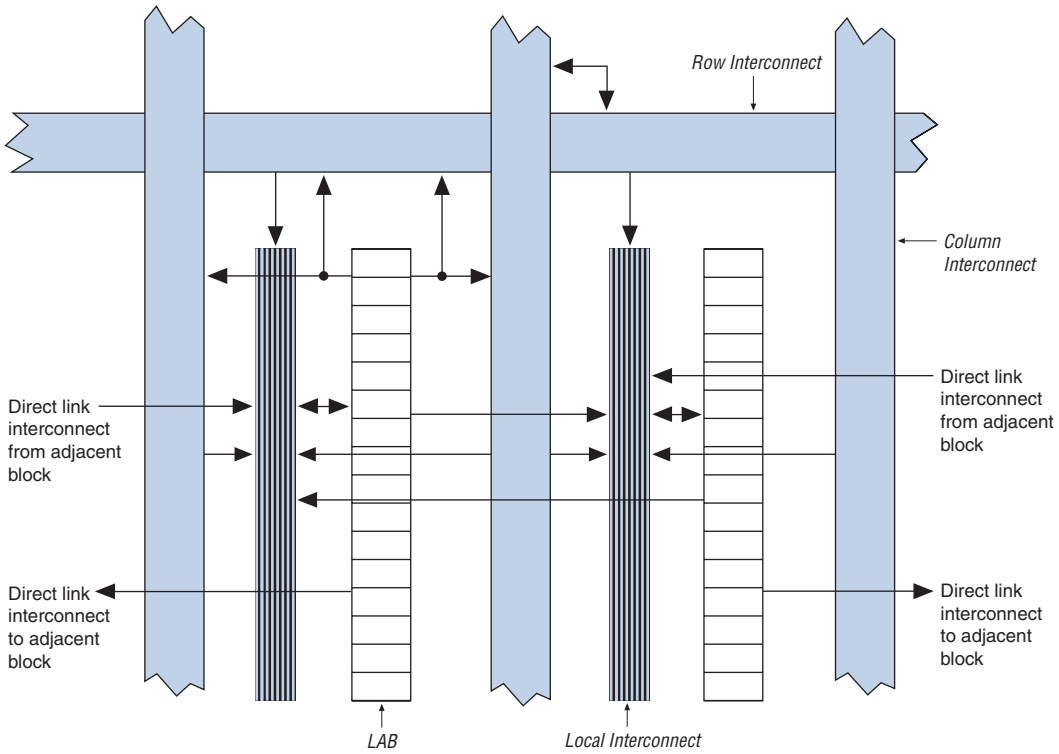
Topology

Each LAB consists of the following:

- 16 LEs
- LAB control signals
- LE carry chains
- Register chains
- Local interconnect

The local interconnect transfers signals between LEs in the same LAB. Register chain connections transfer the output of one LE register to the adjacent LE register within a LAB. The Quartus II Compiler places associated logic within a LAB or adjacent LABs, allowing the use of local, and register chain connections for performance and area efficiency. Figure 2–6 shows the Cyclone III LAB.

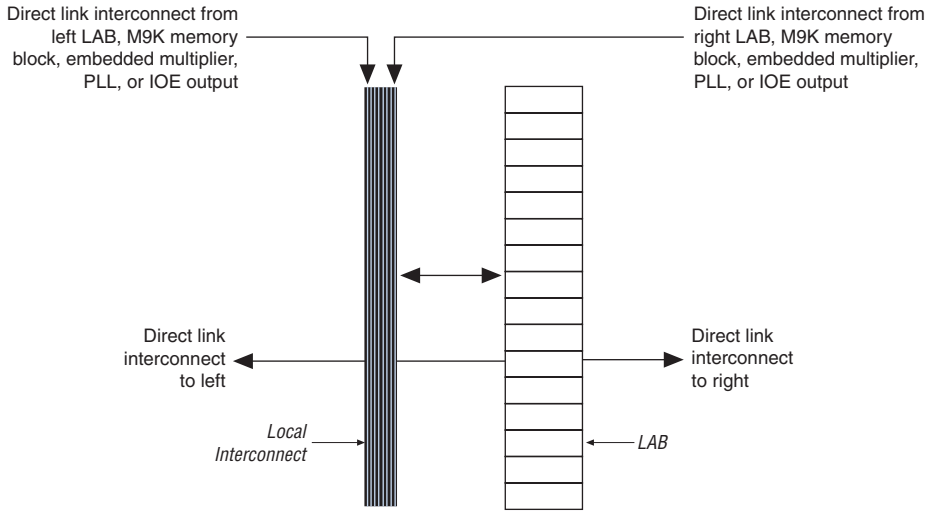
Figure 2–6. Cyclone III LAB Structure



LAB Interconnects

LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, PLLs, M9K RAM blocks, and embedded multipliers from the left and right can also drive the local interconnect of a LAB through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive up to 48 LEs through fast local and direct link interconnects. Figure 2–7 shows the direct link connection.

Figure 2–7. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include:

- Two clocks
- Two clock enables
- Two asynchronous clears
- One synchronous clear
- One synchronous load

You may use up to eight control signals at a time. Register packing and the synchronous load cannot be used simultaneously.

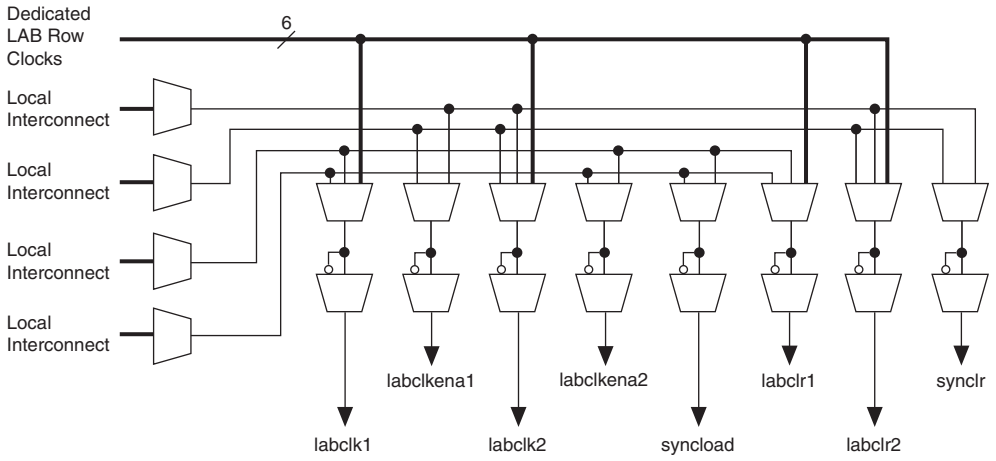
Each LAB can have up to four non-global control signals. You can use additional LAB control signals as long as they are global signals.

Synchronous clear and load signals are useful for implementing counters and other functions. The synchronous clear and synchronous load signals are LAB-wide signals that affect all registers in the LAB.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

The LAB row clocks `[5..0]` and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data distribution. Figure 2–8 shows the LAB control signal generation circuit.

Figure 2–8. LAB-Wide Control Signals



LAB-wide signals control the logic for the register's clear signal. The LE directly supports an asynchronous clear function. Each LAB supports up to two asynchronous clear signals (`labclr1` and `labclr2`).

A LAB-wide asynchronous load signal to control the logic for the register's preset signal is not available. The register preset is achieved by using a NOT gate push-back technique. Cyclone III devices can only support either a preset or asynchronous clear signal.

In addition to the clear port, Cyclone III devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

Conclusion

Cyclone III device LEs and LABs enable you to keep pace with increasing design complexity using a low-cost FPGA device family. The Quartus II software makes it easy to implement Cyclone III device designs in LEs and LABs, making the process invisible to you, thus freeing you from the complexity of LEs and LABs.

Document Revision History

Table 2–1 shows the revision history for this document.

Table 2–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	Removed trademark symbol from "MultiTrack" in "LAB Control Signals" section.	—
March 2007 v1.0	Initial Release.	—

3. MultiTrack Interconnect in Cyclone III Devices

CIII51003-1.1

Introduction

This Cyclone® III handbook chapter, *MultiTrack Interconnect in Cyclone III Devices*, provides in-depth information about the routing architecture of Cyclone III devices. This document explains the connections between each functional block in Cyclone III devices.

This chapter contains the following section:

"MultiTrack Interconnect" on page 3–1

MultiTrack Interconnect

In the Cyclone III device architecture, connections between LEs, M9K memory blocks, embedded multipliers, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different speeds used for inter- and intra-design block connectivity. The Quartus® II Compiler automatically places critical paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row (direct link, R4, and R24) and column (register chain, C4, and C16) interconnects that span fixed distances. A routing structure with fixed-length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

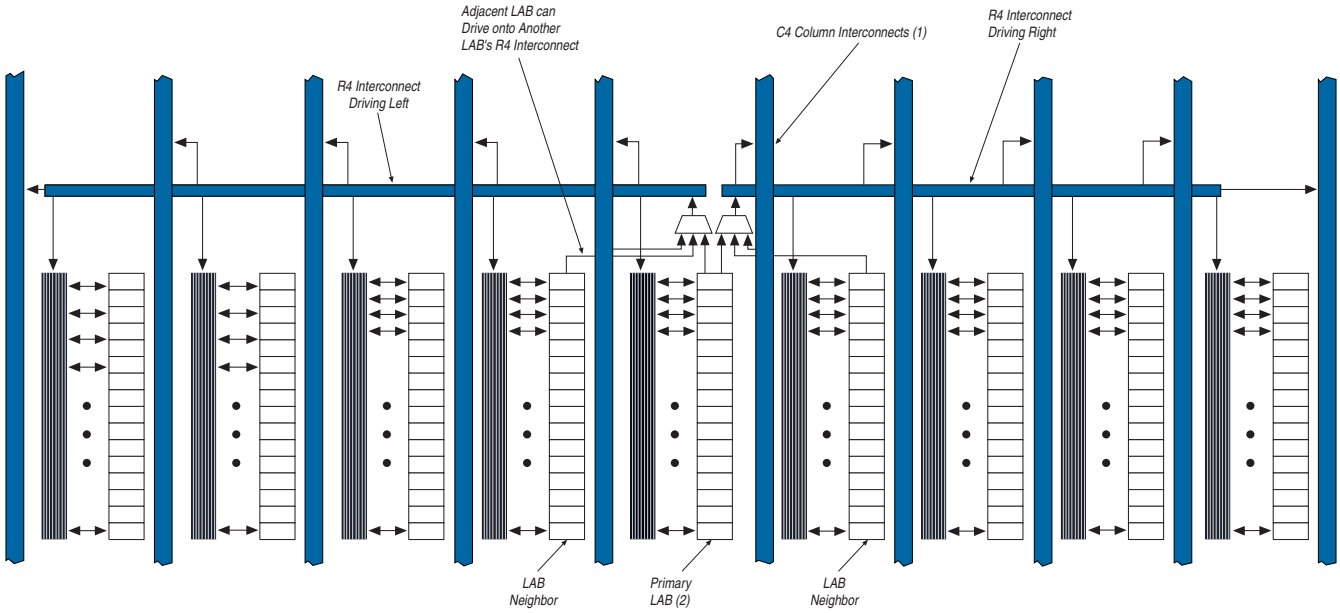
Row interconnects route signals to and from logic array blocks (LABs), phase-locked loops (PLLs), M9K memory blocks, and embedded multipliers within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R24 interconnects for high-speed access across the length of the device

The direct link interconnect allows blocks to drive into the local interconnect of its left and right neighbors. The direct link interconnect provides fast communication between adjacent blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs, and one M9K memory block, or three LABs and one embedded multiplier to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 3–1 shows R4 interconnect connections from a LAB. The R4 interconnects can drive and be driven by LABs, M9K memory blocks, embedded multipliers, PLLs, and row input/output elements (IOEs). For LAB interfacing, a primary LAB or LAB neighbor (Figure 3–1) can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. Additionally, R4 interconnects can drive R24 interconnects, C4, and C16 interconnects for connections from one row to another.

Figure 3–1. R4 Interconnect Connections *Notes (1), (2), (3)*



Notes to Figure 3–1:

(1) The C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

(3) The R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between non-adjacent LABs, M9K memory blocks, dedicated multipliers, and row IOEs. R24 row interconnects drive to other row or column interconnects at every fourth LAB. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects and do not drive directly to LAB local interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

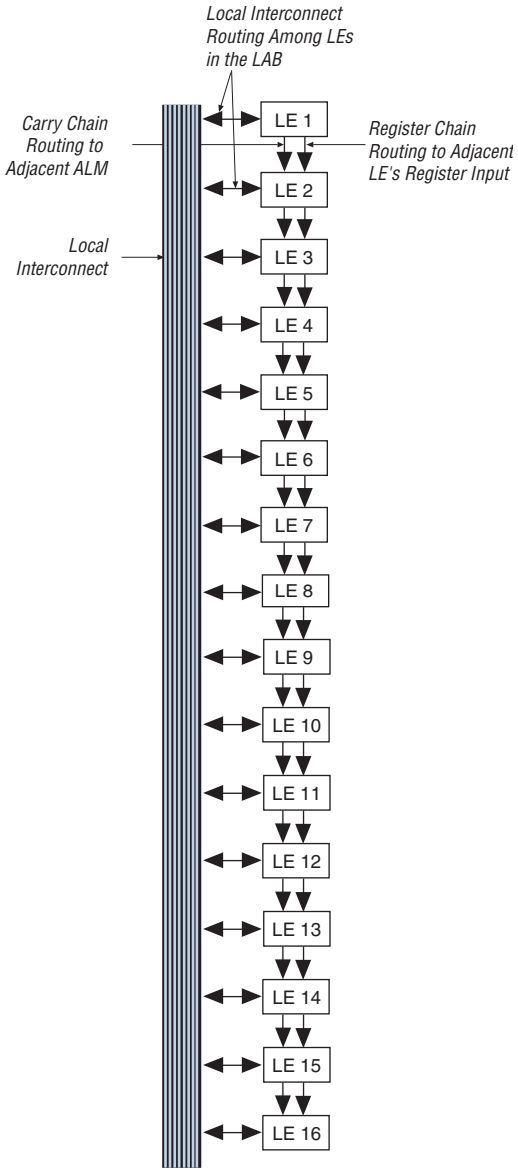
Column Interconnects

The column interconnect operates similar to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, M9K memory blocks, embedded multipliers, and row and column I/O elements. These column resources include:

- Register chain interconnects within a LAB
- C4 interconnects traversing a distance of four blocks in an up or down direction
- C16 interconnects for high-speed vertical routing through the device

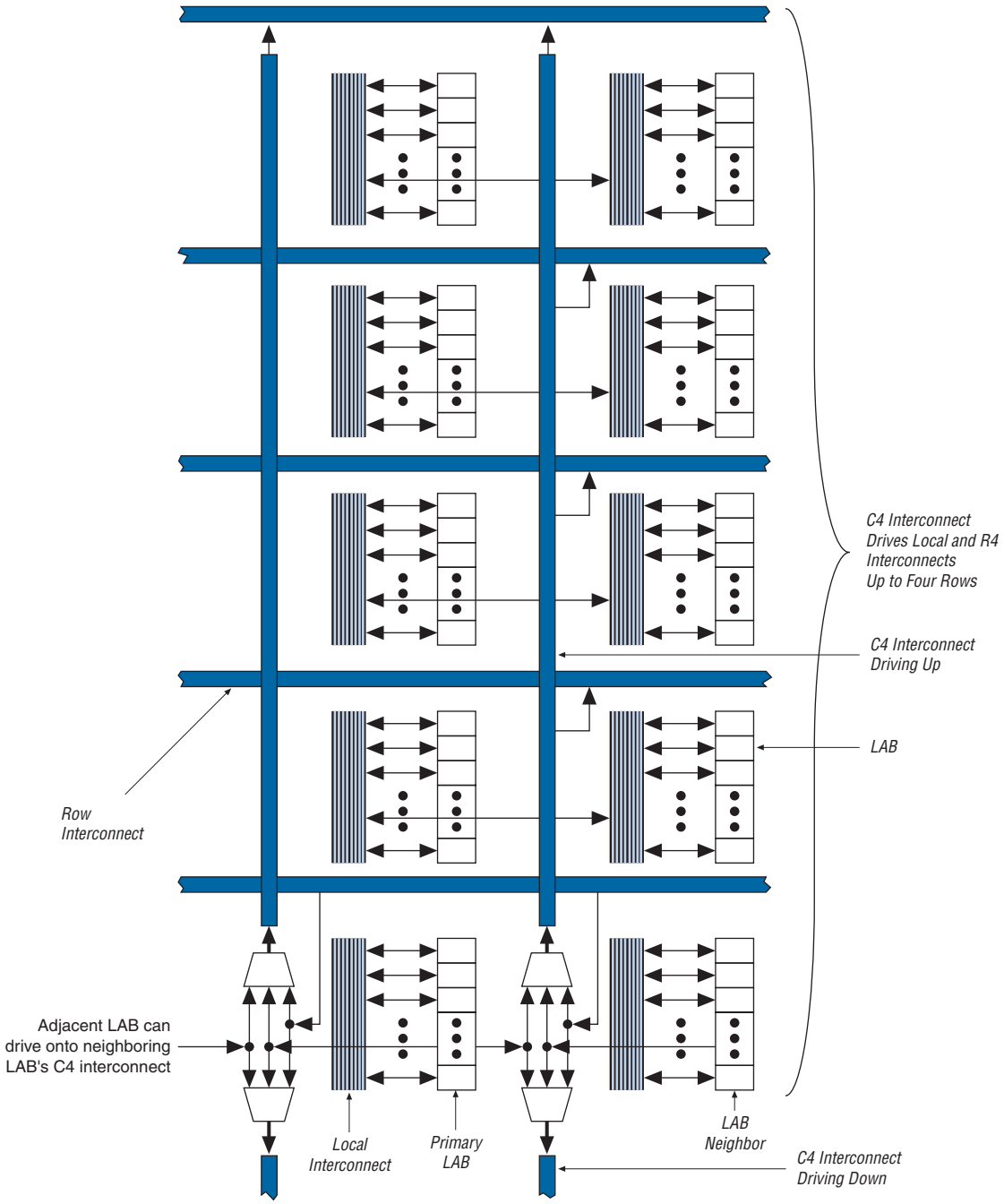
Cyclone III devices include an enhanced interconnect structure within LABs to route logic element (LE) outputs to LE input connections faster by using register chain connections. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus® II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 3–2 shows the register chain interconnects.

Figure 3–2. Register Chain Interconnects



The C4 interconnects span four blocks up or down from a source LAB, M9K block, or embedded multiplier. Every LAB, M9K block, or embedded multiplier has its own set of C4 interconnects to drive either up or down. Figure 3–3 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including M9K memory blocks, embedded multiplier blocks, and column and row I/O elements. The C4 interconnect can be driven by the two neighboring LABs or blocks (Figure 3–3). The C4 interconnects can drive both blocks to extend their range and drive blocks to the left or right for column-to-column connections.

Figure 3–3. C4 Interconnect Connections *Notes (1), (2)*



Notes to Figure 3–3:

(1) Each C4 interconnect can drive either up or down four rows.

(2) The C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, M9K memory blocks, embedded multipliers, and I/O elements. The C16 column interconnects drive to other row and column interconnects at every fourth LAB. The C16 column interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly. The C16 interconnects can drive R24, R4, C16, and C4 interconnects.

Device Routing

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (for example, M9K memory, embedded multiplier, or PLL) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 3–1 shows the Cyclone III device routing scheme.

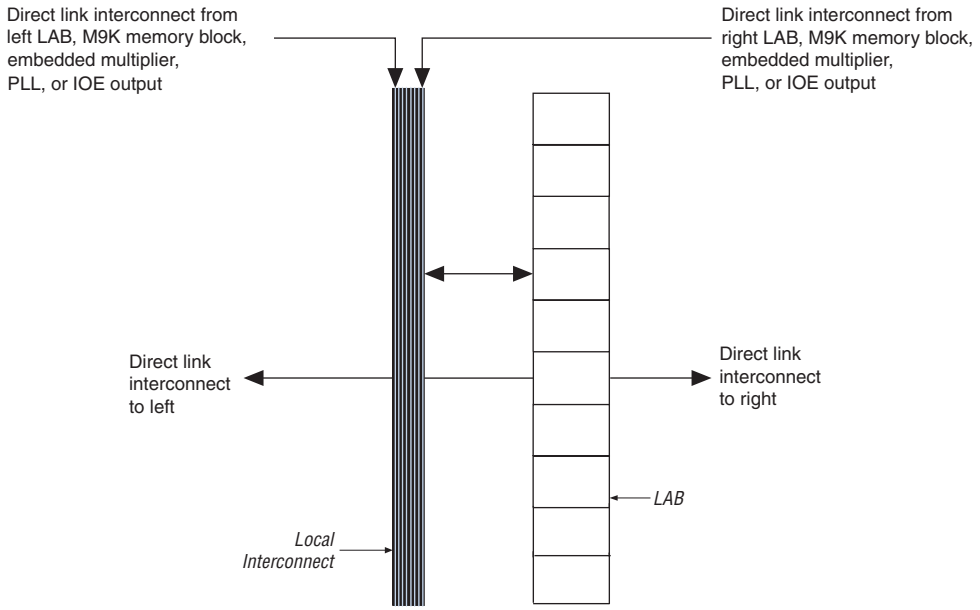
Table 3–1. Cyclone III Device Routing Scheme

Source	Destination											
	Register Chain	Local	Direct Link	R4	R24	C4	C16	LE	M9K RAM Block	Embedded Multiplier	Column IOE	Row IOE
Register Chain	—	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	—	✓	✓	✓	✓	✓
Direct Link Interconnect	—	✓	—	—	—	—	—	—	—	—	—	—
R4 Interconnect	—	✓	—	✓	✓	✓	✓	—	—	—	—	—
R24 Interconnect	—	—	—	✓	✓	✓	✓	—	—	—	—	—
C4 Interconnect	—	✓	—	✓	✓	✓	✓	—	—	—	—	—
C16 Interconnect	—	—	—	✓	✓	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	—	✓	—	—	—	—	—	—
M9K Memory Block	—	✓	✓	✓	—	✓	—	—	—	—	—	—
Embedded Multiplier	—	✓	✓	✓	—	✓	—	—	—	—	—	—
Column I/O Element	—	—	—	—	—	✓	✓	—	—	—	—	—
Row I/O Element	—	—	✓	✓	✓	✓	—	—	—	—	—	—

LAB Local Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 48 LEs through fast local and direct link interconnects. Figure 3–4 shows the direct link connection.

Figure 3–4. Direct Link Connection

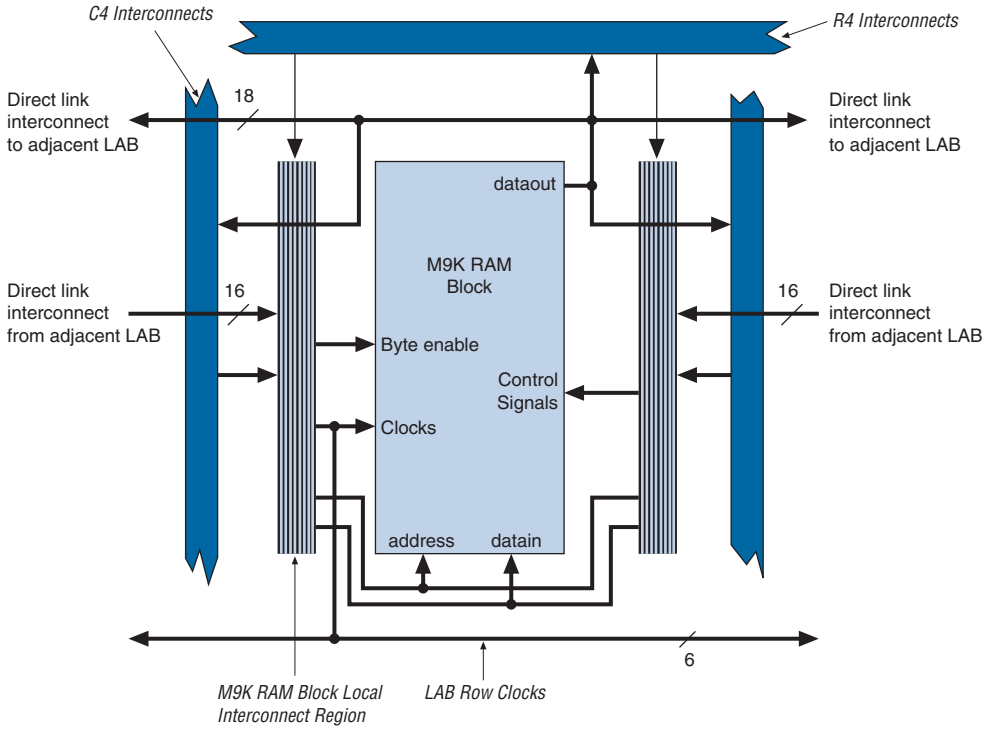


Refer to the *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook* for more information about Cyclone III LABs and LEs.

M9K Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs or blocks drive the M9K block local interconnect. The M9K blocks can communicate with LABs or blocks on either the left or right side through these row resources, or with LAB columns on either left or right with the column resources. Up to 16 direct link input connections to the M9K block are possible from the left adjacent LAB and another 16 possible from the right adjacent LAB. The M9K block outputs can also connect to left and right LABs through each 18 direct link interconnects. Figure 3–5 shows the M9K block to logic array interface.

Figure 3–5. M9K RAM Block LAB Row Interface

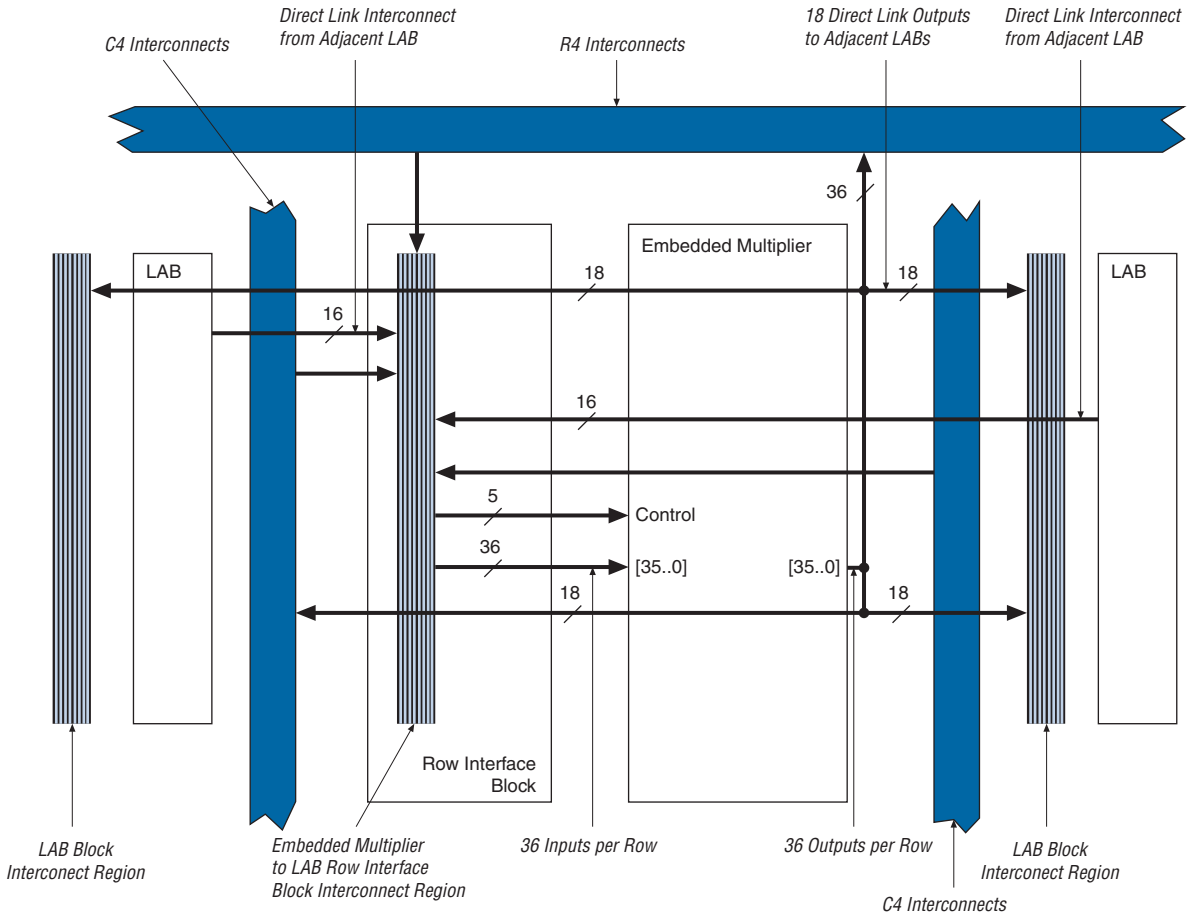


Refer to the *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook* for more information about Cyclone III embedded memory blocks.

Embedded Multiplier Routing Interface

The R4, C4, and direct link interconnects from adjacent LABs drive the embedded multiplier row interface interconnect. The embedded multipliers can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 16 direct link input connections to the embedded multiplier are possible from the left adjacent LABs and another 16 possible from the right adjacent LAB. Embedded multiplier outputs can also connect to left and right LABs through 18 direct link interconnects each. Figure 3–6 shows the embedded multiplier to logic array interface.

Figure 3–6. Embedded Multiplier LAB Row Interface



There are five dynamic control input signals that feed the embedded multiplier:

- `signa`
- `signb`
- `clk`
- `clkena`
- `aclr`

The `signa` and `signb` signals can be registered to match the data signal input path. The `clk`, `clkena`, and `aclr` signals feed all registers within a single embedded multiplier.

Refer to the *Embedded Multipliers* chapter in volume 1 of the *Cyclone III Device Handbook* for more information about Cyclone III embedded multipliers.

Conclusion

The Cyclone III device provides fast and optimal performance interconnections between LEs, M9K memory blocks, embedded multipliers, and device I/O pins. The Quartus II software provides the most suitable routing interconnects for your design to deliver optimum performance.

Referenced Documents

This chapter references the following documents:

- *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Embedded Multipliers* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 3–2 shows the revision history for this document.

Table 3–2. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Removed trademark symbol from “DirectDrive” in “MultiTrack Interconnect” section. • Added chapter TOC and “Referenced Documents” section.	—
March 2007 v1.0	Initial Release.	—

4. Memory Blocks in Cyclone III Devices

CIII51004-1.1

Introduction

Cyclone® III devices feature embedded memory structures to address the on-chip memory needs of Altera® Cyclone III device designs. The embedded memory structure consists of columns of M9K memory blocks that you can configure to provide various memory functions, such as RAM, shift registers, ROM, and first-in first-out (FIFO) buffers. M9K memory blocks provide up to 3.98 Mbit of RAM at a maximum of 260 MHz for synchronous operation (refer to Table 4–2 for total RAM bits-per-density).

This chapter contains the following sections:

- "Memory Modes" on page 4–7
- "Clocking Modes" on page 4–13
- "Design Considerations" on page 4–21

Overview

The M9K blocks support the following features:

- Up to 3.98 Mbit of RAM available without reducing available logic
- 8,192 memory bits per block (9,216 bits per block including parity)
- Independent read-enable and write-enable signals for each port
- Packed mode in which the M9K memory block is split into two 4.5 K single-port RAMs
- Variable port configurations
- Single-port and simple dual-port modes support for all port widths
- True dual-port (one read and one write, two reads, or two writes) operation
- Byte enables for data input masking during writes
- Two clock-enable control signals for each port (port A and port B)
- Initialization file to pre-load content of memory in RAM and ROM modes
- Up to 260 MHz for synchronous only operation

Table 4–1 summarizes the features supported by the M9K memory.

Table 4–1. Summary of M9K Memory Features (Part 1 of 2)

Feature	M9K Blocks
Maximum performance	260 MHz
Total RAM bits (including parity bits)	9,216
Configurations (depth × width)	8192 × 1 4096 × 2 2048 × 4 1024 × 8 1024 × 9 512 × 16 512 × 18 256 × 32 256 × 36
Parity bits	✓
Byte enable	✓
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓

Table 4–1. Summary of M9K Memory Features (Part 2 of 2)

Feature	M9K Blocks
Embedded shift register mode *(1)*	✓
ROM mode	✓
FIFO buffer *(1)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support *(2)*	✓
Memory initialization file (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write/Read operation triggering	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to “Old Data” or “New Data”
Mixed-port read-during-write	Outputs set to “Old Data” or “Don’t Care”

Notes to Table 4–1:

(1) FIFO buffers and embedded shift registers that require external logic elements (LEs) for implementing control logic.

(2) Width modes of ×32 and ×36 are not available.

Table 4–2 shows the capacity and distribution of the M9K memory blocks in each Cyclone III device family member.

Table 4–2. Number of M9K Blocks in Cyclone III Devices

Device	Number of M9K Blocks	Total RAM Bits
EP3C5	46	423,936
EP3C10	46	423,936
EP3C16	56	516,096
EP3C25	66	608,256
EP3C40	126	1,161,216
EP3C55	260	2,396,160
EP3C80	305	2,810,880
EP3C120	432	3.981,312

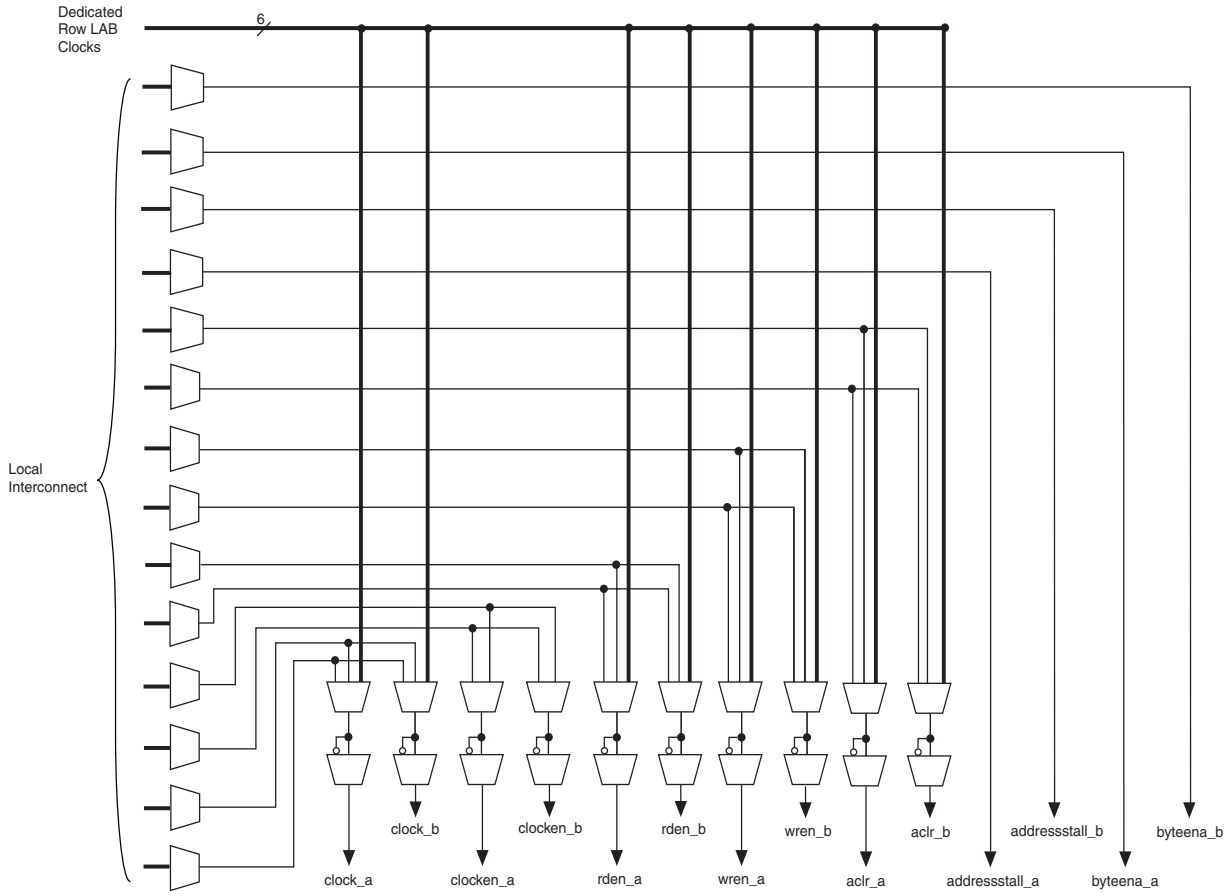
Control Signals

Figure 4–1 shows how the register clocks, clears, and control signals are implemented in the Cyclone III memory block.

The clock-enable control signal controls clock entering for the entire memory block, not just the input and output registers. This signal disables the clock so that the memory block does not see any clock edges and will not perform any operations.

The read-enable (`rden`) and write-enable (`wren`) control signals control the read and write operations for each port of the memory blocks. You can disable read-enable or write-enable signals independently to save power whenever the operation is not required.

Figure 4–1. M9K Control Signal Selection



Parity Bit Support

Parity checking for error detection is possible by using the parity bit along with internal logic resources. Cyclone III M9K memory blocks support a parity bit for each storage byte. You can use this bit optionally as a parity bit or as an additional data bit. No parity function is actually performed on this bit.

Byte Enable Support

Cyclone III M9K memory blocks support byte enables that mask the input data so that only specific bytes of data are written. The unwritten bytes retain the previous written value. The write enable (`wren`) signals, along with the byte enable (`byteena`) signals, control the RAM block's write operations. The default value for the byte-enable signals is high (enabled), in which case writing is controlled only by the write-enable signals. There is no clear port to the byte-enable registers. M9K blocks support byte enables when the write port has a data width of ×16, ×18, ×32, or ×36 bits.

Byte enables operate in one-hot manner, with the least significant bit (LSB) of the `byteena` signal corresponding to the least significant byte of the data bus. For example, if `byteena = 01` and you are using a RAM block in ×18 mode, `data[8..0]` is enabled and `data[17..9]` is disabled. Similarly, if `byteena = 11`, both `data[8..0]` and `data[17..9]` are enabled. Byte enables are active high. Table 4–3 summarizes the byte selection.

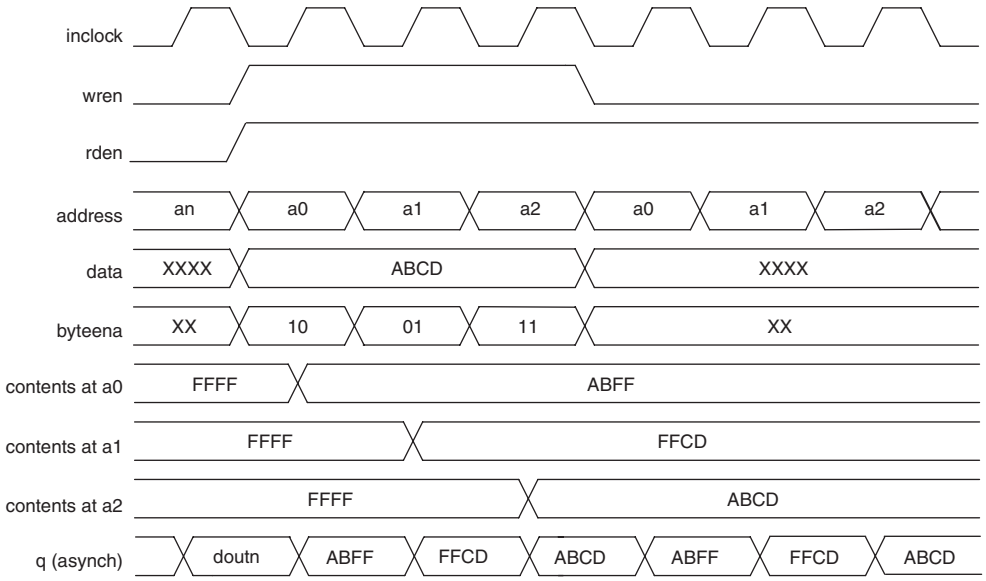
Table 4–3. Byte Enable for Cyclone III M9K Blocks *Note (1)*

byteena[3..0]	Affected Bytes			
	datain×16	datain×18	datain×32	datain×36
[0] = 1	[7..0]	[8..0]	[7..0]	[8..0]
[1] = 1	[15..8]	[17..9]	[15..8]	[17..9]
[2] = 1	—	—	[23..16]	[26..18]
[3] = 1	—	—	[31..24]	[35..27]

Note to Table 4–3:
(1) Any combination of byte enables is possible.

Figure 4–2 shows how the `wren` and `byteena` signals control the operations of the RAM.

Figure 4–2. Cyclone III Byte Enable Functional Waveform *Note (1)*



Note to Figure 4–2:
(1) For this functional waveform, "New Data" mode is selected.

When a byte-enable bit is de-asserted during a write cycle, the old data in the memory appears in the corresponding data-byte output. When a byte-enable bit is asserted during a write cycle, the corresponding data-byte output depends on the setting chosen in the Quartus® II software. It can be either the newly written data or the old data at that location.

Packed Mode Support

Cyclone III M9K memory blocks support packed mode. You can implement two single-port memory blocks in a single block under the following conditions:

- Each of the two independent block sizes is less than or equal to half of the M9K block size. The maximum data width for each independent block is 18-bits wide.
- Each of the single-port memory blocks is configured in single-clock mode.

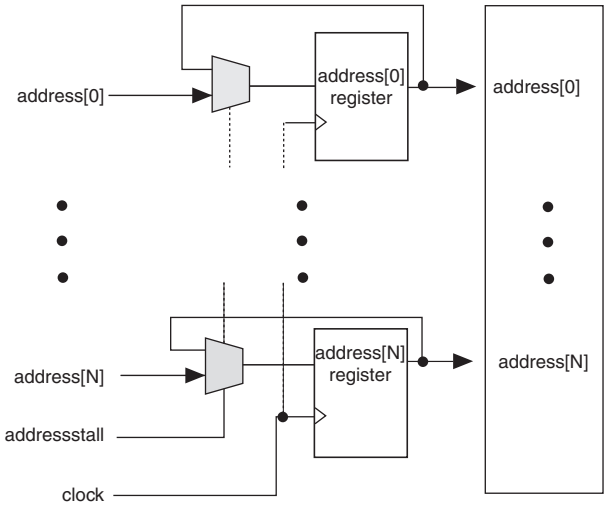
Refer to "Single-Port Mode" on page 4–7 and "Single-Clock Mode" on page 4–18 for more information.

Address Clock Enable Support

All Cyclone III memory blocks support address clock enable, which holds the previous address value for as long as the signal is enabled and `addressstall` is active high (`addressstall = '1'`). When you configure the memory blocks in dual-port mode, each port has its own independent address clock enable.

Figure 4–3 shows an address clock enable block diagram. The address register output feeds back to its input via a multiplexer. The multiplexer output is selected by the address clock enable (`addressstall`) signal.

Figure 4–3. Cyclone III Address Clock Enable Block Diagram



The address clock enable is typically used for cache memory applications to improve efficiency during a cache-miss. The default value for the address clock enable signals is low (disabled). Figures 4–4 and 4–5 show the address clock enable waveforms during read and write cycles, respectively.

Figure 4–4. Cyclone III Address Clock Enable During Read Cycle Waveform

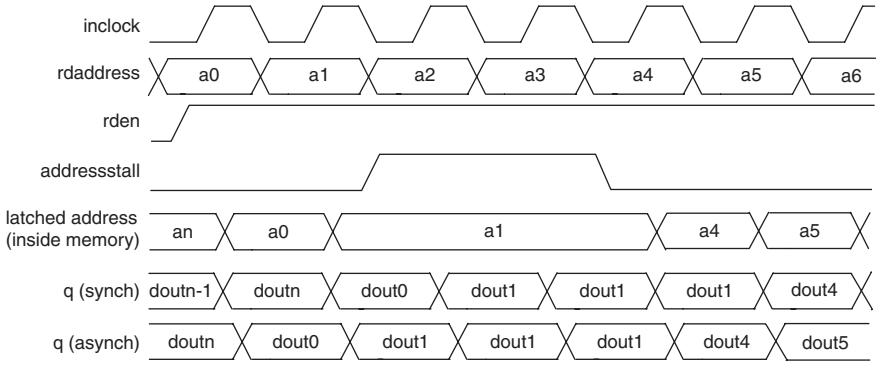
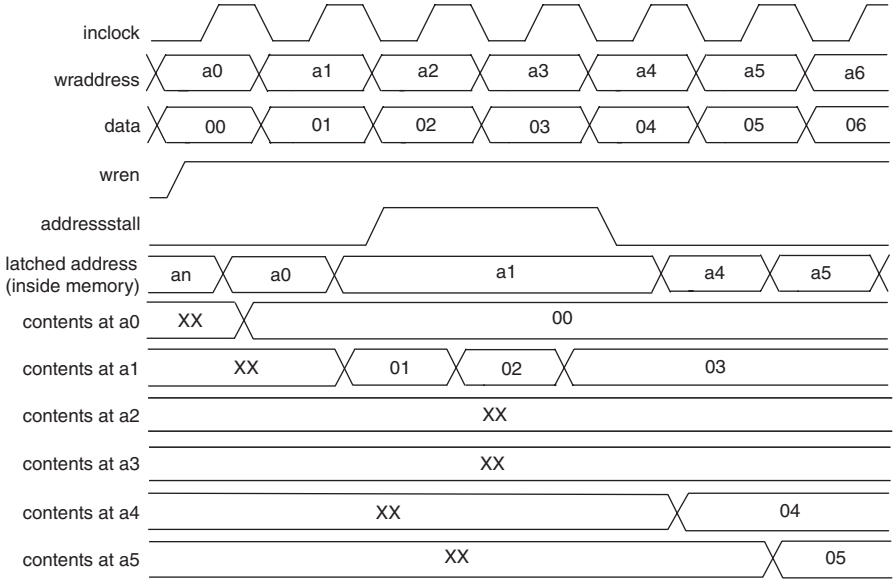


Figure 4–5. Cyclone III Address Clock Enable During Write Cycle Waveform



Mixed-Width Support

M9K memory blocks support mixed data widths. When using simple dual-port, true dual-port, or FIFO modes, mixed width support allows you to read and write different data widths to a memory block. Refer to "Memory Modes" on page 4–7 for details on the different widths supported per memory mode.

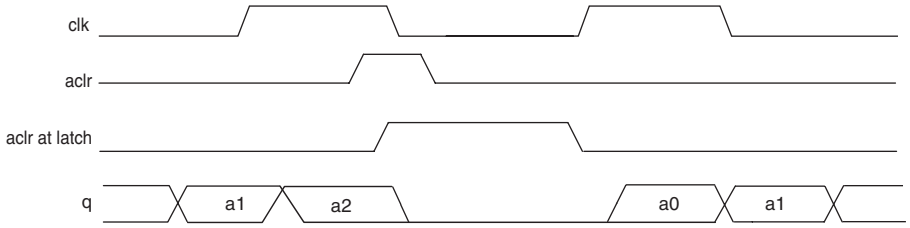
Asynchronous Clear

Cyclone III devices support asynchronous clears for read address registers, output registers and output latches only. Input registers other than read address registers are not supported. When applied to output registers, the asynchronous clear signal clears the output registers. You can see the effects immediately. If your RAM does not use the output registers, you can still clear the RAM outputs via the output latch asynchronous clear.

☞ Asserting asynchronous clear to the read address register during a read operation could corrupt the memory content.

Figure 4–6 shows the functional waveform for this feature.

Figure 4–6. Output Latch Asynchronous Clear Waveform



You can selectively enable asynchronous clears per logical memory via the Quartus II RAM MegaWizard®.

Refer to the *RAM Megafunction User Guide* for more details.

There are three ways to reset registers in the M9K blocks:

- power up the device
- use the `aclr` signal for output register only
- assert the device-wide reset signal using the `DEV_CLRn` option

Memory Modes

The Cyclone III M9K memory blocks allow you to implement fully synchronous SRAM memory in multiple modes of operation. Cyclone III M9K memory does not support asynchronous (unregistered) memory inputs.

The M9K memory blocks support the following modes:

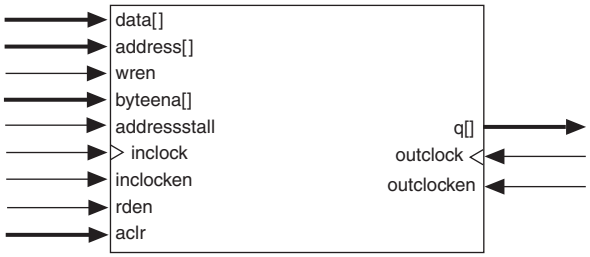
- Single-port
- Simple dual-port
- True dual-port
- Shift-register
- ROM
- FIFO

Violating the setup or hold time on the memory block input registers could corrupt memory contents. This applies to both read and write operations.

Single-Port Mode

Single-port mode supports non-simultaneous read and write operations from a single address. Figure 4–7 shows the single-port memory configuration for Cyclone III memory blocks.

Figure 4–7. Single-Port Memory Notes (1), (2)



Notes to Figure 4–7:
(1) You can implement two single-port memory blocks in a single M9K block.
(2) Refer to "Packed Mode Support" for more details.

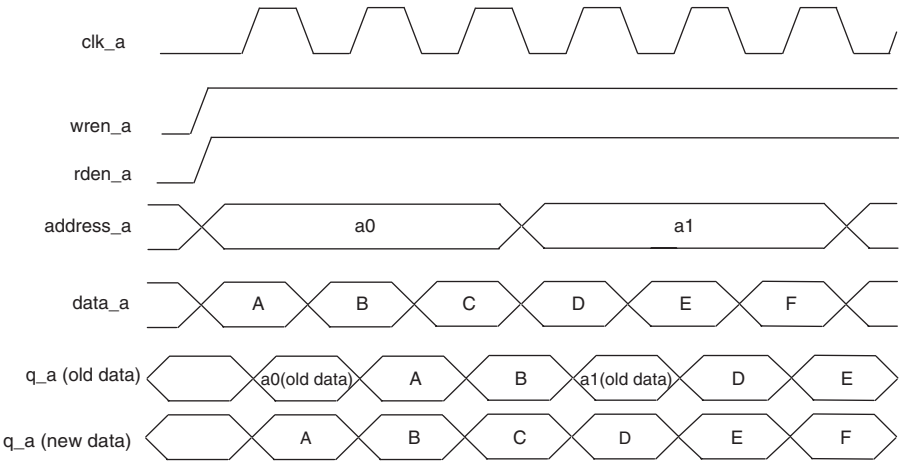
During a write operation, behavior of the RAM outputs is configurable. If you activate read enable during a write operation, RAM outputs shows either the new data being written or the old data at that address. If you perform a write operation with read enable deactivated, the RAM outputs retain the values they held during the most recent active read enable. To choose the desired behavior, set the **Read-During-Write** option to either "New Data" or "Old Data" in the RAM MegaWizard in the Quartus II software. Refer to "Read-During-Write Operations" on page 4–21 for more information about read-during-write mode.

The port width configurations for M9K blocks in single-port mode are as follows:

- 8192 × 1
- 4096 × 2
- 2048 × 4
- 1024 × 8
- 1024 × 9
- 512 × 16
- 512 × 18
- 256 × 32
- 256 × 36

Figure 4–8 shows timing waveforms for read and write operations in single-port mode with unregistered outputs. Registering the RAM's outputs would simply delay the `q` output by one clock cycle.

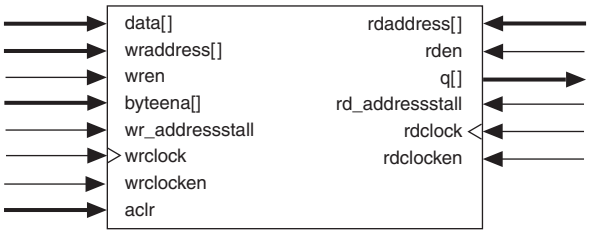
Figure 4–8. Cyclone III Single-Port Mode Timing Waveforms



Simple Dual-Port Mode

Simple dual-port mode supports simultaneous read and write operation to different locations. Figure 4–9 shows the simple dual-port memory configuration.

Figure 4–9. Cyclone III Simple Dual-Port Memory Note (1)



Note to Figure 4–9:
(1) Simple dual-port RAM supports input/output clock mode in addition to the read/write clock mode shown.

Cyclone III memory blocks support mixed-width configurations, allowing different read and write port widths. Table 4–4 shows mixed-width configurations.

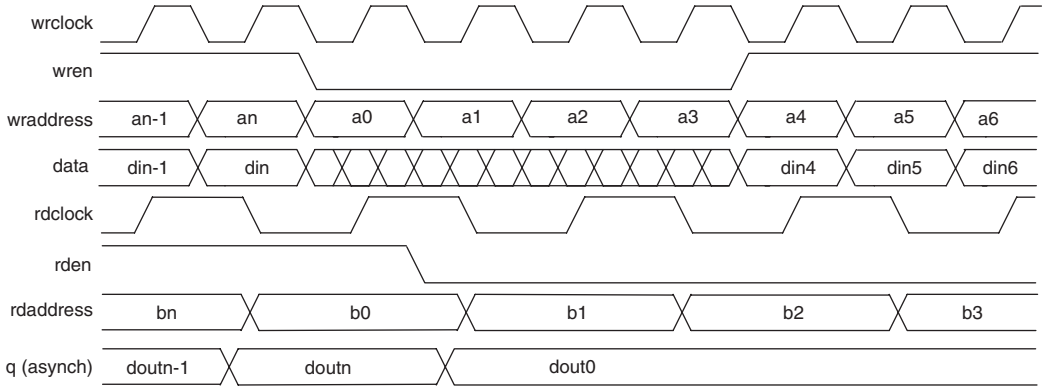
Table 4–4. Cyclone III M9K Block Mixed-Width Configurations (Simple Dual-Port Mode)

Read Port	Write Port								
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	256 × 32	1024 × 9	512 × 18	256 × 36
8192 × 1	✓	✓	✓	✓	✓	✓	—	—	—
4096 × 2	✓	✓	✓	✓	✓	✓	—	—	—
2048 × 4	✓	✓	✓	✓	✓	✓	—	—	—
1024 × 8	✓	✓	✓	✓	✓	✓	—	—	—
512 × 16	✓	✓	✓	✓	✓	✓	—	—	—
256 × 32	✓	✓	✓	✓	✓	✓	—	—	—
1024 × 9	—	—	—	—	—	—	✓	✓	✓
512 × 18	—	—	—	—	—	—	✓	✓	✓
256 × 36	—	—	—	—	—	—	✓	✓	✓

In simple dual-port mode, M9K memory blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output "Don't Care" data at that location or output "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either "Don't Care" or "Old Data" in the RAM MegaWizard in the Quartus II software. Refer to "Read-During-Write Operations" on page 4–21 for more details about this behavior.

Figure 4–10 shows timing waveforms for read and write operations in simple dual-port mode with unregistered outputs. Registering the RAM's outputs would simply delay the q output by one clock cycle.

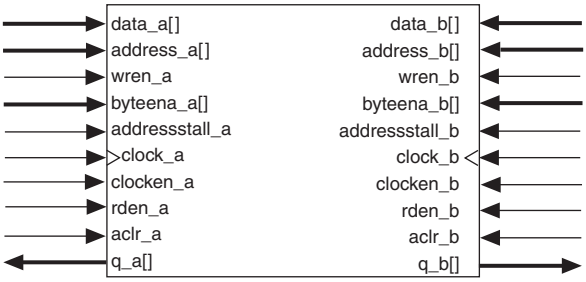
Figure 4–10. Cyclone III Simple Dual-Port Timing Waveforms



True Dual-Port Mode

True dual-port mode supports any combination of two-port operations: two reads, two writes, or one read and one write, at two different clock frequencies. Figure 4–11 shows Cyclone III true dual-port memory configuration.

***Figure 4–11. Cyclone III True Dual-Port Memory** Note (1)*



Note to Figure 4–11:
(1) True dual-port memory supports input/output clock mode in addition to the independent clock mode shown.

The widest bit configuration of the M9K blocks in true dual-port mode is 512 × 16-bit (18-bit with parity).

Table 4–5 lists the possible M9K block mixed-port width configurations.

Table 4–5. Cyclone III M9K Block Mixed-Width Configurations (True Dual-Port Mode)

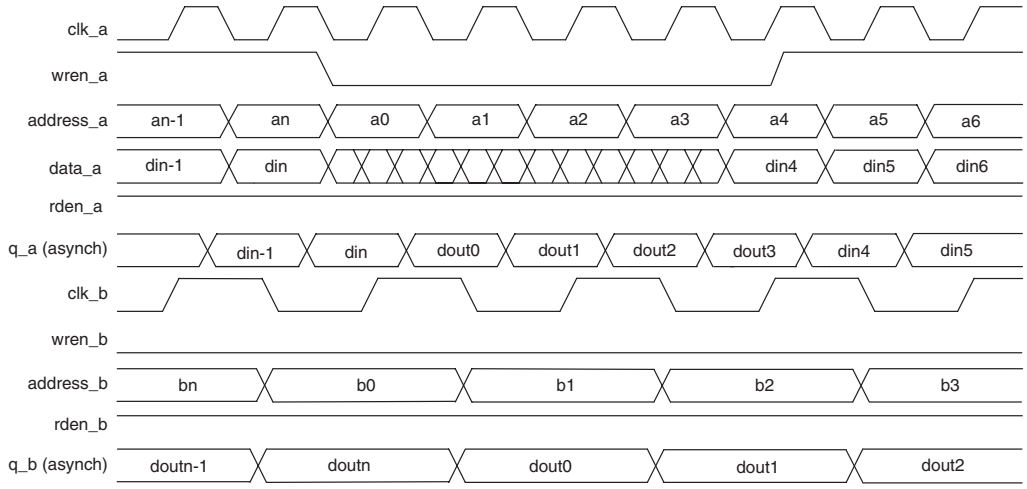
Read Port	Write Port						
	8192 × 1	4096 × 2	2048 × 4	1024 × 8	512 × 16	1024 × 9	512 × 18
8192 × 1	✓	✓	✓	✓	✓	—	—
4096 × 2	✓	✓	✓	✓	✓	—	—
2048 × 4	✓	✓	✓	✓	✓	—	—
1024 × 8	✓	✓	✓	✓	✓	—	—
512 × 16	✓	✓	✓	✓	✓	—	—
1024 × 9	—	—	—	—	—	✓	✓
512 × 18	—	—	—	—	—	✓	✓

In true dual-port mode, M9K memory blocks support separate write-enable and read-enable signals. You can save power by keeping the read-enable signal low (inactive) when not reading. Read-during-write operations to the same address can either output "New Data" at that location or "Old Data". To choose the desired behavior, set the **Read-During-Write** option to either "New Data" or "Old Data" in the RAM MegaWizard in the Quartus II software. Refer to "Read-During-Write Operations" on page 4–21 for more details on this behavior.

In true dual-port mode, you can access any memory location at any time from either port A or port B. When accessing the same memory location from both ports, however, you must avoid possible write conflicts. When you attempt to write to the same address location from both ports at the same time, a write conflict happens. This results in unknown data being stored to that address location. There is no conflict resolution circuitry built into the Cyclone III M9K memory blocks. You must handle address conflicts external to the RAM block.

Figure 4–12 shows true dual-port timing waveforms for the write operation at port A and read operation at port B. Registering the RAM's outputs would simply delay the q outputs by one clock cycle.

Figure 4–12. Cyclone III True Dual-Port Timing Waveforms



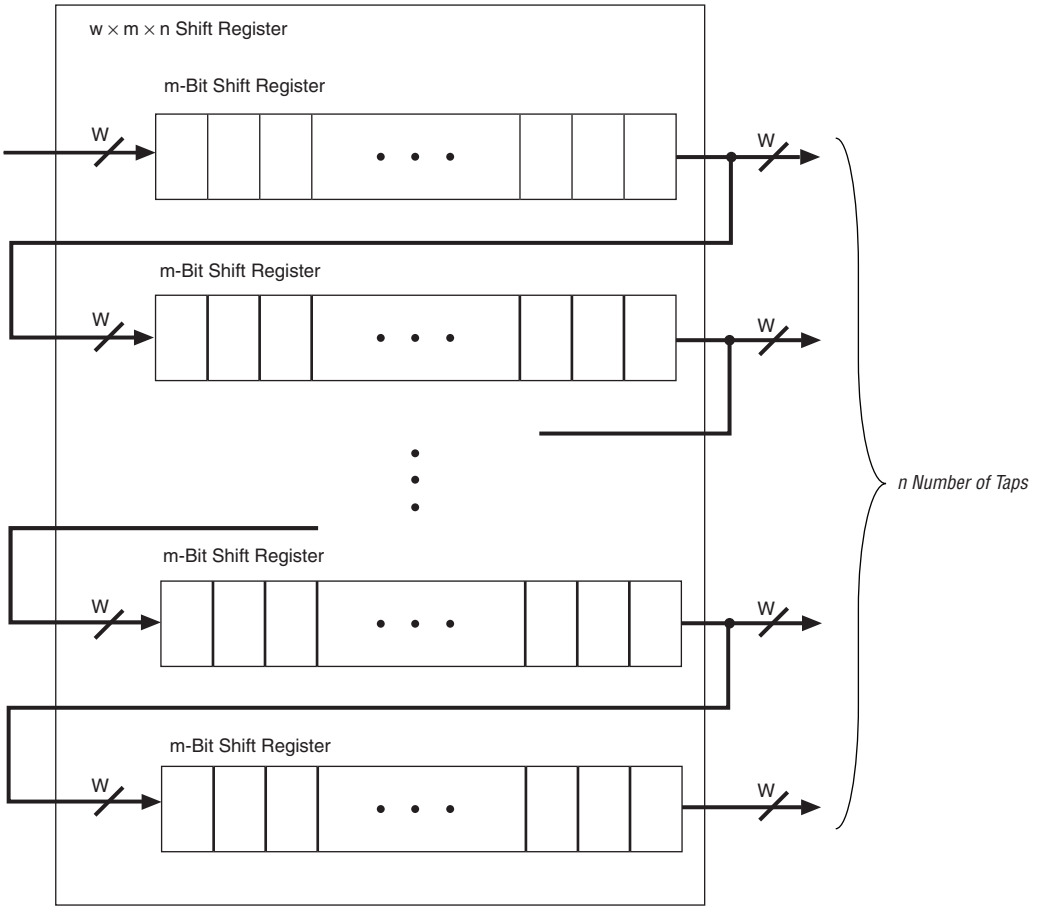
Shift Register Mode

Cyclone III memory blocks can implement shift registers for digital signal processing (DSP) applications, such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto-correlation and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops that quickly exhaust many logic cells for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources.

The size of a ($w \times m \times n$) shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n), and must be less than or equal to the maximum number of memory bits, which is 9,216 bits. In addition, the size of ($w \times n$) must be less than or equal to the maximum width of the block, which is 36 bits. If a larger shift register is required, you can cascade the memory blocks.

Figure 4–13 shows the Cyclone III memory block in the shift register mode.

Figure 4–13. Cyclone III Shift Register Mode Configuration



ROM Mode

Cyclone III memory blocks support ROM mode. A memory initialization file (**.mif**) initializes the ROM contents of these blocks. The address lines of the ROM are registered. The outputs can be registered or unregistered. The ROM read operation is identical to the read operation in the single-port RAM configuration.

FIFO Buffer Mode

Cyclone III memory blocks support single clock or dual clock FIFO buffer. Dual clock FIFO buffers are useful when transferring data from one clock domain to another clock domain. Cyclone III memory blocks do not support simultaneous read and write from an empty FIFO buffer.

Refer to the *Single- and Dual-Clock FIFO Megafunction User Guide* for more information about FIFO buffers.

Clocking Modes

Cyclone III M9K memory blocks support the following clocking modes:

- Independent
- Input/output
- Read/write
- Single-clock

Violating the setup or hold time on the memory block input registers could corrupt the memory contents. This applies to both read and write operations.

Asynchronous clears are available on read address registers, output registers and output latches only.

Table 4–6 shows the clocking mode versus memory mode support matrix.

Table 4–6. Cyclone III Memory Clock Modes

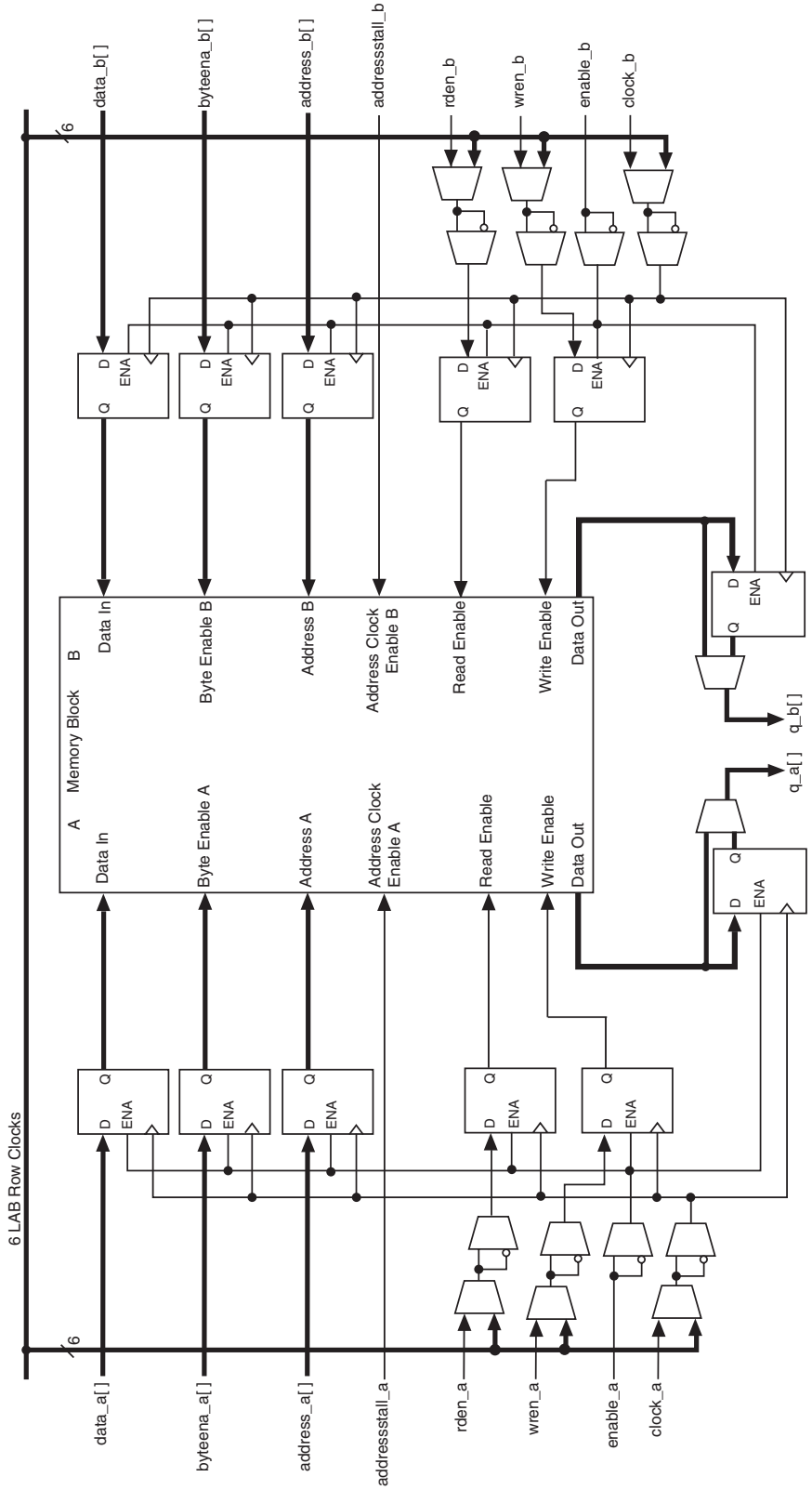
Clocking Mode	True Dual-Port Mode	Simple Dual-Port Mode	Single-Port Mode	ROM Mode	FIFO Mode
Independent	✓	—	—	✓	—
Input/output	✓	✓	✓	✓	—
Read/write	—	✓	—	—	✓
Single-clock	✓	✓	✓	✓	✓

Independent Clock Mode

Cyclone III M9K memory blocks can implement independent clock mode for true dual-port memories. In this mode, a separate clock is available for each port (port A and port B). `Clock A` controls all registers on the port A side, while `clock B` controls all registers on the port B side. Each port also supports independent clock enables for port A and B registers.

Figure 4–14 shows a memory block in independent clock mode.

Figure 4–14. Cyclone III Memory Block in Independent Clock Mode



Input/Output Clock Mode

Cyclone III M9K memory blocks can implement input/output clock mode for FIFO, single-port, true, and simple dual-port memories. In this mode, an input clock controls all input registers to the memory block including data, address, byte enables, write enables and also read-enable registers. An output clock controls the data-output registers. Each memory block port also supports independent clock enables for input and output registers.

Figures 4–15, 4–16, and 4–17 show the memory block in input/output clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

Figure 4–15. Cyclone III Input/Output Clock Mode in True Dual-Port Mode

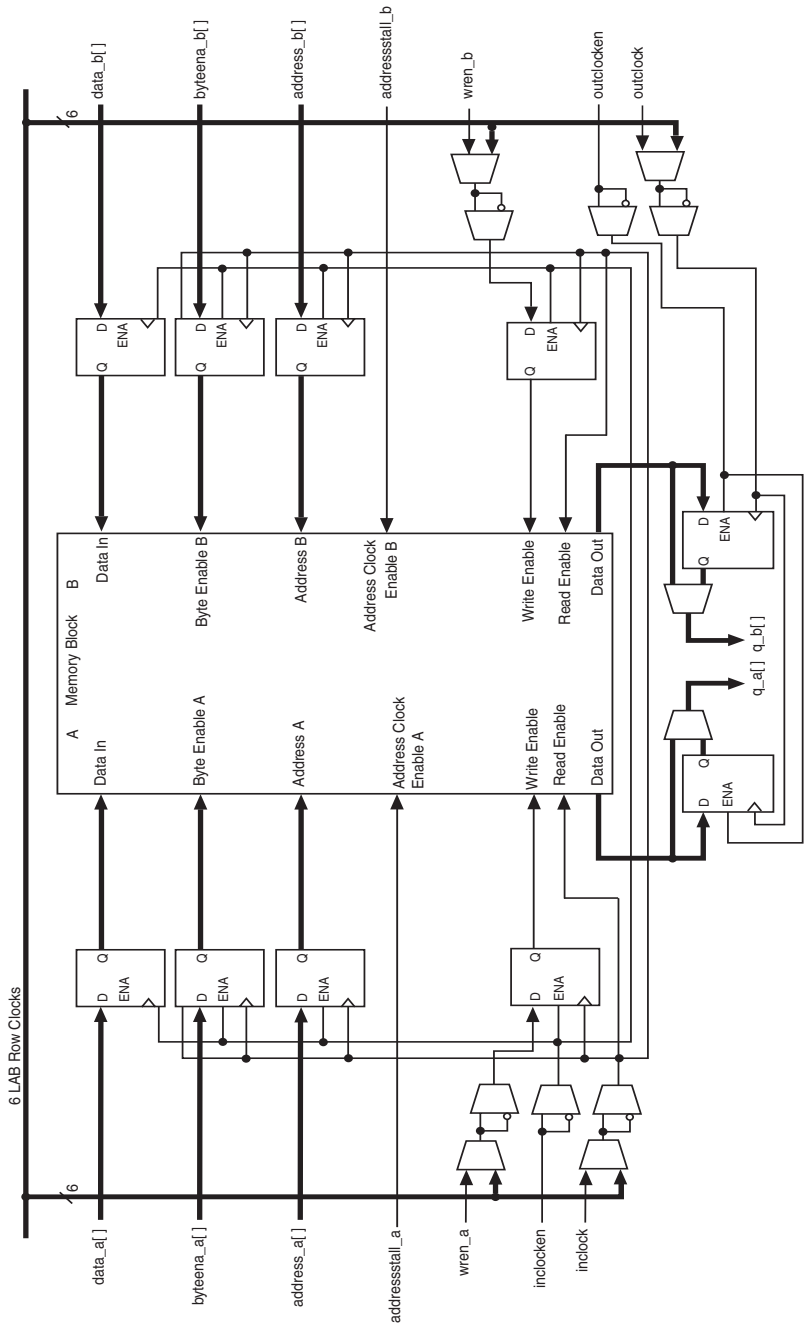
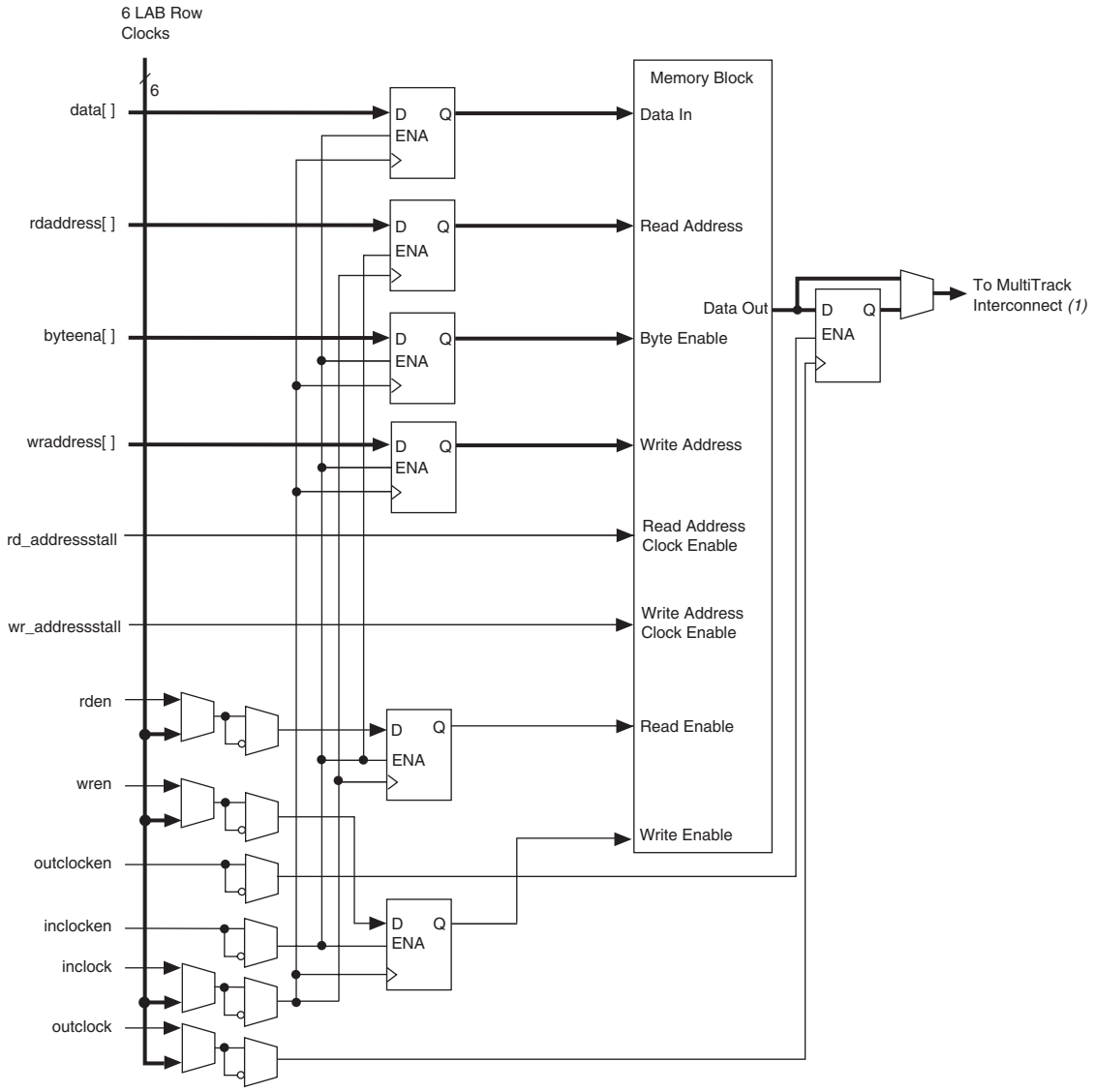


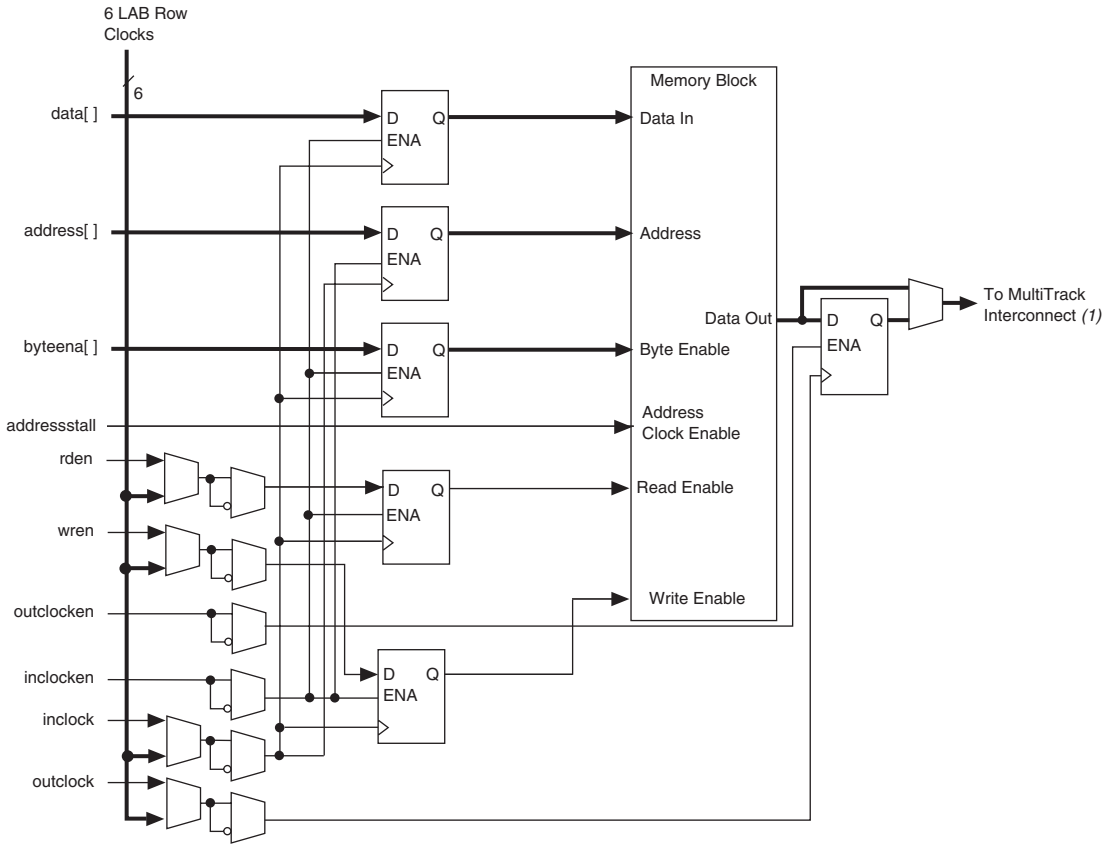
Figure 4–16. Cyclone III Input/Output Clock Mode in Simple Dual-Port Mode



Note to Figure 4–16:

(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Figure 4–17. Cyclone III Input/Output Clock Mode in Single-Port Mode



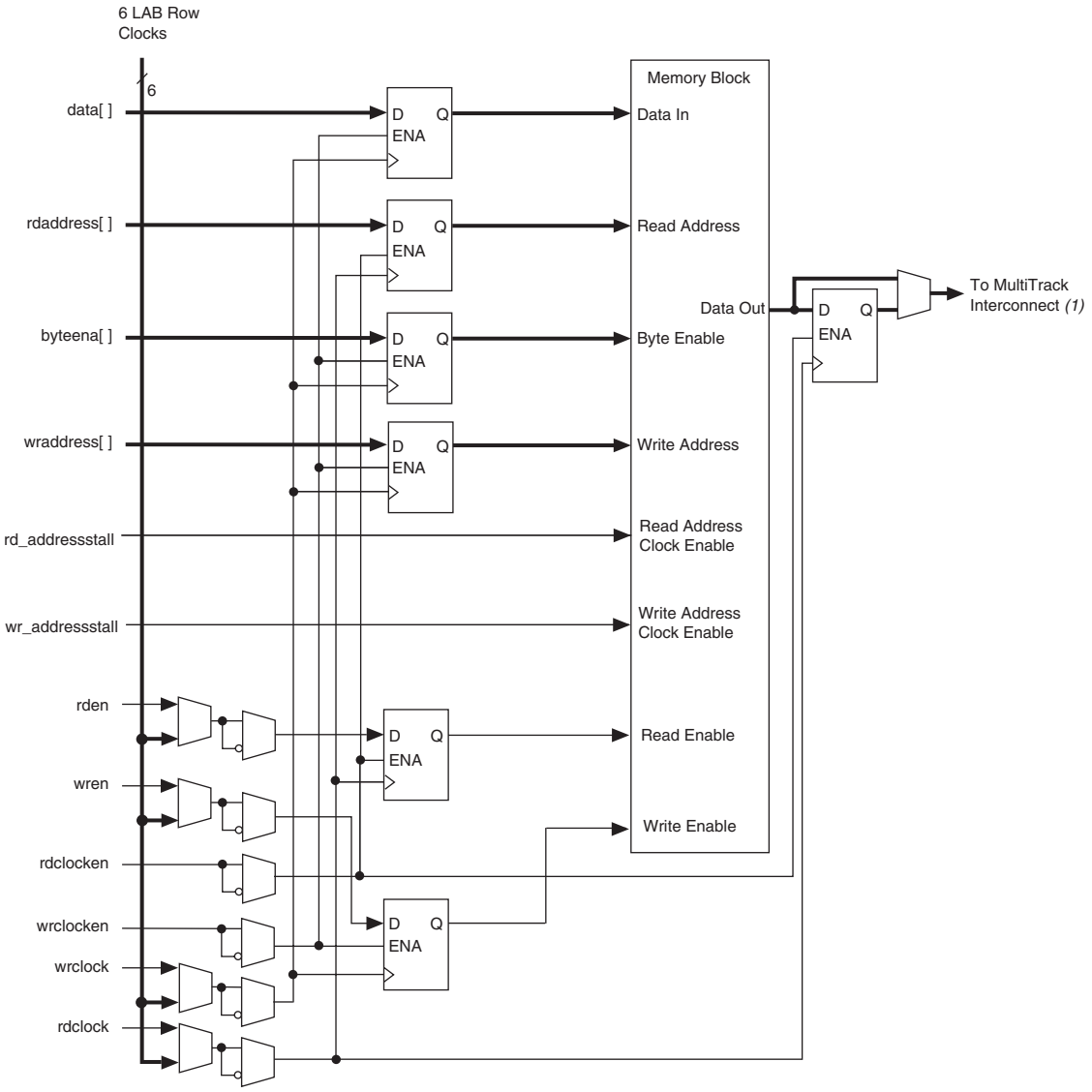
Note to Figure 4–17:

(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Read/Write Clock Mode

Cyclone III M9K memory blocks can implement read/write clock mode for FIFO and simple dual-port memories. In this mode, a write clock controls the data inputs, write address, and write-enable registers. Similarly, a read clock controls the data outputs, read address, and read-enable registers. The memory blocks support independent clock enables for both the read and write clocks. Figure 4–18 shows memory block in read/write clock mode.

Figure 4–18. Cyclone III Read/Write Clock Mode



Note to Figure 4–18:

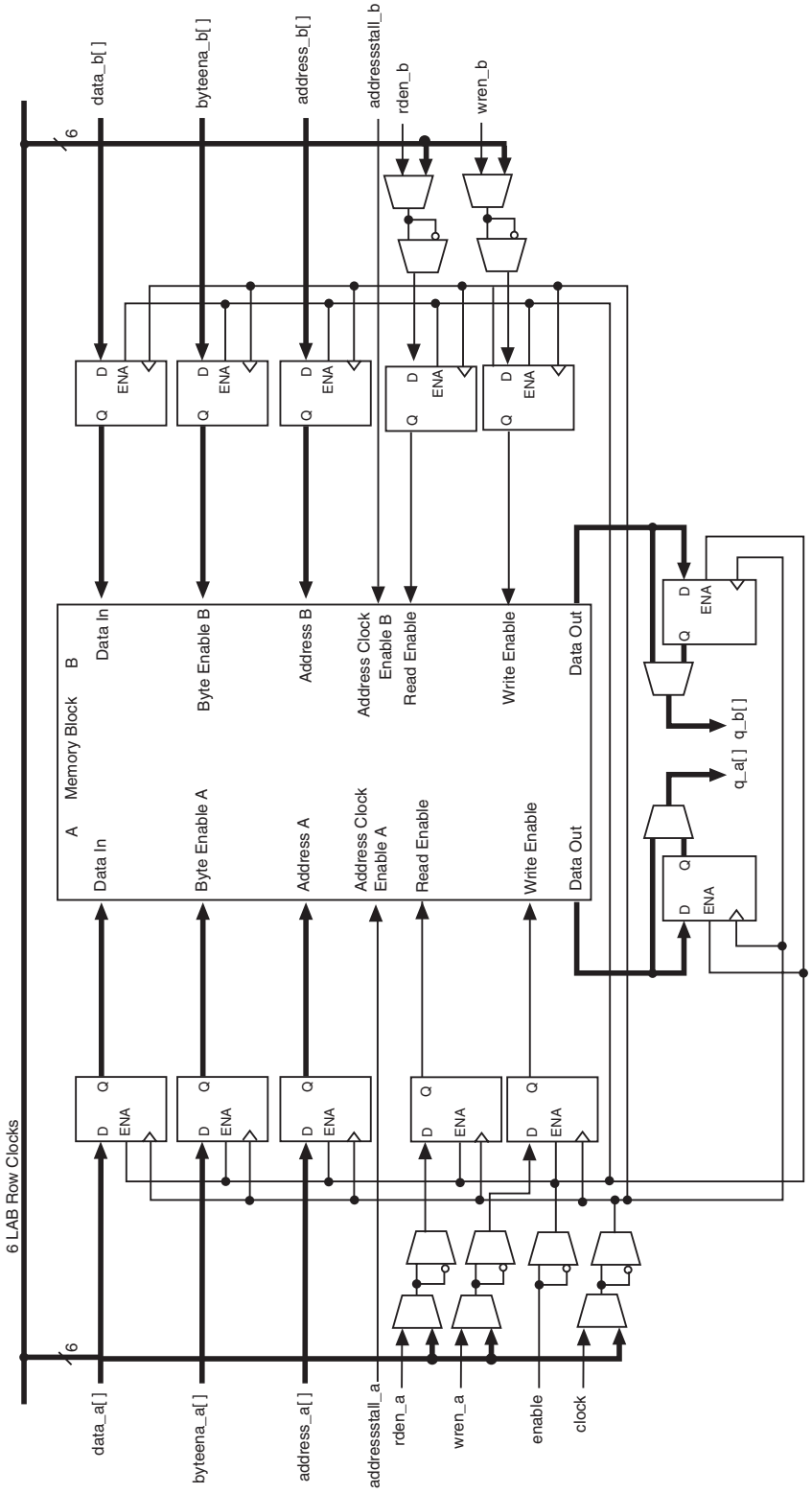
(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Single-Clock Mode

Cyclone III M9K memory blocks can implement single-clock mode for FIFO, ROM, true dual-port, simple dual-port, and single-port memories. In this mode, you can control all registers of the memory block with a single clock together with clock enable.

Figures 4–19, 4–20, and 4–21 show the memory block in single-clock mode for true dual-port, simple dual-port, and single-port modes, respectively.

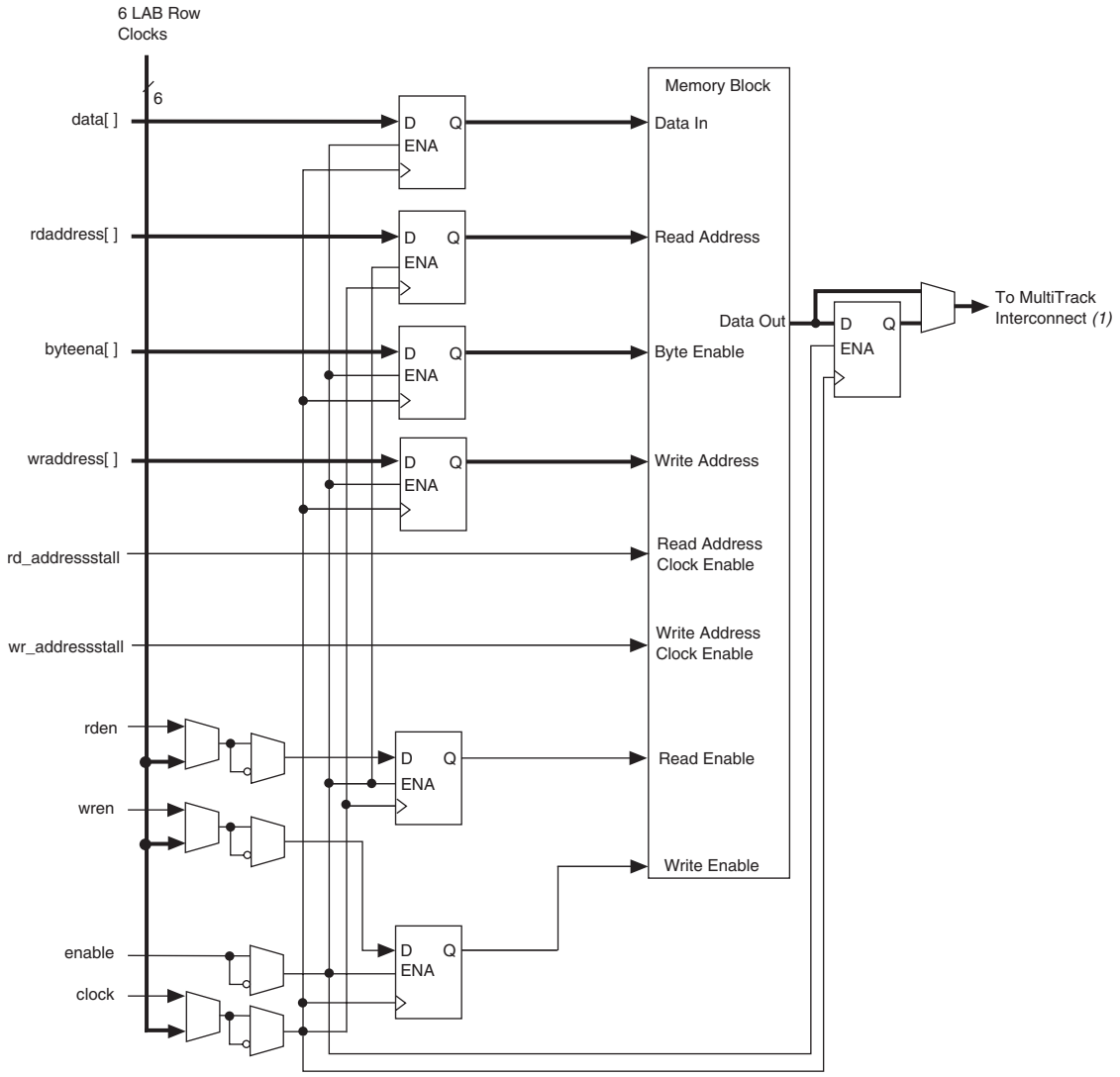
Figure 4–19. Cyclone III Single-Clock Mode in True Dual-Port Mode *Note (1)*



Note to Figure 4–19:

(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

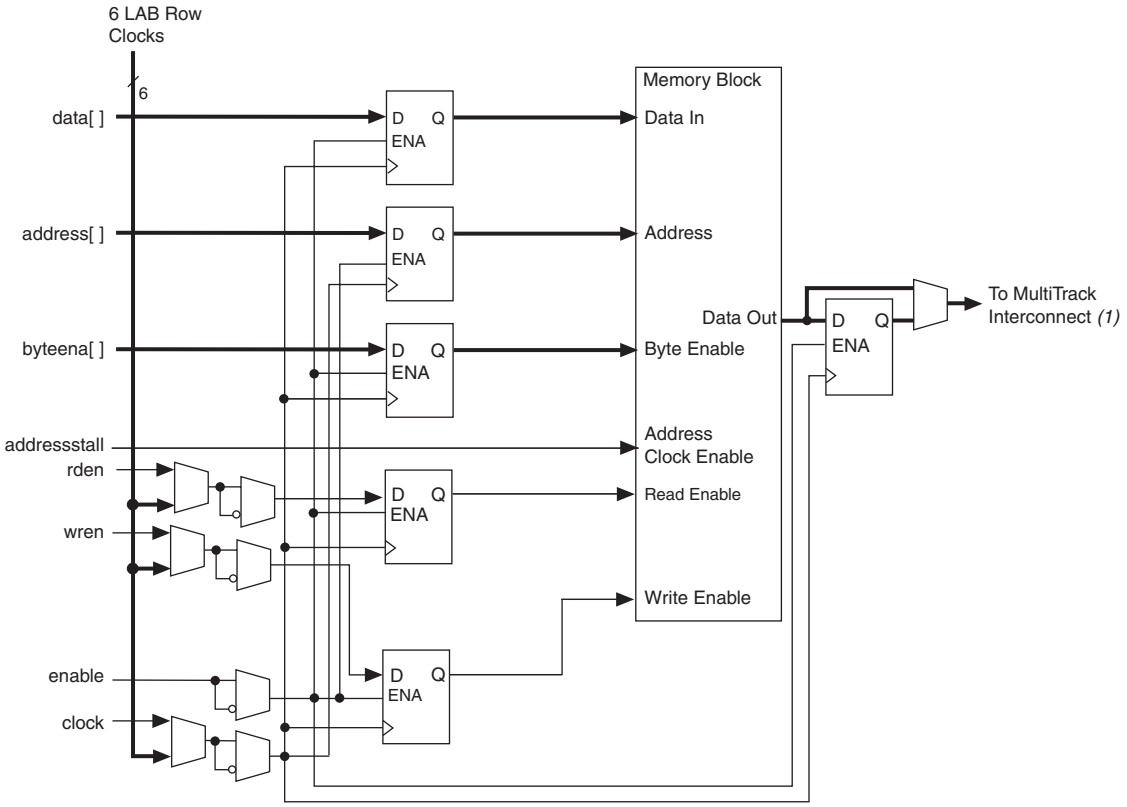
Figure 4–20. Cyclone III Single-Clock Mode in Simple Dual-Port Mode



Note to Figure 4–20:

(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Figure 4–21. Cyclone III Single-Clock Mode in Single-Port Mode



Note to Figure 4–21:

(1) For more information about the MultiTrack interconnect, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Design Considerations

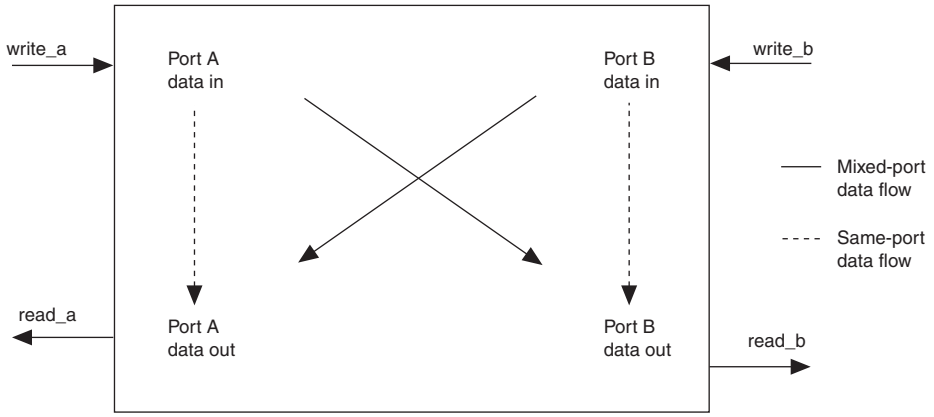
This section describes the guidelines for designing with M9K memory blocks.

Read-During-Write Operations

"Same-Port Read-During-Write Mode" on page 4–22 and "Mixed-Port Read-During-Write Mode" on page 4–23 describe the functionality of the various RAM configurations when reading from an address during a write operation at that same address. There are two read-during-write data flows: same-port and mixed-port.

Figure 4–22 shows the difference between these flows.

Figure 4–22. Cyclone III Read-During-Write Data Flow



Same-Port Read-During-Write Mode

This mode applies to a single-port RAM or the same port of a true dual-port RAM. In the same port read-during-write mode, there are two output choices: "New Data" mode (or flow-through) and "Old Data" mode. In the "New Data" mode, new data is available on the rising edge of the same clock cycle on which it was written. In "Old Data" mode, the RAM outputs reflect the old data at that address before the write operation proceeds.

When using New Data mode together with byte enable (`byteena`), you can control the output of the RAM. When byte enable is high, the data written into the memory passes to the output (flow-through). When byte enable is low, the masked-off data is not written into the memory and the old data in the memory appears on the outputs. Therefore, the output can be a combination of new and old data determined by byte enable.

Figures 4–23 and 4–24 show sample functional waveforms of same port read-during-write behavior with both "New Data" and "Old Data" modes, respectively.

Figure 4–23. Same Port Read-During Write: New Data Mode

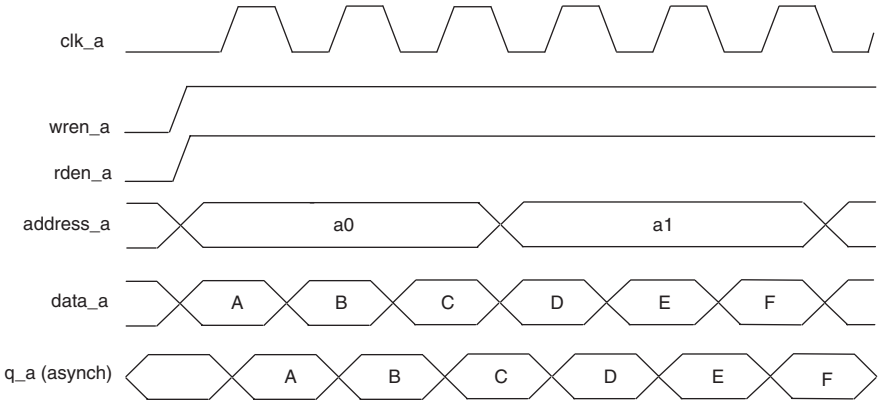
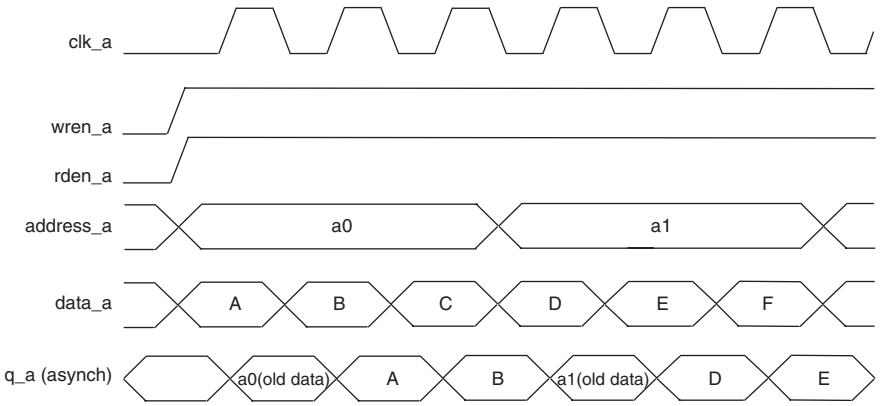


Figure 4–24. Same Port Read-During-Write: Old Data Mode



Mixed-Port Read-During-Write Mode

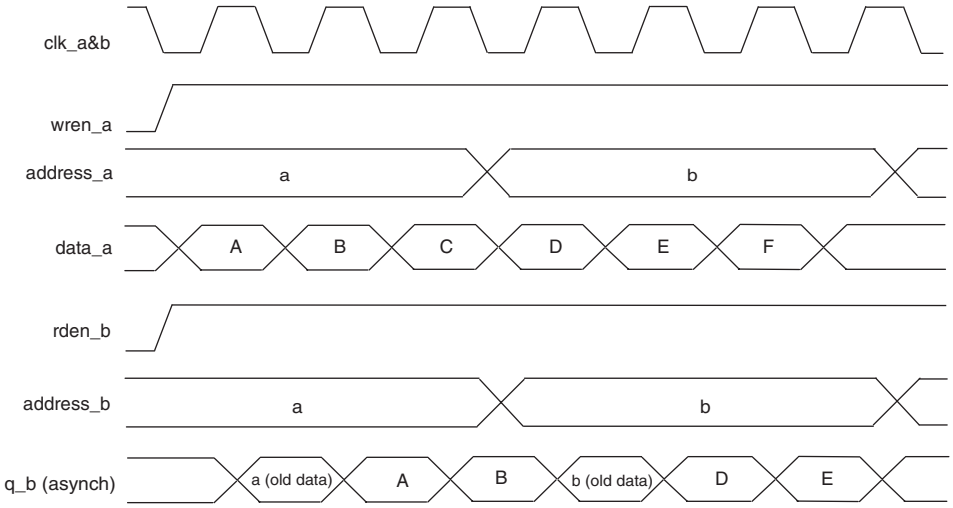
This mode applies to a RAM in simple or true dual-port mode, which has one port reading and the other port writing to the same address location with the same clock.

In this mode, you also have two output choices: “Old Data” or “Don't Care”. In “Old Data” mode, a read-during-write operation to different ports causes the RAM outputs to reflect the old data at that address location. In “Don't Care” mode, the same operation results in a "Don't Care" or unknown value on the RAM outputs.

Refer to the *RAM Megafunction User Guide* for more details about how to implement the desired behavior.

Figure 4–25 shows a sample functional waveform of mixed port read-during-write behavior for the “Old Data” mode. In “Don't Care” mode, the old data shown in the figure is simply replaced with “Don't Care”.

Figure 4–25. Mixed Port Read-During-Write: Old Data Mode



For mixed-port read-during-write operation with dual clocks, the relationship between the clocks determines the output behavior of the memory. If you use the same clock for the two clocks, the output is the old data from the address location. However, if you use different clocks, the output is unknown during the mixed-port read-during-write operation. This unknown value may be the old or the new data at the address location, depending on whether the read happens before or after the write.

Conflict Resolution

When using the memory blocks in true dual-port mode, it is possible to attempt two write operations to the same memory location (address). Since there is no conflict resolution circuitry built into the memory blocks, this results in unknown data being written to that location. Therefore, you need to implement conflict-resolution logic external to the memory block.

Power-Up Conditions and Memory Initialization

The Cyclone III memory block outputs power up to zero (cleared) regardless of whether the output registers are used or bypassed. All memory blocks support initialization via a memory initialization file (**.mif**) file. You can create **.mif**s in the Quartus II software and specify their use via the RAM MegaWizard when instantiating memory in your design. Even if memory is pre-initialized (via a **.mif** file, for example), it still powers up with its outputs cleared. Only the subsequent read after power up outputs the pre-initialized values.

For more information about MIF files, refer to the *RAM Megafunction User Guide* and the *Quartus II Handbook*.

Power Management

Cyclone III memory block clock enables allow you to control clocking of each memory block to reduce AC power consumption. Use the read-enable signal to ensure that read operations only occur when necessary. If your design does not require read-during-write, reduce power consumption by deasserting the read-enable signal during write operations, or any period when there are no memory operations.

The Quartus II software automatically powers down any unused memory blocks in order to save static power.

Conclusion

The Cyclone III M9K embedded memory structure provides flexible memory architecture with high memory bandwidth. It addresses the needs of different memory applications in Cyclone III device designs with features such as different memory modes, byte enables, parity bit storage, address clock enables, mixed clock mode, and mixed-port width support. All these configurations are possible via the Quartus II MegaWizard.

Referenced Documents

This chapter references the following documents:

- *RAM Megafunction User Guide*
- *Single- and Dual-Clock FIFO Megafunction User Guide*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Cyclone III Device Handbook*
- *Quartus II Handbook*

Document Revision History

Table 4–7 shows the revision history for this document.

Table 4–7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release.	—

5. Embedded Multipliers in Cyclone III Devices

CIII51005-1.1

Introduction

Cyclone® III devices offer up to 288 embedded multiplier blocks and support the following modes: one individual 18 bit × 18 bit multiplier per block, or two individual 9 bit × 9 bit multipliers per block.

In addition to embedded multipliers, Cyclone III FPGAs include a combination of on-chip resources and external interfaces that helps increase performance, reduce system cost, and lower the power consumption of digital signal processing (DSP) systems. You can use Cyclone III FPGAs alone, or as DSP device co-processors to improve price-to-performance ratios of DSP systems. Particular focus has been placed on optimizing Cyclone III FPGAs for applications benefiting from an abundance of parallel processing resources including video and image processing, intermediate frequency (IF) modems used in wireless communications systems, and multi-channel communications and video systems. Cyclone III FPGA DSP system design supports the following features:

- Up to 288 18 × 18 multipliers
- Up to 3,981 Kbit of on-chip embedded M9K memory blocks
- High-speed interfaces to external memory such as DDR and DDR2 SDRAM
- DSP intellectual property (IP) cores that include:
  - Common DSP processing functions like finite impulse response (FIR), fast Fourier transform (FFT), and numerically controlled oscillator (NCO) functions
  - Video and image processing suite
- Complete reference designs for end market applications
- DSP Builder interface between the Mathworks Simulink and MATLAB design environment and the Altera® Quartus® II software
- DSP optimized development kits

This chapter focuses on the Cyclone III embedded multiplier blocks. The Quartus II software makes it easy to take advantage of embedded multipliers by instantiating multipliers using dedicated megafunction wizard interfaces or by inferring multipliers directly in VHDL or Verilog code. This chapter contains the following sections:

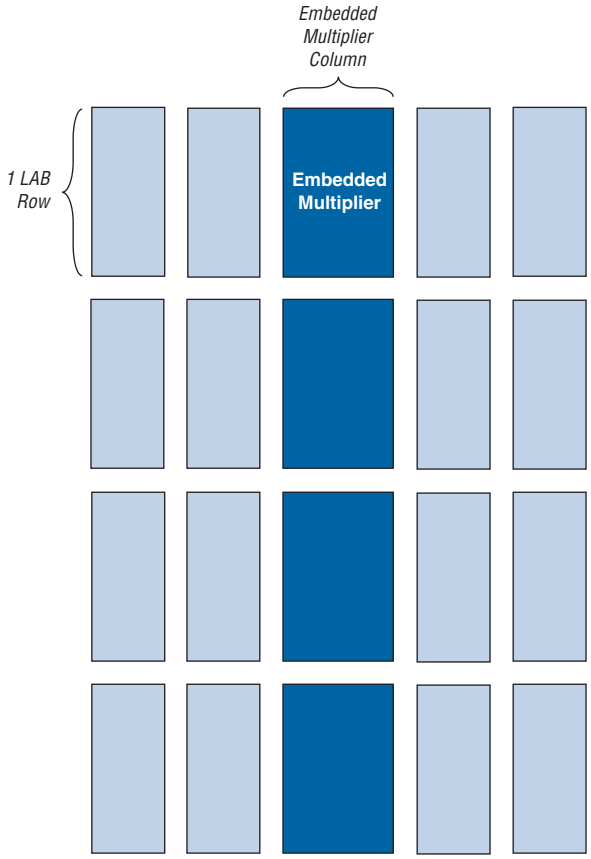
- "Embedded Multiplier Block Overview" on page 5–1
- "Architecture" on page 5–3
- "Operational Modes" on page 5–5
- "Software Support" on page 5–7

For more information about Quartus II software support of Cyclone III embedded multipliers, refer to "Software Support" on page 5–7.

Embedded Multiplier Block Overview

Each Cyclone III device has one to four columns of embedded multipliers that implement multiplication functions. Figure 5–1 shows one of the embedded multiplier columns with the surrounding logic array blocks (LABs). You can configure each embedded multiplier as one 18 × 18 multiplier or two 9 × 9 multipliers. For multiplication greater than 18 × 18, the Quartus II software cascades multiple embedded multiplier blocks together. There is no restriction on the data width of the multiplier, but the greater the data width, the slower the multiplication process.

Figure 5–1. Embedded Multipliers Arranged in Columns with Adjacent LABs



The number of embedded multipliers per column and the number of columns available increases with device density. Table 5–1 shows the number of embedded multipliers in each Cyclone III device and the multiplier modes that you can implement.

Table 5–1. Number of Embedded Multipliers in Cyclone III Devices

Device	Embedded Multipliers	9 x 9 Multipliers *(1)*	18 x 18 Multipliers *(1)*
EP3C5	23	46	23
EP3C10	23	46	23
EP3C16	56	112	56
EP3C25	66	132	66
EP3C40	126	252	126
EP3C55	156	312	156
EP3C80	244	488	244
EP3C120	288	576	288

Note to Table 5–1:

(1) These columns show the number of 9 × 9 or 18 × 18 multipliers for each device. The total number of multipliers for each device is not the sum of all the multipliers.

In addition to the embedded multipliers, you can also implement soft multipliers using Cyclone III M9K memory blocks. You can use M9K blocks as look-up tables (LUTs) that contain partial results from the multiplication of input data with coefficients that implements variable depth/width

high-performance soft multipliers for low-cost, high-volume DSP applications. The availability of soft multipliers increases the number of multipliers available within the device. Table 5–2 shows the total number of multipliers available in Cyclone III devices using embedded multipliers and soft multipliers.

Table 5–2. Number of Multipliers in Cyclone III Devices

Device	Embedded Multipliers (18 × 18)	Soft Multipliers (16 × 16) *(1)*	Total Multipliers *(2)*
EP3C5	23	—	23
EP3C10	23	46	69
EP3C16	56	56	112
EP3C25	66	66	132
EP3C40	126	126	252
EP3C55	156	260	416
EP3C80	244	305	549
EP3C120	288	432	720

Notes to Table 5–2:

(1) Soft multipliers are implemented in sum of multiplication mode. The M9K memory blocks are configured with 18-bit data widths to support 16-bit coefficients. The sum of the coefficients requires 18-bits of resolution to account for overflow.

(2) The total number of multipliers may vary according to the multiplier mode you use.

Refer to the *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook* for more information about Cyclone III M9K memory blocks.

Refer to *AN 306: Implementing Multipliers in FPGA Devices* for more information about soft multipliers.

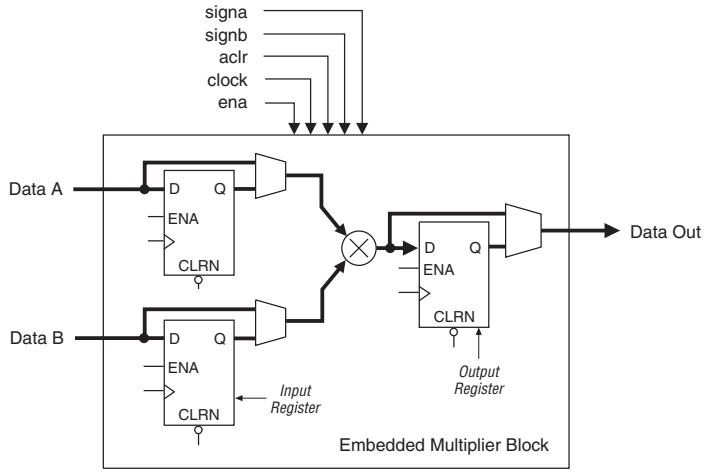
Architecture

Each embedded multiplier consists of the following elements:

- Multiplier stage
- Input and output registers
- Input and output interfaces

Figure 5–2 shows the multiplier block architecture.

Figure 5–2. Multiplier Block Architecture



Input Registers

You can send each multiplier input signal into an input register or directly into the multiplier in 9- or 18-bit sections, depending on the operational mode of the multiplier. You can send each multiplier input signal through a register independently of each other (for example, you can send the multiplier's `data A` signal through a register and send the `data B` signal directly to the multiplier). The following control signals are available to each input register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.

Multiplier Stage

The multiplier stage of an embedded multiplier block supports 9 × 9 or 18 × 18 multipliers as well as other multipliers in between these configurations. Depending on the data width or operational mode of the multiplier, a single embedded multiplier can perform one or two multiplications in parallel.

Refer to "Operational Modes" on page 5–5 for multiplier details.

Each multiplier operand can be a unique signed or unsigned number. Two signals, `signa` and `signb`, control an input of a multiplier and determine if the value is signed or unsigned. If the `signa` signal is high, the `data A` operand is a signed number. If the `signa` signal is low, the `data A` operand is an unsigned number. Table 5–3 shows the sign of the multiplication result for the various operand sign representations. The result of the multiplication is signed if any one of the operands is a signed value.

Table 5–3. Multiplier Sign Representation (Part 1 of 2)

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Unsigned	Low	Unsigned	Low	Unsigned
Unsigned	Low	Signed	High	Signed

Table 5–3. Multiplier Sign Representation (Part 2 of 2)

Data A		Data B		Result
signa Value	Logic Level	signb Value	Logic Level	
Signed	High	Unsigned	Low	Signed
Signed	High	Signed	High	Signed

Each embedded multiplier block has only one `signa` and one `signb` signal to control the sign representation of the input data to the block. If the embedded multiplier block has two 9 × 9 multipliers, the `data A` input of both multipliers share the same `signa` signal, and the `data B` input of both multipliers share the same `signb` signal. You can change the `signa` and `signb` signals dynamically to modify the sign representation of the input operands at run time. You can send the `signa` and `signb` signals through a dedicated input register. The multiplier offers full precision, regardless of the sign representation.

When the `signa` and `signb` signals are unused, the Quartus II software sets the multiplier to perform unsigned multiplication by default.

Output Registers

You can choose to register the embedded multiplier output using the output registers in 18- or 36-bit sections, depending on the operational mode of the multiplier. The following control signals are available to each output register within the embedded multiplier:

- clock
- clock enable
- asynchronous clear

All input and output registers within a single embedded multiplier are fed by the same clock, clock enable, and asynchronous clear signals.

Refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook* for more information about embedded multiplier routing and interface.

Operational Modes

You can use an embedded multiplier block in one of two operational modes, depending on the application needs:

- One 18-bit multiplier
- Up to two 9-bit independent multipliers

The Quartus II software includes megafunctions used to control the operational modes of the multipliers. After you have made the appropriate parameter settings using the megafunction's MegaWizard® Plug-In Manager, the Quartus II software automatically configures the embedded multiplier.

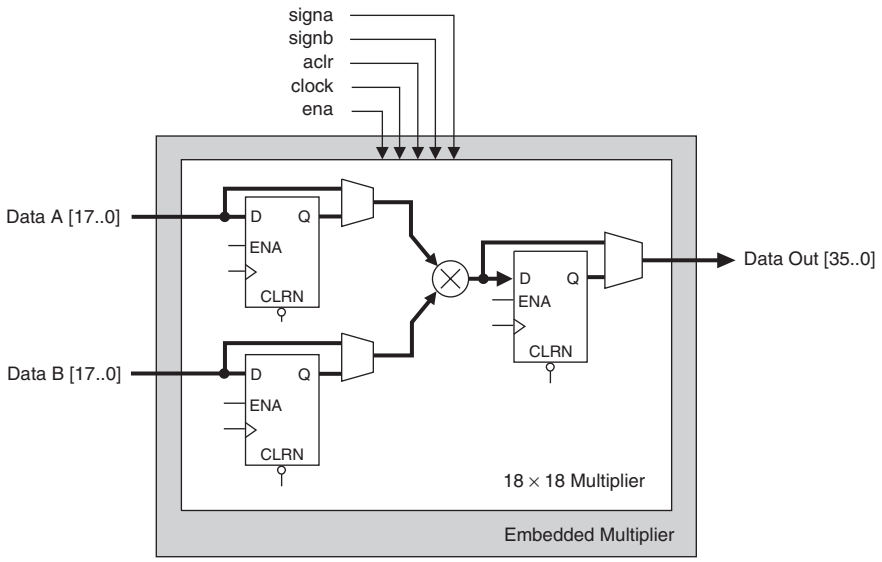
You can also use the Cyclone III embedded multipliers to implement multiplier adder and multiplier accumulator functions where the multiplier portion of the function is implemented using embedded multipliers and the adder or accumulator function is implemented in logic elements (LEs).

For more information about Quartus II support for Cyclone III embedded multipliers, refer to "Software Support" on page 5–7.

18-Bit Multipliers

You can configure each embedded multiplier to support a single 18 × 18 multiplier for input widths of 10 to 18 bits. Figure 5–3 shows the embedded multiplier configured to support an 18-bit multiplier.

Figure 5–3. 18-Bit Multiplier Mode

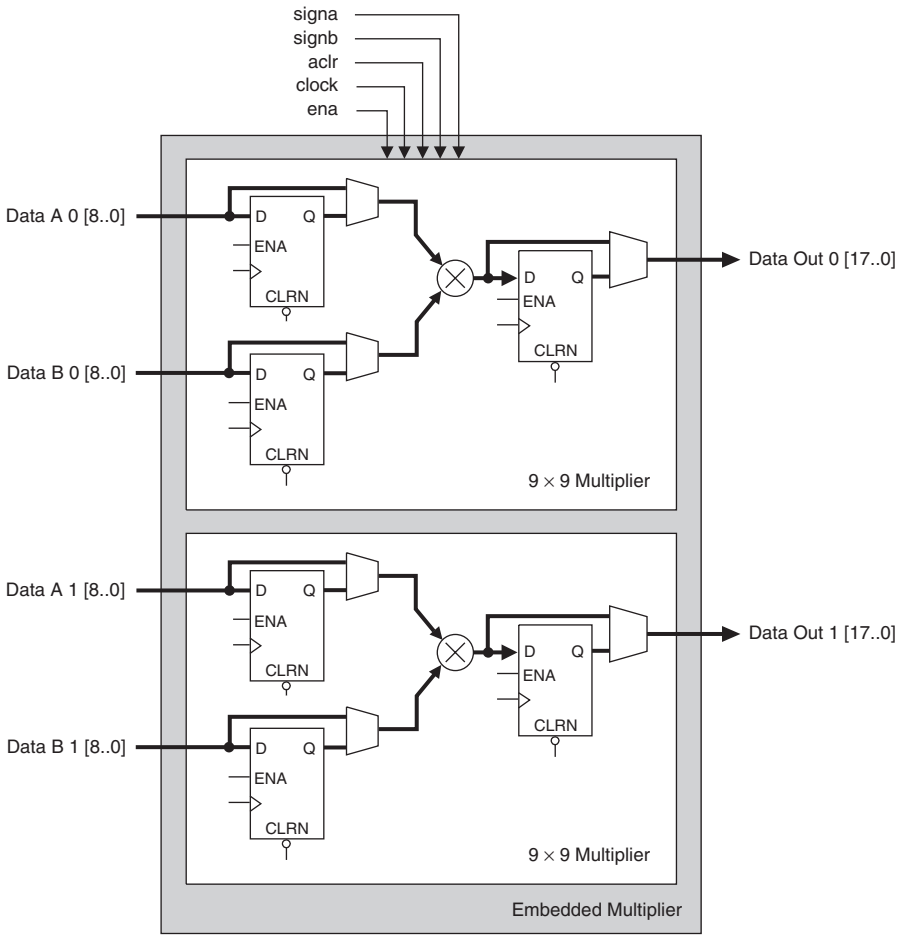


All 18-bit multiplier inputs and results can be sent independently through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Additionally, you can change the `signa` and `signb` signals dynamically and send these signals through dedicated input registers.

9-Bit Multipliers

You can configure each embedded multiplier to support two 9 × 9 independent multipliers for input widths of up to 9 bits. Figure 5–4 shows the embedded multiplier configured to support two 9-bit multipliers.

Figure 5–4. 9-Bit Multiplier Mode



All 9-bit multiplier inputs and results can be sent independently through registers. The multiplier inputs can accept signed integers, unsigned integers, or a combination of both. Two 9 × 9 multipliers in the same embedded multiplier block share the same `signa` and `signb` signal. Therefore, all of the `data A` inputs feeding the same embedded multiplier must have the same sign representation. Similarly, all of the `data B` inputs feeding the same embedded multiplier must have the same sign representation.

Software Support

Altera provides two methods for implementing multipliers in your design using embedded multiplier resources: instantiation and inference. Both methods use the following four Quartus II megafunctions:

- lpm_mult
- altmult_add
- altmult_accum
- altfp_mult

In the first method, you can use the lpm_mult, altmult_add, and altfp_mult megafunctions to implement multipliers. Additionally, you can use the altmult_add megafunction as multiplier-adders where embedded multipliers are used as multiply function an LEs configured as adders.

The altfp_mult megafunction is a floating point multiplier. It implements the embedded multiplier for floating point numbers multiplication.

The altmult_accum megafunction implements multiply accumulate functions where the embedded multiplier implements the multiplier and the accumulator function is implemented in LEs.

For instructions on how to use the megafunction and the MegaWizard Plug-In Manager, refer to the megafunction's associated User Guide and the Quartus II Help.

In the second method, you can infer the megafunctions by creating an HDL design and synthesizing it using Quartus II Native Synthesis, or a third-party synthesis tool such as Cadence or Synplify, which recognizes and infers the appropriate multiplier megafunction. With both options, the Quartus II software maps the multiplier functionality to the embedded multipliers during compilation.

For information about Altera's complete DSP Design and intellectual property offerings, refer to the Altera web site (**www.altera.com)**.

For more information about instantiating and inferring Quartus II megafunctions, refer to the *Synthesis* section in volume 1 of the *Quartus II Handbook*.

Conclusion

Cyclone III embedded multipliers are optimized to support multiplier-intensive DSP applications such as FIR filters, FFT functions, and encoders. You can configure these embedded multipliers to implement multipliers of various bit widths up to 18-bits to suit a particular application, resulting in efficient resource utilization and improved performance and data throughput. The Quartus II software and the Synplify software provide a complete and easy-to-use flow for implementing multiplier functions using embedded multipliers.

Referenced Documents

This chapter references the following documents:

- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *AN 306: Implementing Multipliers in FPGA Devices*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Synthesis* section in volume 1 of the *Quartus II Handbook*

Document Revision History

Table 5–4 shows the revision history for this document.

Table 5–4. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "Introduction" section. • Updated Table 5–1 and Table 5–2. • Added chapter TOC and "Referenced Documents" section.	Added EP3C120 information.
March 2007 v1.0	Initial Release.	—

6. Clock Networks and PLLs in Cyclone III Devices

CIII51006-1.1

Introduction

Cyclone® III devices provide a large number of global clock resources in combination with the clock synthesis precision provided by phase-locked loops (PLLs). This provides a complete clock-management solution. Cyclone III devices provide up to 20 dedicated global clock networks (GCLK). Clock networks that are not being used in the design are automatically turned off in the Quartus® II software to reduce overall power consumption. Cyclone III devices include up to four PLLs per device and up to five outputs per PLL. The additional global clock networks and additional PLL outputs compared to Cyclone II devices enables more efficient use of PLL resources. You can independently program every output, creating a unique, customizable clock frequency with no fixed relation to any other input or output clock. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase shift reconfiguration provide the high-performance precision required in today's high-speed applications.

Cyclone III device PLLs are feature-rich, supporting advanced capabilities such as clock switchover, dynamic phase shifting, and PLL reconfiguration. Dynamic phase reconfiguration allows implementation of high performance, easy to implement, and self calibrating external memory interfaces. Dynamic phase reconfiguration allows support for advanced display applications where the PLL input frequency may not be known ahead of time or may change. Cyclone III PLLs also support spread-spectrum tracking to support clock sources that lower electromagnetic interference (EMI). The Altera® Quartus II software enables the PLL features without requiring any external devices. The following sections describe the Cyclone III clock networks and PLLs in detail.

This chapter contains the following sections:

- "Clock Networks" on page 6–1
- "PLLs in Cyclone III Devices" on page 6–9
- "Cyclone III PLL" on page 6–11
- "Clock Feedback Modes" on page 6–15
- "Hardware Features" on page 6–17
- "Programmable Bandwidth" on page 6–23
- "Phase-Shift Implementation" on page 6–25
- "PLL Cascading" on page 6–27
- "PLL Reconfiguration" on page 6–27
- "Spread-Spectrum Clocking" on page 6–34
- "PLL Specifications" on page 6–35
- "Board Layout" on page 6–35

Clock Networks

Cyclone III devices provide up to 16 dedicated clock pins (`CLK[15..0]`) that can drive the global clock networks. The smaller Cyclone III devices (EP3C5 and EP3C10) support four dedicated clock pins on the left and right sides of the device, capable of driving a total of ten global clock networks. The larger devices (EP3C16 devices and larger) support four dedicated clock pins on each side of the device. These clock pins can drive 20 global clock networks.

Table 6–1 shows the number of global clocks available across the Cyclone III family members.

Table 6–1. Number of Global Clocks Available in Cyclone III Devices (Part 1 of 2)

Device	Number of Global Clocks
EP3C5	10
EP3C10	10
EP3C16	20
EP3C25	20

Table 6–1. Number of Global Clocks Available in Cyclone III Devices (Part 2 of 2)

EP3C40	20
EP3C55	20
EP3C80	20
EP3C120	20

Global Clock Network

Global clocks drive throughout the entire device, feeding all device quadrants. All resources within the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks, and M9K memory blocks) can use the global clock networks as clock sources. You can use these clock network resources for control signals, such as clock enables and clears fed by an external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with high fan-out.

Table 6–2 shows the connectivity of the clock sources to the global networks.

Table 6–2. Global Clock Network Connections (Part 1 of 2)

Global Clock Network Clock Sources	Global Clock Networks																			
	All Cyclone III Devices										EP3C16 through EP3C120 Devices Only									
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CLK0/DIFFCLK_0p	✓	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CLK1/DIFFCLK_0n	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CLK2/DIFFCLK_1p	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CLK3/DIFFCLK_1n	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
CLK4/DIFFCLK_2p	—	—	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—
CLK5/DIFFCLK_2n	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
CLK6/DIFFCLK_3p	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—	—	—	—	—	—
CLK7/DIFFCLK_3n	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
CLK8/DIFFCLK_5n	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	✓	—	—	—	—	—
CLK9/DIFFCLK_5p	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—
CLK10/DIFFCLK_4n	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓	—	—	—	—	—
CLK11/DIFFCLK_4p	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—
CLK12/DIFFCLK_7n	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	✓
CLK13/DIFFCLK_7p	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—
CLK14/DIFFCLK_6n	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	✓
CLK15/DIFFCLK_6p	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL1_c0 *(1)*	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL1_c1 *(1)*	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL1_c2 *(1)*	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL1_c3 *(1)*	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL1_c4 *(1)*	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
PLL2_c0 *(1)*	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—	—
PLL2_c1 *(1)*	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—	—	—	—	—
PLL2_c2 *(1)*	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
PLL2_c3 *(1)*	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—	—

Table 6–2. Global Clock Network Connections (Part 2 of 2)

Global Clock Network Clock Sources	Global Clock Networks																			
	All Cyclone III Devices										EP3C16 through EP3C120 Devices Only									
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
PLL2_c4 *(1)*	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—	—	—	—
PLL3_c0	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—	—
PLL3_c1	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—	—	—	—	—
PLL3_c2	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—	—
PLL3_c3	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—	—
PLL3_c4	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—	—	—	—
PLL4_c0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓	—
PLL4_c1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	✓
PLL4_c2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—	—
PLL4_c3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓	—
PLL4_c4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	✓
DPCLK0	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK1	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK7 *(2)* CDPCLK0 or CDPCLK7 *(3)*	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK2 *(2)* CDPCLK1 CDPCLK2 *(3)*	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK5 *(2)* DPCLK7 *(3)*	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK4 *(2)* DPCLK6 *(3)*	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK6 *(2)* DPCLK5 DPCLK6 *(3)*	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
DPCLK3 *(2)* CDPCLK4 or CDPCLK3 *(3)*	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—	—	—	—
DPCLK8	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—	—
DPCLK11	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—	—
DPCLK9	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—	—
DPCLK10	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—
DPCLK5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—	—
DPCLK2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—	—
DPCLK4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—	—
DPCLK3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	✓	✓

Notes to Table 6–2:

(1) EP3C5 and EP3C10 devices have only PLLs 1 and 2.

(2) This pin only applies to EP3C5 and EP3C10 devices.

(3) These pins only apply to EP3C16 devices and larger. Only one of the two CDPCLK pins can feed the clock control block. The other pin can be used as a regular I/O pin.

If you do not use the dedicated clock pins to feed the global clock networks, you can use them as general-purpose input pins to feed the logic array. However, when using them as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Clock Control Block

The clock control block drives global clock networks. Clock control blocks are located on each side of the device, close to the dedicated clock input pins. Global clock networks are optimized for minimum clock skew and delay.

Table 6–3 lists the sources that can feed the clock control block, which in turn feeds the global clock networks.

Table 6–3. Clock Control Block Inputs

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as synchronous and asynchronous clears, presets, or clock enables onto given global clock networks.
Dual-purpose clock (`DPCLK` and `CDPCLK`) I/O inputs	`DPCLK` and `CDPCLK` I/O pins are bidirectional dual function pins that can be used for high fan-out control signals, such as protocol signals, `TRDY` and `IRDY` signals for PCI, via the global clock network. Clock control blocks which have inputs driven by internal logic will not be able to drive PLL inputs.
PLL outputs	The PLL counter outputs can drive the global clock network.
Internal logic	You can drive the global clock network through the logic array routing to enable internal logic (LEs) to drive a high fan-out, low skew signal path. Clock control blocks that have inputs driven by internal logic will not be able to drive PLL inputs.

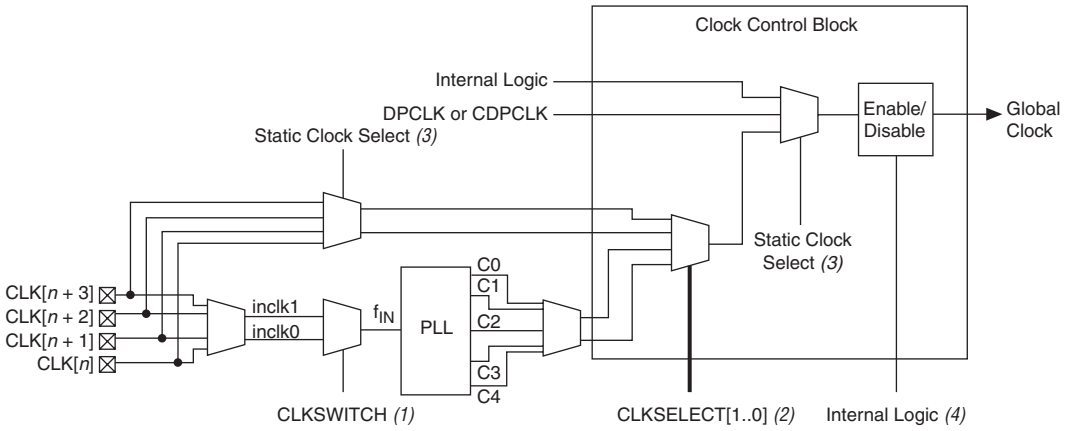
In Cyclone III devices, the dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each global clock network. The output from the clock control block in turn feeds the corresponding global clock network. This global clock can drive the PLL input if the clock control block inputs are outputs of another PLL or dedicated clock input pins. The clock control blocks are at the device periphery and there are a maximum of 20 clock control blocks available per Cyclone III device.

The control block has two functions:

- Dynamic global clock network clock source selection (not applicable for `DPCLK` or `CDPCLK` and internal logic input)
- Global clock network power-down (dynamic enable and disable)

Figure 6–1 shows the clock control block.

Figure 6–1. Clock Control Block *Notes (1), (2), (3), (4)*



Notes to Figure 6–1:

(1) The `clkswitch` signal can either be set through the configuration file or dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input clock (f_{IN}) for the PLL.

(2) The `clkselect[1..0]` signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file. Therefore, dynamic control when the device is in user mode is not feasible.

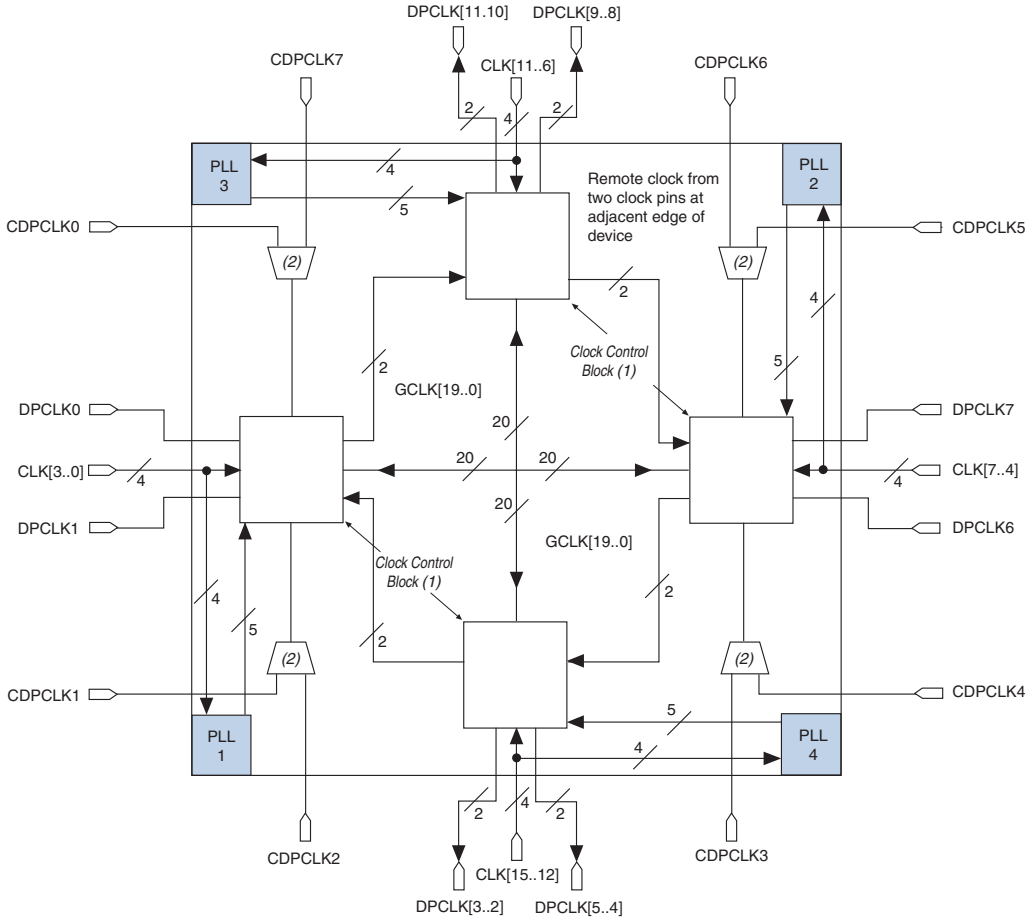
(4) You can use internal logic to enable or disable the global clock network in user mode.

Each PLL generates five clock outputs through the `c[4..0]` counters. Two of these clocks can drive the global clock network through a clock control block as shown in Figure 6–1.

Global Clock Network Clock Source Generation

There are a total of ten clock control blocks in the smaller Cyclone III devices (EP3C5 and EP3C10), and a total of 20 clock control blocks in the larger Cyclone III devices (EP3C16 devices and larger). Figure 6–2 and Figure 6–3 show the Cyclone III PLL, clock inputs, and the clock control block location for different device densities.

Figure 6–2. EP3C16 and Larger PLL, CLK[], DPCLK[] and Clock Control Block Locations Note (1)

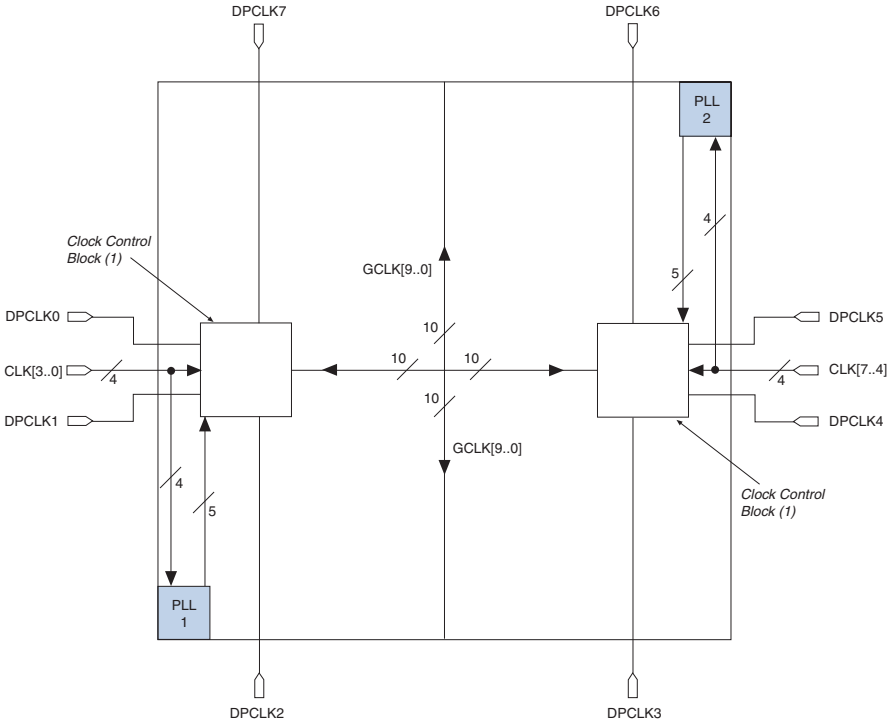


Notes to Figure 6–2:

(1) There are five clock control blocks on each side.

(2) Only one of the corner CDPCLK pins in each corner can feed the clock control block at a time. The other CDPCLK pins can be used as general-purpose I/O pins.

Figure 6–3. Cyclone III Clock Control Blocks Placement



Note to Figure 6–3:
(1) There are five clock control blocks on each side.

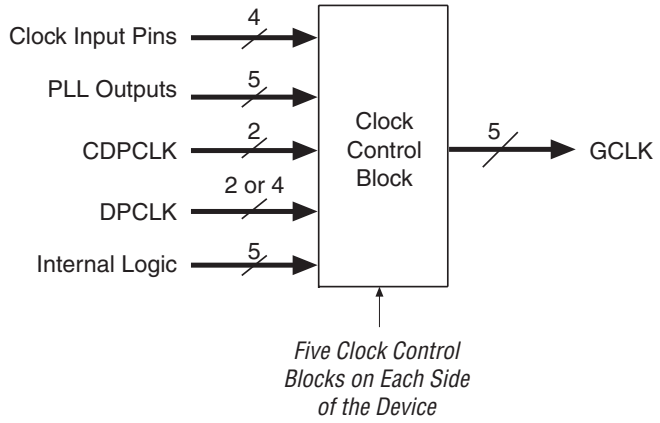
The inputs to the five clock control blocks on each side must be chosen from among the following clock sources:

- Four clock input pins
- Five PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Five signals from internal logic

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control block, as shown in Figure 6–1. Out of these five inputs to any clock control block, the two clock input pins and two PLL outputs can be dynamically selected to feed a global clock network. The clock control block supports static selection of the signal from internal logic.

Figure 6–4 shows the simplified version of the five clock control blocks on each side of the Cyclone III device periphery. The Cyclone III devices support up to 20 of these clock control blocks and this allows for up to a maximum of 20 global clocks in Cyclone III devices.

Figure 6–4. Clock Control Blocks on Each Side of the Cyclone III Device *Note (1)*



Note to Figure 6–4:

(1) The left and right sides of the device have two `DPCLK` pins, and the top and bottom of the device have four `DPCLK` pins.

Global Clock Network Power Down

You can disable the Cyclone III global clock network (power down) by both static and dynamic approaches. In the static approach, configuration bits are set in the configuration file generated by the Quartus II software, which automatically disables unused global clock networks. The dynamic clock enable or disable feature allows internal logic to control clock enable or disable of the global clock networks in the Cyclone III device.

When a clock network is disabled, all the logic fed by the clock network is in an off-state, thereby reducing the overall power consumption of the device. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 6–1 on page 6–5. The input clock sources and the `clkena` signals for the global clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction.

Refer to the *altclkctrl Megafunction User Guide* for more information.

Clkena Signals

Cyclone III devices support `clkena` signals at the clock network level. Figure 6–5 shows how to implement `clkena`. This allows you to gate off the clock even when a PLL is used. Upon re-enabling the output clock, the PLL does not need a resynchronization or re-lock period because the circuit gates off the clock at the clock network level. In addition, the PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected.

Figure 6–5. Clkena Implementation

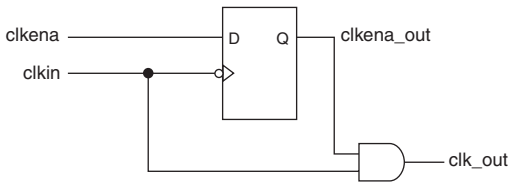
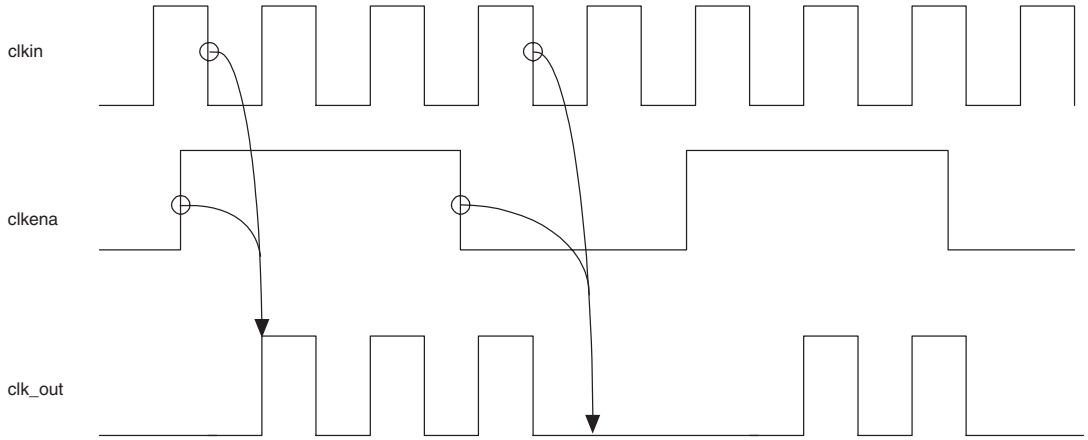


Figure 6–6 shows the waveform example for a clock output enable. The `clkena` signal is sampled on the falling edge of the clock (`clkin`).

This feature is useful for applications that require a low power or sleep mode.

Figure 6–6. Clkena Implementation - Output Enable



The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the `clkena` signals when switching the clock source to the PLLs or the global clock network. The recommended sequence is:

1. Disable the primary output clock by deasserting the `clkena` signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before reasserting the `clkena` signal. The exact number of clock cycles you need to wait before enabling the secondary clock is design-dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

PLLs in Cyclone III Devices

Cyclone III devices offer up to four PLLs that provide robust clock management and synthesis for device clock management, external system clock management, and high-speed I/O interfaces. Table 6–4 shows the PLLs available for each Cyclone III device.

Table 6–4. Cyclone III Device Availability

Device	PLL1	PLL 2	PLL 3	PLL 4
EP3C5	✓	✓	—	—
EP3C10	✓	✓	—	—
EP3C16	✓	✓	✓	✓
EP3C25	✓	✓	✓	✓
EP3C40	✓	✓	✓	✓
EP3C55	✓	✓	✓	✓
EP3C80	✓	✓	✓	✓
EP3C120	✓	✓	✓	✓

All Cyclone III PLLs have the same core analog structure. Table 6–5 shows the features available in Cyclone III PLLs.

Table 6–5. Cyclone III PLL Hardware Features

Hardware Features	Availability
C (output counters)	5
M, N, C counter sizes	1 to 512 *(1)*
Dedicated clock outputs	1 single-ended or 1 differential
Clock input pins	4 single-ended or 2 differential pins
Spread-spectrum input clock tracking	✓ *(2)*
PLL cascading	Through GCLK
Compensation modes	Source-Synchronous Mode, No Compensation Mode, Normal Mode, and Zero Delay Buffer Mode
Phase shift resolution	Down to 96-ps increments *(3)*
Programmable duty cycle	✓
Output counter cascading	✓
Input clock switchover	✓
User mode reconfiguration	✓
Loss of lock detection	✓

Notes to Table 6–5:

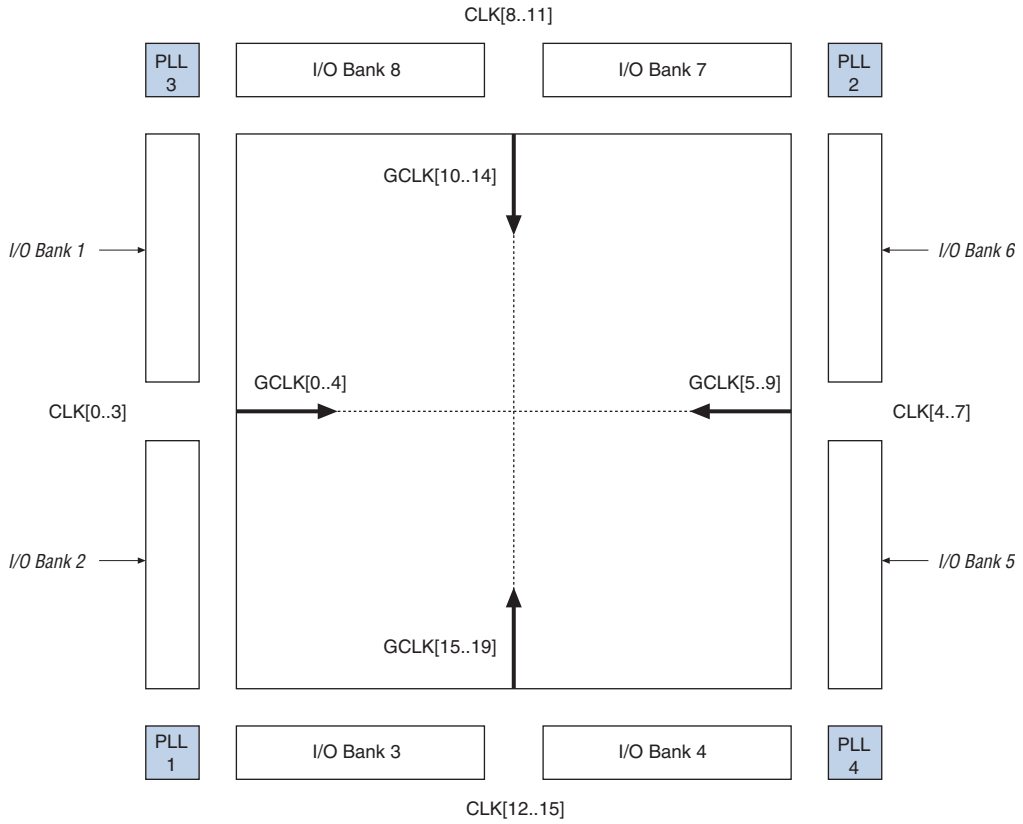
(1) C counters range from 1 through 512 if the output clock uses a 50% duty cycle. For any output clocks using a non-50% duty cycle, the post-scale counters range from 1 through 256.

(2) Provided input clock jitter is within input jitter tolerance specifications.

(3) The smallest phase shift is determined by the V_{CO} period divided by eight. For degree increments, the Cyclone III device can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

Figure 6–7 shows the location of PLLs in Cyclone III devices.

***Figure 6–7. Cyclone III PLL Locations** Note (1)*



Note to Figure 6–7:

(1) This figure shows the PLL and clock inputs in the EP3C16 through EP3C120 devices. The EP3C5 and EP3C10 devices have only eight global clock input pins (`CLK[0..3]` and `CLK[4..7]`) and PLLs 1 and 2.

Cyclone III PLL

Cyclone III PLL Hardware Overview

Cyclone III devices contain up to four PLLs with advanced clock management features. The main goal of a PLL is to synchronize the phase and frequency of an internal or external clock to an input reference clock. There are a number of components that comprise a PLL to achieve this phase alignment.

Cyclone III PLLs align the rising edge of the input reference clock to a feedback clock using the phase-frequency detector (PFD). The duty-cycle specifications determine the falling edges. The PFD produces an `up` or `down` signal that determines whether the voltage-controlled oscillator (VCO) needs to operate at a higher or lower frequency. The output of the PFD feeds the charge pump and loop filter, which produces a control voltage for setting the VCO frequency. If the PFD produces an `up` signal, then the VCO frequency increases. A `down` signal decreases the VCO frequency. The PFD generates these `up` and `down` signals to a charge pump. If the charge pump receives an `up` signal, it drives current into the loop filter. Conversely, if it receives a `down` signal, it draws current from the loop filter.

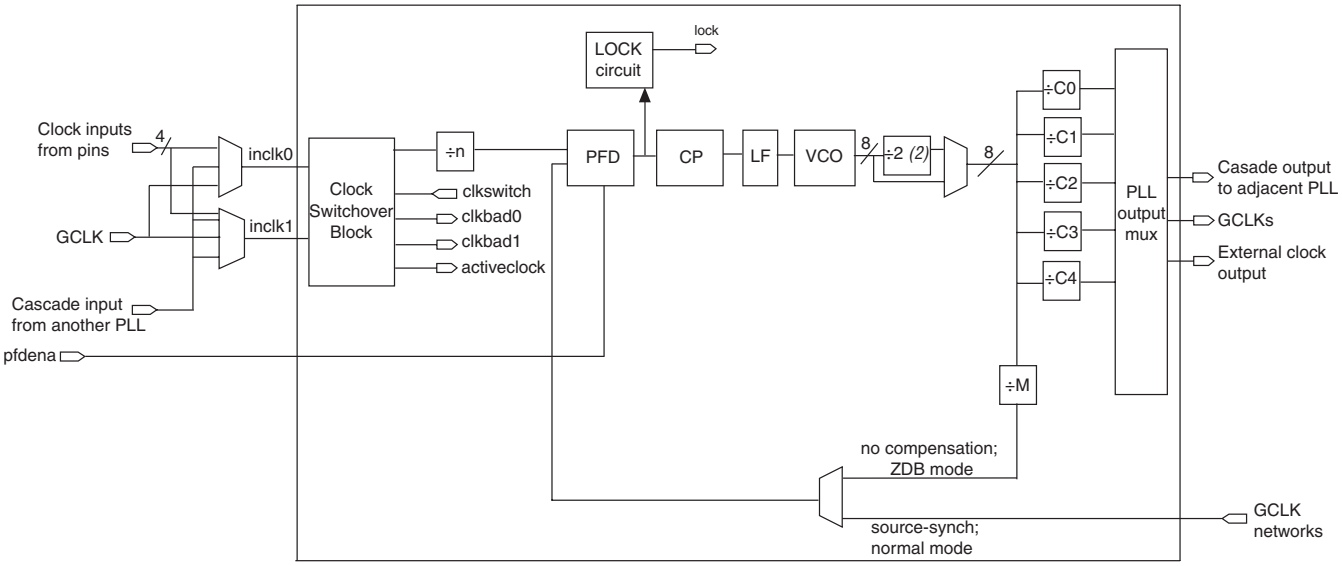
The loop filter converts these `up` and `down` signals to a voltage used to bias the VCO. The loop filter also removes glitches from the charge pump and prevents voltage over-shoot, which filters the jitter on the VCO. The voltage from the loop filter determines how fast the VCO operates. A divide counter (m) is inserted in the feedback loop to increase the VCO frequency above the input reference clock. VCO frequency (f_{VCO}) is equal to (m) times the input reference clock (f_{REF}). The input reference clock

(f_{REF}) to the PFD is equal to the input clock (f_{IN}) divided by the pre-scale counter. Therefore, the feedback clock (f_{FB}) applied to one input of the PFD is locked to the f_{REF} that is applied to the other input of the PFD.

The VCO output from the PLLs can feed five post-scale counters (`C[4..0]`). These post-scale counters allow the PLL to produce a number of harmonically related frequencies.

Figure 6–8 shows a simplified block diagram of the major components of the Cyclone III PLL.

***Figure 6–8. Cyclone III PLL** Notes (1), (2)*



Notes to Figure 6–8:

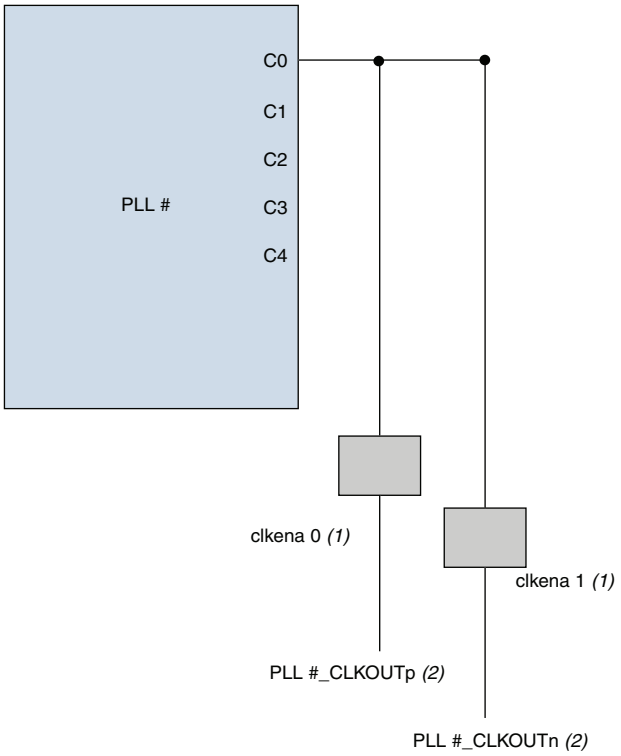
(1) Each clock source can come from any of the four clock pins located on the same side of the device as the PLL.

(2) This is the VCO post-scale counter K.

External Clock Outputs

Cyclone III PLLs each support one single-ended clock output (or one differential pair). Only the c0 output counter can feed the dedicated external clock outputs, as shown in Figure 6–9.

***Figure 6–9. External Clock Outputs for PLLs** Notes (1), (2)*



Notes to Figure 6–9:

(1) These external clock enable signals are available only when using the altclkctrl megafunction.

(2) `PLL#_CLKOUTp` and `PLL#_CLKOUTn` pins are dual-purpose I/O pins that can be used as one single-ended or one differential clock output.

Each pin of a differential output pair is 180° out of phase. The Quartus II software places the NOT gate in the design into the I/O element to implement 180° phase with respect to the other pin in the pair. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, differential HSTL, and differential SSTL.

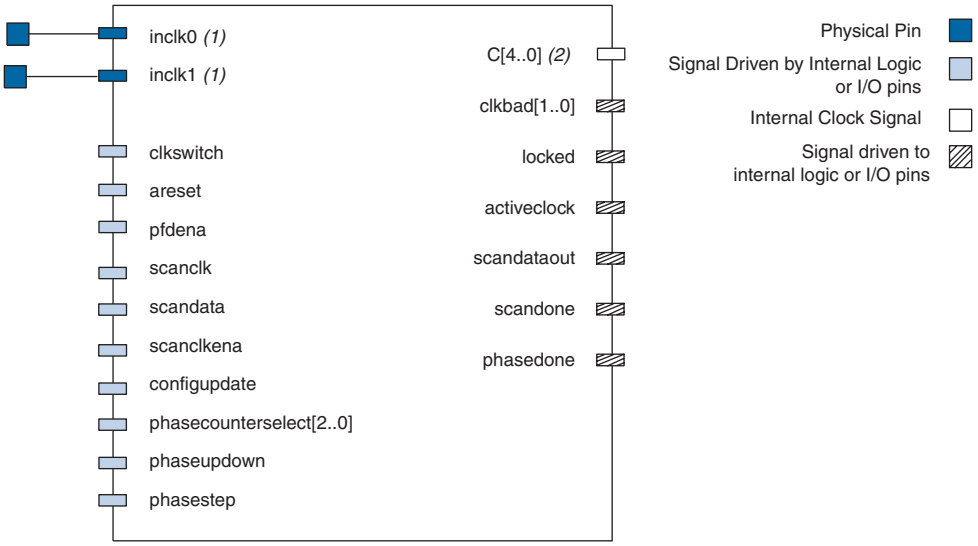
Refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook* to determine which I/O standards are supported by the PLL clock input and output pins.

Cyclone III PLLs can also drive out to any regular I/O pin through the global clock network. You can also use the external clock output pins for general purpose I/O pins if you do not need external PLL clocking.

Cyclone III PLL Software Overview

The altpll megafunction in Quartus II software enables the Cyclone III PLLs. Figure 6–10 shows the Cyclone III PLL ports as named in the altpll megafunction of the Quartus II software.

Figure 6–10. Cyclone III PLL Ports Notes (1), (2)



Notes to Figure 6–10:

(1) You can feed `inclk0` or `inclk1` clock input from any one of the four clock pins located on the same side of the device as the PLL. This input port can also be fed by an output from another PLL, a pin-driven dedicated global clock, or through a clock control block if the clock control block is fed by an output from another PLL or a pin-driven dedicated global clock. An internally generated global signal cannot drive the PLL.

(2) You can drive to global clock network (`C[4..0]`) or dedicated external clock output pins (only C0).

Table 6–6 and Table 6–7 describe all the basic PLL ports. Refer to "PLL Reconfiguration" on page 6–27 for additional information about real-time PLL reconfiguration ports and dynamic phase shifting.

Table 6–6. PLL Input Signals

Port	Description	Source	Destination
`inclk0`	Clock input to the PLL.	Dedicated input clock pin or another PLL	Clock switchover circuit
`inclk1`	Clock input to the PLL.	Dedicated input clock pin or another PLL	Clock switchover circuit
`clkswitch`	Switchover signal used to initiate external clock switchover control. Active high.	Logic array	PLL switchover circuit
`areset`	Signal used to reset the PLL, which resynchronizes all the counter outputs. Active high.	Logic array	General PLL control signal
`pfdena`	Enables the outputs from the phase frequency detector. Active high.	Logic array	PFD

Table 6–7. PLL Output Signals (Part 1 of 2)

Port	Description	Source	Destination
`c[4..0]`	PLL output counters driving global or external clocks.	PLL counter	Internal or external clock (only c0)
`clkbad[1..0]`	Signals indicating which reference clock is no longer toggling. `clkbad1` indicates `inclk1` status, clkbad0 indicates `inclk0` status. 1 = good; 0 = bad	PLL switchover circuit	Logic array

Table 6–7. PLL Output Signals (Part 2 of 2)

Port	Description	Source	Destination
`locked`	Lock output from lock detect circuit. Active high.	PLL lock detect	Logic array
`activeclock`	Signal to indicate which clock (0=inclk0 or 1=inclk1) is driving the PLL. If this signal is low, inclk0 drives the PLL. If this signal is high, inclk1 drives the PLL.	PLL clock multiplexer	Logic array

Clock Feedback Modes

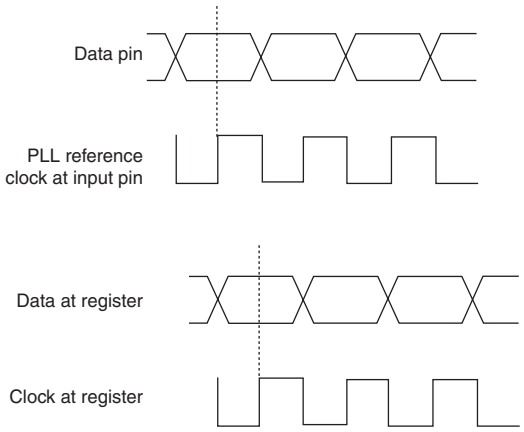
Cyclone III PLLs support up to four different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and programmable duty cycle.

☞ The input/output delays are fully compensated by the PLL only when using the dedicated clock input pins associated with a given PLL as the clock sources. For example, when using PLL1 in normal mode, the clock delays from the input pin to PLL and PLL clock output-to-destination register are fully compensated provided the clock input pin is one of the following four pins: `CLK0`, `CLK1`, `CLK2`, or `CLK3`. When driving the PLL using the GCLK network, the input/output delays may not be fully compensated in the Quartus II software.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, the phase relationship between them remains the same at the clock and data ports of any I/O element input register. Figure 6–11 shows an example waveform of the clock and data in this mode. You should use this mode for source-synchronous data transfers. Data and clock signals at the I/O element experience similar buffer delays as long as the same I/O standard is used.

Figure 6–11. Phase Relationship Between Clock and Data in Source-Synchronous Mode



The source-synchronous mode compensates for delay of the clock network used plus any difference in the delay between these two paths:

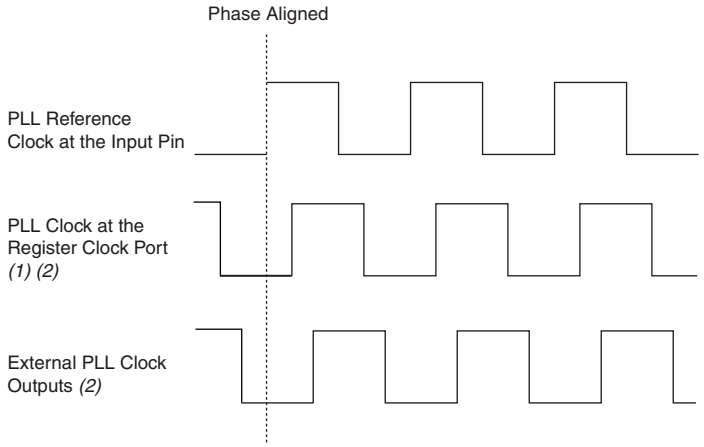
- Data pin to I/O element register input
- Clock input pin to the PLL PFD input

☞ Set the input pin to the register delay chain within the I/O element to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL. Also, all data pins must use the PLL COMPENSATED logic option in the Quartus II software.

No Compensation Mode

In the no compensation mode, the PLL does not compensate for any clock networks. This provides better jitter performance because the clock feedback into the PFD does not pass through as much circuitry. Both the PLL internal and external clock outputs are phase shifted with respect to the PLL clock input. Figure 6–12 shows a waveform example of the phase relationship of the PLL clock in this mode.

Figure 6–12. Phase Relationship between PLL Clocks in No Compensation Mode *Notes (1), (2)*

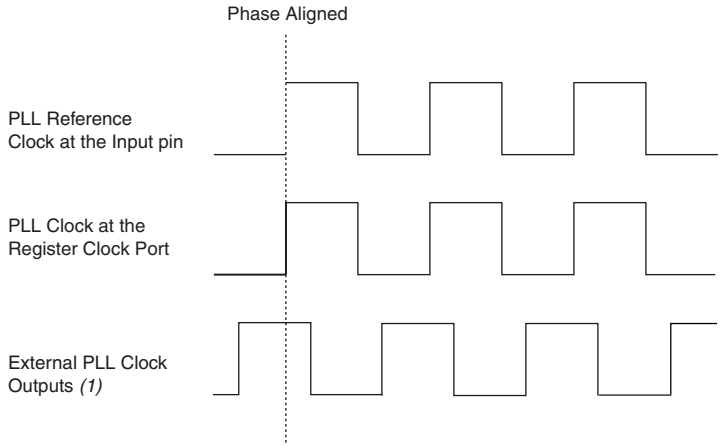


Notes to Figure 6–12:
(1) Internal clocks fed by the PLL are phase-aligned to each other.
(2) The PLL clock outputs can lead or lag the PLL input clocks.

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode. The Quartus II software timing analyzer reports any phase difference between the two. In normal mode, the PLL fully compensates the delay introduced by the GCLK network. Figure 6–13 shows a waveform example of the PLL clocks' phase relationship in this mode.

Figure 6–13. Phase Relationship Between PLL Clocks in Normal Mode *Note (1)*



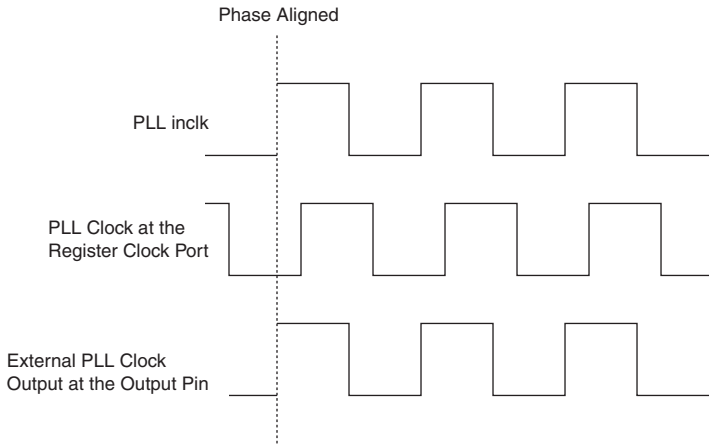
Note to Figure 6–13:
(1) The external clock output can lead or lag the PLL internal clock signals.

Zero Delay Buffer Mode

In the zero delay buffer (ZDB) mode, the external clock output pin is phase-aligned with the clock input pin for zero delay through the device. When using this mode, you must use the same I/O standard on the input clock and output clocks in order to guarantee clock alignment at the input and output pins.

Figure 6–14 shows an example waveform of the PLL clocks' phase relationship in ZDB mode.

Figure 6–14. Phase Relationship between PLL Clocks in Zero Delay Buffer Mode



Hardware Features

Cyclone III PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementations and programmable duty cycles.

Clock Multiplication and Division

Each Cyclone III PLL provides clock synthesis for PLL output ports using $m/(n$*post-scale counter) scaling factors. The input clock is divided by a pre-scale factor, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match f_{IN} (m/n). Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO value is the least common multiple of the output frequencies that meets its frequency specifications. For example, if output frequencies required from one PLL are 33 and 66 MHz, then the Quartus II software sets the VCO to 660 MHz (the least common multiple of 33 and 66 MHz within the VCO range). Then, the post-scale counters scale down the VCO frequency for each output port.

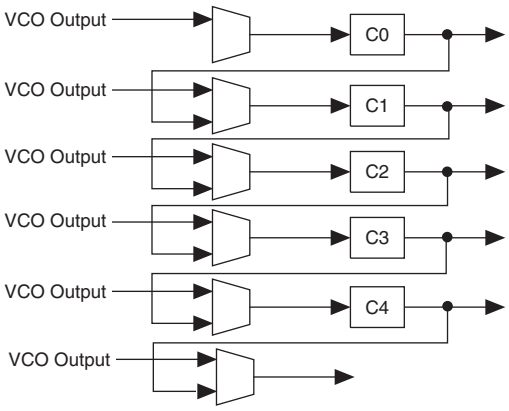
There is one pre-scale counter, n, and one multiply counter, m, per PLL, with a range of 1 to 512 for both m and n. The n counter does not use duty cycle control since the purpose of this counter is only to calculate frequency division. There are five generic post-scale counters per PLL that can feed GCLKs, or external clock outputs. These post-scale counters range from 1 to 512 with a 50% duty cycle setting. The post-scale counters range from 1 to 256 with any non-50% duty cycle setting. The sum of the high/low count values chosen for a design selects the divide value for a given counter.

The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered into the altpll megafunction.

Post-Scale Counter Cascading

The Cyclone III PLLs supports post-scale counter cascading to create counters larger than 512. This is implemented by feeding the output of one C counter into the input of the next C counter as shown in Figure 6–15.

Figure 6–15. Counter Cascading



When cascading counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter settings. For example, if C0 = 4 and C1 = 2, then the cascaded value is C0 × C1 = 8.

Post-scale counter cascading is automatically set by the Quartus II software in the configuration file. It cannot be done using PLL reconfiguration.

Programmable Duty Cycle

The programmable duty cycle allows PLLs to generate clock outputs with a variable duty cycle. This feature is supported on the PLL post-scale counters. You can achieve the duty cycle setting by a low and high time count setting for the post-scale counters. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices. The post-scale counter value determines the precision of the duty cycle. The precision is defined by 50% divided by the post-scale counter value. For example, if the C0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

Combining the programmable duty cycle with programmable phase shift allows the generation of precise non-overlapping clocks.

PLL Control Signals

You can use the following three signals to observe and/or control the PLL operation and resynchronization.

pfdena

Use the `pfdena` signal to maintain the last locked frequency so that your system has time to store its current settings before shutting down. The `pfdena` signal controls the PFD output with a programmable gate. If you disable the PFD, the VCO operates at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The PLL continues running even though it goes out of lock or the input clock is disabled. You can use your own control signal or the control signals available from the clock switchover circuit (`activeclock`, `clkbad[0]`, or `clkbad[1]`) to control `pfdena`.

areset

The `areset` signal is the reset or resynchronization input for each PLL. The device input pins or internal logic can drive these input signals. When driven high, the PLL counters reset, clearing the PLL output and placing the PLL out of lock. The VCO is then set back to its nominal setting. When driven low again, the PLL resynchronizes to its input as it re-locks.

You must assert the `areset` signal every time the PLL loses lock to guarantee the correct phase relationship between the PLL input clock and output clocks. You must include the `areset` signal in your designs if one of the following conditions is true:

- PLL reconfiguration or clock switchover enabled in the design
- Phase relationships between the PLL input clock and output clocks need to be maintained after a loss of lock condition

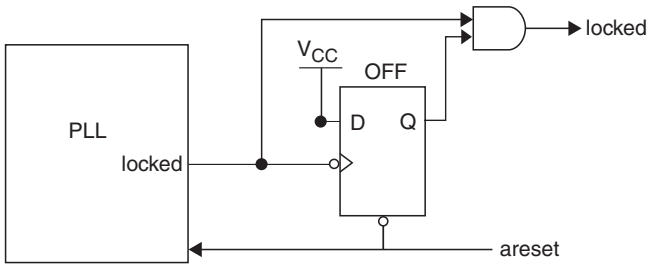
☞ If the input clock to the PLL is toggling or unstable upon power up, assert the `areset` signal after the input clock is stable and within specifications.

locked

The `locked` output indicates that the PLL has locked onto the reference clock and the PLL clock outputs are operating at the desired phase and frequency set in the Quartus II MegaWizard. Without any additional circuitry, the lock signal toggles as the PLL begins the locking process. The lock detection block provides a signal to core-logic that gives an indication if the feedback clock has locked onto the reference clock both in phase and frequency.

☞ Altera recommends that you use the `areset` and `locked` signals in your designs to control and observe the status of your PLL. When both the `areset` and `locked` signals are enabled, there will be extra logic added in the altpll megafunction to improve the robustness of the locked signal. The implementation is illustrated in Figure 6–16.

Figure 6–16. Locked Signal Implementation



If you use the SignalTap® II tool to probe the `locked` signal before the D flip-flop, the `locked` signal goes low only when `areset` is deasserted. If `areset` signal is not enabled, the extra logic is not implemented in the altpll megafunction.

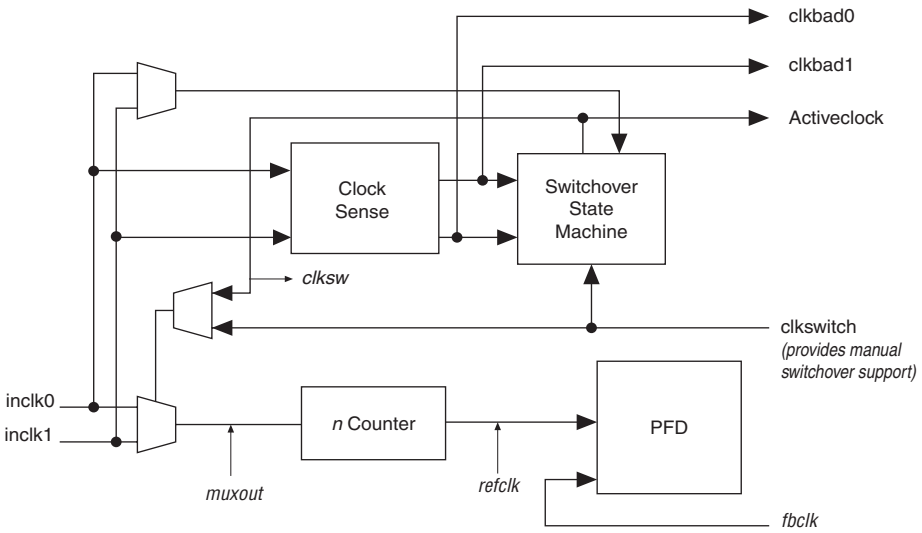
Clock Switchover

The clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy or for a dual-clock domain application such as in a system that turns on the redundant clock if the previous clock stops running. The design can perform clock switchover automatically, when the clock is no longer toggling, or based on a user control signal, `clkswitch`.

Automatic Clock Switchover

Cyclone III device PLLs support a fully configurable clock switchover capability. Figure 6–17 shows the block diagram of the switchover circuit built into the PLL. When the current reference clock is not present, the clock-sense block automatically switches to the backup clock for PLL reference. The clock switchover circuit also sends out three status signals—`clkbad[0]`, `clkbad[1]`, and `activeclock`—from the PLL to implement a custom switchover circuit. You can select a clock source at the backup clock by connecting it to the `inclk1` port of the PLL in your design.

Figure 6–17. Automatic Clock Switchover Circuit Block Diagram



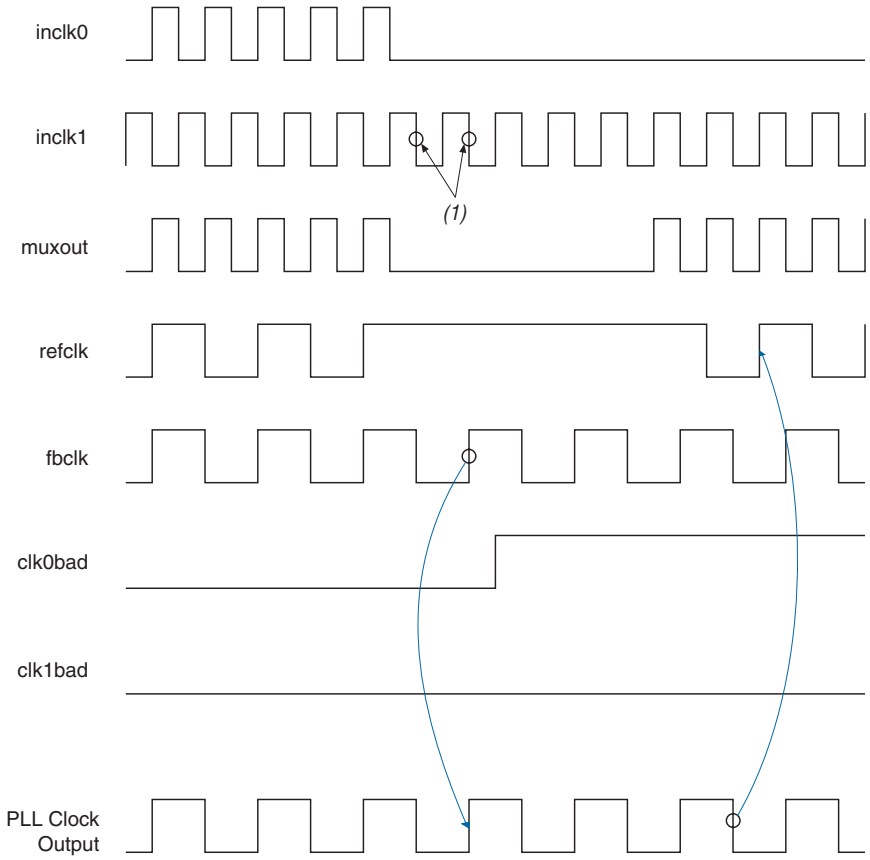
There are two possible ways to use the clock switchover feature.

- Use the switchover circuitry for switching from `inclk0` to `inclk1` running at the same frequency. For example, in applications that require a redundant clock with the same frequency as the reference clock, the switchover state machine generates a signal that controls the multiplexer select input shown in Figure 6–17. In this case, `inclk1` becomes the reference clock for the PLL. This automatic switchover can switch back and forth between `inclk0` and `inclk1` clocks any number of times, when one of the two clocks fails and the other clock is available.

- Use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 200 MHz, you must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than 20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. You should choose the secondary clock frequency so the VCO operates within the recommended frequency range. You should also set the *m*, *n*, and *c* counters accordingly to keep the VCO operating frequency in the recommended range.

Figure 6–18 shows a waveform example of the switchover feature when using the automatic loss of clock detection. Here, the `inclk0` signal remains low. After the `inclk0` signal remains low for approximately two clock cycles, the clock-sense circuitry drives the `clkbad[0]` signal high. Also, because the reference clock signal is not toggling, the switchover state machine controls the multiplexer through the `clksw` signal to switch to `inclk1`.

Figure 6–18. Automatic Switchover Upon Clock Loss Detection Note (1)



Note to Figure 6–18:

(1) Switchover is enabled on the falling edge of `INCLK0` or `INCLK1`, depending on which clock is available. In this figure, the switchover is enabled on the falling edge of `INCLK1`.

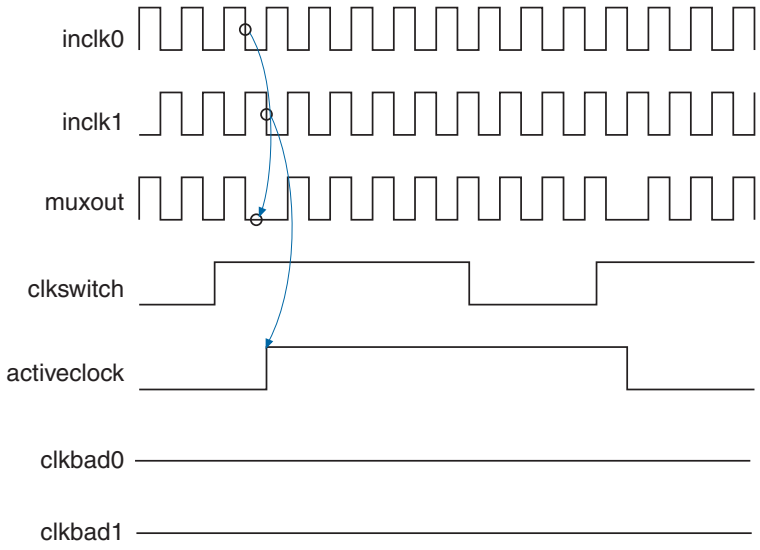
Manual Override

When using automatic switchover, you can switch input clocks by using the manual override feature with the `clkswitch` input.

Figure 6–19 shows an example of a waveform illustrating the switchover feature when controlled by `clkswitch`. In this case, both clock sources are functional and `inclk0` is selected as the reference clock. A low-to-high transition of the `clkswitch` signal initiates the switchover sequence. The `clkswitch` signal must be high for at least three clock cycles (at least three of the longer clock period if `inclk0` and `inclk1` have different frequencies). On the falling edge of `inclk0`, the counter's reference clock, `muxout`, is gated off to prevent any clock glitching. On the falling edge of `inclk1`, the reference clock multiplexer switches from `inclk0` to `inclk1` as the PLL reference. This is also when the `activeclock` signal changes to indicate which clock is currently feeding the PLL.

In this mode, the `activeclock` signal mirrors the `clkswitch` signal. As both blocks are still functional during the manual switch, neither `clkbad` signals go high. Since the switchover circuit is positive edge-sensitive, the falling edge of the `clkswitch` signal does not cause the circuit to switch back from `inclk1` to `inclk0`. When the `clkswitch` signal goes high again, the process repeats. The `clkswitch` signal and automatic switch only work if the clock being switched to is available. If the clock is not available, the state machine waits until the clock is available.

Figure 6–19. Clock Switchover Using the clkswitch Control



Manual Clock Switchover

Cyclone III PLLs support manual switchover, where the `clkswitch` signal controls whether `inclk0` or `inclk1` is the input clock to the PLL. The characteristics of the manual switchover is similar to the manual override feature in an automatic clock switchover, where the switchover circuit is edge-sensitive. When the `clkswitch` signal goes high, the switchover sequence starts. The falling edge of the `clkswitch` signal does not cause the circuit to switch back to the previous input clock.

For more information about PLL software support in the Quartus II software, refer to the *altpll Megafunction User Guide*.

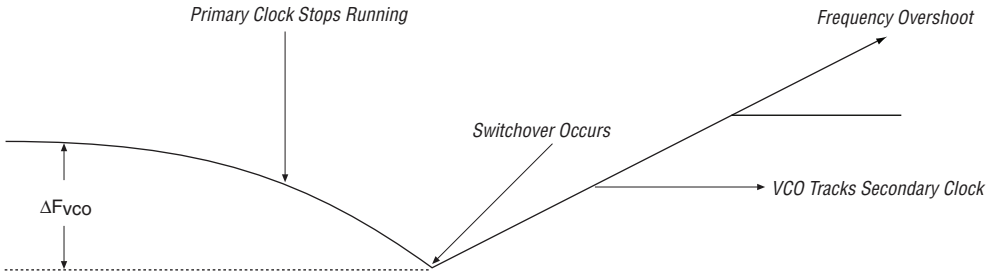
Guidelines

Use the following guidelines to design with clock switchover in PLLs.

- Clock loss detection and automatic clock switchover requires that the `inclk0` and `inclk1` frequencies be within 20% of each other. Failing to meet this requirement causes the `clkbad[0]` and `clkbad[1]` signals to function improperly.
- When using manual clock switchover, the difference between `inclk0` and `inclk1` can be more than 20%. However, differences between the two clock sources (frequency, phase, or both) will likely to cause the PLL to lose lock. Resetting the PLL ensures that the correct phase relationships are maintained between input and output clocks.
- Applications that require a clock switchover feature and a small frequency drift should use a low-bandwidth PLL. The low-bandwidth PLL reacts slower than a high-bandwidth PLL to reference input clock changes. When the switchover happens, a low-bandwidth PLL propagates the stopping of the clock to the output slower than a high-bandwidth PLL. A low-bandwidth PLL filters out jitter on the reference clock. However, be aware that the low-bandwidth PLL also increases lock time.
- After a switchover occurs, there may be a finite resynchronization period for the PLL to lock onto a new clock. The exact amount of time it takes for the PLL to re-lock is dependent on the PLL configuration.
- If the phase relationship between the input clock to the PLL and output clock from the PLL is important in your design, assert `areset` for 10 ns after performing a clock switchover. Wait for the locked signal (or gated lock) to go high before re-enabling the output clocks from the PLL.

- Figure 6–20 shows how the VCO frequency gradually decreases when the primary clock is lost and then increases as the VCO locks on to the secondary clock. After the VCO locks on to the secondary clock, some overshoot can occur (an over-frequency condition) in the VCO frequency.

Figure 6–20. VCO Switchover Operating Frequency



- Disable the system during switchover if it is not tolerant to frequency variations during the PLL resynchronization period. You can use the `clkbad[0]` and `clkbad[1]` status signals to turn off the PFD (`pfdena = 0`) so the VCO maintains its last frequency. You can also use the switch over state machine to switch over to the secondary clock. Upon enabling the PFD, output clock enable signals (`clkena`) can disable clock outputs during the switchover and resynchronization period. Once the lock indication is stable, the system can re-enable the output clock(s).

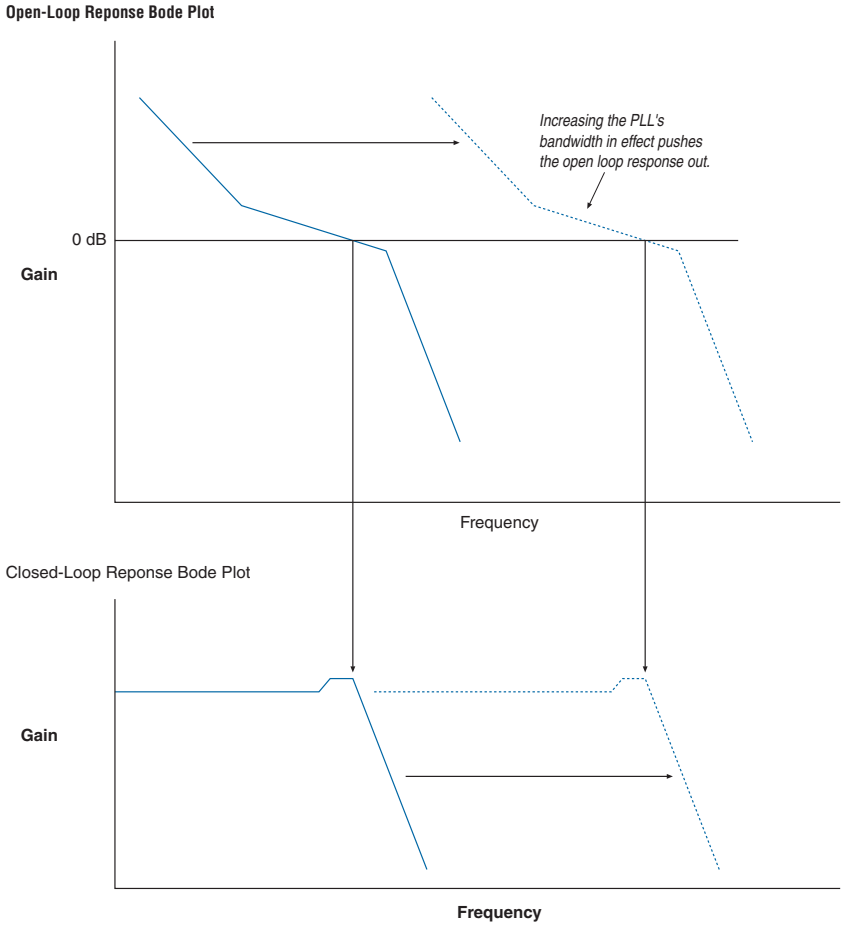
Programmable Bandwidth

Cyclone III PLLs provide advanced control of the PLL bandwidth using the PLL loop's programmable characteristics, including loop filter and charge pump.

Background

PLL bandwidth is the measure of the PLL's ability to track the input clock and its associated jitter. The closed-loop gain 3-dB frequency in the PLL determines the PLL bandwidth. The bandwidth is approximately the unity gain point for open-loop PLL response. As Figure 6–21 shows, these points correspond to approximately the same frequency. Cyclone III PLLs provide three bandwidth settings—low, medium (default), and high.

Figure 6–21. Open- and Closed-Loop Response Bode Plots



A high-bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low-bandwidth PLL filters out reference clock jitter but increases lock time. Cyclone III PLLs allow you to control the bandwidth over a finite range to customize the PLL characteristics for a particular application. The programmable bandwidth feature in Cyclone III PLLs benefits applications requiring clock switchover and PLL cascading.

A high-bandwidth PLL can benefit a system that needs to accept a spread-spectrum clock signal. Cyclone III PLLs can track a spread-spectrum clock by using a high-bandwidth setting. Using a low-bandwidth in this case could cause the PLL to filter out the jitter on the input clock.

A low-bandwidth PLL can benefit a system using clock switchover. When the clock switchover happens, the PLL input temporarily stops. A low-bandwidth PLL reacts more slowly to changes on its input clock and takes longer to drift to a lower frequency (caused by the input stopping) than a high-bandwidth PLL.

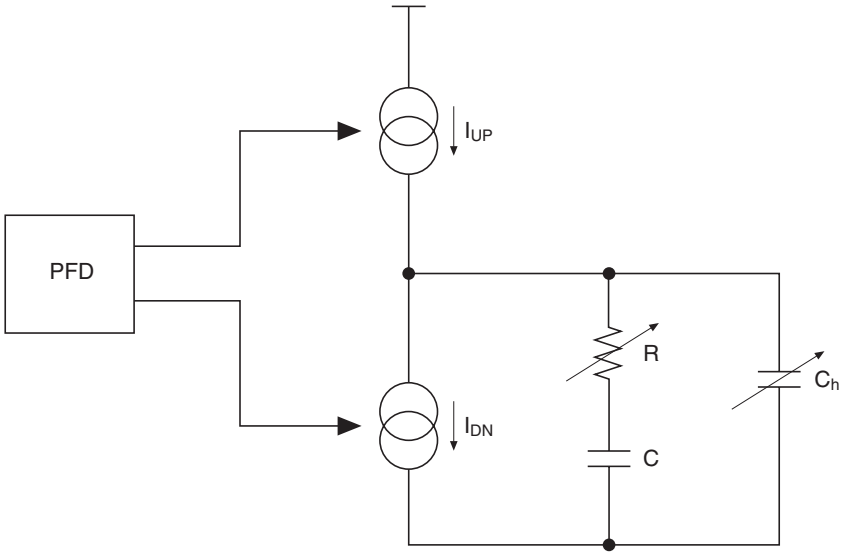
Implementation

Traditionally, external components such as the VCO or loop filter control a PLL's bandwidth. Most loop filters consist of passive components such as resistors and capacitors that take up unnecessary board space and increase cost. With Cyclone III PLLs, all the components are contained within the device to increase performance and decrease cost.

When you specify the bandwidth setting (low, medium, or high) in the altpll megawizard, the Quartus II software automatically sets the corresponding charge pump and loop filter (I_{CP}, R, C) values to achieve the desired bandwidth range.

Figure 6–22 shows the loop filter and the components that you can set using the Quartus II software. The components are the loop filter resistor, R, the high frequency capacitor, C_H, and the charge pump current, I_{UP} or I_{DN}.

Figure 6–22. Loop Filter Programmable Components



Phase-Shift Implementation

Phase shift is used to implement a robust solution for clock delays in Cyclone III devices. Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase output and counter starting time is the most accurate method of inserting delays, since it is purely based on counter settings, which are independent of process, voltage, and temperature.

You can phase shift the output clocks from the Cyclone III PLLs in either:

- Fine resolution using VCO phase taps
- Coarse resolution using counter starting time

Fine resolution phase shifts are implemented by allowing any of the output counters (C[4..0]) or the *m* counter to use any of the eight phases of the VCO as the reference clock. This allows you to adjust the delay time with a fine resolution. The minimum delay time that you can insert using this method is defined by:

(1)
$$\Phi_{\text{fine}} = \frac{T_{VCO}}{8} = \frac{1}{8f_{VCO}} = \frac{N}{8Mf_{REF}}$$

where f_{REF} is input reference clock frequency.

For example, if f_{REF} is 100 MHz, $N = 1$, and $M = 8$, then f_{VCO} = 800 MHz, and Φ_{fine} = 156.25 ps. The PLL operating frequency defines this phase shift, a value that depends on the reference clock frequency and the counter settings.

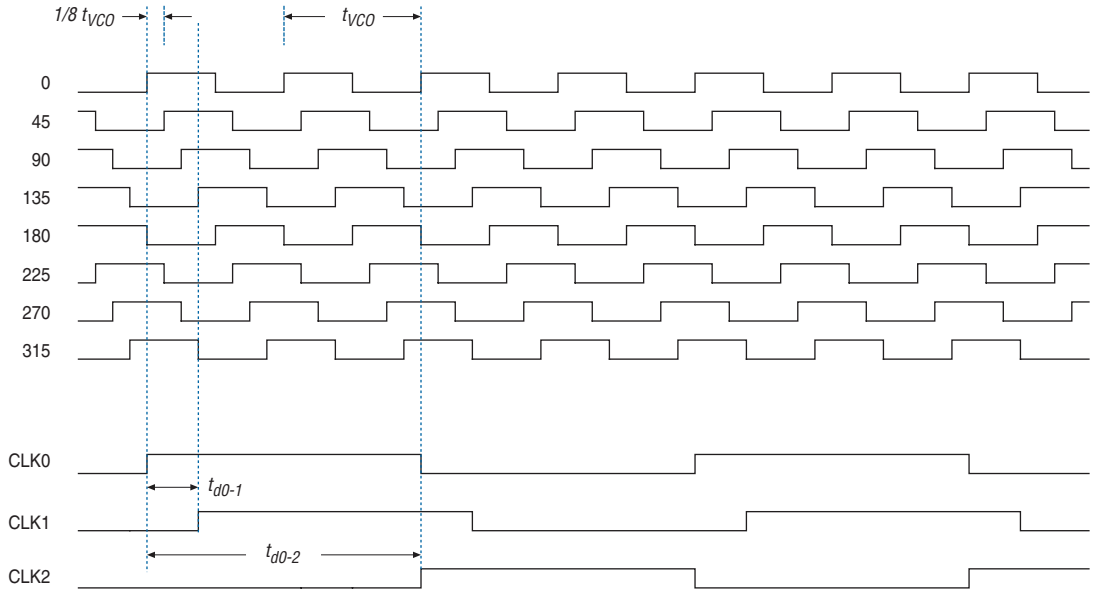
Coarse resolution phase shifts are implemented by delaying the start of the counters for a predetermined number of counter clocks. You can express coarse phase shift as:

$$\Phi_{coarse} = \frac{C-1}{f_{VCO}} = \frac{(C-1)N}{Mf_{REF}} \quad (2)$$

C is the count value set for the counter delay time (this is the initial setting in the PLL usage section of the compilation report in the Quartus II software). If the initial value is 1, *C* – 1 = 0° phase shift.

Figure 6–23 shows an example of phase shift insertion using the fine resolution through VCO phase taps method. The eight phases from the VCO are shown and labeled for reference. For this example, `CLK0` is based on the 0° phase from the VCO and has the C value for the counter set to one. The `CLK1` signal is divided by four, two VCO clocks for high time and two VCO clocks for low time. `CLK1` is based on the 135° phase tap from the VCO and has the C value for the counter set to one. The `CLK1` signal is also divided by 4. In this case, the two clocks are offset by 3 Φ_{fine}. `CLK2` is based on the 0° phase from the VCO but has the *C* value for the counter set to three. This creates a delay of 2 Φ_{coarse} (two complete VCO periods).

Figure 6–23. Delay Insertion Using VCO Phase Output and Counter Delay Time



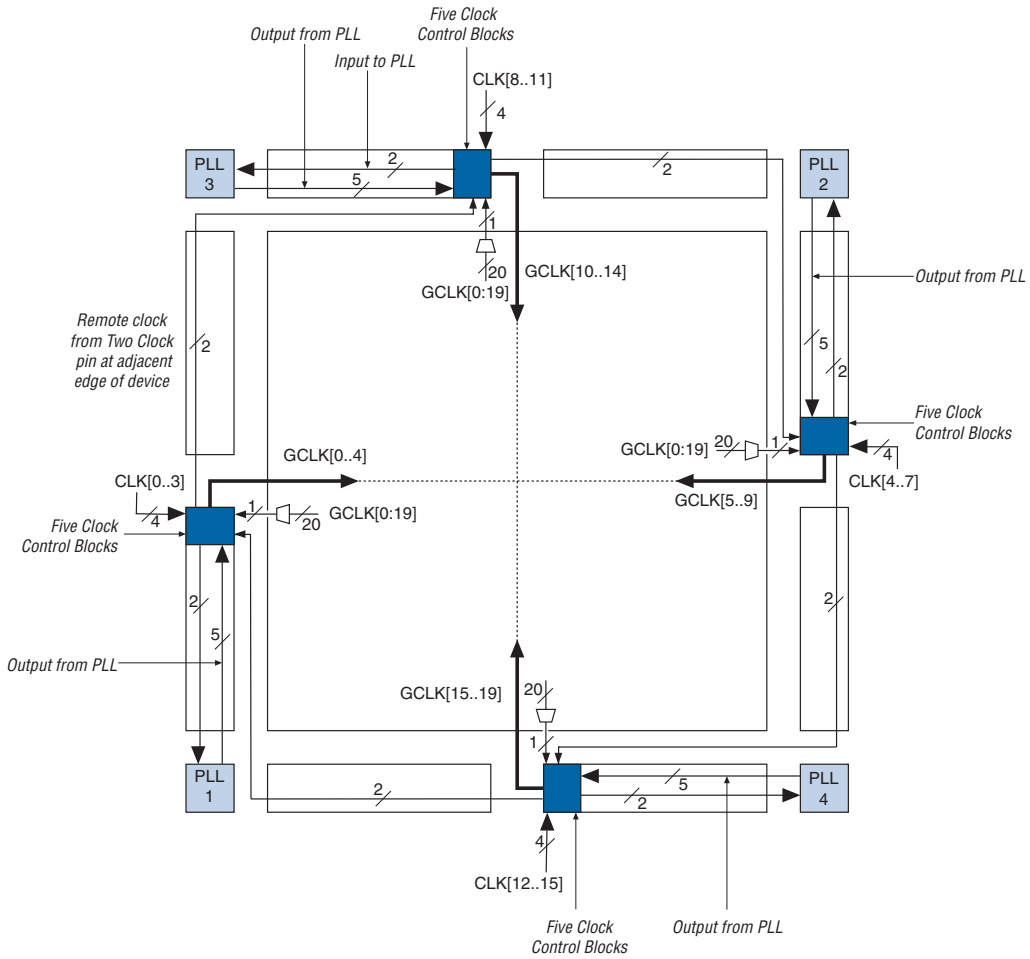
You can use the coarse and fine phase shifts to implement clock delays in Cyclone III devices.

Cyclone III devices support dynamic phase shifting of VCO phase taps only. The phase shift is configurable for any number of times, and each phase shift takes about one `SCANCLK` cycle, allowing you to implement large phase shifts quickly.

PLL Cascading

Two PLLs may be cascaded to each other through the clock network. If the design cascades PLLs, the source (upstream) PLL should have a high-bandwidth setting, while the destination (downstream) PLL should have a low-bandwidth setting. Figure 6–24 shows usage of GCLK while cascading PLLs.

Figure 6–24. PLL Cascading Using GCLK *Note (1)*



Note to Figure 6–24:

(1) For the EP3C5 and EP3C10 devices, there are only two PLLs (PLL1 and PLL2), ten clock control blocks and ten GCLKs.

PLL Reconfiguration

PLLs use several divide counters and different VCO phase taps to perform frequency synthesis and phase shifts. In Cyclone III PLLs, you can reconfigure both the counter settings and phase shift the PLL output clock in real time. You can also change the charge pump and loop filter components, which dynamically affects the PLL bandwidth. You can use these PLL components to update the output clock frequency, PLL bandwidth, and phase-shift in real time—without reconfiguring the entire FPGA.

The ability to reconfigure the PLL in real time is useful in applications that might operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output clock phase dynamically. For instance, a system generating test patterns is required to generate and transmit patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring the PLL components in real time allows you to switch between two such output frequencies within a few microseconds.

You can also use this feature to adjust clock-to-out (t_{CO}) delays in real time by changing the PLL output clock phase shift. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

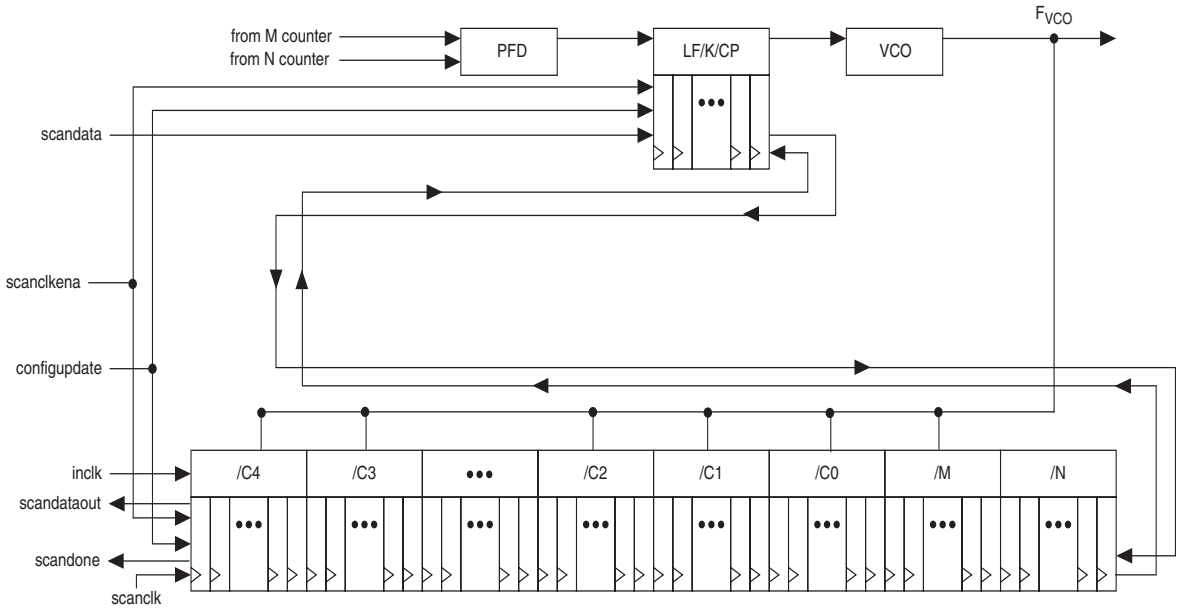
PLL Reconfiguration Hardware Implementation

The following PLL components are configurable in real time.

- Pre-scale counter (*n*)
- Feedback counter (*m*)
- Post-scale output counters (`c0-c4`)
- Dynamically adjust the charge pump current (I_{CP}), loop filter components (R, C) to facilitate on-the-fly reconfiguration of the PLL bandwidth

Figure 6–25 shows how to adjust PLL counter settings dynamically by shifting their new settings into a serial shift register chain or scan chain. Serial data shifts to the scan chain via the `scandataport` and shift registers are clocked by `scanclk`. The maximum `scanclk` frequency is 100 MHz. After shifting the last bit of data, asserting the `configupdate` signal for at least one `scanclk` clock cycle synchronously updates the PLL configuration bits with the data in the scan registers.

Figure 6–25. PLL Reconfiguration Scan Chain



The counter settings are updated synchronously to the clock frequency of the individual counters. Therefore, not all counters update simultaneously.

Table 6–8 shows how the programmable logic device (PLD) logic array or I/O pins drive these signals.

Table 6–8. Real-Time PLL Reconfiguration Ports

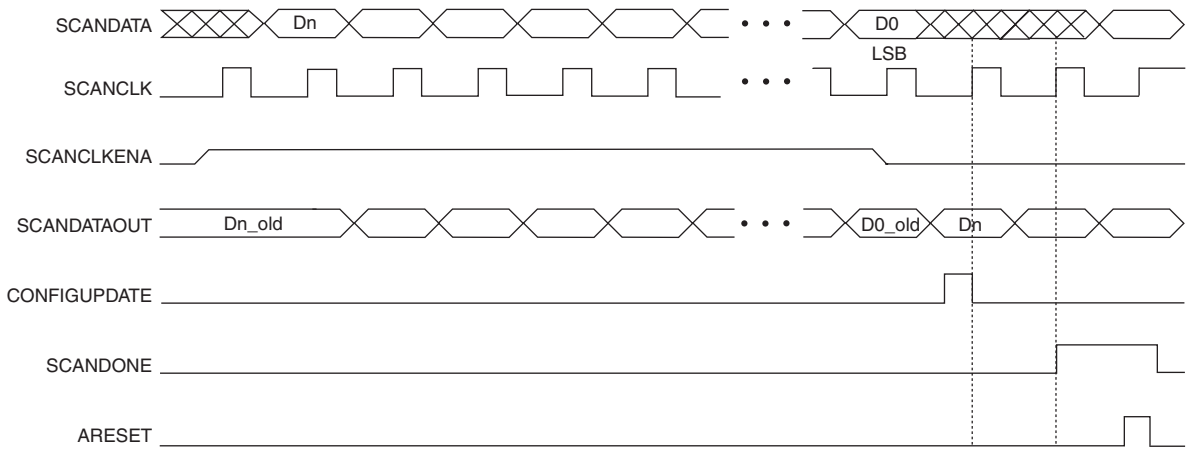
PLL Port Name	Description	Source	Destination
scandata	Serial input data stream to scan chain.	Logic array or I/O pins	PLL reconfiguration circuit
scanclk	Serial clock input signal. This clock can be free running.	Logic array or I/O pins	PLL reconfiguration circuit
configupdate	Updates data in the scan chain to the PLL. Active high.	Logic array or I/O pins	PLL reconfiguration circuit
scanclkena	Enables scanclk and allows the scandata to be loaded in the scan chain. Active high.	Logic array or I/O pins	PLL reconfiguration circuit
scandone	A high pulse indicates the PLL has finished reconfiguration.	PLL reconfig. circuit	Logic array or I/O pins
scandataout	Shifts out contents of the scan chain.	PLL reconfig. circuit	Logic array or I/O pins

To reconfigure the PLL counters, perform the following steps:

1. The scanclkena signal is asserted at least one scanclk cycle prior to shifting in the first bit of scandata (Dn).
2. Serial data (scandata) is shifted into the scan chain on the second rising edge of scanclk.
3. After all 144 bits have been scanned into the scan chain, the scanclkena signal is deasserted to prevent inadvertent shifting of bits in the scan chain.
4. The configupdate signal is asserted for one scanclk cycle to update the PLL counters with the contents of the scan chain.
5. The scandone signal goes high indicating that the PLL is being reconfigured. A falling edge indicates that the PLL counters have been updated with new settings.
6. Reset the PLL using the areset signal if you make any changes to the M, N counters or the I_{CP}, R, C settings. You do not need to reset the PLL when reconfiguring just the post-scale counters.
7. Steps 1 through 5 can be repeated to reconfigure the PLL any number of times.

Figure 6–26 shows a functional simulation of the PLL reconfiguration feature.

Figure 6–26. PLL Reconfiguration Scan Chain



When reconfiguring the counter clock frequency, the corresponding counter phase-shift settings cannot be reconfigured using the same interface. You can reconfigure phase shifts in real time using the dynamic phase-shift reconfiguration interface. If you reconfigure the counter frequency, but wish to keep the same non-zero phase-shift setting (for example, 90°) on the clock output, then you will need to reconfigure the phase shift after reconfiguring the counter clock frequency.

Post-Scale Counters (c0 to c4)

The multiply or divide values and duty cycle of post-scale counters can be configured in real time. Each counter has an 8-bit high time setting and an 8-bit low time setting. The duty cycle is the ratio of output high or low time to the total cycle time, which is the sum of the two. Additionally, these counters have two control bits, `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

When the `rbypass` bit is set to 1, it bypasses the counter, resulting in a divide by 1. When this bit is set to 0, the PLL computes the effective division of the VCO output frequency based on the high and low time counters. For example, if the post-scale divide factor is 10, the high and low count values could be set to 5 and 5 respectively, to achieve a 50–50% duty cycle. The PLL implements this duty cycle by transitioning the output clock from high to low on the rising edge of the VCO output clock. However, a 4 and a 6 setting for the high and low count values, respectively, would produce an output clock with 40–60% duty cycle.

The `rselodd` bit indicates an odd divide factor for the VCO output frequency with a 50% duty cycle. For example, if the post-scale divide factor is 3, the high and low time count values is 2 and 1, respectively, to achieve this division. This implies a 67%–33% duty cycle. If you need a 50%–50% duty cycle, you must set the `rselodd` control bit to 1 to achieve this duty cycle despite an odd division factor. The PLL implements this duty cycle by transitioning the output clock from high to low on a falling edge of the VCO output clock. When you set `rselodd` = 1, you subtract 0.5 cycles from the high time and you add 0.5 cycles to the low time. For example:

- High time count = 2 cycles
- Low time count = 1 cycle
- `rselodd` = 1 effectively equals:
  - High time count = 1.5 cycles
  - Low time count = 1.5 cycles
  - Duty cycle = (1.5/3) % high time count and (1.5/3) % low time count

Scan Chain Description

Cyclone III PLLs have a 144-bit scan chain. Table 6–9 shows the number of bits for each component of the PLL.

Table 6–9. Cyclone III PLL Reprogramming Bits

Block Name	Number of Bits		
	Counter	Other	Total
C4 *(1)*	16	2 *(2)*	18
C3	16	2 *(2)*	18
C2	16	2 *(2)*	18
C1	16	2 *(2)*	18
C0	16	2 *(2)*	18
M	16	2 *(2)*	18
N	16	2 *(2)*	18
Charge Pump	9	0	9
Loop Filter *(3)*	9	0	9
Total number of bits:			144

Notes to Table 6–9:

(1) LSB bit for C4 low-count value is the first bit shifted into the scan chain.

(2) These two control bits include `rbypass`, for bypassing the counter, and `rselodd`, to select the output clock duty cycle.

(3) MSB bit for loop filter is the last bit shifted into the scan chain.

Figure 6–27 shows the scan chain order of PLL components.

Figure 6–27. PLL Component Scan Chain Order

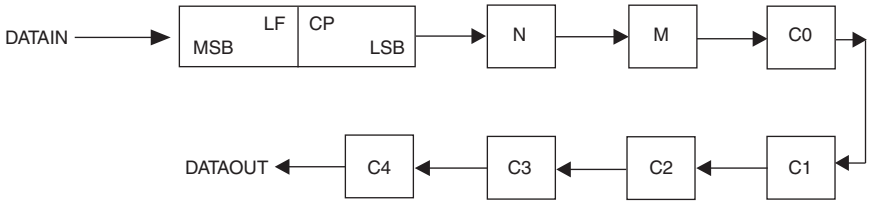
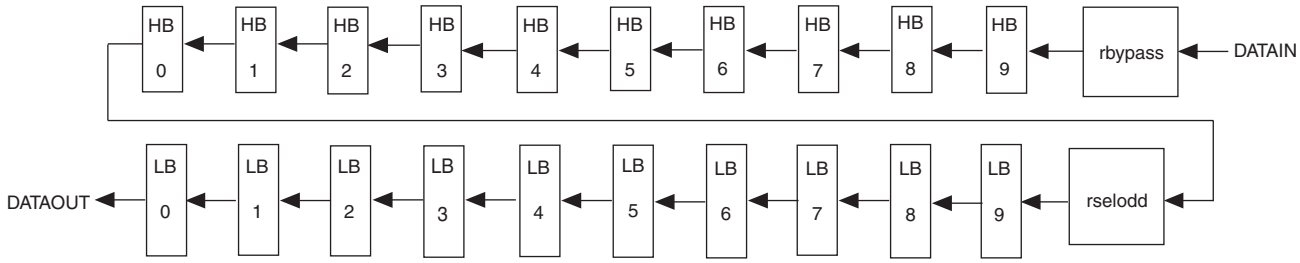


Figure 6–28 shows the scan chain bit order sequence for one PLL post-scale counter in Cyclone III PLLs.

Figure 6–28. Scan Chain Bit Order



Charge Pump and Loop Filter

You can reconfigure the charge pump and loop filter settings to update the PLL bandwidth in real time. Table 6–10, Table 6–11, and Table 6–12 show the possible settings for charge pump (I_{CP}) and loop filter resistor (R) and capacitor (C) values for the Cyclone III PLLs.

Table 6–10. Charge Pump Bit Control

CP[2]	CP[1]	CP[0]	Setting (Decimal)
0	0	0	0
1	0	0	1
1	1	0	3
1	1	1	7

Table 6–11. Loop Filter Resistor Value Control

LFR[4]	LFR[3]	LFR[2]	LFR[1]	LFR[0]	Setting (Decimal)
0	0	0	0	0	0
0	0	0	1	1	3
0	0	1	0	0	4
0	1	0	0	0	8
1	0	0	0	0	16
1	0	0	1	1	19
1	0	1	0	0	20
1	1	0	0	0	24
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	1	0	30

Table 6–12. Loop Filter Control of High Frequency Capacitor

LFC[1]	LFC[0]	Setting (Decimal)
0	0	0
0	1	1
1	1	3

Bypassing PLL Counter

Bypassing a PLL counter results in a multiply (*m* counter) or a divide (*n*, *C0* to *C4* counters) factor of one. Table 6–13 shows the settings for bypassing the counters in Cyclone III PLLs.

Table 6–13. PLL Counter Settings

PLL Scan Chain Bits [0..8] Settings									Description
LSB								MSB	
X	X	X	X	X	X	X	X	1 *(1)*	PLL counter bypassed
X	X	X	X	X	X	X	X	0 *(1)*	PLL counter not bypassed

Note to Table 6–13:
(1) Bypass bit.

To bypass any of the PLL counters, set the bypass bit to 1. This ignores the values on the other bits.

Dynamic Phase Shifting

The dynamic phase shifting feature allows the output phase of individual PLL outputs to be dynamically adjusted relative to each other and the reference clock without the need to send serial data through the scan chain of the corresponding PLL. This simplifies the interface and allows you to quickly adjust clock-to-out (t_{CO}) delays by changing output clock phase shift in real time. This is achieved by incrementing or decrementing the VCO phase-tap selection to a given C counter or to the M counter. The phase is shifted by 1/8 the VCO frequency at a time. The output clocks are active during this phase reconfiguration process.

Table 6–14 shows the control signals that are used for dynamic phase shifting.

Table 6–14. Dynamic Phase Shifting Control Signals

Signal Name	Description	Source	Destination
PHASECOUNTERSELECT [2:0]	Counter Select. Three bits decoded to select either the M or one of the C counters for phase adjustment. One address map to select all C counters. This signal is registered in the PLL on the rising edge of SCANCLK.	Logic array or I/O pins	PLL reconfiguration circuit
PHASEUPDOWN	Selects dynamic phase shift direction; 1= UP; 0 = DOWN. Signal is registered in the PLL on the rising edge of SCANCLK.	Logic array or I/O pins	PLL reconfiguration circuit
PHASESTEP	Logic high enables dynamic phase shifting.	Logic array or I/O pins	PLL reconfiguration circuit
SCANCLK	Free running clock from core used in combination with PHASESTEP to enable/disable dynamic phase shifting. Shared with SCANCLK for dynamic reconfiguration.	GCLK or I/O pins	PLL reconfiguration circuit
PHASEDONE	When asserted, it indicates to core-logic that the phase adjustment is complete and PLL is ready to act on a possible second adjustment pulse. Asserts based on internal PLL timing. Deasserts on rising edge of SCANCLK.	PLL reconfiguration circuit	Logic array or I/O pins

Table 6–15 shows the PLL counter selection based on the corresponding PHASECOUNTERSELECT setting.

Table 6–15. Phase Counter Select Mapping

PHASECOUNTERSELECT [2]	[1]	[0]	Selects
0	0	0	All Output Counters
0	0	1	M Counter
0	1	0	C0 Counter
0	1	1	C1 Counter
1	0	0	C2 Counter
1	0	1	C3 Counter
1	1	0	C4 Counter

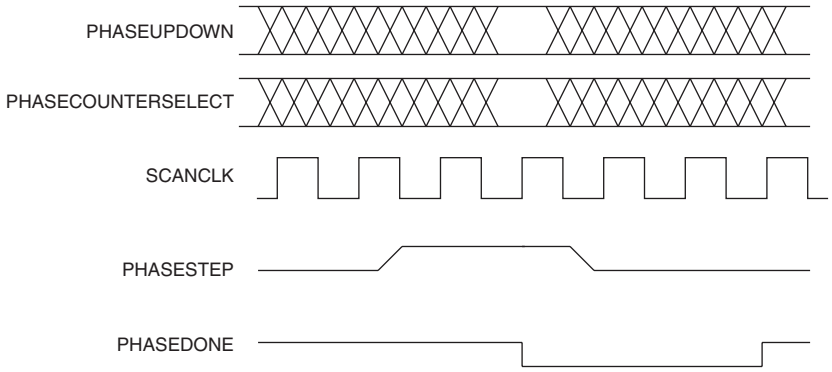
To perform one dynamic phase shift step, perform the following procedure:

1. Set phaseupdown and phasecounterselect as required.
2. Assert phasestep. Each phasestep pulse enables one phase shift. The phasestep pulses must be at least one scanclk cycle apart.

3. Wait for `phasedone` to go low.
4. Deassert `phasestep`.
5. Wait for `phasedone` to go high.
6. Repeat steps 1 through 5 as many times as required to get multiple phase shifts.

All signals are synchronous to `scanclk`, so they will be latched on the `scanclk` edges and must meet t_{SU}/t_H requirements (with respect to the `scanclk` edges).

Figure 6–29. PLL Dynamic Phase Shift



Dynamic phase shifting can be repeated indefinitely. All signals are synchronous to `scanclk`, so they must meet t_{SU}/t_H requirements with respect to `scanclk` edges.

The `phasestep` signal is latched on the negative edge of `scanclk`. In Figure 6–29, this is shown by the second `scanclk` falling edge. `Phasestep` must stay high for at least two `scanclk` cycles. On the second `scanclk` rising edge after phasestep is latched (indicated by the fourth rising edge), the values of `phaseupdown` and `phasecounterselect` are latched and the PLL starts dynamic phase shifting for the specified counter or counters and in the indicated direction. On the fourth `scanclk` rising edge, `phasedone` goes high to low and remains low until the PLL finishes dynamic phase shifting. You can perform another dynamic phase shift after the `phasedone` signal goes from low to high.

Depending on the VCO and `scanclk` frequencies, `phasedone` low time may be greater than or less than one `scanclk` cycle. The maximum time for reconfiguring phase shift dynamically is to be determined (TBD) based on device characterization.

After `phasedone` goes from low to high, you can perform another dynamic phase shift. Phasestep pulses must be at least one `scanclk` cycle apart.

For details about the altpll_reconfig megawizard Plug-In Manager, refer to the *altpll_reconfig Megafunction User Guide*.

Spread-Spectrum Clocking

Cyclone III devices can accept a spread-spectrum input with typical modulation frequencies. However, the device cannot automatically detect that the input is a spread-spectrum signal. Instead, the input signal looks like deterministic jitter at the input of the PLL. Cyclone III PLLs can track a spread-spectrum input clock as long as it is within the input jitter tolerance specifications. Cyclone III devices cannot generate spread-spectrum signals internally.

PLL Specifications

Refer to the Cyclone III Device datasheet in the *DC and Switching Characteristics* chapter in volume 1 of the *Cyclone III Device Handbook* for information about PLL timing specifications.

Board Layout

The PLL circuits in Cyclone III devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components.

VCCA and GNDA

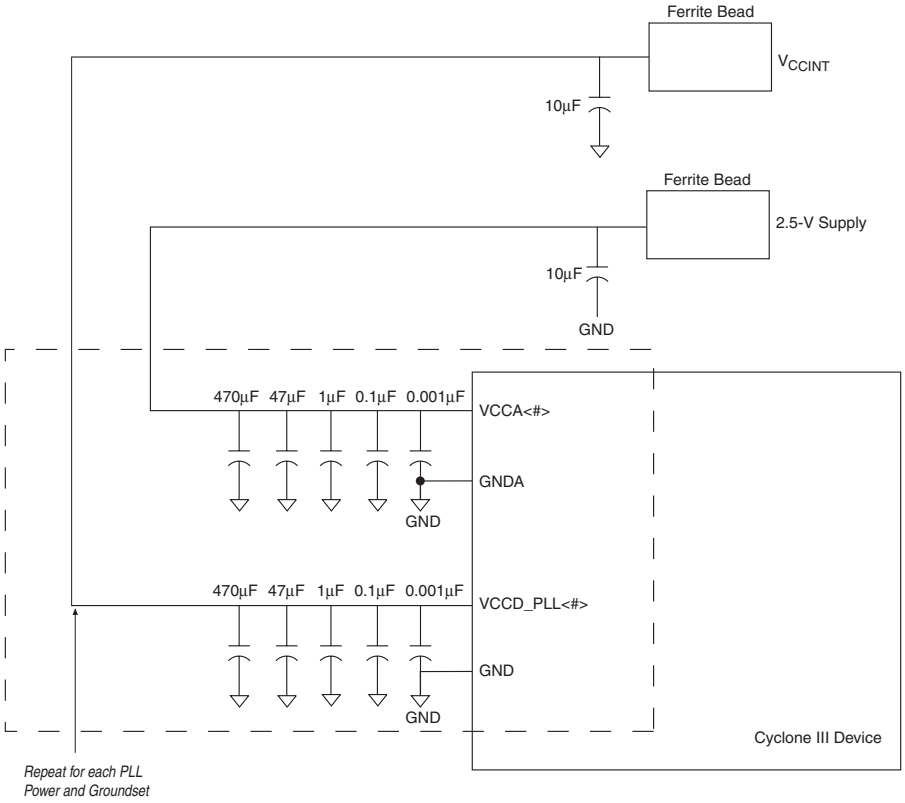
Each Cyclone III PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called `VCCA`<*PLL number*> and `GNDA`. Connect the `VCCA` power pin to a 2.5-V power supply, even if you do not use the PLL. Run a thick trace from the power supply to each `VCCA` pin. The traces should be at least 20 mils thick.

VCCD and GND

The digital power and ground pins are labeled `VCCD_PLL`<*PLL number*> and `GND`. The `VCCD` pin supplies the power for the digital circuitry in the PLL. Connect these `VCCD` pins to the quietest digital supply on the board. In most systems, this is the digital 1.2-V supply to the device's `VCCINT` pins. Connect the `VCCD` pins to a power supply even if you do not use the PLL. You can connect the `GND` pins directly to the same ground plane as the device's digital ground.

You should filter each `VCCA` and `VCCD` pin with a decoupling circuit shown in Figure 6–30. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10 µF tantalum parallel capacitor where the power enters the board. Decouple each `VCCA` pin with a 0.1 µF, 0.001 µF, 1 µF, 47 µF, and 470 µF parallel combination of ceramic capacitors located as close as possible to the Cyclone III device. You can connect the `GNDA` pins directly to the same ground plane as the device's digital ground.

Figure 6–30. PLL Power Schematic for Cyclone III PLLs Note (1)



Note to Figure 6–30:

(1) Applies to PLL 1 through 4.

Conclusion

Cyclone III device PLLs provide you with complete control of device clocks and system timing. The ability to reconfigure the PLL counter clock frequency and phase shift in real time can be especially useful in prototyping environments, allowing you to sweep PLL output frequencies and adjust the output clock phase shift dynamically. These PLLs are capable of offering flexible system-level clock management that was previously only available in discrete PLL devices. Cyclone III PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.

Referenced Documents

This chapter references the following documents:

- *altclkctrl Megafunction User Guide*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *altpll Megafunction User Guide*
- *altpll_reconfig Megafunction User Guide*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*

Document Revision History

Table 6–16 shows the revision history for this document.

Table 6–16. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated Table 6–1and Table 6–4 with EP3C120 information. • Updated "Clock Control Block" section. • Updated `locked` signal information in "PLL Control Signals" section and added Figure 6–16. • Updated "Manual Override" section. • Updated "Manual Clock Switchover" section. • Added new "Programmable Bandwidth" section with Figure 6–21 and Figure 6–22. • Replaced Figure 6–30 with correct diagram. • Added chapter TOC and "Referenced Documents" section.	• Updated document with EP3C120 information.
March 2007 v1.0	Initial Release.	N/A

Section 2. I/O and External Memory Interfaces

This section provides information about Cyclone® III device I/O features and high-speed differential and external memory interfaces.

This section includes the following chapters:

- Chapter 7, Cyclone III Device I/O Features
- Chapter 8, High-Speed Differential Interfaces in Cyclone III Devices
- Chapter 9, External Memory Interfaces in Cyclone III Devices

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

7. Cyclone III Device I/O Features

CIII51007-1.1

Introduction

Two key factors affecting board design today drove the design of Cyclone® III devices I/O capabilities. The first is the diversification of I/O standards in many low-cost applications. The second is a significant increase in the required I/O performance. Our objective was to create a device that made accommodating these design needs easy and flexible.

Cyclone III I/O flexibility has been increased from previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and by adding dedicated differential buffers, eliminate the need for external resistors in many applications, such as display system interfaces. The Altera® Quartus® II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter contains the following sections:

- "Cyclone III I/O Element" on page 7–1
- "I/O Element Features" on page 7–7
- "On-Chip Termination Support" on page 7–11
- "I/O Standards" on page 7–15
- "Termination Scheme for I/O Standards" on page 7–16
- "I/O Banks" on page 7–19

Overview

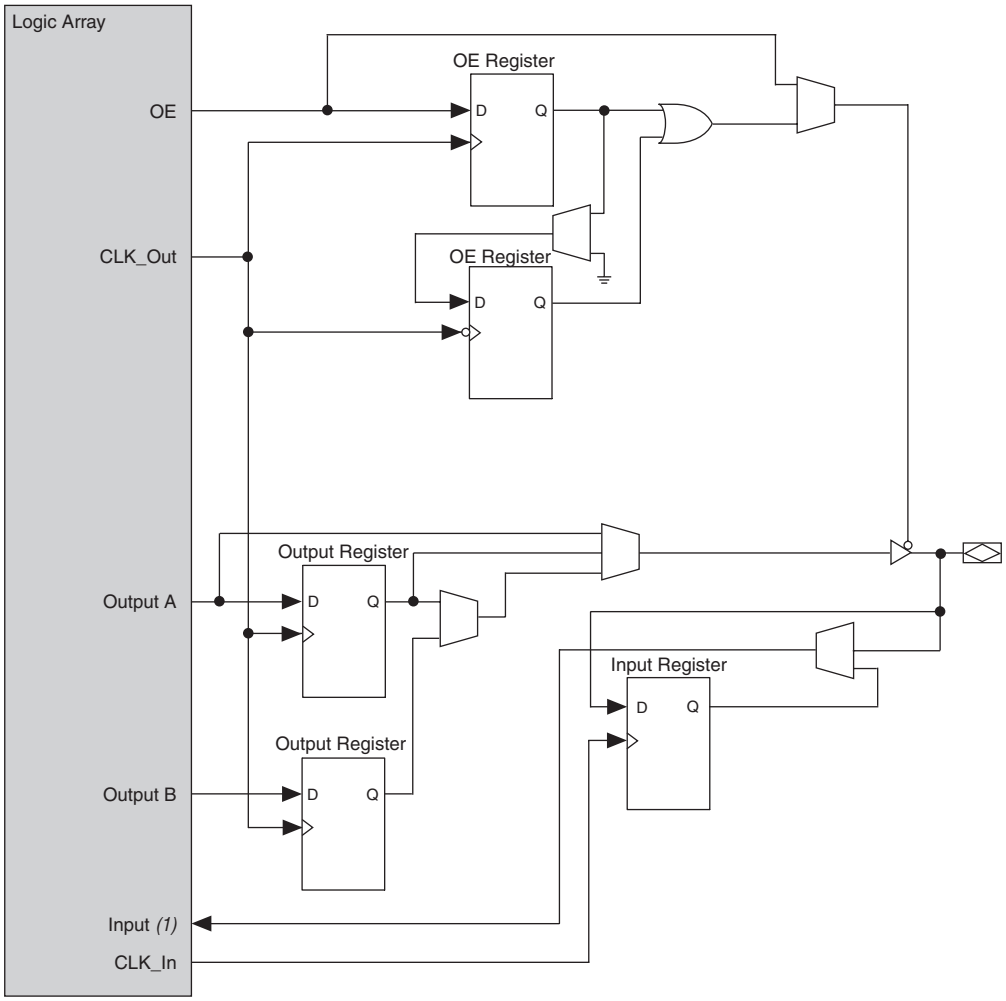
Each Cyclone III device I/O pin is fed by an I/O element (IOE) located at the ends of logic array block (LAB) rows and columns around the periphery of the Cyclone III device. The I/O pins support various single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and five registers for registering input, output, and output-enable signals. Cyclone III I/O supports a wide range of features, including:

- Single-ended non-voltage-referenced and voltage-referenced I/O standards
- Differential I/O standards
- Output current strength control
- Programmable slew rate control
- Open-drain outputs
- Bus-hold circuitry
- PCI-clamp diode
- Programmable pull-up resistors in user mode
- Programmable input and output delays
- Programmable low-voltage differential signaling (LVDS) pre-emphasis
- On-chip termination with and without calibration

Cyclone III I/O Element

Cyclone III device IOEs contain a bidirectional I/O buffer and five registers for complete embedded bidirectional single-data rate transfer. Figure 7–1 shows the Cyclone III IOE structure. The IOE contains one input register, two output registers, and two output-enable registers. The two output registers and two output-enable registers are utilized for double-data rate (DDR) applications. You can use the input registers for fast setup times and the output registers for fast clock-to-output times. Additionally, you can use the output-enable (OE) registers for fast clock-to-output enable timing. You can use IOEs for input, output, or bidirectional data paths.

Figure 7–1. Cyclone III IOE Structure



Note to Figure 7–1:

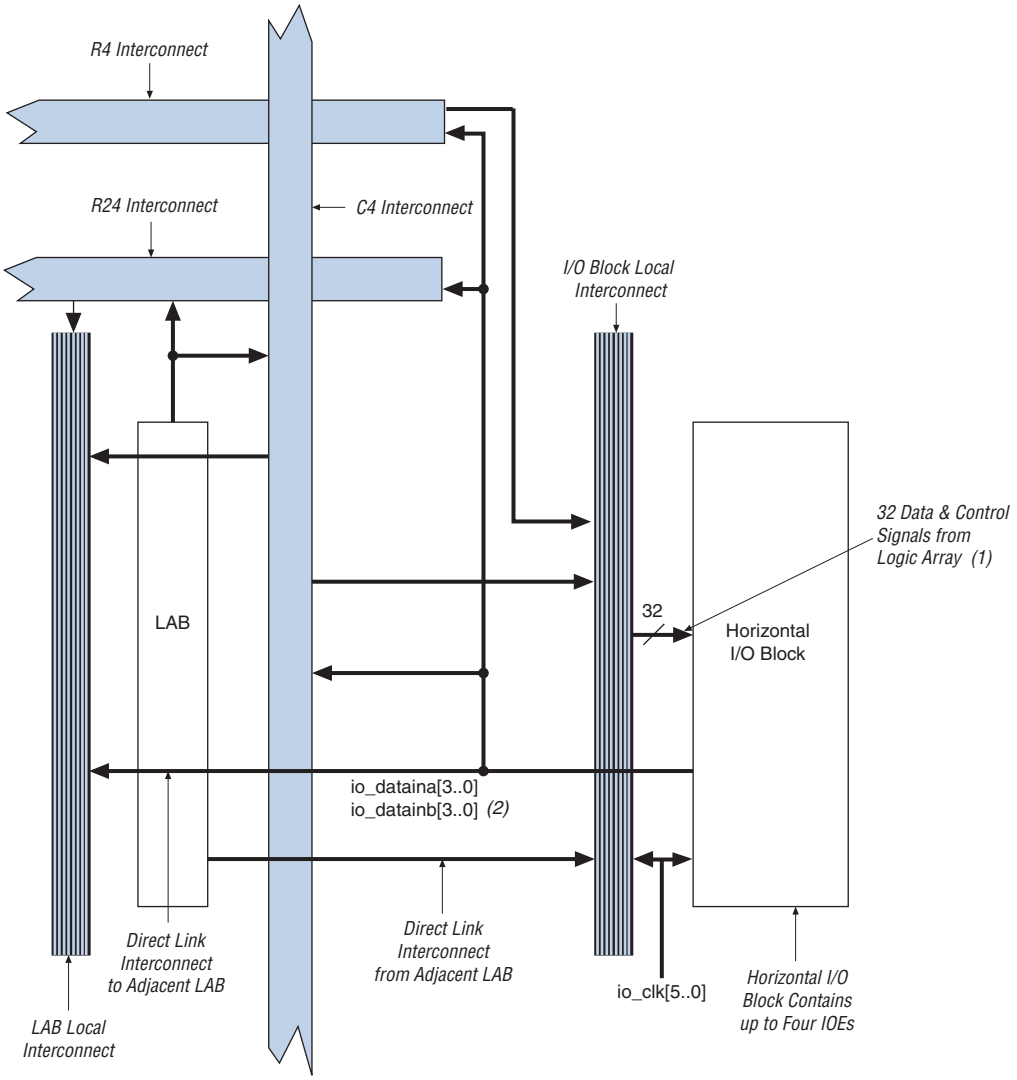
(1) There are two paths available for combinational or registered inputs to the logic array. Each path contains a unique programmable delay chain.

The IOEs are located in I/O blocks around the periphery of the Cyclone III device. There are up to four IOEs per row I/O block and up to five IOEs per column I/O block (column I/O blocks span two columns), depending on logic element (LE)-rich or I/O-rich devices.

The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 7–2 shows how a row I/O block connects to the logic array. Figures 7–3 and 7–4 show how a column I/O block connects to the logic array.

For more information about Cyclone III routing architecture, refer to the *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*.

Figure 7–2. Row I/O Block Connection to the Interconnect

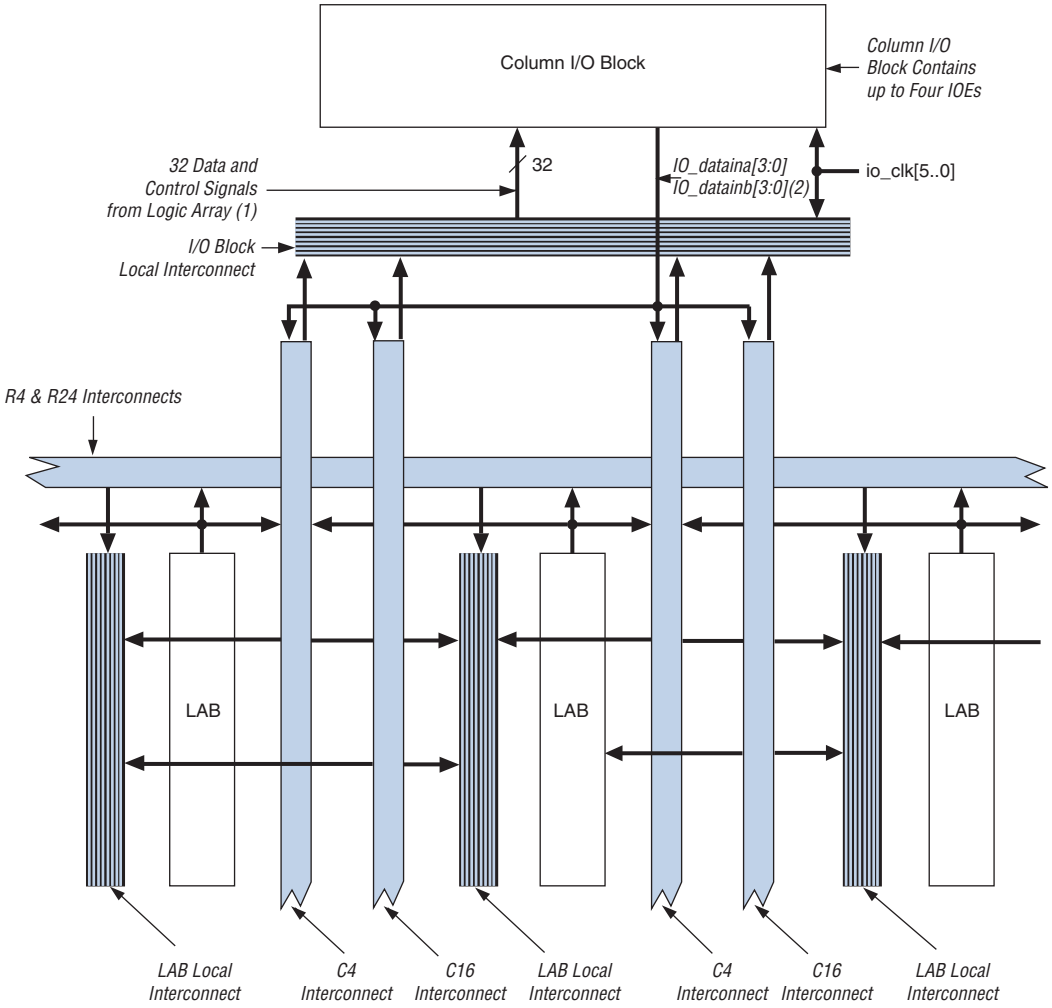


Notes to Figure 7–2

(1) The 32 data and control signals are used to support up to four IOEs on each row I/O block.

(2) Each of the four IOEs in the row I/O block can have two `io_datain` (combinational or registered) inputs.

Figure 7–3. Column I/O Block Connection to the Interconnect for LE-Rich Devices (EP3C5, EP3C10, EP3C25, EP3C55, EP3C80, and EP3C120)

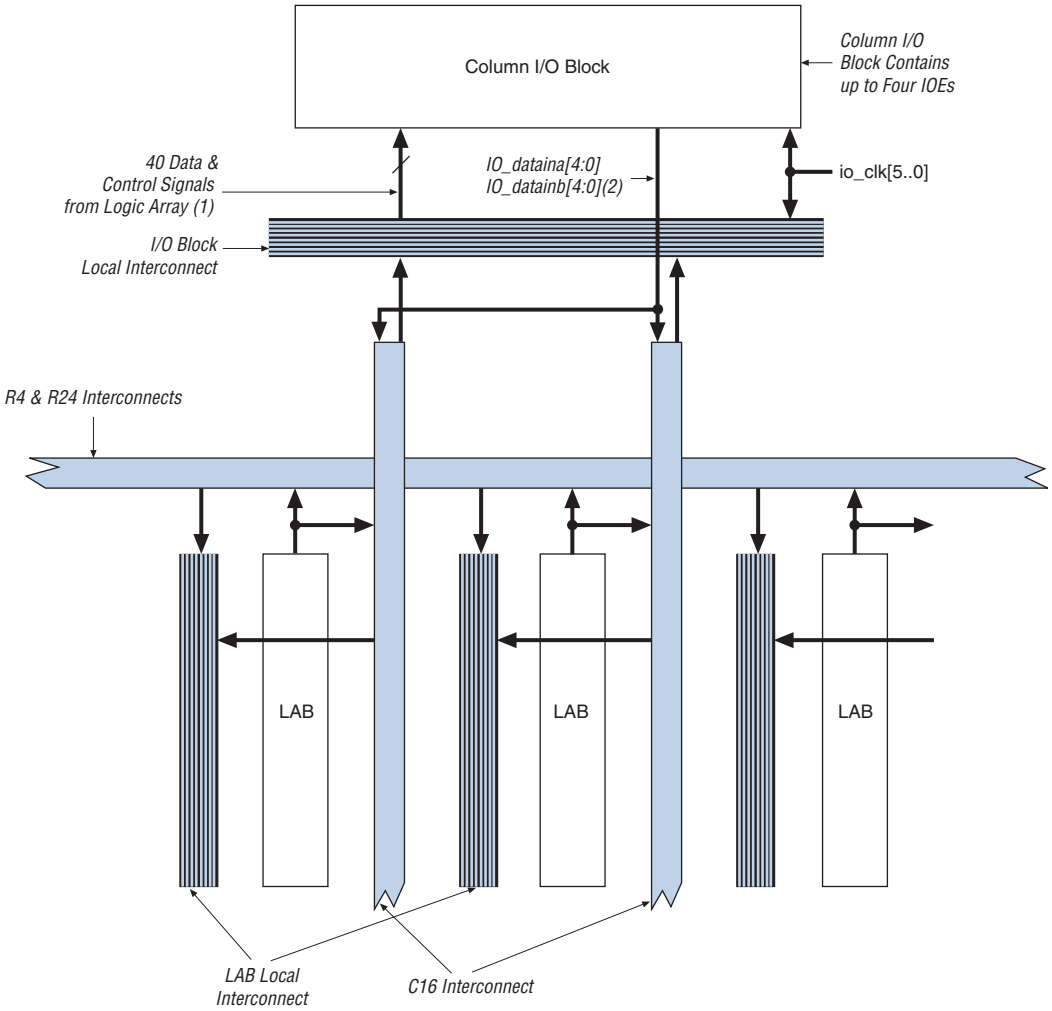


Notes to Figure 7–3:

(1) The 32 data and control signals are used to support up to four IOEs per two column I/O blocks.

(2) Each of the four IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.

Figure 7–4. Column I/O Block Connection to the Interconnect for I/O-Rich Devices (EP3C16 and EP3C40)



Notes to Figure 7–4:

(1) The 40 data and control signals are used to support up to five IOEs per two column I/O block.

(2) Each of the five IOEs in the column I/O block can have two `io_datain` (combinational or registered) inputs.

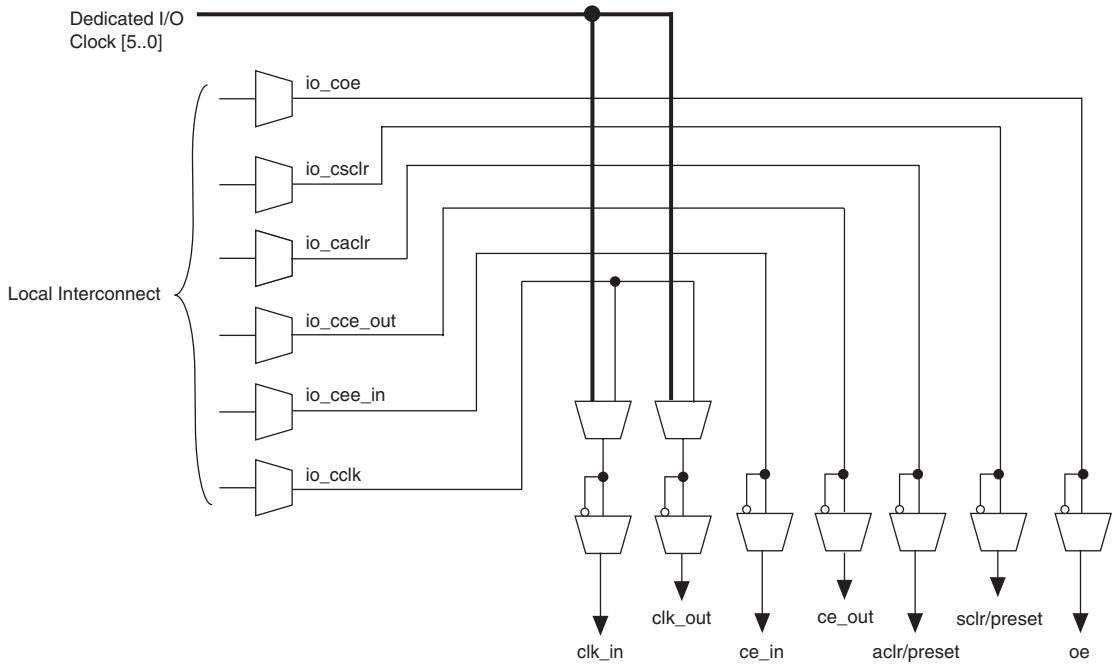
The pin's `datain` signals can drive the logic array. The logic array drives the control and data signals, providing a flexible routing resource. The row or column IOE clocks (`io_clk[5..0]`) provide a dedicated routing resource for low-skew, high-speed clocks. The global clock network generates the IOE clocks that feed the row or column I/O regions.

Each IOE contains its own control signal selection for the following control signals:

- `oe`
- `ce_in`
- `ce_out`
- `aclr/preset`
- `sclr/preset`
- `clk_in`
- `clk_out`

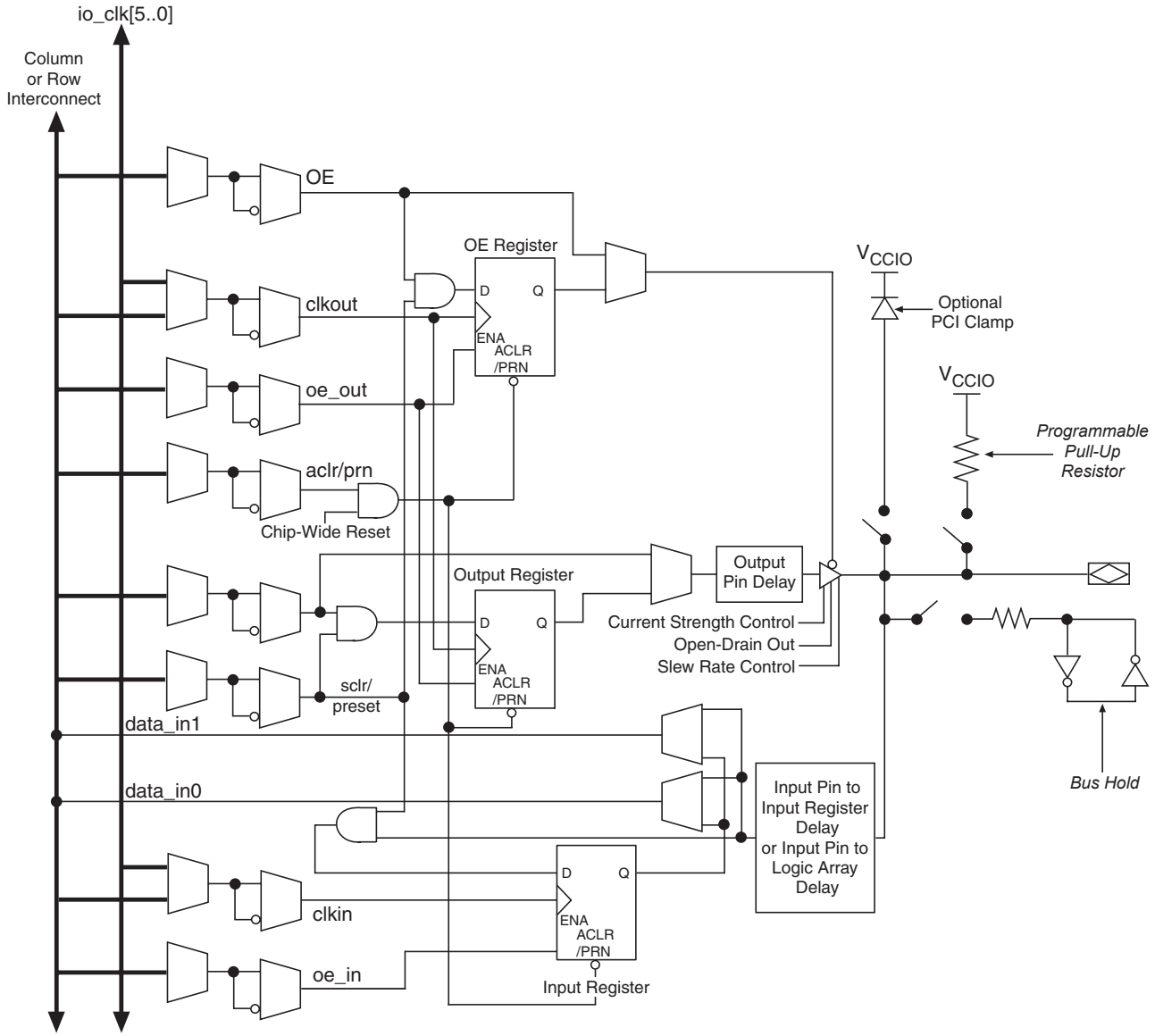
Figure 7–5 illustrates the control signal selection.

Figure 7–5. Control Signal Selection Per IOE



In bidirectional operation, you can use the input register for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. You can use the output register for data requiring fast clock-to-output performance. The OE register is available for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock-enable source from the local interconnect in the associated LAB, dedicated I/O clocks, or column and row interconnects. All registers share `sclr` and `aclr`, but each register can individually disable `sclr` and `aclr`. Figure 7–6 shows the IOE in bidirectional configuration.

Figure 7–6. Cyclone III IOE in Bidirectional I/O Configuration



I/O Element Features

Programmable Current Strength

The output buffer for each Cyclone III device I/O pin has a programmable current strength control for certain I/O standards. The LVTTL, LVCMOS, SSTL-2 Class I and II, SSTL-18 Class I and II, HSTL-18 Class I and II, HSTL-15 Class I and II, and HSTL-12 Class I and II standards have several levels of current strength that you can control.

For more information, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Table 7–1 shows the possible settings for the I/O standards with current strength control. These programmable current-strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for I_{OH} and I_{OL} of the corresponding I/O standard.

When you use programmable current strength, on-chip series termination is not available.

Table 7–1. Programmable Current Strength Note (1) (Part 1 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Left and Right I/O Pins
1.2-V LVCMOS	2	2
	4	4
	6	6
	8	8
	10	10
	12	—
1.5-V LVCMOS	2	2
	4	4
	6	6
	8	8
	10	10
	12	12
	16	16
1.8-V LVTTL/LVCMOS	2	2
	4	4
	6	6
	8	8
	10	10
	12	12
	16	16
2.5-V LVTTL/LVCMOS	4	4
	8	8
	12	12
	16	16
3.0-V LVCMOS	4	4
	8	8
	12	12
	16	16
3.0-V LVTTL	4	4
	8	8
	12	12
	16	16
3.3-V LVCMOS *(2)*	***2***	***2***
3.3-V LVTTL *(2)*	4	4
	8	***8***
HSTL-12 Class I	8	8
	10	10
	12	—
HSTL-12 Class II	14	—

Table 7–1. Programmable Current Strength Note (1) (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Left and Right I/O Pins
HSTL-15 Class I	8	8
	10	10
	12	12
HSTL-15 Class II	16	16
HSTL-18 Class I	8	8
	10	10
	12	12
HSTL-18 Class II	16	16
SSTL-18 Class I	8	8
	10	10
	12	12
SSTL-18 Class II	12	12
	16	16
SSTL-2 Class I	8	8
	12	12
SSTL-2 Class II	16	16

Note to Table 7–1:

(1) The default setting in the Quartus II software is 50 Ω OCT without calibration for all non-voltage reference and HSTL/SSTL class I I/O standards. The default setting is 25 Ω OCT without calibration for HSTL/SSTL class II I/O standards.

(2) The default current setting in the Quartus II software is highlighted in italic bold for 3.3-V LVTTL and 3.3-V LVCMOS I/O standard.

Cyclone III devices can interface to 3.3 V systems using 3.3 V and 3.0 V I/O standards by following a few simple guidelines. For more information, refer to *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

Slew Rate Control

The output buffer for each Cyclone III device I/O pin provides optional programmable output slew-rate, with three settings for each supported I/O standard: slow, medium, and fast. The default slew rate is the fastest setting. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Since each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength 8 mA or higher. 3.3-V LVTTL and 3.3-V LVCMOS I/O standards do not support slew rate control.

For more information, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Open-Drain Output

Cyclone III devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write-enable signals) that can be asserted by multiple devices in your system.

For more information, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Bus Hold

Each Cyclone III device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on the dedicated clock pins.

The bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

For more information, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

For the specific sustaining current for each V_{CCIO} voltage level driven through the resistor and for the overdrive current used to identify the next driven input level, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Programmable Pull-Up Resistor

Each Cyclone III device I/O pin provides an optional programmable pull-up resistor while in user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

If you enable the programmable pull-up, the device cannot use the bus-hold feature. The programmable pull-up resistors are not supported on the dedicated configuration, Joint Test Action Group (JTAG), and dedicated clock pins.

For more information, refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

Programmable Delay

The Cyclone III device IOE includes programmable delays to ensure zero hold times, minimize setup times, or increase clock-to-output times.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays minimize setup time. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Table 7–2 shows the programmable delays for Cyclone III devices.

Table 7–2. Cyclone III Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Input delay from pin to internal cells
Input pin to input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to the internal LE registers that reside in two different areas of the device. You set the two combinational input delays by using the **Input delay from pin to internal cells** logic option in the Quartus II software for each path. If the pin uses the input register, one of delays is disregarded and the delay is set by using the **Input delay from pin to input register** logic option in the Quartus II software.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power up. If one register in an IOE uses a preset or clear signal, then all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

For more information about how to set the input and output pin delay, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

PCI-Clamp Diode

Cyclone III devices provide an optional PCI-clamp diode enabled input and output for each I/O pin. The PCI-clamp diode is available for 3.3-V LVTTL, 3.3-V LVCMOS, 3.0-V LVTTL, 3.0-V LVCMOS, PCI, and PCI-X I/O standards. If the input I/O standard is 3.3-V LVTTL, 3.3-V LVCMOS, 3.0-V LVTTL, 3.3-V LVCMOS, PCI, or PCI-X, the PCI clamp diod is enabled by default in Quartus II.

For more information refer to the *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*.

For more information about Cyclone III PCI-clamp diode support, refer to *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

LVDS Transmitter Programmable Pre-Emphasis

The Cyclone III dedicated LVDS transmitter supports programmable pre-emphasis. Programmable pre-emphasis is used to compensate the frequency-dependent attenuation of the transmission line. It increases the amplitude of the high-frequency components of the output signal, which cancels out much of the high-frequency loss of the transmission line.

Programmable pre-emphasis supports on and off settings. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You need to adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal as well.

For more information about Cyclone III high-speed differential interface support, refer to *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

On-Chip Termination Support

Cyclone III devices feature OCT to provide I/O impedance matching and termination capabilities. OCT helps to prevent reflections and maintain signal integrity while minimizing the need for external resistors in high pin-count ball grid array (BGA) packages. Cyclone III devices provide I/O driver on-chip impedance matching and on-chip series termination for single-ended outputs and bidirectional pins.

When using on-chip series termination, programmable current strength is not available.

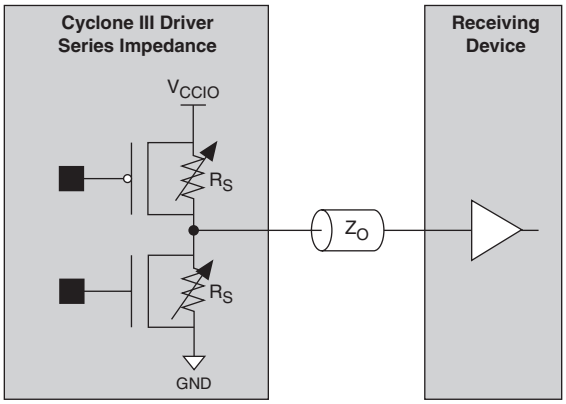
There are two ways to implement OCT in Cyclone III devices:

- OCT with calibration
- OCT without calibration

On-Chip Termination with Calibration

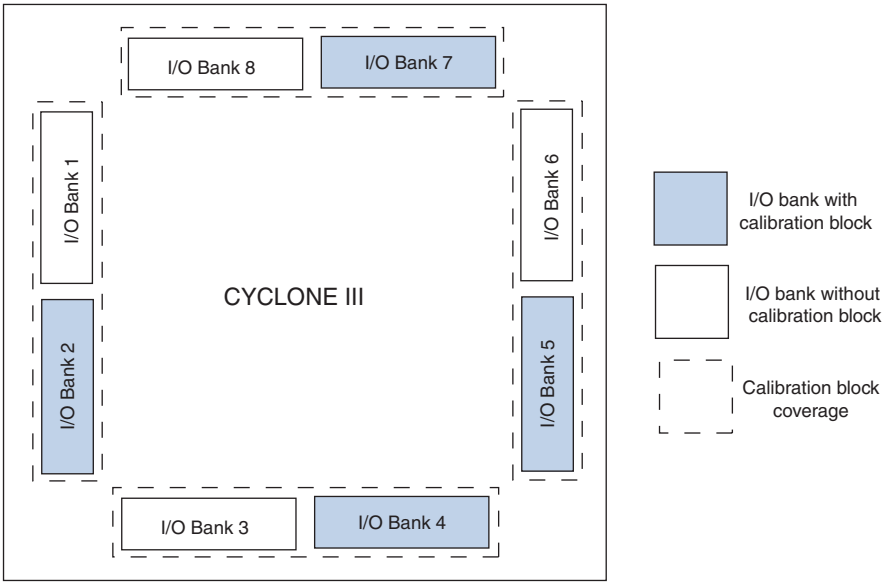
Cyclone III devices support on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the I/O buffer to the external 25 Ω ±1% or 50 Ω ±1% resistors connected to the R_{UP} and R_{DN} pins, and dynamically adjusts the I/O buffer impedance until they match (as shown in Figure 7–7). The RS shown in Figure 7–7 is the intrinsic impedance of the transistors that make up the I/O buffer.

Figure 7–7. Cyclone III On-Chip Series Termination with Calibration



OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in bank 2, 4, 5, and 7. Each calibration block supports each side of the I/O banks. Since there are two I/O banks sharing the same calibration block, both banks must have the same V_{CCIO} if both banks enable OCT calibration. If two related banks have different V_{CCIOs}, only the bank where the calibration block resides can enable the OCT calibration. Figure 7–8 shows the top-level view of the OCT calibration blocks placement.

Figure 7–8. Cyclone III OCT Block Placement



Each calibration block comes with a pair of R_{UP} and R_{DN} pins. When you use OCT with calibration, these two pins need to be connected with external resistors of 25 Ω ±1% or 50 Ω ±1%. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust the buffer impendance. When OCT calibration is not used, R_{UP} and R_{DN} pins can be used as regular I/Os.

Table 7–3 lists the I/O standards that support impedance matching and series termination.

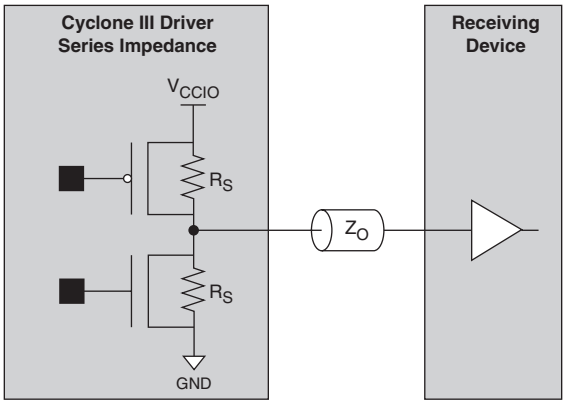
Table 7–3. Selectable I/O Drivers for On-Chip Termination without Calibration

I/O Standard	On–Chip Series Termination without Calibration Setting, in ohms (Ω)	
	Row I/O	Column I/O
3.0-V LVTTL	50	50
	25	25
3.0-V LVCMOS	50	50
	25	25
2.5-V LVTTL/ LVCMOS	50	50
	25	25
1.8-V LVTTL/LVCMOS	50	50
	25	25
1.5-V LVCMOS	50	50
	25	25
1.2-V LVCMOS	50	50
	—	25
SSTL-2 Class I	50	50
SSTL-2 Class II	25	25
SSTL-18 Class I	50	50
SSTL-18 Class II	25	25
HSTL-18 Class I	50	50
HSTL-18 Class II	25	25
HSTL-15 Class I	50	50
HSTL-15 Class II	25	25
HSTL-12 Class I	50	50
HSTL-12 Class II	—	25

On-Chip Termination without Calibration

Cyclone III devices support driver impedance matching to the impedance of the transmission line, typically 25 or 50 Ω . When used with the output drivers, on-chip termination sets the output driver impedance to 25 or 50 Ω . Cyclone III devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18. Figure shows the single-ended I/O standards for on-chip termination without calibration. The R_S shown is the intrinsic transistor impedance.

Figure 7–9. Cyclone III On-Chip Series Termination without Calibration



All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination. Table 7–4 lists the I/O standards that support impedance matching the series termination.

Table 7–4. Selectable I/O Drivers for On-Chip Termination without Calibration

I/O Standard	On Chip Series Termination without Calibration Setting, in Watts (W)	
	Row I/O	Column I/O
3.0-V LVTTL	50	50
	25	25
3.0-V LVCMOS	50	50
	25	25
2.5-V LVTTL/LVCMOS	50	50
	25	25
1.8-V LVTTL/LVCMOS	50	50
	25	25
1.5-V LVCMOS	50	50
	25	25
1.2-V LVCMOS	50	50
	—	25
SSTL-2 Class I	50	50
SSTL-2 Class II	25	25
SSTL-18 Class I	50	50
SSTL-18 Class II	25	25
HSTL-18 Class I	50	50
HSTL-18 Class II	25	25
HSTL-15 Class I	50	50
HSTL-15 Class II	25	25
HSTL-12 Class I	50	50
HSTL-12 Class II	—	25

On-chip series termination is supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins to enable on-chip series termination in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} are not conflicting.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage, and temperature.

For more information about tolerance specification refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

I/O Standards

Cyclone III devices support multiple single-ended and differential I/O standards. Apart from 3.3, 3.0, 2.5, 1.8, and 1.5 V support, Cyclone III devices also support 1.2 V I/O standards. Table 7–5 summarizes the I/O standards supported by Cyclone III devices and which I/O pins support them.

Table 7–5. Cyclone III Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Top and Bottom I/O Pins			Side I/O Pins	
			Input	Output	CLK, DQS	PLL_ OUT	User I/O Pins	CLK, DQS	User I/O Pins
3.3-V LVTTL *(1)*	Single-ended	JESD8-B	3.3 3.0 2.5	3.3	✓	✓	✓	✓	✓
3.3-V LVCMOS *(1)*	Single-ended	JESD8-B	3.3 3.0 2.5	3.3	✓	✓	✓	✓	✓
3.0-V LVTTL *(1)*	Single-ended	JESD8-B	3.3 3.0 2.5	3.0	✓	✓	✓	✓	✓
3.0-V LVCMOS *(1)*	Single-ended	JESD8-B	3.3 3.0 2.5	3.0	✓	✓	✓	✓	✓
2.5-V LVTTL / LVCMOS	Single-ended	JESD8-5	3.3 3.0 2.5	2.5	✓	✓	✓	✓	✓
1.8-V LVTTL / LVCMOS	Single-ended	JESD8-7	1.8 1.5	1.8	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single-ended	JESD8-11	1.8 1.5	1.5	✓	✓	✓	✓	✓
1.2-V LVCMOS	Single-ended	JESD8-12A	1.2	1.2	✓	✓	✓	✓	✓
SSTL-2 Class I	Voltage referenced	JESD8-9A	2.5	2.5	✓	✓	✓	✓	✓
SSTL-2 Class II	Voltage referenced	JESD8-9A	2.5	2.5	✓	✓	✓	✓	✓
SSTL-18 Class I	Voltage referenced	JESD815	1.8	1.8	✓	✓	✓	✓	✓
SSTL-18 Class II	Voltage referenced	JESD815	1.8	1.8	✓	✓	✓	✓	✓
HSTL-18 class I	Voltage referenced	JESD8-6	1.8	1.8	✓	✓	✓	✓	✓
HSTL-18 class II	Voltage referenced	JESD8-6	1.8	1.8	✓	✓	✓	✓	✓
HSTL-15 Class I	Voltage referenced	JESD8-6	1.5	1.5	✓	✓	✓	✓	✓

Table 7–5. Cyclone III Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Top and Bottom I/O Pins			Side I/O Pins	
			Input	Output	CLK, DQS	PLL_ OUT	User I/O Pins	CLK, DQS	User I/O Pins
HSTL-15 Class II	Voltage referenced	JESD8-6	1.5	1.5	✓	✓	✓	✓	✓
HSTL-12 Class I	Voltage referenced	JESD8-16a	1.2	1.2	✓	✓	✓	✓	✓
HSTL-12 Class II	Voltage referenced	JESD8-16a	1.2	1.2	✓	✓	✓	—	—
PCI and PCI-X	Single ended	—	3.0	3.0	✓	✓	✓	✓	✓
Differential SSTL-2 Class I or Class II	Differential *(2)*	JESD8-9A	—	2.5	—	✓	—	—	—
			2.5	—	✓	—	—	✓	—
Differential SSTL-18 Class I or Class II	Differential *(2)*	JESD815	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-18 Class I or Class II	Differential *(2)*	JESD8-6	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-15 Class I or Class II	Differential *(2)*	JESD8-6	—	1.5	—	✓	—	—	—
			1.5	—	✓	—	—	✓	—
Differential HSTL-12 Class I or Class II	Differential *(2)*	JESD8-16A	—	1.2	—	✓	—	—	—
			1.2	—	✓	—	—	✓	—
PPDS® *(3) (5)*	Differential	—	—	2.5	—	✓	✓	—	✓
LVDS	Differential	—	2.5	2.5	✓	✓	✓	✓	✓
RSDS® and mini-LVDS *(3) (5)*	Differential	—	—	2.5	—	✓	✓	—	✓
LVPECL *(4)*	Differential	—	2.5	—	✓	—	—	✓	—

Notes to Table 7–5:

(1) The PCI-clamp diode needs to be enabled for 3.3-V/3.0-V LVTTL/LVCMOS.

(2) Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them. Differential HSTL and SSTL only supported on `CLK` pins.

(3) PPDS, mini-LVDS, and RSDS are only supported on output pins.

(4) LVPECL is only supported on clock inputs.

(5) RSDS and PPDS are registered trademarks of National Semiconductor.

Termination Scheme for I/O Standards

This section describes the recommended termination schemes for voltage-referenced and differential I/O standards.

The following I/O standards do not specify a recommended termination scheme per the JEDEC standard:

- 3.3-V LVTTL
- 3.0-V LVTTL and LVCMOS
- 2.5-V LVTTL and LVCMOS
- 1.8-V LVTTL and LVCMOS
- 1.5-V LVCMOS
- 1.2-V LVCMOS
- 3.0-V PCI and PCI-X

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require both an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figures 7–10 and 7–11.

Figure 7–10. Cyclone III HSTL I/O Standard Termination

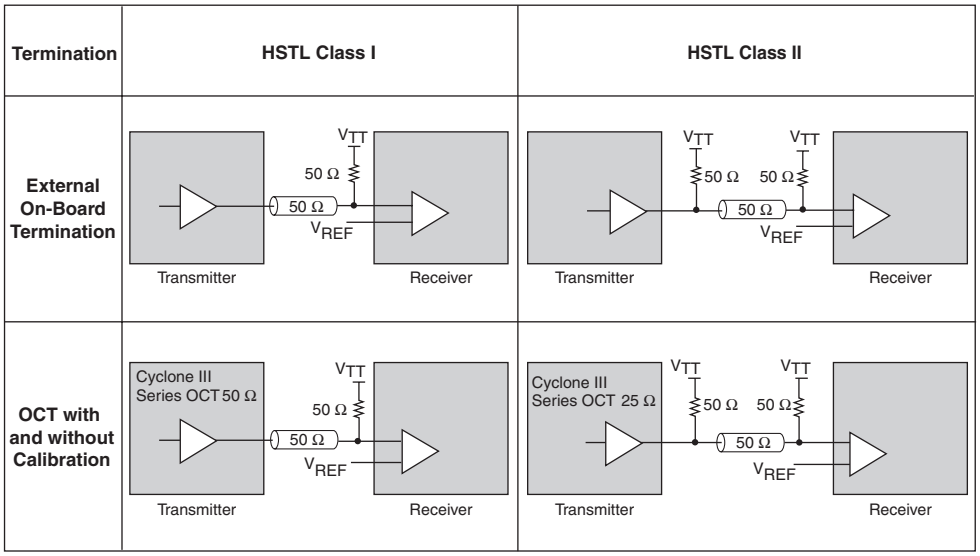
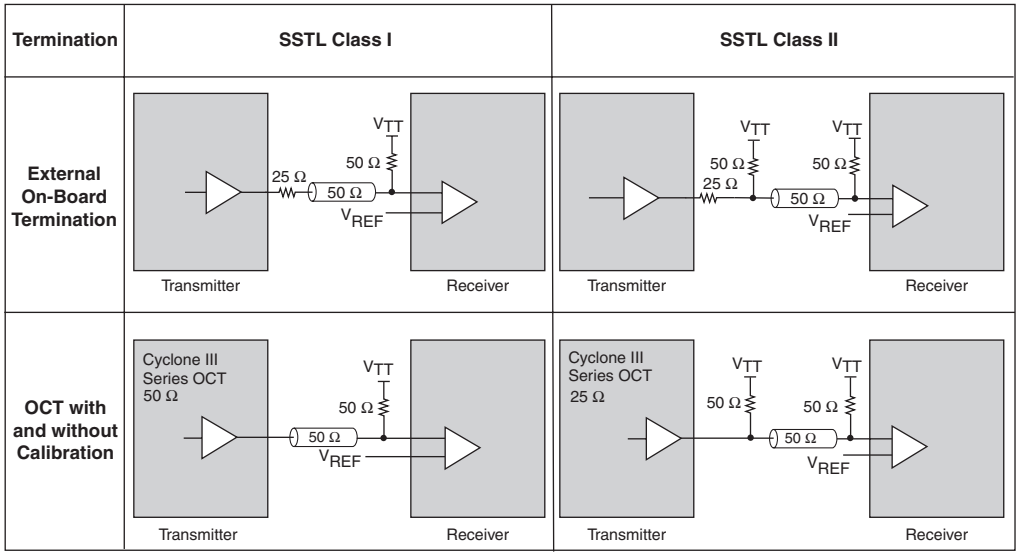


Figure 7–11. Cyclone III SSTL I/O Standard Termination



Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus (refer to Figures 7–12 and 7–13).

Cyclone III devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12, PPDS, LVDS, RSDS, mini-LVDS, and differential LVPECL.

Figure 7–12. Cyclone III Differential HSTL I/O Standard Termination

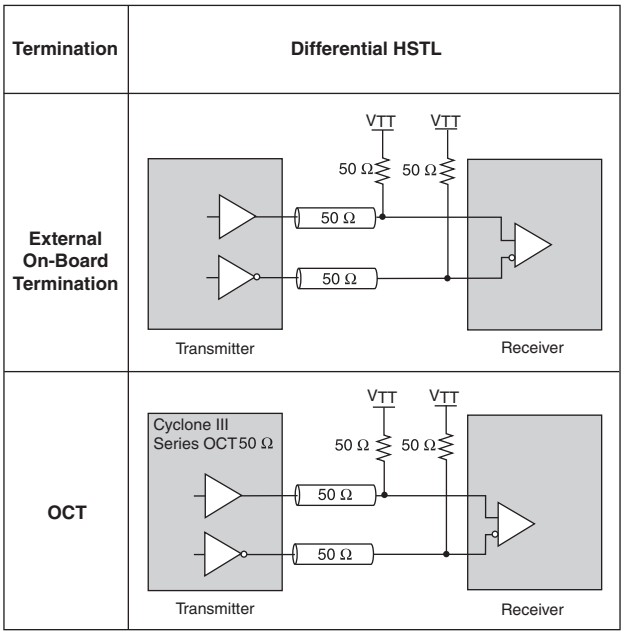
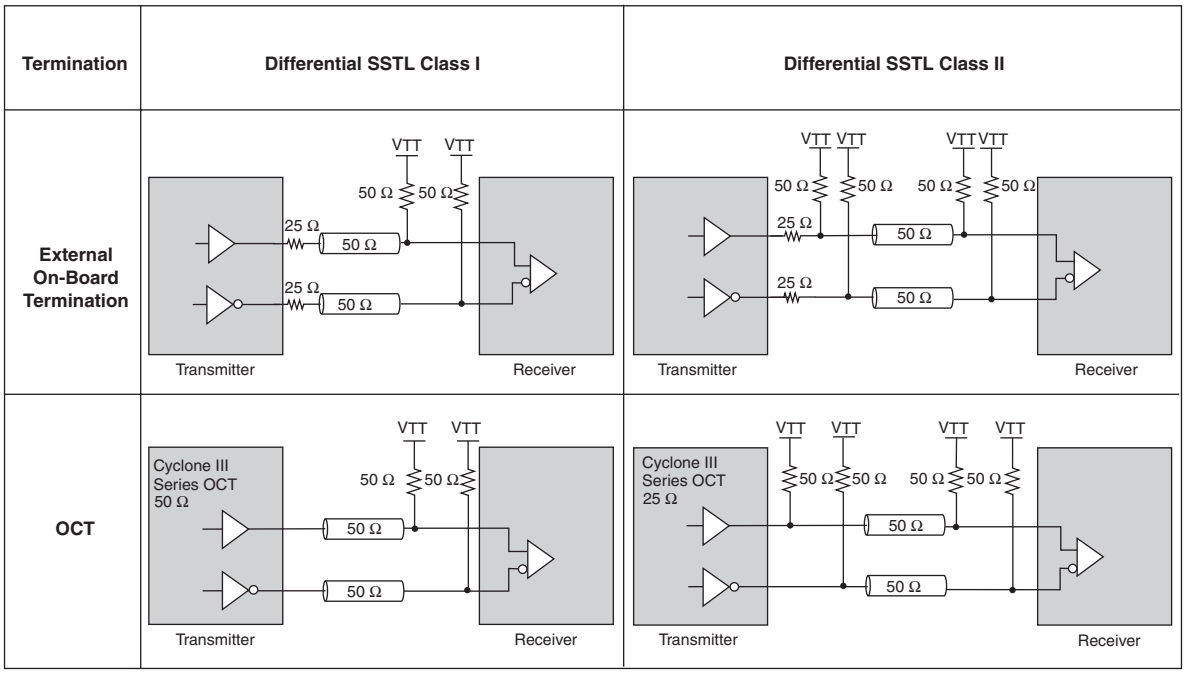


Figure 7–13. Cyclone III Differential SSTL I/O Standard Termination



Note to Figure 7–13:

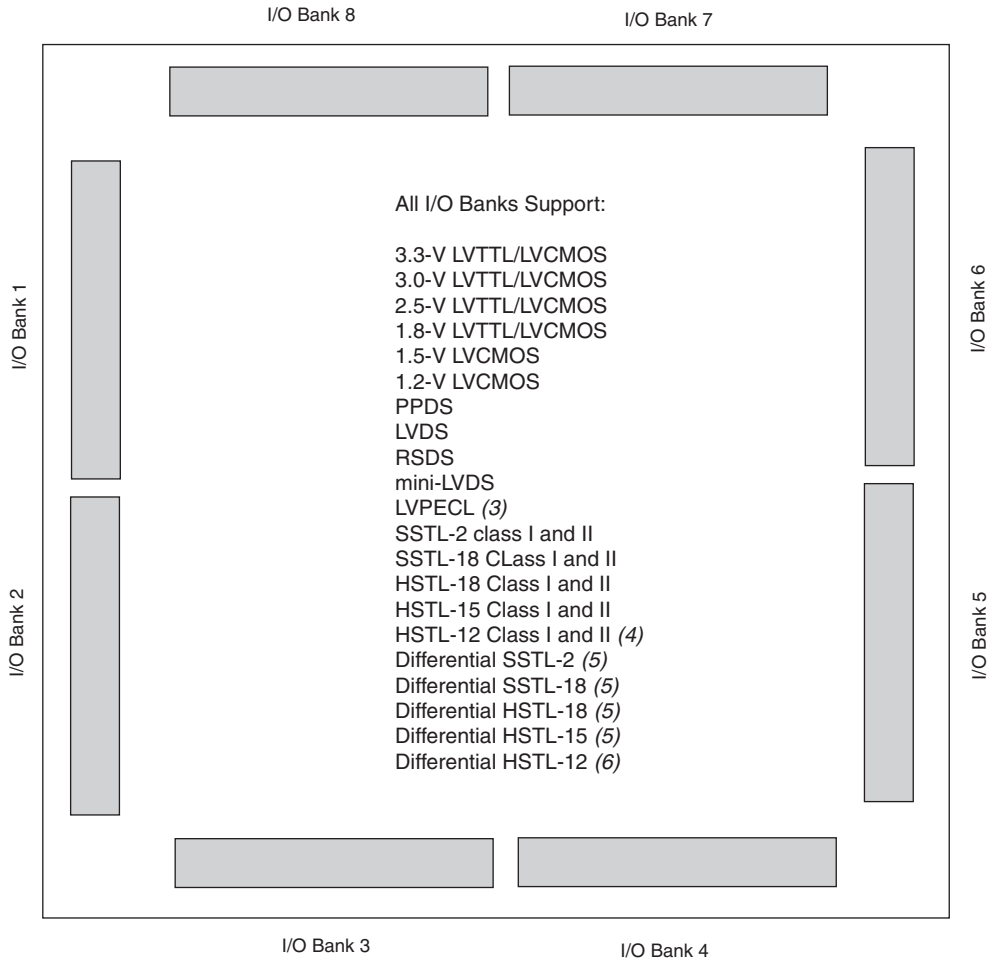
(1) Only Differential SSTL-2 I/O standard supports Class II output.

For information about Cyclone III differential PPDS, LVDS, mini LVDS, and RSDS I/O standard termination, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*.

I/O Banks

The I/O pins on Cyclone III devices are grouped together into I/O banks, and each bank has a separate power bus. All Cyclone III devices have eight I/O banks, as shown in Figure 7–14. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported in all banks except HSTL-12 class II, which is only supported in column I/O banks. All differential I/O standards are supported in all banks. The only exception is HSTL-12 class II, which is only supported in column I/O banks.

Figure 7–14. Cyclone III Device I/O Banks Notes (1), (2)



Notes to Figure 7–14:

(1) This is a top view of the silicon die. This is a graphic representation only. Refer to the pin list and the Quartus II software for exact pin locations.

(2) Dedicated PPDS, LVDS, mini-LVDS, and RSDS I/O standards are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.

(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are only supported on clock input pins and PLL output clock pins. Differential SSTL-18, differential HSTL-18 and HSTL-15 I/O standards do not support Class II output.

(6) The differential HSTL-12 I/O standards is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 class II is only supported in column I/O banks 3, 4, 7 and 8 only.

Table 7–6 shows I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of Cyclone III devices.

Table 7–6. Cyclone III I/O Standards Support (Part 1 of 2)

I/O Standard	I/O Banks							
	1	2	3	4	5	6	7	8
3.3-V LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓
3.3-V LVTTL	✓	✓	✓	✓	✓	✓	✓	✓
3.0-V LVTTL	✓	✓	✓	✓	✓	✓	✓	✓
3.0-V LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓

Table 7–6. Cyclone III I/O Standards Support (Part 2 of 2)

I/O Standard	I/O Banks							
	1	2	3	4	5	6	7	8
2.5-V LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓
1.8-V LVTTL/LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓
1.5-V LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓
1.2-V LVCMOS	✓	✓	✓	✓	✓	✓	✓	✓
3.0-V PCI / PCI-X	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class II	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class I	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-2 Class II	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class II	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-18 Class I	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-18 Class II	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-15 Class I	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-15 Class II	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-12 Class I	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-12 Class II	—	—	✓	✓	—	—	✓	✓
Differential SSTL-2	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
Differential SSTL-18	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
Differential HSTL-18	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
Differential HSTL-15	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
Differential HSTL-12	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
PPDS *(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
LVDS *(2)*	✓	✓	✓	✓	✓	✓	✓	✓
RSDS and mini-LVDS	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
Differential LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*

Notes to Table 7–6:

(1) These differential I/O standards are only supported for clock inputs and dedicated `PLL_OUT` outputs.

(2) Dedicated LVDS I/O standard is supported in row I/O banks only. LVDS I/O standard in column I/O banks require external resistors network.

(3) This I/O standard is supported for outputs only.

(4) This I/O standard is supported for clock inputs only.

Each Cyclone III I/O bank has a V_{REF} bus to accommodate voltage-referenced I/O standards. When using V_{REF} pins, you must properly connect each V_{REF} pin to the appropriate voltage level. In the event that you do not use these pins as V_{REF} pins, you may use them as regular I/O pins. However, they will have slightly higher pin capacitance than regular user I/O pins when used with regular user I/O pins. Table 7–7 summarizes the number of V_{REF} pins in each I/O bank.

Table 7–7. Number of V_{REF} Pins Per I/O Banks

Device	Package	Pin Count	I/O Banks							
			1	2	3	4	5	6	7	8
EP3C5	EQFP	144	1	1	1	1	1	1	1	1
	FBGA	256	1	1	1	1	1	1	1	1
EP3C10	EQFP	144	1	1	1	1	1	1	1	1
	FBGA	256	1	1	1	1	1	1	1	1
EP3C16	EQFP	144	2	2	2	2	2	2	2	2
	PQFP	240	2	2	2	2	2	2	2	2
	FBGA	256	2	2	2	2	2	2	2	2
	FBGA	484	2	2	2	2	2	2	2	2
EP3C25	EQFP	144	1	1	1	1	1	1	1	1
	PQFP	240	1	1	1	1	1	1	1	1
	FBGA	256	1	1	1	1	1	1	1	1
	FBGA	324	1	1	1	1	1	1	1	1
EP3C40	PQFP	240	4	4	4	4	4	4	4	4
	FBGA	324	4	4	4	4	4	4	4	4
	FBGA	484	4	4	4	4	4	4	4	4
	FBGA	780	4	4	4	4	4	4	4	4
EP3C55	FBGA	484	2	2	2	2	2	2	2	2
	FBGA	780	2	2	2	2	2	2	2	2
EP3C80	FBGA	484	3	3	3	3	3	3	3	3
	FBGA	780	3	3	3	3	3	3	3	3
EP3C120	FBGA	484	3	3	3	3	3	3	3	3
	FBGA	780	3	3	3	3	3	3	3	3

Each Cyclone III I/O bank has its own V_{CCIO} pins. Any single I/O bank can only support one V_{CCIO} setting from among 1.2, 1.5, 1.8, 2.5, 3.0, or 3.3 V. Although there can only be one V_{CCIO} voltage per I/O bank, Cyclone III devices permit additional input signaling capabilities.

Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank, as long as they use compatible V_{CCIO} levels for input and output pins. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V LVTTL inputs and outputs, 2.5-V LVDS-compatible inputs and outputs, and 3.0-V LVTTL and 3.3-V LVCMOS inputs only.

Voltage-referenced standards can be supported in an I/O bank using any number of single-ended or differential standards, as long as they use the same V_{REF} and a compatible V_{CCIO} value. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone III device, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

Table 7–8 shows the acceptable input and output levels with corresponding bank voltage.

Table 7–8. Acceptable Input and Output Levels

Bank V_{CCIO} (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.0 V	3.3 V	1.2 V	1.5 V	1.8 V	2.5 V	3.0 V	3.3 V
1.2 V	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5 V	—	✓	✓ (1)	—	—	—	—	✓	—	—	—	—
1.8 V	—	✓(2)	✓	—	—	—	—	—	✓	—	—	—
2.5 V	—	—	—	✓	✓ (3)	✓ (3)	—	—	—	✓	—	—
3.0 V	—	—	—	✓ (2)	✓ (3)	✓ (3)	—	—	—	—	✓	—
3.3 V	—	—	—	✓ (2)	✓ (3)	✓ (3)	—	—	—	—	—	✓

Notes to Table 7–8:

(1) These input values overdrive the input buffer, so the pin leakage current is slightly higher than the default value.

(2) Because the input level does not drive to the rail, the input buffer does not completely shut off. The I/O current is slightly higher than the default value.

(3) The PCI clamping diode is enabled by default in the Quartus II software for input signals with V_{CCIO} at 2.5 V, 3.0 V, or 3.3 V. The designer is responsible for managing overshoot/undershoot to stay within the absolute maximum ratings and recommended operating conditions provided in the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

For more information about Cyclone III I/O interface support, refer to *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

High-Speed Differential Interfaces

Cyclone III devices can transmit and receive data through LVDS signals. For the LVDS transmitter and receiver, the Cyclone III device's input and output pins support serialization and de-serialization through internal logic.

The reduced swing differential signaling (RSDS) and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The point-to-point differential signalling (PPDS) standard is the next generation of RSDS standard introduced by National Semiconductor Corporation. Cyclone III devices meet the National Semiconductor Corporation PPDS Interface Specification and support the PPDS standard for outputs only. All of the I/O banks of Cyclone III devices support the PPDS standard for output pins only.

You can use I/O pins and internal logic to implement the LVDS I/O receiver and transmitter in Cyclone III devices. Cyclone III devices do not contain dedicated serialization or de-serialization circuitry. Therefore, shift registers, internal PLLs, and IOEs are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

The LVDS standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for top and bottom I/O banks.

For more information about Cyclone III high-speed differential interface support, refer to the *High-Speed Differential Interfaces in Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

External Memory Interfacing

Cyclone III devices support I/O standards required to interface with a broad range of external memory interfaces such as DDR SDRAM, DDR2 SDRAM, and QDRII SRAM.

For more information about Cyclone III external memory interface support, refer to the *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook.*

Pad Placement and DC Guidelines

This section provides pad placement guidelines for the programmable I/O standards supported by Cyclone III devices and includes essential information for designing systems using the devices' selectable I/O capabilities. This section also discusses DC limitations and guidelines.

The Quartus II software provides user-controlled restriction relaxation options for some placement constraints. When you relax a default restriction, the Quartus II Fitter generates warnings.

For more information about how Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in the *Quartus II Handbook*.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, there are restrictions on placement of single-ended I/O pads in relation to differential pads. Follow the guidelines to place single-ended pads with respect to differential pads and to place differential output pads in Cyclone III devices.

For the LVDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVDS I/O pad.
- Single-ended outputs can be no closer than five pads away from an LVDS I/O pad.
- Use a maximum of four 160-MHz LVDS output channels per V_{CCIO} and ground pair in column I/O banks.
- Use a maximum of three 320-MHz LVDS output channels per V_{CCIO} and ground pair in column I/O banks.
- Use a maximum of four 210-MHz LVDS output channels per V_{CCIO} and ground pair in row I/O banks.
- Use a maximum of three 420-MHz LVDS output channels per V_{CCIO} and ground pair in row I/O banks.

The Quartus II software only checks the first two cases.

For the RSDS and mini-LVDS I/O standards:

- Single-ended inputs can be no closer than four pads away from an RSDS and mini-LVDS output pad.
- Single-ended outputs can be no closer than five pads away from an RSDS and mini-LVDS output pad.
- Use a maximum of three 85-MHz RSDS and mini-LVDS output channels per V_{CCIO} and ground pair in column I/O banks.
- Use a maximum of three 180-MHz RSDS output channels per V_{CCIO} and ground pair in row I/O banks.
- Use a maximum of three 220-MHz mini-LVDS output channels per V_{CCIO} and ground pair in row I/O banks.

The Quartus II software only checks the first two cases.

For the PPDS I/O standard:

- Single-ended inputs can be no closer than four pads away from an PPDS output pad.
- Single-ended outputs can be no closer than five pads away from an PPDS output pad.

- Use a maximum of three 85-MHz PPDS output channels per V_{CCIO} and ground pair in column I/O banks.
- Use a maximum of three 220-MHz PPDS output channels per V_{CCIO} and ground pair in row I/O banks.

The Quartus II software only checks the first two cases.

For the LVPECL I/O standard:

- Single-ended inputs can be no closer than four pads away from an LVPECL input pad.
- Single-ended outputs can be no closer than five pads away from an LVPECL input pad.

V_{REF} Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply and to prevent output switching noise from shifting the V_{REF} rail, there are restrictions on the placement of single-ended voltage referenced I/Os with respect to V_{REF} pads and V_{CCIO} and ground pairs. Use the following guidelines for placing single-ended pads in Cyclone III devices.

The Quartus II software performs all of the calculations listed in this section automatically.

Input Pads

Each V_{REF} pad supports up to 32 input pads for FineLine BGA devices. Each V_{REF} pad supports up to 21 input pads for quad flat pack (QFP) devices. This is irrespective of V_{CCIO} and ground pairs and is guaranteed by the Cyclone III architecture.

Output Pads

When no voltage referenced input or bidirectional pads exist in a bank, there is no limit to the number of output pads that can be implemented in that bank. When a voltage referenced input exists, each V_{CCIO} and ground pair supports nine outputs for Fineline BGA packages or five outputs for QFP packages. Any non-SSTL and non-HSTL output can be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels. Altera recommends that any SSTL or HSTL output, except for pintable defined DQ and DQS outputs (when used for DDR/DDR2/QDRII applications), to be no closer than two pads away from a V_{REF} pad to maintain acceptable noise levels. Refer to "DDR/DDR2 and QDRII Pads" on page 7–27 for details about guidelines for DQ and DQS pad placement.

Bidirectional Pads

Bidirectional pads must satisfy input and output guidelines simultaneously. Refer to "DDR/DDR2 and QDRII Pads" on page 7–27 for details about guidelines for DQ and DQS pad placement.

If the bidirectional pads are all controlled by the same output enable (OE) and there are no other outputs or voltage referenced inputs in the bank, there would be no case where a voltage referenced input is active at the same time as an output. Therefore, the output limitation does not apply. However, because the bidirectional pads are linked to the same OE, all the bidirectional pads act as inputs at the same time. Therefore, the input limitation of 32 input pads (per V_{REF} pad) for FineLine BGA packages and 21 input pads (per V_{REF} pad) for QFP packages applies.

If the bidirectional pads are all controlled by different OEs, and there are no other outputs or voltage referenced inputs in the bank, there may be a case where one group of bidirectional pads is acting as inputs while another group is acting as outputs. In such cases, apply the formulas shown in Table 7–9.

Table 7–9. Input-Only Bidirectional Pad Limitation Formulas

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 9 (per V_{CCIO} and ground pair)
QFP	(Total number of bidirectional pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 5 (per V_{CCIO} and ground pair)

When at least one additional voltage referenced input and no other outputs exist in the same V_{REF} bank, the bidirectional pad limitation applies in addition to the input and output limitations. Refer to equations 1 and 2:

(1) $$\text{Total number of bidirectional pads} + \text{total number of input pads} \leq 32 \quad \text{for Fineline BGA packages}$$

(2) $$\text{Total number of bidirectional pads} + \text{total number of input pads} \leq 21 \quad \text{for QFP packages}$$

After applying equation 1 or 2, apply one of the equations in Table 7–10, depending on the package type.

Table 7–10. Bidirectional Pad Limitation Formulas (Where V_{REF} Inputs Exist)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) ≤ 9 (per VCCIO and ground pair)
QFP	(Total number of bidirectional pads) ≤ 5 (per VCCIO and ground pair)

When at least one additional output exists but no voltage referenced inputs exist, apply the appropriate formula from Table 7–11 for more details.

Table 7–11. Bidirectional Pad Limitation Formulas (Where V_{REF} Outputs Exist)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 9 (per V_{CCIO} and ground pair)
QFP	(Total number of bidirectional pads) + (Total number of additional output pads) – (Total number of pads from the smallest group of pads controlled by an OE) ≤ 5 (per V_{CCIO} and ground pair)

When additional voltage referenced inputs and other outputs exist in the same V_{REF} bank, the bidirectional pad limitation must again simultaneously adhere to the input and output limitations. As such, the following rules apply:

(3) $$\text{Total number of bidirectional pads} + \text{total number of input pads} \leq 32 \quad \text{for Fineline BGA packages}$$

(4) $$\text{Total number of bidirectional pads} + \text{total number of input pads} \leq 21 \quad \text{for QFP packages}$$

After applying equation 3 or 4, apply one of the equations in Table 7–12, depending on the package type.

Table 7–12. Bidirectional Pad Limitation Formulas (Multiple V_{REF} Inputs and Outputs)

Package Type	Formula
FineLine BGA	(Total number of bidirectional pads) + (Total number of output pads) ≤ 9 (per V_{CCIO}/GND pair)
QFP	Total number of bidirectional pads + Total number of output pads ≤ 5 (per V_{CCIO}/GND pair)

Each I/O bank can only be set to a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time. Pins of different I/O standards can share the bank if they have compatible V_{CCIO} values and compatible V_{REF} voltage levels (refer to Table 7–7 on page 7–22 for more details).

DDR/DDR2 and QDRII Pads

For dedicated DQ and DQS pads on a DDR interface, DQ pads must be on the same I/O bank as DQS pads. With the DDR and DDR2 memory interfaces, a V_{CCIO} and ground pair can have a maximum of five DQ pads. No other I/O can be placed within the same power pair where DQ pins are located, except DDR/DDR2 usage pins.

For a QDRII interface, D is the QDRII output and Q is the QDRII input. D pads and Q pads must be on the same I/O bank as CQ. With the QDR and QDRII memory interfaces, a V_{CCIO} and ground pair can have a maximum of five D and Q pads. No other I/O can be placed within the same power pair where D or Q pins located. Furthermore, the D, cmd, and address pads cannot be placed at the same V_{REF} bank where Q pads are located.

By default, the Quartus II software assigns D and Q pads as regular I/O pins. If you do not specify the function of a D or Q pad in the Quartus II software, the software sets them as regular I/O pins. If this occurs, Cyclone III QDR and QDRII performance is not guaranteed.

DC Guidelines

There is a current limit of 240 mA per twelve consecutive output top and bottom pins per power pair, as shown by equation 5:

$$\sum_{pin}^{pin+11} I_{PIN} < 240 \text{ mA per power pair} \quad (5)$$

There is a current limit of 240 mA per 14 consecutive output side pins (left and right) per power pair, as shown by equation 6:

$$\sum_{pin}^{pin+13} I_{PIN} < 240 \text{ mA per power pair} \quad (6)$$

In all the cases listed above, the Quartus II software generates an error message for illegally placed pads. The I_{PIN} varies with programmable current strength and is the same as the current strength as set in the Quartus II software.

For more information about Cyclone III FPGAs power estimation, refer to the *PowerPlay III Early Power Estimator User Guide for Cyclone III FPGAs*.

Conclusion

Cyclone III device I/O capabilities enable you to keep pace with increasing design complexity utilizing a low-cost FPGA device family. Support for various I/O standard compatibility allow Cyclone III devices to fit into a wide variety of applications. Quartus II software makes it easy to use these I/O standards in Cyclone III device designs.

After design compilation, the software also provides clear, visual representations of pads and pins and the selected I/O standards. Taking advantage of the support of these I/O standards in Cyclone III devices allows you to lower your design costs without compromising design flexibility or complexity.

Referenced Documents

This chapter references the following documents:

- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Assignment Editor* chapter in volume 2 of the *Quartus II Handbook*
- *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*
- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *External Memory Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*
- *I/O Management* chapter in volume 2 of the *Quartus II Handbook*
- *PowerPlay III Early Power Estimator User Guide for Cyclone III FPGAs*

Document Revision History

Table 7–13 shows the revision history for this document.

Table 7–13. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated feetpara note in "Programmable Current Strength" section. • Updated feetpara note in "Slew Rate Control" section. • Updated feetpara note in "Open-Drain Output" section. • Updated feetpara note in "Bus Hold" section. • Updated feetpara note in "Programmable Pull-Up Resistor" section. • Updated feetpara note in "PCI-Clamp Diode" section. • Updated Figure 7–12. • Updated Figure 7–13 and added *Note (1)*. • Updated "I/O Banks" section. • Updated *Note (5)* to Figure 7–14. • Updated "DDR/DDR2 and QDRII Pads" section and corrected 'cms' to 'cmd'. • Updated *Note (3)* in Table 7–8. • Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release.	N/A

8. High-Speed Differential Interfaces in Cyclone III Devices

CIII51008-1.1

Introduction

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. In response to the current market need, Altera® Cyclone® III devices support various differential I/O standards, including low-voltage differential signaling (LVDS), reduced swing differential signaling (RSDS®), mini-LVDS, and point-to-point differential signaling (PPDS®).

RSDS and PPDS are registered trademarks of National Semiconductor.

LVDS is the technology of choice from high-speed backplane applications to high-end switch boxes. LVDS is a low-voltage differential signaling standard, providing higher noise immunity than single-ended I/O technologies. Its low-voltage swing allows for high-speed data transfers, low power consumption, and reduced electromagnetic interference (EMI). LVDS I/O signaling is a data interface standard defined in the TIA/EIA-644 and IEEE Std. 1596.3 specifications.

Cyclone III devices can receive LVDS signals at 875 megabits per second (Mbps) on all I/O banks. Cyclone III devices include dedicated differential output buffers to transmit LVDS signals at up to 840 Mbps on the left and right I/O banks, with no external resistors required. The top and bottom I/O banks can transmit data at up to 640 Mbps using a simple resistor network.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. Because the RSDS and mini-LVDS I/O standards have smaller voltage swing than LVDS does, they provide increased power benefits and reduced EMI. National Semiconductor Corporation and Texas Instruments introduced the RSDS and mini-LVDS specifications, respectively. Currently, many designers use these specifications for flat panel display links between the controller and the display column drivers. Cyclone III devices support the RSDS and mini-LVDS I/O standards at speeds up to 360 Mbps and 400 Mbps, respectively, at the dedicated transmitter located on the left and right I/O banks, with no external resistors required.

The PPDS standard is the next generation of the RSDS standard introduced by National Semiconductor Corporation. PPDS technology was introduced to address the requirements for LCD television interfaces to improve display performance. PPDS applications include multi-function LCD monitor and high-performance professional LCD monitor. Cyclone III devices support the PPDS I/O standards at speed up to 440 Mbps with no external resistors required at the dedicated transmitter located on the left and right I/O banks.

The differential interface data serializers and deserializers (SERDES) are constructed automatically in Cyclone III logic elements with Quartus® II software altlvds megafunction.

This chapter describes how to use Cyclone III I/O pins for differential signaling and contains the following sections:

- "Cyclone III High-Speed I/O Banks" on page 8–2
- "Cyclone III High-Speed I/O Interface" on page 8–3
- "High-Speed I/O Standards Support" on page 8–5
- "High-Speed I/O Timing in Cyclone III Devices" on page 8–17
- "Design Guidelines" on page 8–18
- "Software Overview" on page 8–19

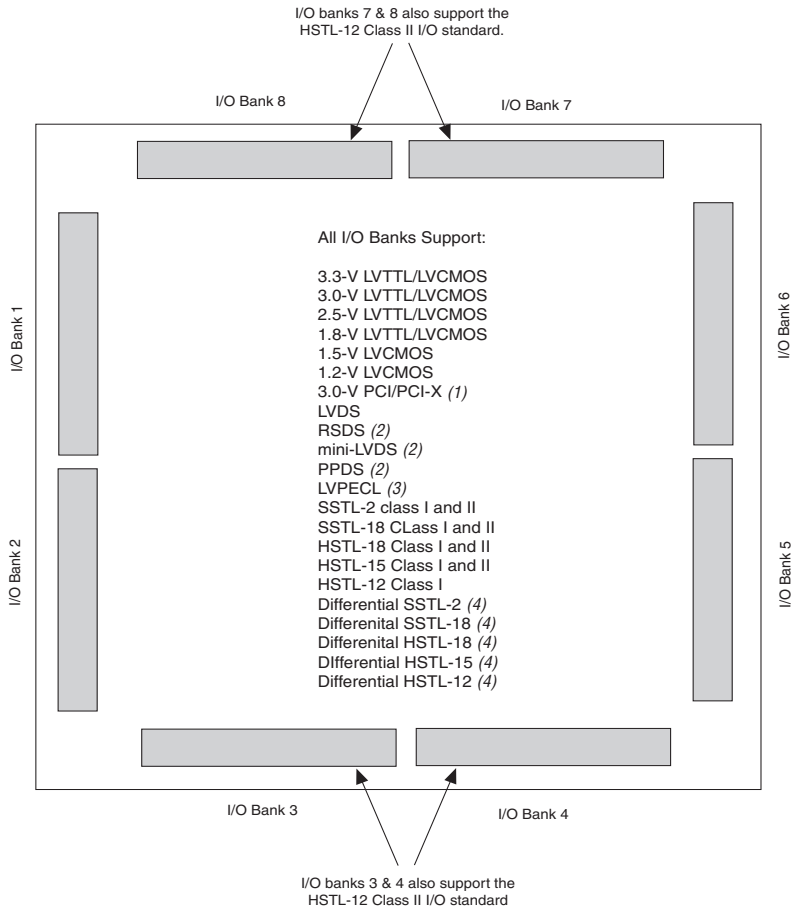
Cyclone III High-Speed I/O Banks

Cyclone III device I/Os are separated into eight I/O banks, as shown in Figure 8–1. Each bank has an independent power supply. Dedicated output drivers for LVDS, RSDS, mini-LVDS, and PPDS are on the left and right I/O banks. These I/O standards are also supported on the top and bottom I/O banks using external resistors. On the left and right I/O banks, some of the differential pin pairs (p and n pins) of the dedicated output drivers are not located on adjacent pins. In these cases, a power pin is located between the p and n pins.

Refer to the pin tables on the Altera web site at **www.altera.com** for more details about the location of the dedicated differential pins.

Table 8–1 shows the performance target for various differential I/O standards.

Figure 8–1. Cyclone III I/O Banks



Notes to Figure 8–1:

(1) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.

(2) The RSDS, mini-LVDS, and PPDS I/O standards are only supported on output pins. These I/O standards are not supported on input pins.

(3) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported on output pins.

(4) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on dedicated clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

Table 8–1. Performance Targets for Various Differential I/O Standards

Differential I/O Standards	I/O Bank Location	Pintable Package *(1)*	External Resistor Network at Transmitter	f_{MAX} (Mbps)	
				Transmitter (TX)	Receiver (RX)
LVDS	1,2,5,6	Adj.	Not required	840	875
	1,2,5,6	Sep.	Not required	640	875
	3,4,7,8	Res.	Three resistors	640	875
RSDS	1,2,5,6	Adj.	Not required	360	Not supported
	1,2,5,6	Sep.	Not required	*(4)*	
	3,4,7,8	Res.	Three resistors	*(4)*	
	3,4,7,8	Res.	Single resistor	*(4)*	
mini-LVDS	1,2,5,6	Adj.	Not required	400	Not supported
	1,2,5,6	Sep.	Not required	*(4)*	
	3,4,7,8	Res.	Three resistors	*(4)*	
PPDS	1,2,5,6	Adj.	Not required	440	Not supported
	1,2,5,6	Sep.	Not required	*(4)*	
	3,4,7,8	Res.	Three resistors	*(4)*	
LVPECL *(2)*	All	NA	NA	Not supported	875
Differential SSTL-2 *(3)*	All	NA	NA	200	200
Differential SSTL-18 *(3)*	1,2,5,6	NA	NA	200	200
	3,4,7,8	NA	NA	267	267
Differential HSTL-18 *(3)*	All	NA	NA	200	200
Differential HSTL-15 *(3)*	All	NA	NA	200	200
Differential HSTL-12 *(3)*	All	NA	NA	*(4)*	*(4)*

Notes to Table 8–1:

(1) "Adj." denotes the dedicated differential output drivers with `p` and `n` pins located adjacent to each other.
"Sep." denotes the dedicated differential output drivers with `p` and `n` pins not located adjacent to each other.
"Res." denotes the differential output drivers that require an external resistor network.
Refer to the pin tables on the Altera web site (**www.altera.com**) for details on the location of these pins.

(2) The LVPECL I/O standard is only supported on dedicated clock input pins.

(3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

(4) The performance target is pending device characterization.

Cyclone III High-Speed I/O Interface

Cyclone III devices provide a multi-protocol interface that allows communication between a variety of I/O standards, including LVDS, RSDS, mini-LVDS, PPDS, LVPECL, differential HSTL, and differential SSTL. This feature makes the Cyclone III device family ideal for applications that require multiple I/O standards, such as protocol translation.

You can use I/O pins and internal logic to implement a high-speed I/O receiver and transmitter in Cyclone III devices. Cyclone III devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

Table 8–2 shows the numbers of Cyclone III device differential channels.

Table 8–2. Cyclone III Device Differential Channels *Notes (1), (2)*

Device	Package	Pin Count	Number of Differential Channels		
			User I/O	Clock Pin	Total
EP3C5	EQFP	144	16	4	20
	FBGA	256	62	4	66
EP3C10	EQFP	144	16	4	20
	FBGA	256	62	4	66
EP3C16	EQFP	144	7	8	15
	EQFP	240	35	8	43
	FBGA	256	43	8	51
	FBGA	484	128	8	136
EP3C25	EQFP	144	6	8	14
	EQFP	240	31	8	39
	FBGA	256	42	8	50
	FBGA	324	71	8	79
EP3C40	EQFP	240	14	8	22
	FBGA	324	49	8	57
	FBGA	484	115	8	123
	FBGA	780	215	8	223
EP3C55	FBGA	484	123	8	131
	FBGA	780	151	8	159
EP3C80	FBGA	484	101	8	109
	FBGA	780	169	8	177
EP3C120	FBGA	484	94	8	102
	FBGA	780	221	8	229

Notes to Table 8–2:
(1) User I/O pins can be used as inputs or outputs; clock input pins can be used as inputs only.
(2) The pin count figures are preliminary.

Table 8–3 shows the numbers of Cyclone III device differential channels that are migratable.

Table 8–3. Cyclone III Device Migratable Differential Channels (Part 1 of 2)

Package Type	Migration between Devices	Migratable Channels		
		User I/O	CLK	Total
T144	EP3C5 and EP3C10	16	4	20
	EP3C5 and EP3C16	5	4	9
	EP3C5 and EP3C25	6	4	10
	EP3C10 and EP3C16	5	4	9
	EP3C10 and EP3C25	6	4	10
	EP3C16 and EP3C25	5	8	13
Q240	EP3C16 and EP3C25	23	8	31
	EP3C16 and EP3C40	11	8	19
	EP3C25 and EP3C40	12	8	20

Table 8–3. Cyclone III Device Migratable Differential Channels (Part 2 of 2)

Package Type	Migration between Devices	Migratable Channels		
		User I/O	CLK	Total
F256	EP3C5 and EP3C10	62	4	66
	EP3C5 and EP3C16	39	4	43
	EP3C5 and EP3C25	40	4	44
	EP3C10 and EP3C16	39	4	43
	EP3C10 and EP3C25	40	4	44
	EP3C16 and EP3C25	33	8	41
F324	EP3C25 and EP3C40	47	8	55
F484	EP3C16 and EP3C40	102	8	110
	EP3C16 and EP3C55	98	8	106
	EP3C16 and EP3C80	79	8	87
	EP3C16 and EP3C120	72	8	80
	EP3C40 and EP3C55	102	8	110
	EP3C40 and EP3C80	84	8	92
	EP3C40 and EP3C120	74	8	82
	EP3C55 and EP3C80	98	8	106
	EP3C55 and EP3C120	85	8	93
	EP3C80 and EP3C120	88	8	96
F780	EP3C40 and EP3C55	46	8	54
	EP3C40 and EP3C80	51	8	59
	EP3C40 and EP3C120	54	8	62
	EP3C55 and EP3C80	144	8	152
	EP3C55 and EP3C120	142	8	150
	EP3C80 and EP3C120	160	8	168

High-Speed I/O Standards Support

This section provides information about the high-speed I/O standards that Cyclone III devices support.

LVDS I/O Standard Support in Cyclone III Devices

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and general purpose I/O interface standard. The Cyclone III device meets the ANSI/TIA/EIA-644 standard with the following exceptions:

- The maximum voltage output differential (VOD) is increased to 600 mV. The maximum VOD for ANSI specification is 450 mV.
- The input voltage range can be reduced to the range of 1.0 V to 1.6 V, 0.5 V to 1.85 V or 0 V to 1.8 V based on different frequency ranges. The ANSI/TIA/EIA-644 specification supports an input voltage range of 0 V to 2.4 V.

For the LVDS I/O standard electrical specifications, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook.*

All of the Cyclone III device I/O banks support LVDS channels. The left and right I/O banks support dedicated LVDS transmitters. On the top and bottom I/O banks, the LVDS transmitters are supported using external resistors. The LVDS standard does not require an input reference voltage; however, it does require an external 100-Ω termination resistor between the two signals at the input buffer.

LVDS Transmitter

Cyclone III LVDS dedicated transmitters, which are located on the left and right I/O banks, support a data rate up to 840 Mbps, and the transmitters located on the top and bottom I/O banks support up to 640 Mbps (using external resistors).

For LVDS data rates in Cyclone III devices with different speed grades, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Figure 8–2 shows a simple point-to-point LVDS application using a Cyclone III dedicated transmitter in which the source of the data is an LVDS transmitter. These LVDS signals are typically transmitted over a pair of printed circuit board (PCB) traces, but a combination of a PCB trace, connectors, and cable is a common application setup.

Figure 8–2. Typical LVDS Application

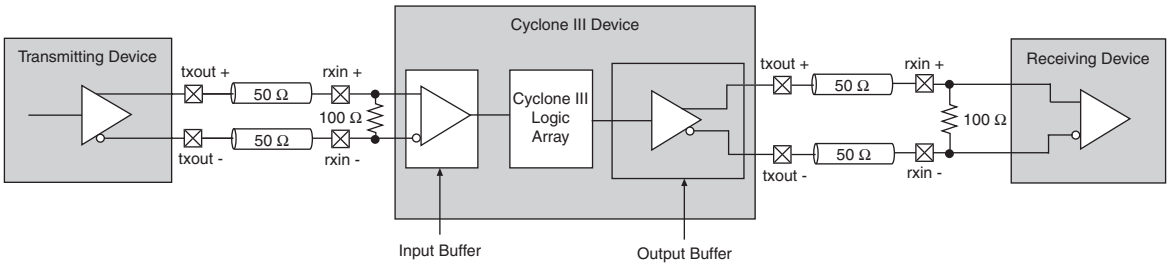


Figure 8–3 shows the LVDS I/O interface with dedicated output buffer on the left and right I/O banks. Figure 8–4 shows the LVDS I/O interface with external resistor network on the top and bottom I/O banks.

Figure 8–3. LVDS Interface with Dedicated Output Buffer on the Left and Right I/O Banks

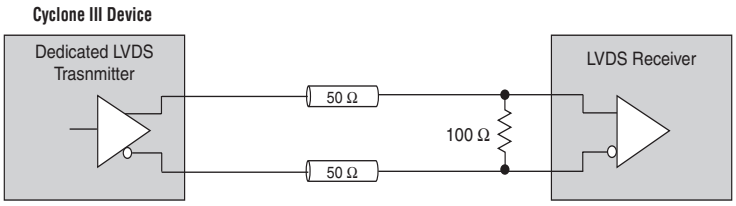
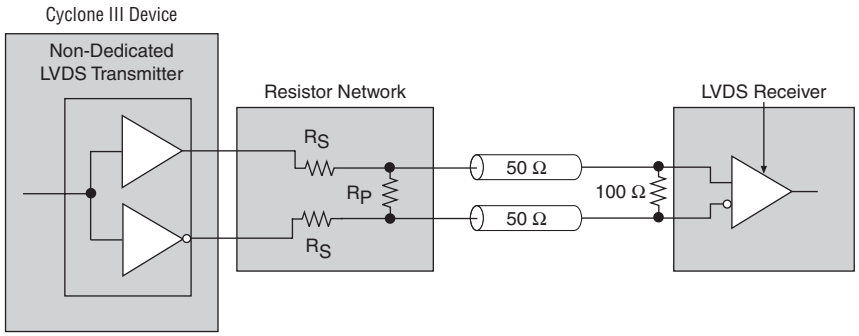


Figure 8–4. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks

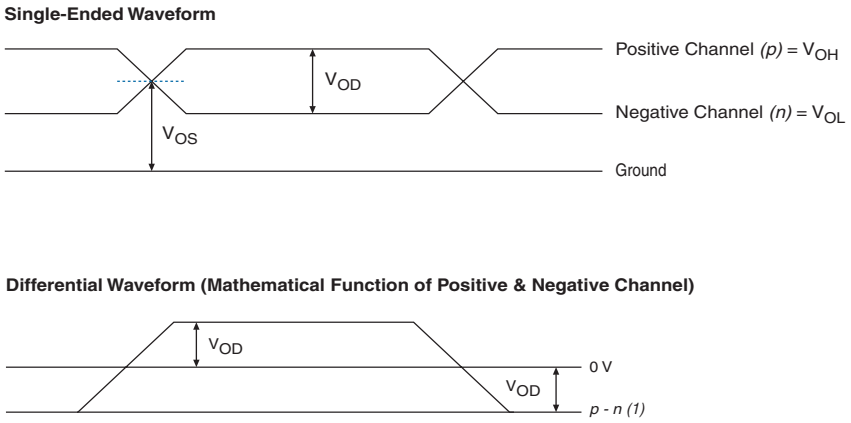


Note to Figure 8–4:

(1) The R_S and R_P values are pending device characterization.

Figure 8–5 shows the signaling level for LVDS transmitter outputs.

Figure 8–5. Transmitter Output Waveforms for the LVDS Differential I/O Standard



Note to Figure 8–5:

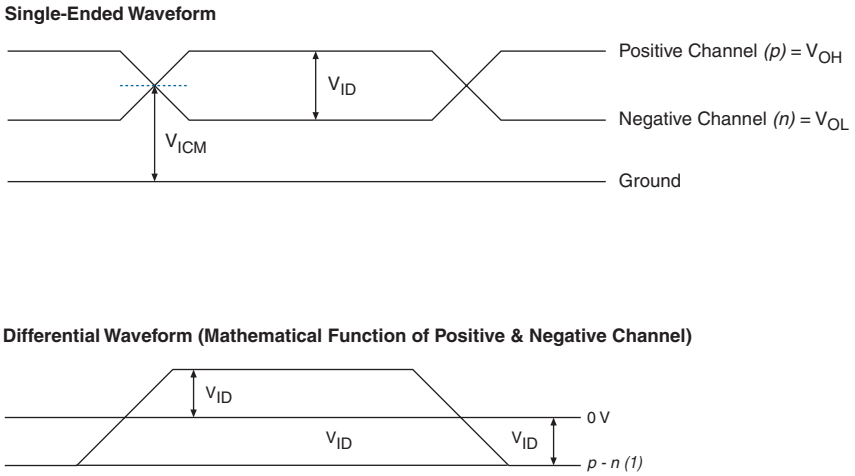
(1) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

LVDS Receiver

Cyclone III LVDS receivers support a data rate up to 875 Mbps. All the Cyclone III device I/O banks support dedicated receivers. The maximum internal clock frequency for the receiver is 437.5 MHz.

Figure 8–6 shows the signaling level for LVDS receiver inputs.

Figure 8–6. Receiver Input Waveforms for the LVDS Differential I/O Standard



Note to Figure 8–6:

(1) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

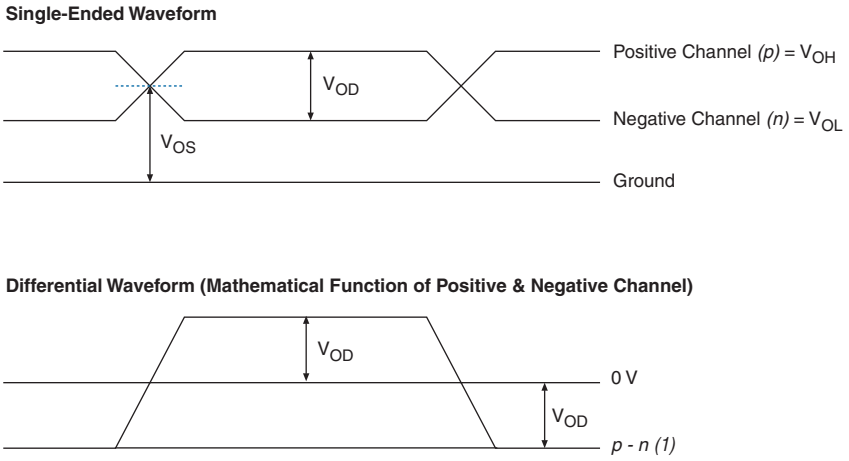
RSDS I/O Standard Support in Cyclone III Devices

The RSDS specification is used in chip-to-chip applications between the timing controller and the column drivers on the display panels. Cyclone III devices meet the National Semiconductor Corporation RSDS Interface Specification and support the RSDS output standard. All of the Cyclone III device I/O banks support the RSDS output standard. The left and right I/O banks support dedicated RSDS transmitters which are able to run at up to 360 Mbps. On the top and bottom I/O banks, the RSDS transmitters are supported using external resistors. The performance target is pending device characterization. The RSDS standard does not require an input reference voltage; however, it does require a 100-Ω termination resistor between the two signals at the input buffer.

For the RSDS I/O standard electrical specifications, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Figure 8–7 shows the RSDS transmitter output signal waveforms.

Figure 8–7. Transmitter Output Signal Level Waveforms for RSDS



Note to Figure 8–7:

(1) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

Designing with RSDS

No external resistor network is required when using a dedicated RSDS output buffer. Figure 8–8 shows the RSDS I/O interface with a dedicated output buffer on the left and right I/O banks. For a non-dedicated output buffer on the top and bottom I/O banks, an external resistor network is required, as shown in Figure 8–9.

Figure 8–8. RSDS Interface with Dedicated Output Buffer on the Left and Right I/O Banks

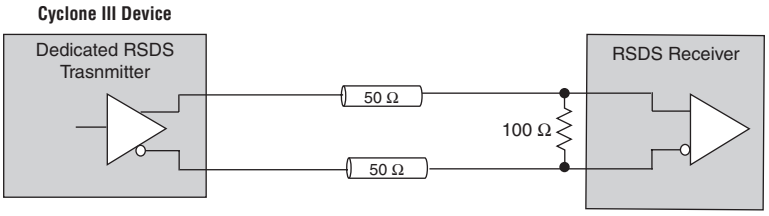
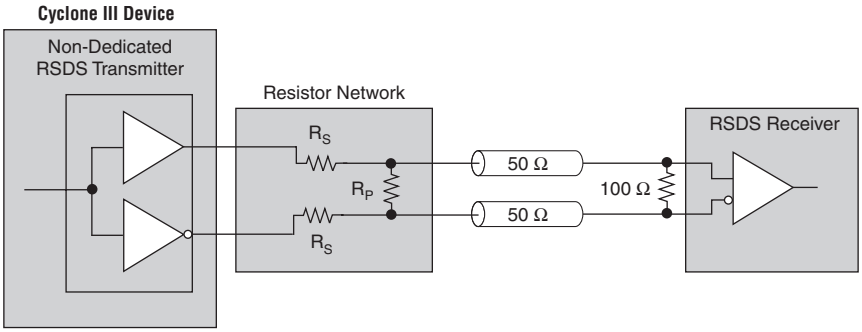


Figure 8–9. RSDS Interface with External Resistor Network on the Top and Bottom I/O Banks



Note to Figure 8–9:

(1) The R_S and R_P values are pending device characterization.

For more information about the RSDS I/O standard, refer to the RSDS specification from the National Semiconductor web site **(www.national.com)**.

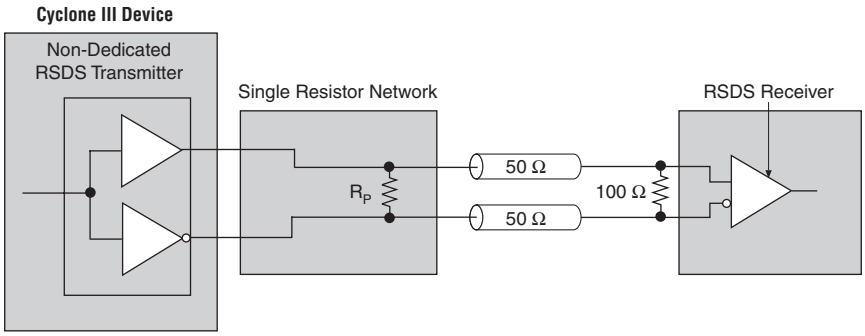
A resistor network is required to attenuate the output voltage swing to meet RSDS specifications when using non-dedicated RSDS transmitters. You can modify the resistor network values to reduce power or improve the noise margin. The resistor values chosen should satisfy equation 1:

(1)
$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\ \Omega$$

You should perform additional simulations using the IBIS models to validate that custom resistor values meet the RSDS requirements.

Instead of using three resistors in the resistor network, it is possible to use a single external resistor. The external single-resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. However, the performance of the single-resistor solution is lower than the performance with the resistor network. The performance target for a single-resistor solution is pending device characterization. To transmit the RSDS signal, an external resistor (Rp) is connected in parallel between the two adjacent I/O pins on the board, as shown in Figure 8–10.

Figure 8–10. RSDS Interface with Single Resistor Network on the Top and Bottom I/O Banks



Note to Figure 8–10:

(1) The R_P value is pending device characterization.

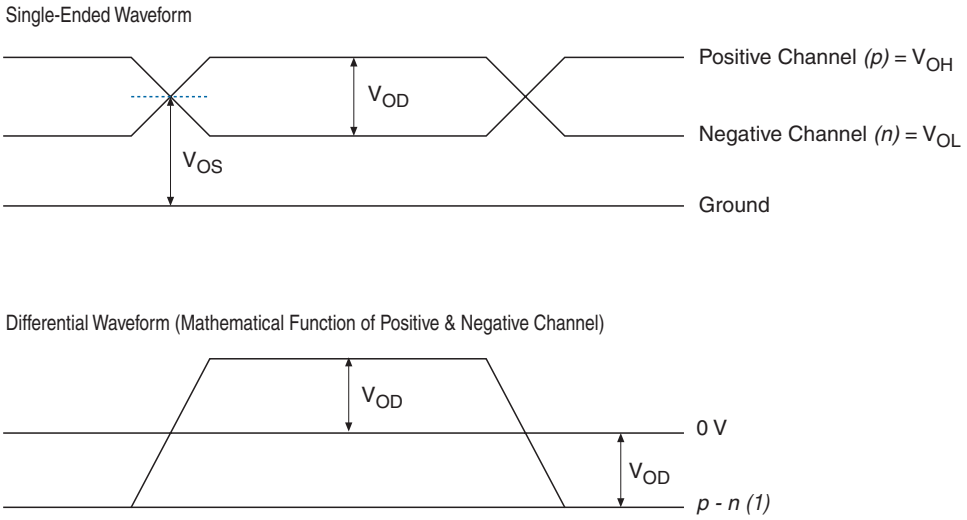
Mini-LVDS I/O Standard Support in Cyclone III Devices

The mini-LVDS specification defines its use in chip-to-chip applications between the timing controller and the column drivers on display panels. Cyclone III devices meet the Texas Instruments mini-LVDS Interface Specification and support the mini-LVDS output standard. All of the Cyclone III device I/O banks support the mini-LVDS output standard. The left and right I/O banks support dedicated mini-LVDS transmitters which are able to run at up to 400 Mbps. On the top and bottom I/O banks, the mini-LVDS transmitters are supported using external resistors. The performance target is pending device characterization. The mini-LVDS standard does not require an input reference voltage; however, it does require a 100-Ω termination resistor between the two signals at the input buffer.

For the mini-LVDS I/O standard electrical specifications, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Figure 8–11 shows the mini-LVDS transmitter output signal waveforms.

Figure 8–11. Transmitter Output Signal Level Waveforms for mini-LVDS



Note to Figure 8–11:

(1) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

Designing with Mini-LVDS

Similar to RSDS, there is no external resistor network required when you use a dedicated mini-LVDS output buffer on the left and right I/O banks. Figure 8–12 shows the mini-LVDS I/O interface with a dedicated output buffer. For a non-dedicated output buffer on the top and bottom I/O banks, an external resistor network is required, as shown in Figure 8–13. The resistor values chosen should satisfy Equation 1 on page 8–10.

Figure 8–12. mini-LVDS Interface with Dedicated Output Buffer on the Left and Right I/O Banks

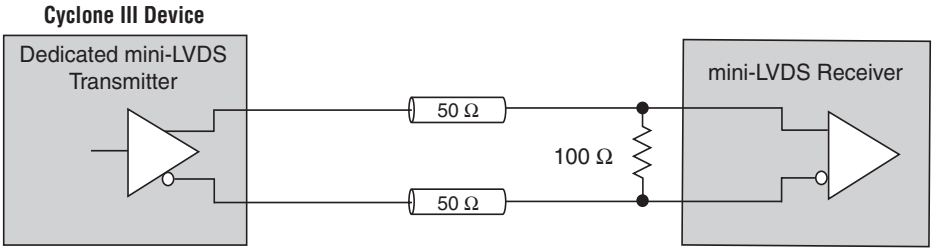
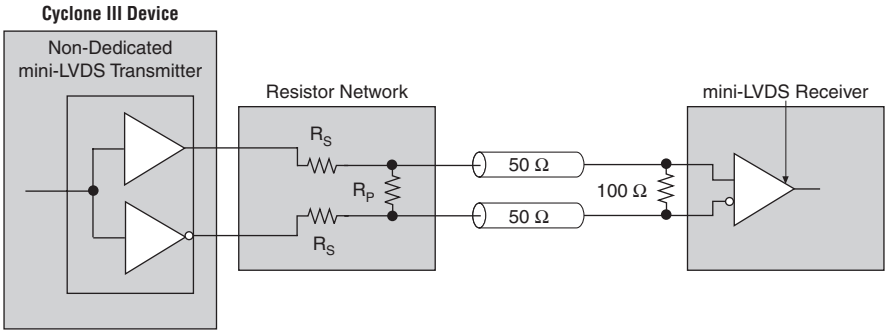


Figure 8–13. mini-LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks



Note to Figure 8–13:

(1) The R_S and R_P values are pending device characterization.

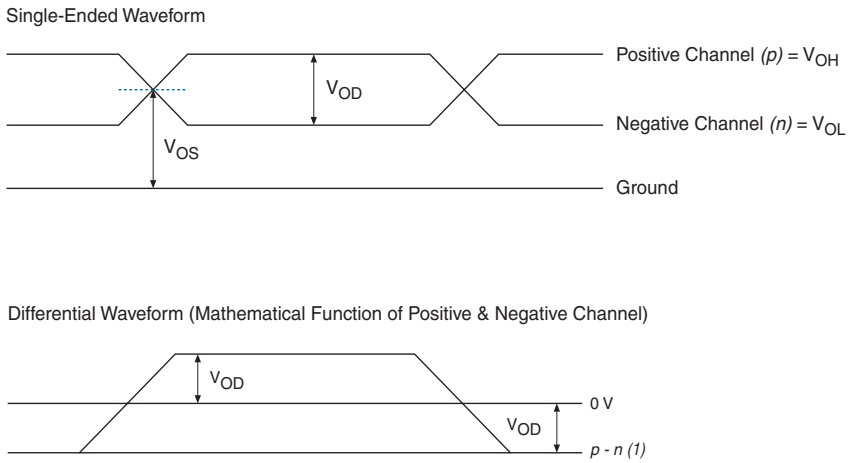
PPDS I/O Standard Support in Cyclone III Devices

The PPDS specification is used in chip-to-chip applications between the timing controller and the column drivers on display panels such as LCD monitor panels and LCD televisions. Cyclone III devices meet the National Semiconductor Corporation PPDS Interface Specification and support the PPDS output standard. All the Cyclone III device I/O banks support the PPDS output standard. The left and right I/O banks support dedicated PPDS transmitters which run at up to 440 Mbps. On the top and bottom I/O banks, the PPDS transmitters are supported using external resistors. The performance target is pending device characterization. The PPDS standard does not require an input reference voltage; however, it does require a 100-Ω termination resistor between the two signals at the input buffer.

For the PPDS I/O standard electrical specification, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Figure 8–14 shows the PPDS transmitter output signal waveforms.

Figure 8–14. Transmitter Output Signal Level Waveforms for PPDS



Note to Figure 8–14:

(1) The $p - n$ waveform is a function of the positive channel (p) and the negative channel (n).

Designing with PPDS

Similar to RSDS and mini-LVDS, no external resistor network is required when you use a dedicated PPDS output buffer. Figure 8–15 shows the PPDS I/O interface with a dedicated output buffer. For a non-dedicated output buffer, an external resistor network is required, as shown in Figure 8–16. The resistor values chosen should satisfy the equation shown in "Designing with RSDS" on page 8–9.

Figure 8–15. PPDS Interface with Dedicated Output Buffer on the Left and Right I/O Banks

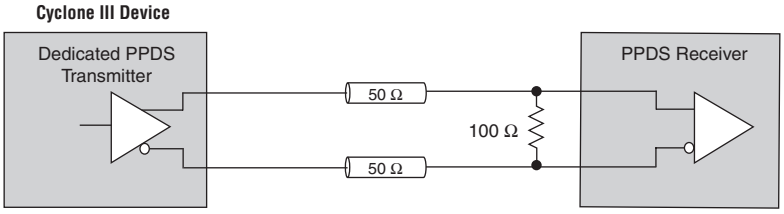
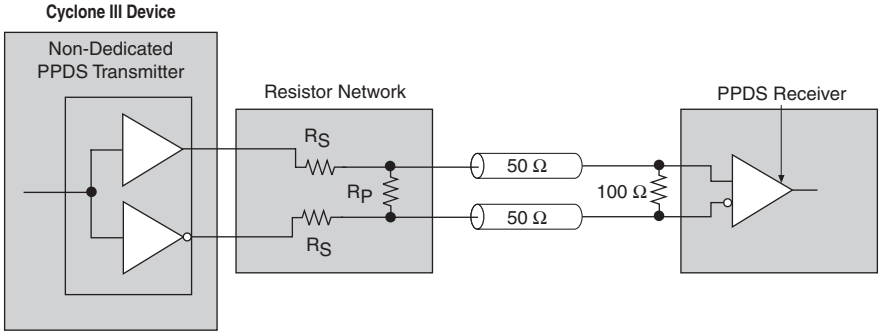


Figure 8–16. PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks



Note to Figure 8–16:

(1) The R_S and R_P values are pending device characterization.

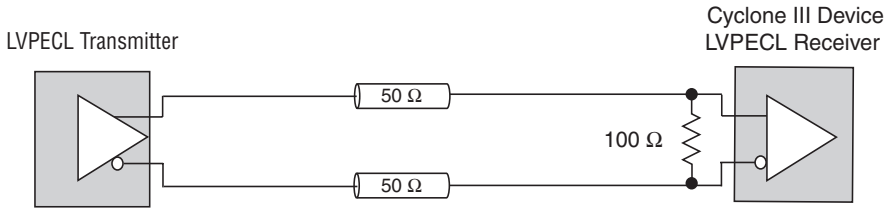
LVPECL I/O Support in Cyclone III Devices

The LVPECL I/O standard is a differential interface standard that requires a 2.5-V V_{CCIO}. This standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The high-speed, low-voltage swing LVPECL I/O standard uses a positive power supply. Cyclone III devices support the LVPECL input standard at the dedicated clock input pins only. The LVPECL standard does not require an input reference voltage; however, it does require an external 100-Ω termination resistor between the two signals at the input buffer.

For the LVPECL I/O standard electrical specification, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Figure 8–17 shows the LVPECL I/O interface.

Figure 8–17. LVPECL I/O Interface



Differential SSTL I/O Standard Support in Cyclone III Devices

The differential SSTL I/O standard is a memory-bus standard used for applications such as high-speed double-data rate (DDR) SDRAM interfaces. The differential SSTL I/O standard AC and DC specifications are similar to SSTL single-ended specifications. The standard requires two differential inputs with an external reference voltage (V_{REF}) as well as an external termination voltage (V_{TT}) of 0.5 x V_{CCIO} to which termination resistors are connected. Cyclone III devices support differential SSTL-2 and SSTL-18 I/O standards. A 2.5-V output source voltage is required for differential SSTL-2, and a 1.8-V output source voltage is required for differential SSTL-18. The differential SSTL output standard is only supported at `PLL#_CLKOUT` pins using two single-ended SSTL output buffers (`PLL#_CLKOUTp` and `PLL#_CLKOUTn)` programmed to have opposite polarity.

The differential SSTL input standard is supported at the global clock (`GCLK`) pins only, where it treats differential inputs as two single-ended SSTL and only decodes one of them.

For SSTL signaling characteristics, refer to the *Cyclone III Device I/O Features* chapter and the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volumes 1 and 2, respectively, of the *Cyclone III Device Handbook*.

Figures 8–18 and 8–19 show the differential SSTL class I and II interfaces, respectively.

Figure 8–18. Differential SSTL Class I Interface

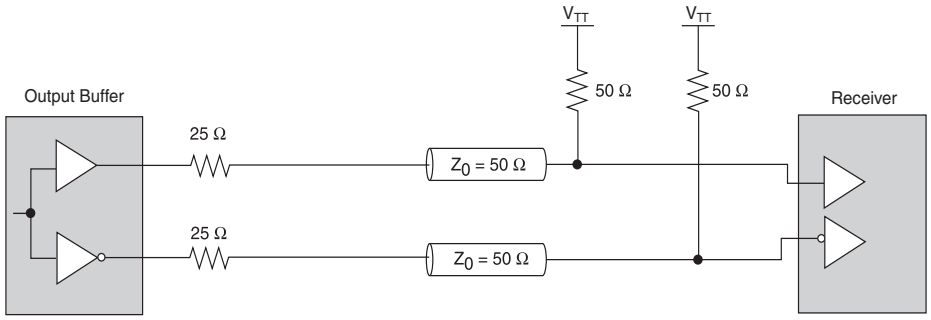
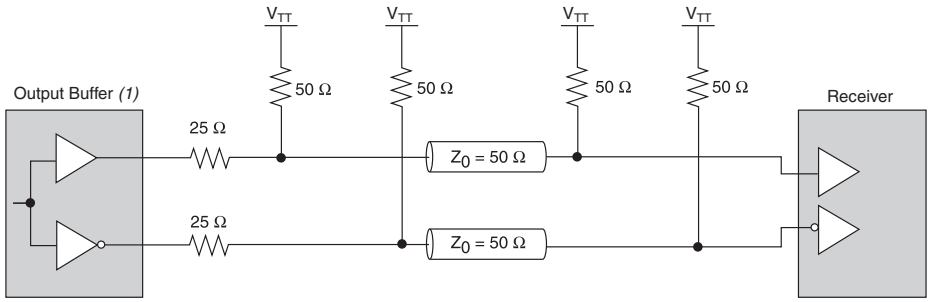


Figure 8–19. Differential SSTL Class II Interface



Note to Figure 8–19:
(1) PLL output clock pins do not support differential SSTL-18 Class II I/O standard.

Differential HSTL I/O Standard Support in Cyclone III Devices

The differential HSTL I/O standard is used for the applications designed to operate in the 0 V to 1.2 V, 0 V to 1.5 V, or 0 V to 1.8 V HSTL logic switching range. Cyclone III devices support differential HSTL-18, HSTL-15, and HSTL-12 I/O standards. The differential HSTL AC and DC specifications are the same as the HSTL single-ended specifications. The differential HSTL input standard is available on the `GCLK` pins only, treating differential inputs as two single-ended HSTL and only decoding one of them. The differential HSTL output standard is only supported at the `PLL#_CLKOUT` pins using two single-ended HSTL output buffers (`PLL#_CLKOUTp` and `PLL#_CLKOUTn`), with the second output programmed as inverted. The standard requires two differential inputs with an external reference voltage (V_{REF}), as well as an external termination voltage (V_{TT}) of 0.5 × V_{CCIO} to which termination resistors are connected.

For HSTL signaling characteristics, refer to the *Cyclone III Device I/O Features* chapter and the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volumes 1 and 2, respectively, of the *Cyclone III Device Handbook*.

Figures 8–20 and 8–21 show differential HSTL class I and II interfaces, respectively.

Figure 8–20. Differential HSTL Class I Interface

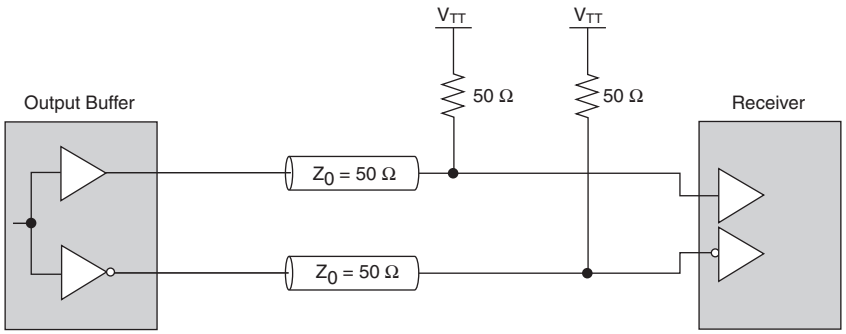
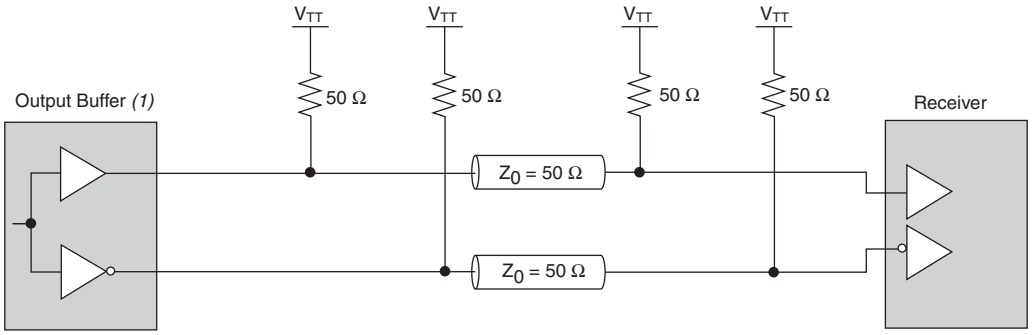


Figure 8–21. Differential HSTL Class II Interface



Note to Figure 8–21:
(1) Cyclone III devices do not support differential HSTL Class II interface on outputs. It is only supported as inputs on `GCLK` pins.

Feature of the Dedicated Output Buffer

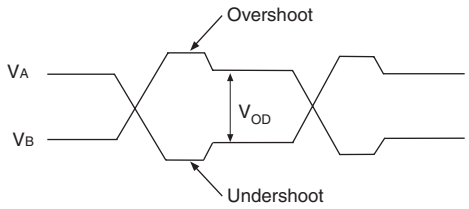
Cyclone III dedicated differential transmitters offer programmable pre-emphasis to further improve the signal integrity in high frequency applications.

Programmable Pre-Emphasis

The programmable pre-emphasis boosts the high frequencies of the output signal, which may be attenuated in the transmission media. It is used to compensate the frequency-dependant attenuation of the transmission line to maximize the data eye opening at the far-end receiver. Without pre-emphasis, the output current is limited by the V_{OD} specification and the output impedance of the transmitter. At high frequency, the slew rate may not be fast enough to reach full V_{OD} before the next edge; this may lead to pattern dependent jitter. With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching and does not produce ringing. Figure 8–22 shows the differential output signal with pre-emphasis.

The pre-emphasis setting in Cyclone III devices is programmable—you can choose to turn it on or off. You may need to enable the pre-emphasis if there is high attenuation in the transmission line.

Figure 8–22. The Output Signal with Pre-Emphasis



High-Speed I/O Timing in Cyclone III Devices

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone III devices. LVDS, RSDS, mini-LVDS, PPDS, and LVEPCL I/O standards enable high-speed data transmission. Timing for these high-speed signals is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by integrated circuit (IC) vendors and requires consideration of board skew, cable skew, and clock jitter. This section provides details on high-speed I/O standards timing parameters in Cyclone III devices.

Table 8–4 defines the parameters of the timing diagram shown in Figure 8–23. Figure 8–24 shows the Cyclone III high-speed I/O timing budget.

Table 8–4. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $RSKM = \frac{(TUI - SW - TCCS)}{2}$
Input jitter tolerance (peak-to-peak)	—	Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)	—	Peak-to-peak output jitter from the PLL.

Note to Table 8–4:

(1) The TCCS specification applies to the entire bank of differential I/O as long as the SERDES logic is placed within the LAB adjacent to the output pins.

Figure 8–23. High-Speed I/O Timing Diagram

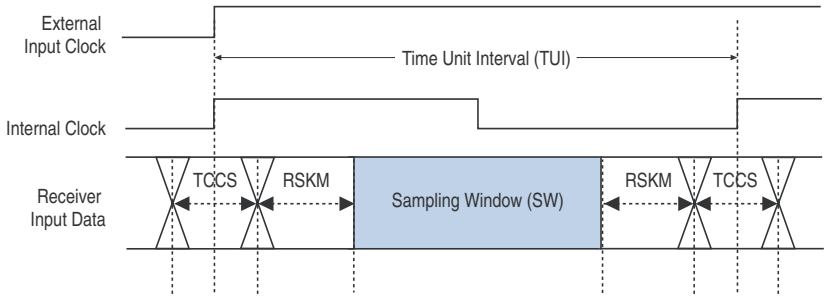
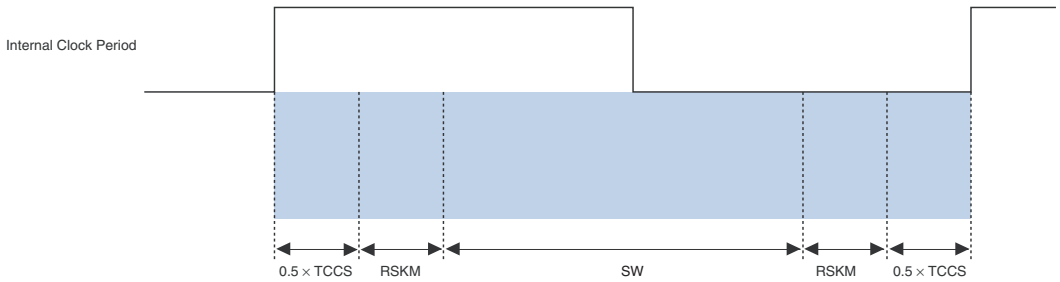


Figure 8–24. Cyclone III High-Speed I/O Timing Budget Note (1)



Note to Figure 8–24:

(1) The equation for the high-speed I/O timing budget is: Period = 0.5 × TCCS + RSKM + SW + RSKM + 0.5 × TCCS.

For more details, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

Design Guidelines

This section provides guidelines for designing with Cyclone III devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, you must observe some restrictions on placement of single-ended I/O pins in relation to differential pads.

For guidelines on placing single-ended pads with respect to differential pads in Cyclone III devices, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Board Design Considerations

This section explains how to achieve the optimal performance from the Cyclone III I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. You must consider the critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques to get the best performance from the IC. Cyclone III devices generate signals that travel over the media at frequencies as high as 840 Mbps.

Use the following general guidelines for improved signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters, such as trace width, trace thickness, and the distance between two differential traces.
- Maintain equal distance between traces in differential I/O standard pairs as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces should be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° corners.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the impedance of the connector and/or termination.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the channel-to-channel skew (TCCS) value increases.
- Limit vias because they cause discontinuities.

- Use common bypass-capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the high-speed PLL power and ground planes.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs.*

Software Overview

Cyclone III device high-speed I/O system interfaces are created in core logic by a Quartus II software megafunction, because they do not have a dedicated circuit for the SERDES. Cyclone III devices use the I/O registers and logic element (LE) registers to improve the timing performance and support the SERDES. Altera Quartus II software allows you to design your high-speed interfaces using its altlvds megafunction. This megafunction implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the altlvds megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use the Cyclone III resources to create the high-speed I/O interfaces in the most effective manner.

For more details in designing your high-speed I/O systems interfaces using the Quartus II software, refer to the *altlvds Megafunction User Guide* and the *Quartus II Handbook*.

Conclusion

Cyclone III dedicated differential buffers allow you to transmit data at high speeds. Their use reduces cost and complexity, and lowers board space requirements by eliminating the need for external resistors in many backplane and video display applications.

Referenced Documents

This chapter references the following documents:

- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *AN 224: High-Speed Board Layout Guidelines*
- *AN 315: Guidelines for Designing High-Speed FPGA PCBs*
- *altlvds Megafunction User Guide*
- *Quartus II Handbook*

Document Revision History

Table 8–5 shows the revision history for this document.

Table 8–5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated *Note (4)* to Figure 8–1. • Updated *Note (3)* to Table 8–1. • Added new Table 8–3. • Added *Note (1)* to Figure 8–19. • Added *Note (1)* to Figure 8–21. • Added chapter TOC and "Referenced Documents" section.	• Added note that PLL output clock pins do not support Class II type of selected differential I/O standards. • Added Table 8–3 that lists the number of differential channels which are migratable across densities and packages.
March 2007 v1.0	Initial Release.	—

9. External Memory Interfaces in Cyclone III Devices

CIII51009-1.1

Introduction

In addition to an abundant supply of on-chip memory, Cyclone® III devices can easily interface to a broad range of external memory including DDR2 SDRAM, DDR SDRAM, and QDRII SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

Cyclone III devices are supported with a comprehensive infrastructure to create robust external memory interfaces. Table 9–1 highlights the major benefits of Cyclone III external memory interfaces.

Table 9–1. Major Benefits of Cyclone III Memory Interfaces

Benefit	Cyclone III Solution Description
Robust	Self-calibrating to adjust for process, voltage, and temperature changes
Easy to use	• Push button timing closure • DDR2/DDR available on all sides to ease PCB layout constraints • Half rate solution available to lower f_{MAX} requirements
Resource Efficient	Maximum of 5 global clocks for ×72 interface
Good Performance	200 MHz DDR2 SDRAM on fastest speed grade

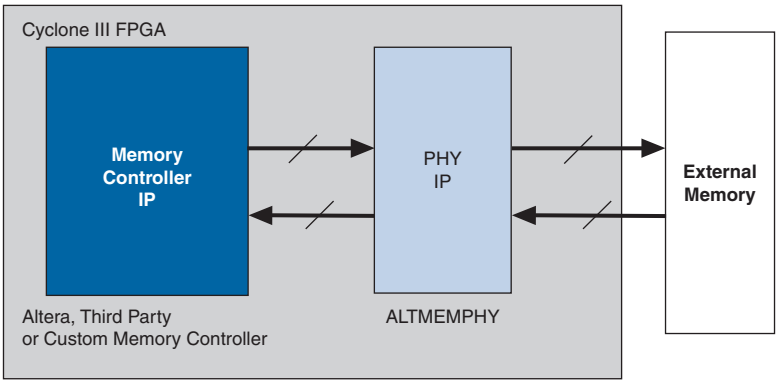
The Cyclone III external memory interface infrastructure includes the components listed in Table 9–2.

Table 9–2. Cyclone III External Memory Interface Infrastructure

Memory Interface Feature	Description
Auto-calibrating ALTMEMPHY megafunction	Manages the physical (PHY) interfaces between the FPGA device and the external memory devices. Comes as a megafunction and is available in the Quartus® II software version 7.0 and later.
Altera, third party, or user-designed memory controller	Controls the PHY interface and the interface between the PHY and the user's application. The Altera® controllers are included with Altera software subscriptions as part of the IP-BASE Suite.
Silicon enhancements	The phase-locked loop (PLL) reconfiguration feature adjusts the clock phase shifts in the system to calibrate changes in voltage and temperature. Two additional registers were added to Cyclone III input/output elements (IOEs) to enhance double-data rate I/O (DDIO) timing.
Quartus II Timing Analyzer and Classic Timing Analyzer	Uses industry standard synopsys design constraint (SDC) language to easily support source-synchronous timing analysis.

Altera recommends that you construct all DDR2/DDR SDRAM and QDRII SRAM external memory interfaces using the Altera ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2/DDR SDRAM or QDRII SRAM memory controllers, third party controllers, or a custom controller for unique application needs. Figure 9–1 shows an overview of a Cyclone III external memory interface.

Figure 9–1. Cyclone III External Memory Interface Overview



This chapter includes a description of the hardware interfaces for external memory interfaces available in the Cyclone III devices. For more information about implementing complete external memory interfaces, refer to the following documents found at the Altera web site at **www.altera.com**:

- *ALTMEMPHY Megafunction User Guide*
- *DDR and DDR2 SDRAM Controller Compiler User Guide*
- *AN 445: Design Guidelines for Implementing DDR & DDR2 SDRAM Interfaces in Cyclone III Devices*
- *AN 438: Constraining and Analyzing Timing for External Memory Interfaces*

This chapter contains the following sections:

- "Cyclone III Memory Support Overview" on page 9–3
- "Cyclone III Memory Interfaces Pin Support" on page 9–4
- "Cyclone III Memory Interfaces Features" on page 9–10

Cyclone III Memory Support Overview

This section describes the interface between Cyclone III devices and external memory standards. Table 9–3 summarizes the maximum clock rate that Cyclone III devices can support with external memory interfaces.

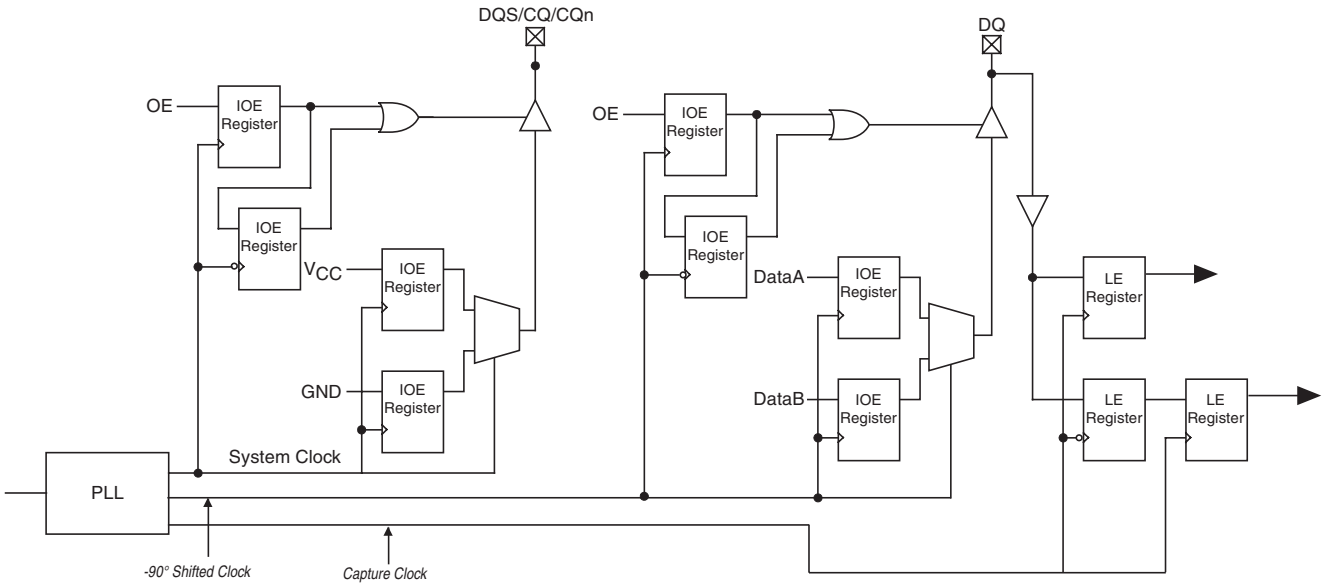
Table 9–3. Cyclone III Maximum Clock Rate Support for External Memory Interfaces Note (1)

Memory Standard	I/O Standard	Commercial					
		–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)	
		Top/Bottom I/O Banks	Left/Right I/O Banks	Top/Bottom I/O Banks	Left/Right I/O Banks	Top/Bottom I/O Banks	Left/Right I/O Banks
DDR2 SDRAM *(2)*	SSTL-18 class I	200	167	167	150	167	133
	SSTL-18 class II	133	125	125	*(3)*	*(3)*	*(3)*
DDR SDRAM *(2)*	SSTL-2 class I	167	150	150	133	133	125
	SSTL-2 class II	133	125	125	100	100	*(3)*
QDRII SRAM *(4)*	1.8-V HSTL class I	167	150	150	133	133	125
	1.8V HSTL class II	100	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*

Notes to Table 9–3:
(1) These numbers are preliminary until characterization is final.
(2) The values apply for interfaces with both modules and components.
(3) Support will be evaluated after characterization.
(4) QDRII SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O drive strength.

Figure 9–2 shows the block diagram of a typical external memory interface data path in Cyclone III devices.

Figure 9–2. Cyclone III External Memory Data Path Note (1)

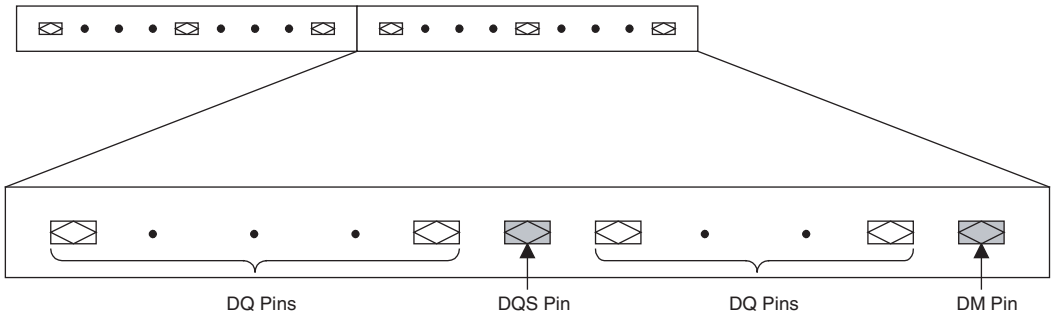


Note to Figure 9–2:
(1) All clocks shown here are global clocks.

Cyclone III Memory Interfaces Pin Support

Cyclone III devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory. Some memory interfaces use the data mask (DM) or byte write select (BWS#) pins to enable data masking. This section describes how Cyclone III supports all these different pins. Figure 9–3 illustrates the DQ and DQS pins.

Figure 9–3. Cyclone III DQ and DQS pins *Notes (1), (2), (3)*



Notes to Figure 9–3:
(1) Each DQ group consists of a DQS pin, a DM pin and DQ pins.
(2) DQ groups on the left and right sides of EP3C16, EP3C25, and EP3C40 (of the 240-pin PQFP package) do not support DM pin.
(3) DQ groups on the bottom sides of EP3C10, EP3C16, and EP3C25 (of the 144-pin EQFP package) do not support DM pin.

Data and Data Clock/Strobe Pins

Cyclone III data pins for external memory interfaces are called D for write data, Q for read data, or DQ for shared read and write data pins. The read-data strobes or read clocks are called DQS pins. Cyclone III devices support both bidirectional data strobes and unidirectional read clocks. Depending on the external memory standard, the DQ and DQS are bidirectional signals (in DDR2 and DDR SDRAM) or unidirectional signals (in QDRII SRAM). Connect the bidirectional DQ data signals to the same Cyclone III DQ pins. For unidirectional D or Q signals, connect the read-data signals to a group of DQ pins and the write-data signals to a different group of DQ pins.

In QDRII SRAM, the Q read-data group must be placed at a different V_{ref} bank location from the D write-data, command or address pins.

In Cyclone III devices, DQS is used only during write mode in DDR2 and DDR SDRAM interfaces. Cyclone III devices ignore DQS as the read-data strobe because the physical layer (PHY) internally generates the read capture clock for read mode. However, you must connect the DQS pin to the DQS signal in DDR2 and DDR SDRAM interfaces, or to the CQ signal in QDRII SRAM interfaces.

Cyclone III does not support differential strobe pins, which is an optional feature in DDR2 SDRAM devices.

When you use the Altera Memory Controller MegaCores, the PHY is instantiated for you. For more information about the memory interface data path, refer to the *ALTMEMPHY Megafunction User Guide*.

ALTMEMPHY is a self-calibrating megafunction, enhanced to simplify the implementation of the read-data path in different memory interfaces. The auto-calibration feature of ALTMEMPHY provides ease-of-use by optimizing clock phases and frequencies across process, voltage, and temperature (PVT) variations. You can save on the global clock resources in Cyclone III devices through the ALTMEMPHY megafunction because you do not need to route the DQS signals on the global clock buses (because DQS is ignored for read capture). Resynchronization issues do not arise because no transfer occurs from the memory domain clock (DQS) to the system domain for capturing data DQ.

All the I/O banks in Cyclone III devices support DQ and DQS signals with DQ-bus modes of ×8, ×9, ×16, ×18, ×32, and ×36. In ×8, ×16, and ×32 modes, one DQS pin drives up to 8, 16, or 32 DQ pins, respectively, within the group, to support DDR2 and DDR SDRAM interfaces.

In the ×9, ×18, and ×36 modes, a pair of DQS pins (CQ and CQ#) drives up to 9, 18, or 36 DQ pins, respectively, within the group, to support one, two, or four parity bits and the corresponding data bits. The ×9, ×18, and ×36 modes support the QDRII memory interface. CQ# is the inverted read-clock signal which is connected to the complementary data strobe (DQS/CQ#) pin. You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signals. Table 9–4 shows the number of DQS/DQ groups supported on each side of the Cyclone III device.

Table 9–4. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device Note (1) (Part 1 of 3)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C5	144-pin EQFP (2)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (3)	1	0	0	0	—	—
		Bottom (4),(5)	1	0	0	0	—	—
	256-pin FineLine BGA (2)	Left (5),(6)	1	1	0	0	—	—
		Right (5),(7)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C10	144-pin EQFP (2)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (3)	1	0	0	0	—	—
		Bottom (4),(5)	1	0	0	0	—	—
	256-pin FineLine BGA (2)	Left (5),(6)	1	1	0	0	—	—
		Right (5),(7)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C16	144-pin EQFP (2)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (3)	1	0	0	0	—	—
		Bottom (4),(5)	1	0	0	0	—	—
	240-pin PQFP (2)	Left (5),(8)	1	1	0	0	—	—
		Right (4),(5)	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA (2)	Left (5),(6)	1	1	0	0	—	—
		Right (5),(7)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1

Table 9–4. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device Note (1) (Part 2 of 3)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C25	144-pin EQFP *(2)*	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top *(3)*	1	0	0	0	—	—
		Bottom *(4),(5)*	1	0	0	0	—	—
	240-pin PQFP *(2)*	Left *(5),(8)*	1	1	0	0	—	—
		Right *(4),(5)*	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA *(2)*	Left *(5),(6)*	1	1	0	0	—	—
		Right *(5),(7)*	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	324-pin FineLine BGA *(2)*	Left	2	2	1	1	—	—
		Right *(9)*	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C40	240-pin PQFP	Left *(5),(8)*	1	1	0	0	0	0
		Right *(4),(5)*	1	0	0	0	0	0
		Top	1	1	0	0	0	0
		Bottom	1	1	0	0	0	0
	324-pin FineLine BGA	Left	2	2	1	1	0	0
		Right *(9)*	2	2	1	1	0	0
		Top	2	2	1	1	0	0
		Bottom	2	2	1	1	0	0
	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C55	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Table 9–4. Cyclone III DQS and DQ Bus Mode Support for Each Side of the Device Note (1) (Part 3 of 3)

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3C80	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C120	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Notes to Table 9–4:

(1) These numbers are preliminary until characterization is final.
(2) This device package does not support ×32/×36 mode.
(3) For the top side of the device, the R_{UP}, R_{DN}, PLLCLKOUT3n and PLLCLKOUT3p are shared with the DQ/DM pins to gain ×8 DQ group. You cannot use these groups if you are using the R_{UP} and R_{DN} pins for on-chip termination (OCT) calibration or if you are using PLLCLKOUT3n and PLLCLKOUT3p.
(4) There is no DM pin support for these groups.
(5) The R_{UP} and R_{DN} are shared with the DQ pins. You cannot use these groups if you are using the R_{UP} and R_{DN} pins for OCT calibration.
(6) The ×8 DQ group can be formed in Bank 2.
(7) The ×8 DQ group can be formed in Bank 5.
(8) There is no DM and BWS# pins support for these groups.
(9) The R_{UP} is shared with the DQ pin to gain ×9 or ×18 DQ group. You cannot use these groups if you are using the R_{UP} and R_{DN} pins for OCT calibration.

The DQS pins are listed in the Cyclone III pin tables as DQSXY, where X indicates the DQS grouping number and Y indicates which side of the I/O bank the DQS pins belong. The Y can be T for pins on the top, B for pins on the bottom, L for pins on the left, or R for pins on the right side of the device. Similarly, the corresponding DQ pins are marked as DQXY, where the X denotes which DQ group the pins belong to and Y denotes the I/O bank location of the DQ pins. The Y can be T for pins on the top, B for pins on the bottom, L for pins on the left, or R for pins on the right side of the device. For example, DQS2T indicates a DQS pin belonging to group 2, located on the top side of the device. Similarly, the DQ pins belonging to that group is shown as DQ2T.

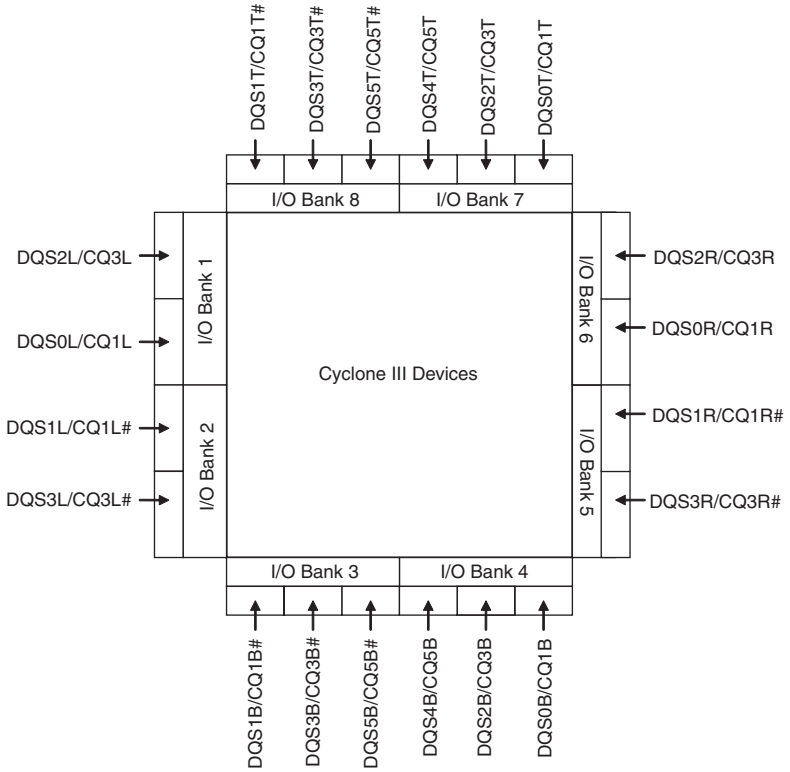
☞ Each DQ group is associated with its corresponding DQS pins, as defined in the Cyclone III pin tables; for example:

- For DDR2/DDR SDRAM, a x8 DQ group DQ3B[7:0] pins are associated with the DQS3B pin (same 3B group index).
- For QDRII SRAM, a x9 Q read-data group DQ3L[8..0] pins are associated with DQS2L/CQ3L and DQS3L/CQ3L# pins (same 3L group index).

The Quartus II software issues an error message if a DQ group is not placed properly with its associated DQS.

DQ pin numbering is based on ×8/×9 mode. There are up to 20 DQS/DQ groups in ×8 mode or up to 8 DQS/DQ groups in ×9 mode in the I/O banks, that can be utilized for the external memory interface. Figure 9–4 and Figure 9–5 show the location and numbering of the DQS/DQ/CQ# pins in the Cyclone III I/O banks.

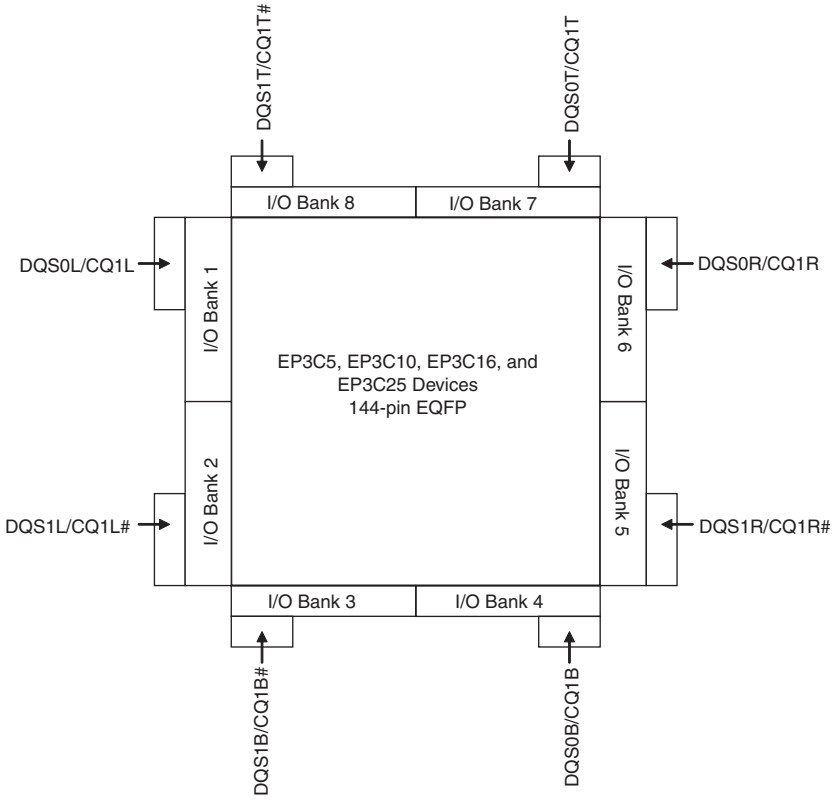
Figure 9–4. DQS/CQ/CQ# Pins in Cyclone III I/O Banks *Note (1)*



Note to Figure 9–4:

(1) The DQS/CQ/CQ# pin locations in this diagram applies to all packages in the Cyclone III family except EP3C5, EP3C10, EP3C16 and EP3C25 devices in 144-pin EQFP package.

Figure 9–5. DQS/CQ/CQ# Pins in EP3C5, EP3C10, EP3C16, and EP3C25 Devices in the 144-Pin EQFP Package



In Cyclone III devices, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as ×32 mode, with four additional DQ pins that serve as regular I/O pins in ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

Optional Parity, DM, and ECC Pins

Cyclone III devices support parity in the ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in the Cyclone III devices because the parity pins are treated and configured like DQ pins.

The data mask (DM) pins are only required when writing to DDR2 and DDR SDRAM devices. QDRII SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the –90° shifted clock.

In Cyclone III devices, the DM pins are preassigned in the device pinouts. The Quartus II Fitter treats the DQ and DM pins in a DQS group equally for placement purposes. The preassigned DQ and DM pins are the preferred pins to use.

Some DDR2 SDRAM and DDR SDRAM devices support error correction coding (ECC), a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR2 or DDR SDRAM, there are eight ECC pins and 64 data pins. Connect the DDR2 and DDR SDRAM ECC pins to a DQS/DQ group in Cyclone III devices. The memory controller needs additional logic to encode and decode the ECC data.

Address and Control/Command Pins

The address signals and the control or command signals are typically sent at a single data rate. You can use any of the user I/O pins on all I/O banks of Cyclone III devices to generate the address and control or command signals to the memory device.

Cyclone III devices do not support QDRII SRAM in the burst length of two.

Memory Clock Pins

In DDR2 and DDR SDRAM memory interfaces, the memory clock signals (`CK` and `CK#`) are used to capture the address signals and the control or command signals. Similarly, QDRII SRAM devices use the write clocks (`K` and `K#`) to capture the address and command signals. The `CK/CK#` and `K/K#` signals are generated to mimic the write-data strobe using the DDIO registers in Cyclone III devices. You can use any regular adjacent I/O pins (preferably differential I/O pair) to generate the `CK/CK#` for DDR2 and DDR SDRAM interface or `K/K#` for QDRII SRAM.

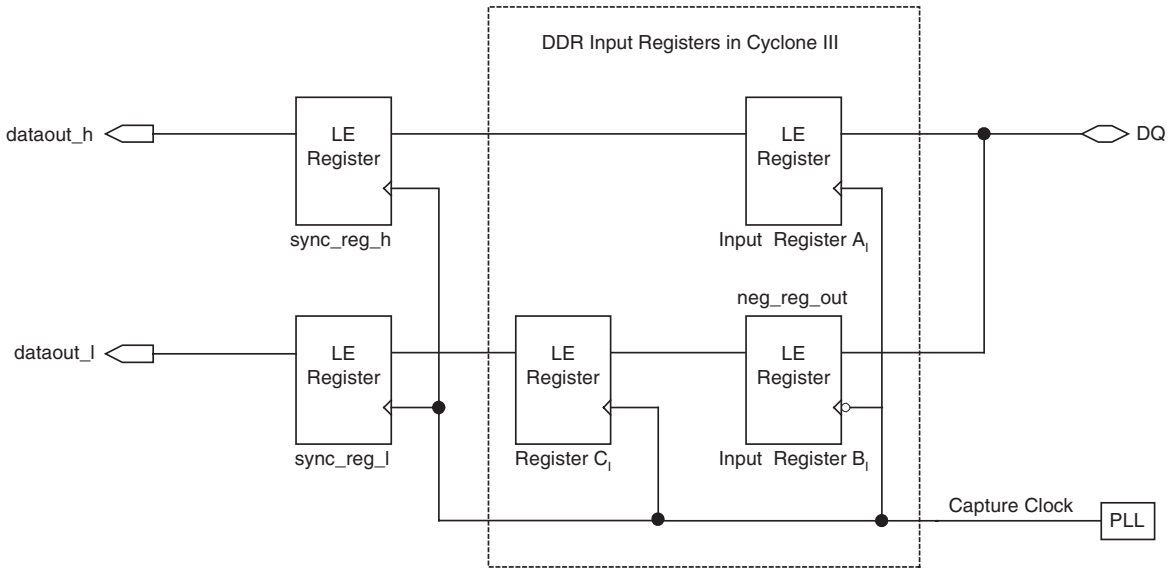
Cyclone III Memory Interfaces Features

In this section, Cyclone III memory interfaces, including DDR input registers, DDR output registers, on-chip termination, and PLLs, are discussed.

DDR Input Registers

The DDR input registers are implemented with three internal logic element (LE) registers for every `DQ` pin. These LE registers are located in the logic array block (LAB) adjacent to the DDR input pin. Figure 9–6 illustrates the Cyclone III DDR input registers.

Figure 9–6. Cyclone III DDR Input Registers



The DDR data is first fed to two registers, input register A_I and input register B_I.

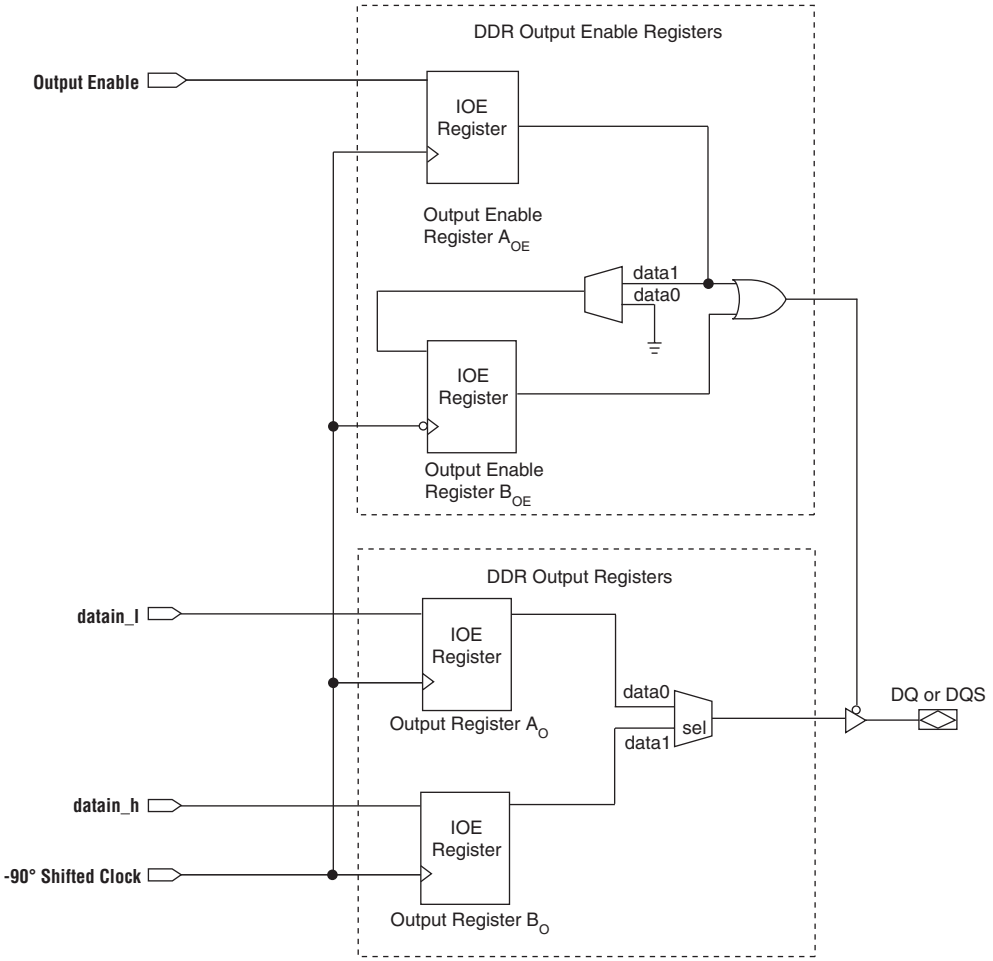
- Input register A_I captures the DDR data present during the rising edge of the clock
- Input register B_I captures the DDR data present during the falling edge of the clock
- Register C_I aligns the data before it is synchronized with the system clock

The sync_reg_h and sync_reg_l registers accept the data from the DDR input registers, then transfer the data to a FIFO to synchronize the two data streams to the rising edge of the system clock. Since the read-capture clock is generated by the PLL, the read-data strobe signal (DQS or CQ) is not used during read in Cyclone III devices. Hence, postamble is not a concern in this case.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths. Figure 9–7 shows how the Cyclone III dedicated write DDIO block is implemented in the IOE registers.

Figure 9–7. Cyclone III Dedicated Write DDIO



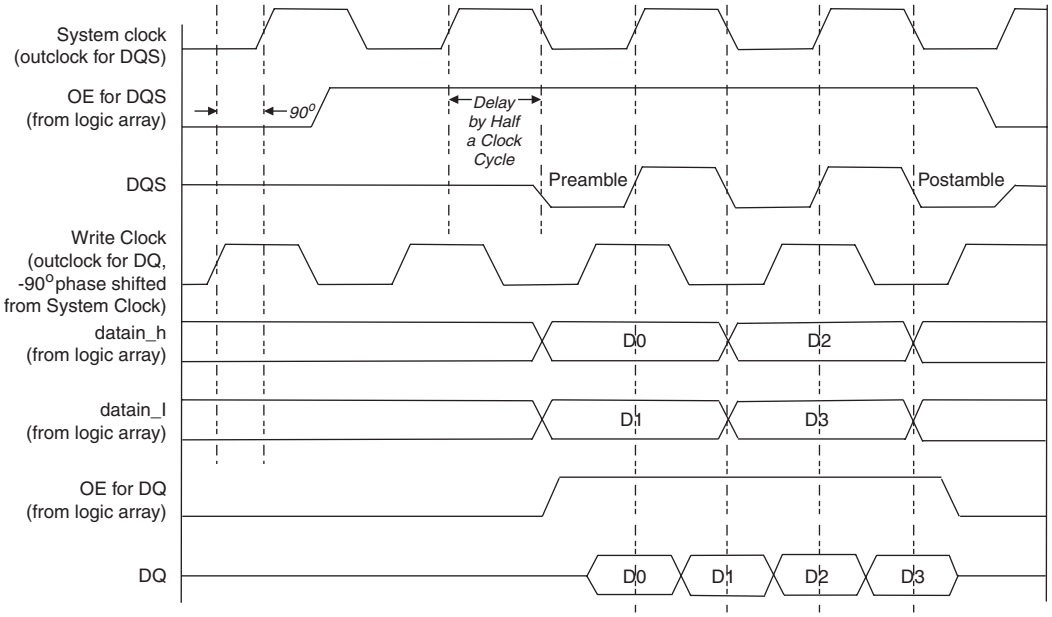
The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through datain_l and datain_h, are fed into two registers, output register A_o and output register B_o, respectively, on the same clock edge. The output from output register A_o is captured on the falling edge of the clock, while the output from output register B_o is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the DQS strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the

pin by half a clock cycle to provide the external memory's DQS write preamble time specification. Figure 9–8 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.

For more information about the Cyclone III IOE registers, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

Figure 9–8. Extending the OE Disable by Half a Clock Cycle for a Write Transaction *Note (1)*



Note to Figure 9–8:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

On-Chip Termination (OCT)

Cyclone III supports calibrated on-chip series termination (OCT R_S) in both vertical and horizontal I/O banks. To use the calibrated OCT, you need to use the R_{UP} and R_{DN} pins for each OCT R_S control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

For more information about the Cyclone III OCT calibration block, refer to the *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by –90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

The PLL is instantiated within the ALTMEMPHY megafunction. All the outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories.

For more information about usage of the PLL outputs by the ALTMEMPHY megafunction, refer to the *ALTMEMPHY Megafunction User Guide*.

For more information about the Cyclone III PLL, refer to the *Clock Networks and PLLs in Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

Conclusion

Cyclone III devices support DDR2 SDRAM, DDR SDRAM, and QDRII SRAM external memory interfaces. The self-calibrating ALTMEMPHY megafunction simplifies the implementation of data paths for different memory interfaces and dynamically calibrates out the process, voltage, and temperature variations in Cyclone III devices and external memory devices without interrupting normal operation.

Cyclone III allows a transfer data rate between external memory interfaces of up to 200 MHz/400 Mbps for DDR2 SDRAM, 167 MHz/333 Mbps for DDR SDRAM, and 167 MHz/667 Mbps for QDRII SRAM devices. Cyclone III devices also offer dedicated write DDIO registers to improve the output duty cycle and provide a better write margin.

Referenced Documents

This chapter references the following documents:

- *ALTMEMPHY Megafunction User Guide*
- *DDR and DDR2 SDRAM Controller Compiler User Guide*
- *AN 445: Design Guidelines for Implementing DDR & DDR2 SDRAM Interfaces in Cyclone III Devices*
- *AN 438: Constraining and Analyzing Timing for External Memory Interfaces in Stratix III and Cyclone III Devices*
- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Logic Elements and Logic Array Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *MultiTrack Interconnect* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Memory Blocks* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Clock Networks and PLLs* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*

Document Revision History

Table 9–5 shows the revision history for this document.

Table 9–5. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "Data and Data Clock/Strobe Pins" section. • Updated Table 9–4. • Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release.	—

Section 3. Configuration, Hot Socketing, Remote Upgrades, and SEU Mitigation

This section includes the following chapters:

- Chapter 10, Configuring Cyclone III Devices
- Chapter 11, Hot Socketing and Power-On Reset in Cyclone III Devices
- Chapter 12, Remote System Upgrade With Cyclone III Devices
- Chapter 13, SEU Mitigation in Cyclone III Devices
- Chapter 14, IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

10. Configuring Cyclone III Devices

CIII51010-1.1

Introduction

Cyclone® III devices use SRAM cells to store configuration data. Because SRAM memory is volatile, configuration data must be downloaded to Cyclone III devices each time the device powers up. Depending on device densities or package options, Cyclone III devices can be configured using one of five configuration schemes:

- Active serial (AS)
- Active parallel (AP)
- Passive serial (PS)
- Fast passive parallel (FPP)
- Joint Test Action Group (JTAG)

AS and AP schemes use an external flash memory, such as a serial configuration device or a supported flash memory, respectively. PS, FPP, and JTAG schemes use either an external controller (for example, a MAX® II device or microprocessor), or a download cable. When used in a multi-device configuration scheme for PS and FPP, the external controller for the slave Cyclone III device is a master Cyclone III device set in the AS and AP mode, respectively. Refer to the "Configuration Features" on page 10–4 for more information.

In some applications, it may be necessary for a device to wake up very quickly to begin operation. Cyclone III devices offer the Fast-On feature for fast power-on reset (POR) time to support fast wake-up time applications such as in the automotive market. Cyclone III devices support a new configuration scheme, such as the AP scheme, which uses commodity parallel flash as configuration memory without the need for an external host which lowers system costs and offers fast configuration time. Additionally, Cyclone III devices can receive a compressed configuration bitstream and decompress the data in real-time, reducing storage requirements and configuration time. Furthermore, Cyclone III devices support remote system upgrade in the active configuration modes. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

This chapter explains the Cyclone III device configuration features and describes how to configure Cyclone III devices using the supported configuration schemes. This chapter also includes configuration pin descriptions and the Cyclone III device configuration file formats. In this chapter, the generic term "device" includes all Cyclone III devices.

This chapter contains the following sections:

- "Configuration Features" on page 10–4
- "Configuration Requirements" on page 10–7
- "Active Serial Configuration (Serial Configuration Devices)" on page 10–9
- "Active Parallel Configuration (Supported Flash Memories)" on page 10–19
- "Passive Serial Configuration" on page 10–30
- "Fast Passive Parallel Configuration" on page 10–41
- "JTAG Configuration" on page 10–47
- "Cyclone III JTAG Instructions" on page 10–59
- "Device Configuration Pins" on page 10–63

Configuration Devices

The Altera® serial configuration devices (EPCS64, EPCS16, and EPCS4) are used in the AS configuration scheme for Cyclone III devices. Serial configuration devices offer a low-cost, low-pin count configuration solution.

For information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

In the AP configuration scheme, the commodity parallel flash is used as configuration memory.

For information about the supported families for the commodity parallel flash, refer to Table 10–9 on page 10–20.

Configuration Schemes

A configuration scheme with different configuration voltage standards is selected by driving the Cyclone III device's MSEL pins either high or low as shown in Table 10–1. The MSEL pins are powered by the V_{CCINT} power supply of the bank in which they reside. The MSEL[3..0] pins have 5-kΩ internal pull-down resistors that are always active.

To avoid any problems with detecting an incorrect configuration scheme, hard-wire the MSEL pins to V_{CCA} or GND without any pull-up or pull-down resistors. Do not drive the MSEL pins with a microprocessor or another device.

Table 10–1. Cyclone III Configuration Schemes

Configuration Scheme	MSEL3 *(10)*	MSEL2	MSEL1	MSEL0	Configuration Voltage Standard *(9)*
Passive Serial Standard (PS Standard POR) *(6)*	0	0	0	0	3.3/2.5 V *(11)*
Active Serial Standard (AS Standard POR) *(1)*, *(5)*, *(6)*	0	0	1	0	3.3 V *(11)*
Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)*	0	1	0	1	3.3 V *(11)*
Active Parallel ×16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)*	0	1	1	0	1.8 V
Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)*	0	1	1	1	3.3 V *(11)*
Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)*	1	0	0	0	1.8 V
Active Parallel ×16 (AP Standard POR) *(1)*, *(2)*, *(3)*	1	0	1	1	3.0/2.5 V *(11)*
Passive Serial Fast (PS Fast POR) *(6)*	1	1	0	0	3.3/2.5 V *(11)*
Active Serial Fast (AS Fast POR) *(1)*, *(5)*, *(6)*	1	1	0	1	3.3 V *(11)*
Fast Passive Parallel Fast (FPP Fast POR) *(4)*	1	1	1	0	3.3/2.5 V *(11)*
Fast Passive Parallel Fast (FPP Fast POR) *(4)*	1	1	1	1	1.8/1.5 V
JTAG-based configuration *(8)*	*(7)*	*(7)*	*(7)*	*(7)*	—

Notes to Table 10–1:

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using remote system upgrade feature. You can enable of disable the remote update mode with an option setting in the Quartus® II software. For more information about remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

(2) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme. For more information, refer to Table 10–2.

(3) In the AP configuration scheme, the commodity parallel flash is used as configuration memory. For information about the supported families for the commodity parallel flash, refer to Table 10–9 on page 10–20.

(4) Some of the smaller Cyclone III devices or package options do not support the FPP configuration scheme. For more information, refer to Table 10–2.

(5) The EPCS16 and EPCS64 devices support up to a 40 MHz DCLK and are supported in Cyclone III devices. Existing batches of EPCS4 manufactured on 0.15 µ process geometry supports up to a 40 MHz DCLK and are supported in Cyclone III devices. However, batches of EPCS4 manufactured on 0.18 µ process geometry does not support AS configuration in Cyclone III devices. For information about product traceability and transition date to differentiate between supported and non-supported EPCS4 serial configuration devices, refer to *PCN 0514 Manufacturing Changes on EPCS Family* process change notification. For information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

(6) These schemes support data decompression.

(7) Do not leave the MSEL pins floating. Connect them to V_{CCA} or GND. These pins support the non-JTAG configuration scheme used in production. If only JTAG configuration is used, you should connect the MSEL pins to GND.

(8) JTAG-based configuration takes precedence over other configuration schemes, which means MSEL pin settings are ignored.

(9) Configuration voltage standard applied to V_{CCIO}.

(10) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2.

(11) You must follow specific requirements when interfacing Cyclone III devices with 2.5 V/3.0 V/3.3 V configuration voltage standards. For information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 10–8.

In Cyclone III devices, the supported configuration schemes differ for different device densities and package options. Table 10–2 shows the supported configuration schemes across device densities and package options.

Table 10–2. Cyclone III Devices Supported Configuration Schemes Across Device Densities and Package Options Note (1)

Device	Package Options (4)							
	E144	Q240	F256	F324	F484	F780	U256	U484
EP3C5	AS, PS, JTAG (2)	—	AS, PS, FPP, JTAG (2)	—	—	—	AS, PS, FPP, JTAG (2)	—
EP3C10	AS, PS, JTAG (2)	—	AS, PS, FPP, JTAG (2)	—	—	—	AS, PS, FPP, JTAG (2)	—
EP3C16	AS, PS, JTAG (2)	AS, PS, FPP, JTAG (2)	AS, PS, FPP, JTAG (2)	—	AS, PS, FPP, AP, JTAG (3)	—	AS, PS, FPP, JTAG (2)	AS, PS, FPP, AP, JTAG (3)
EP3C25	AS, PS, JTAG (2)	AS, PS, FPP, JTAG (2)	AS, PS, FPP, JTAG (2)	AS, PS, FPP, AP, JTAG (3)	—	—	AS, PS, FPP, JTAG (2)	—
EP3C40	—	AS, PS, FPP, JTAG (2)	—	AS, PS, FPP, AP, JTAG (3)	AS, PS, FPP, AP, JTAG (3)	AS, PS, FPP, AP, JTAG (3), (5)	—	AS, PS, FPP, AP, JTAG (3)
EP3C55	—	—	—	—	AS, PS, FPP, AP, JTAG (3)	AS, PS, FPP, AP, JTAG (3)	—	AS, PS, FPP, AP, JTAG (3)
EP3C80	—	—	—	—	AS, PS, FPP, AP, JTAG (3)	AS, PS, FPP, AP, JTAG (3)	—	AS, PS, FPP, AP, JTAG (3)
EP3C120	—	—	—	—	AS, PS, FPP, AP, JTAG (3)	AS, PS, FPP, AP, JTAG (3)	—	—

Notes to Table 10–2:

(1) AS is active serial, PS is passive serial, FPP is fast passive parallel, and AP is active parallel.
(2) These packages do not support AP configuration scheme and do not have the `MSEL[3]` pin.
(3) These packages support all the configuration schemes shown in Table 10–9 on page 10–20.
(4) For information about vertical package migration and package options for Cyclone III devices, refer to the *Cyclone III FPGA Device Family Overview* chapter and the *Package Information for Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.
(5) EP3C40 package option F780 only partially supports vertical package migration to other F780 package options.

For information about vertical package migration and package options for Cyclone III devices, refer to the *Cyclone III FPGA Device Family Overview* chapter and the *Package Information for Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

Cyclone III devices offer decompression and remote system upgrade features. Cyclone III devices can receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. Data decompression is supported in AS and PS configuration schemes. You can make real-time system upgrades from remote locations of your Cyclone III designs with the remote system upgrade feature. Remote update is supported in AS and AP configuration schemes.

Configuration File Format

Table 10–3 shows the approximate uncompressed configuration file sizes for Cyclone III devices. To calculate the amount of storage space required for multiple device configurations, add the file size of each device together.

Table 10–3. Cyclone III Uncompressed Raw Binary File Sizes Notes (1), (2) (Part 1 of 2)

Device	Data Size (Mbits)
EP3C5	3.5
EP3C10	3.5

Table 10–3. Cyclone III Uncompressed Raw Binary File Sizes Notes (1), (2) (Part 2 of 2)

Device	Data Size (Mbits)
EP3C16	4.5
EP3C25	6.5
EP3C40	10.5
EP3C55	16.0
EP3C80	21.0
EP3C120	30.5

Notes to Table 10–3:
(1) These values are preliminary.
(2) Raw Binary File (**.rbf**)

Use the data in Table 10–3 only to estimate the file size before design compilation. Different configuration file formats, such as a Hexidecimal (**.hex**) or Tabular Text File (**.ttf**) formats, have different file sizes. However, for any specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio is dependent on the design.

For more information about setting device configuration options or creating configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

Configuration Features

Cyclone III devices offer configuration data decompression to reduce configuration file storage and remote system upgrade to allow for remotely updating your Cyclone III designs. Table 10–4 summarizes which configuration features you can use in each configuration scheme.

Table 10–4. Cyclone III Configuration Features Note (2)

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade *(2)*
Active Serial Fast (AS Fast POR)	Serial Configuration Device	✓	✓
Active Serial Standard (AS Standard POR)	Serial Configuration Device	✓	✓
Active Parallel x16 Fast (AP Fast POR)	Supported flash memory *(1)*	—	✓
Active Parallel x16 (AP Standard POR)	Supported flash memory *(1)*	—	✓
Passive Serial Fast (PS Fast POR)	MAX II device or a Microprocessor with flash memory	✓	—
	Download cable	✓	—
Passive Serial Standard (PS Standard POR)	MAX II device or a Microprocessor with flash memory	✓	—
	Download cable	✓	—
Fast Passive Parallel Fast (FPP Fast POR)	MAX II device or a Microprocessor with flash memory	—	—
JTAG-based configuration	MAX II device or a Microprocessor with flash memory	—	—
	Download cable	—	—

Notes to Table 10–4:
(1) For information about the supported families for the Intel commodity parallel flash, refer to Table 10–9 on page 10–20.
(2) Remote update mode is supported when using remote system upgrade feature. You can enable or disable the remote update mode with an option setting in the Quartus II software. For more information about remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

Configuration Data Decompression

Cyclone III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Cyclone III devices. During configuration, Cyclone III devices decompress the bitstream in real time and programs its SRAM cells.

Preliminary data indicates that compression typically reduces configuration bitstream size by 35 to 55%.

Cyclone III devices support decompression in the AS and PS configuration schemes. Decompression is not supported in the AP configuration scheme, FPP configuration scheme, or in JTAG-based configuration.

In PS mode, you should use the Cyclone III decompression feature because sending compressed configuration data reduces configuration time. You should use the Cyclone III decompression feature during AS configuration if you must save configuration memory space in the serial configuration device.

When you enable compression, the Quartus II software generates configuration files with compressed configuration data. This compressed file reduces the storage requirements in the configuration device or flash memory and decreases the time needed to transmit the bitstream to the Cyclone III device. The time required by a Cyclone III device to decompress a configuration file is less than the time needed to transmit the configuration data to the device.

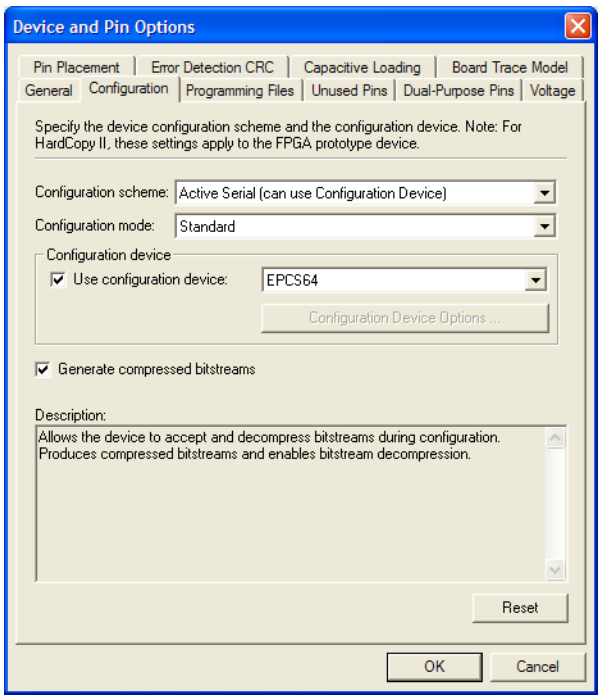
There two methods for enabling compression for Cyclone III bitstreams in the Quartus II software:

- Before design compilation (via the **Compiler Settings** menu)
- After design compilation (via the **Convert Programming Files** window)

To enable compression in the project's compiler settings, perform the following steps in the Quartus II software:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device & Pin Options**. The **Device & Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. Turn on **Generate compressed bitstreams** (Figure 10–1).
5. Click **OK**.
6. In the **Settings** dialog box, click **OK**.

Figure 10–1. Enabling Compression for Cyclone III Bitstreams in Compiler Settings

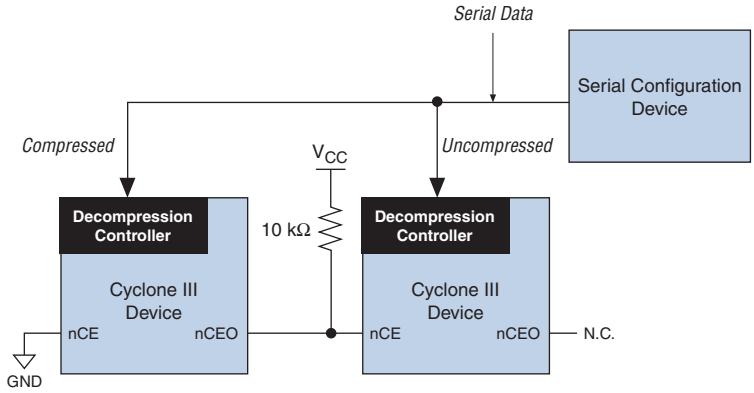


Compression can also be enabled when creating programming files from the **Convert Programming Files** window.

1. On the File menu, click **Convert Programming Files**.
2. Under **Output programming file**, from the drop-down menu, select your desired file type.
3. If you select the Programmer Object File (**.pof**), you must specify a configuration device, directly under the file type.
4. In the **Input files to convert** box, select **SOF Data**.
5. Click **Add File** to browse to the Cyclone III device SRAM Object file or files.
6. On the Convert Programming Files window, select the **.pof** file you added to SOF Data and click **Properties**.
7. On the SOF File Properties dialog box, turn on **Compression**.

When multiple Cyclone III devices are cascaded, you can selectively enable the compression feature for each device in the chain. Figure 10–2 depicts a chain of two Cyclone III devices. The first Cyclone III device has compression enabled and receives a compressed bitstream from the configuration device. The second Cyclone III device has the compression feature disabled and receives uncompressed data.

Figure 10–2. Compressed and Uncompressed Configuration Data in the Same Configuration File



You can generate programming files for this setup from the **Convert Programming Files** dialog box in the Quartus II software, from the File menu.

Remote System Upgrade

Cyclone III devices support remote update mode when using the remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

Cyclone III devices support remote update in the AS and AP configuration schemes. You can implement remote update in conjunction with real-time decompression of configuration data if you need to save configuration memory space in the serial configuration device with AS configuration.

For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in the *Cyclone III Device Handbook.*

Configuration Requirements

Power-On Reset Circuit

The POR circuit keeps the device in reset state until the power supply voltage levels have stabilized on power-up. Upon power-up, the device does not release `nSTATUS` until V_{CCINT}, V_{CCA}, and V_{CCIO} of banks 1, 6, 7, and 8 are above the device's POR trip point. On power-up, V_{CCINT} and V_{CCA} are monitored for brown-out conditions.

V_{CCA} is the analog power to the PLL.

In Cyclone III devices you can select between a fast POR time or a standard POR time depending on the `MSEL` pin settings. The fast POR time is 3 ms < T_{POR} < 9 ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms which has a lower power ramp rate. In both cases, you can extend the POR time by using an external component to assert the `nSTATUS` pin low. Table 10–5 shows the supported POR times for each configuration scheme.

Table 10–5. Cyclone III Supported Power-On Reset Times Across Configuration Schemes (Part 1 of 2)

Configuration Scheme	Fast POR Time (3 ms < T_{POR} < 9 ms)	Standard POR Time (50 ms < T_{POR} < 200 ms)	Configuration Voltage Standard *(1)*
Passive Serial Standard (PS Standard POR)	—	✓	3.3/2.5 V
Active Serial Standard (AS Standard POR)	—	✓	3.3 V
Active Parallel ×16 Fast (AP Fast POR)	✓	—	3.3 V

Table 10–5. Cyclone III Supported Power-On Reset Times Across Configuration Schemes (Part 2 of 2)

Configuration Scheme	Fast POR Time (3 ms < T_{POR} < 9 ms)	Standard POR Time (50 ms < T_{POR} < 200 ms)	Configuration Voltage Standard *(1)*
Active Parallel × 16 Fast (AP Fast POR)	✓	—	1.8 V
Active Parallel × 16 (AP Standard POR)	—	✓	3.3 V
Active Parallel × 16 (AP Standard POR)	—	✓	1.8 V
Active Parallel × 16 (AP Standard POR)	—	✓	3.0/2.5 V
Passive Serial Fast (PS Fast POR)	✓	—	3.3/2.5 V
Active Serial Fast (AS Fast POR)	✓	—	3.3 V
Fast Passive Parallel Fast (FPP Fast POR)	✓	—	3.3/2.5 V
Fast Passive Parallel Fast (FPP Fast POR)	✓	—	1.8/1.5 V
JTAG-based configuration	*(2)*	*(2)*	—

Notes to Table 10–5:

(1) Configuration voltage standard applied to V_{CCIO}.

(2) JTAG-based configuration takes precedence over other configuration schemes, which means `MSEL` pin settings are ignored. However, the POR time is dependent on the `MSEL` pin settings.

In some applications, it may be necessary for a device to wake up very quickly to begin operation. The Cyclone III device family offers the fast POR time option to support fast wake-up time applications. The fast POR time option has stricter power-up requirements compared to the standard POR time option. You can select either the fast POR option or the standard POR option using the `MSEL` pin settings.

☞ The fast POR time feature in Cyclone III devices is similar to the Fast-On feature in Cyclone II devices designated with an "A" in the ordering code.

☞ The Cyclone III devices' fast wake-up time meets the requirement of common bus standards in automotive applications, such as Media Orientated Systems Transport (MOST) and Controller Area Network (CAN).

For more information about wake-up time and power-on reset circuit, refer to the *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*.

Configuration and JTAG Pin I/O Requirements

Cyclone III devices are manufactured using TSMC's 65-nm low-k dielectric process. Although Cyclone III devices use TSMC 2.5-V transistor technology in I/O buffers, the devices are compatible and able to interface with 2.5 V/3.0 V/3.3 V configuration voltage standards. However, you must follow specific requirements when interfacing Cyclone III devices with 2.5 V/3.0 V/3.3 V configuration voltage standards.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. When using a serial configuration device in the AS configuration scheme, you must connect a 25-Ω series resistor at the near end of the serial configuration device for the `DATA[0]`. When cascading Cyclone III devices in multi-device configuration, you must connect repeater buffers between the Cyclone III master and slave device or devices for `DATA` and `DCLK`. The output resistance of the repeater buffers has to fit the maximum overshoot equation given by: $0.8Z_O \leq R_E \leq 1.8Z_O$

In this equation, Z_O is the transmission line impedence and R_E is the equivalent resistance of the output buffer.

Active Serial Configuration (Serial Configuration Devices)

In the AS configuration scheme, Cyclone III devices are configured using a serial configuration device. These configuration devices are low-cost devices with non-volatile memories that feature a simple four-pin interface and a small form factor. These features make serial configuration devices an ideal low-cost configuration solution.

For more information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* in the *Configuration Handbook*.

In Cyclone III devices, the active master clock frequency runs at a maximum of 40 MHz, and around a typical 30 MHz. Cyclone III devices only work with serial configuration devices that support up to 40 MHz. Existing batches of EPCS4 manufactured on 0.15 µ process geometry supports AS configuration in Cyclone III devices up to 40 MHz. However, batches of EPCS4 manufactured on 0.18 µ process geometry support only up to 20 MHz. EPCS16 and EPCS64 serial configuration devices are not affected.

For information about product traceability and transition date to differentiate between 0.15 µ process geometry and 0.18 µ process geometry EPCS4 serial configuration devices, refer to the *PCN 0514 Manufacturing Changes on EPCS Family* process change notification.

Serial configuration devices provide a serial interface to access configuration data. During device configuration, Cyclone III devices read configuration data via the serial interface, decompress data if necessary, and configure their SRAM cells. This scheme is referred to as the AS configuration scheme because the device controls the configuration interface. This scheme contrasts with the PS configuration scheme, where the external host controls the interface.

The Cyclone III decompression, and remote system upgrade features are available when configuring your Cyclone III device using AS configuration scheme.

Table 10–6 shows the `MSEL` pin settings when using the AS configuration scheme with different configuration voltage standard.

Table 10–6. Cyclone III MSEL Pin Settings for AS Configuration Schemes

Configuration Scheme	MSEL3 *(5)*	MSEL2	MSEL1	MSEL0	Configuration Voltage Standard *(3)*
Active Serial Standard (AS Standard POR) *(1)*, *(2)*	0	0	1	0	3.3 V *(4)*
Active Serial Fast (AS Fast POR) *(1)*, *(2)*	1	1	0	1	3.3 V *(4)*

Notes to Table 10–6:

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade with Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

(2) These schemes support data decompression.

(3) Configuration voltage standard applied to V_{CCIO}.

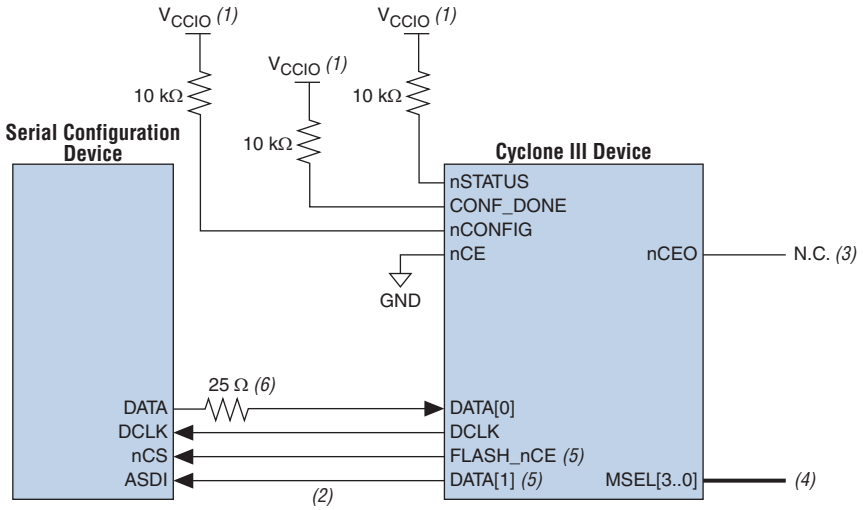
(4) You must follow specific requirements when interfacing Cyclone III devices with 2.5V/3.0V/3.3V configuration voltage standards. For information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 10–8.

(5) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2 on page 10–3.

Single Device AS Configuration

The four-pin interface of serial configuration devices consists of a serial clock input (DCLK), serial data output (DATA), AS data input (ASDI), and an active-low chip select (nCS). This four-pin interface connects to Cyclone III device pins, as shown in Figure 10–3.

Figure 10–3. Single Device AS Configuration



Notes to Figure 10–3:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.
(2) Cyclone III devices use the DATA[1] to ASDI path to control the configuration device.
(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed another device's nCE pin.
(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–6 on page 10–9. Connect the MSEL pins directly to V_{CCA} or GND.
(5) These are dual-purpose I/O pins. FLASH_nCE pin functions as the nCSO pin in AS configuration scheme. DATA[1] pin functions as the ASDO pin in AS configuration scheme.
(6) Connect the series resistor at the near end of the serial configuration device.

When connecting a serial configuration device to the Cyclone III device in single device AS configuration, you must connect a 25 Ω series resistor at the near end of the serial configuration device for the DATA[0].

In single device AS configuration, the board trace length between the serial configuration device to the Cyclone III device should be within a maximum of 10 inches.

Upon power-up, the Cyclone III devices go through a POR. The POR delay is dependent on the MSEL pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast or a standard POR time is available. The fast POR time is 3 ms < T_{POR} < 9ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms, which has a lower power ramp rate. During POR, the device resets, holds nSTATUS and CONF_DONE low, and tri-states all user I/O pins. When the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration can be found in the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. After POR, the Cyclone III devices release nSTATUS, which is pulled high by an external 10-KΩ pull-up resistor, and enters configuration mode.

To begin configuration, power the V_{CCINT}, V_{CCA}, and V_{CCIO} (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

The serial clock (DCLK) generated by the Cyclone III device controls the entire configuration cycle and provides the timing for the serial interface. Cyclone III devices use an internal oscillator to generate DCLK. Cyclone III devices use a 40 MHz oscillator. There is some variation in the internal oscillator frequency because of the process, voltage, and temperature conditions in Cyclone III devices. The internal oscillator is designed such that its maximum frequency is guaranteed to meet EPCS device specifications.

The EPCS1 device does not support any Cyclone III devices because of its insufficient memory capacity.

For information about serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* chapter in volume 2 of the *Configuration Handbook*.

Table 10–7 shows the active serial DCLK output frequency.

Table 10–7. Active Serial DCLK Output Frequency *Note (1)*

Oscillator	Minimum	Typical	Maximum	Units
40 MHz	20	30	40	MHz

Note to Table 10–7:
(1) These values are preliminary.

In AS configuration scheme, the serial configuration device latches input and control signals on the rising edge of DCLK and drives out configuration data on the falling edge. Cyclone III devices drive out control signals on the falling edge of DCLK and latch configuration data on the falling edge of DCLK.

The FLASH_nCE pin and DATA[1] pin are dual-purpose I/O pins. The FLASH_nCE pin functions as the nCSO pin in the AS configuration scheme. The DATA[1] pin functions as the ASDO pin in the AS configuration scheme.

In configuration mode, the Cyclone III device enables the serial configuration device by driving the FLASH_nCE output pin low, which connects to the chip select (nCS) pin of the configuration device. The Cyclone III device uses the serial clock (DCLK) and serial data output (DATA[1]) pins to send operation commands and/or read address signals to the serial configuration device. The configuration device provides data on its serial data output (DATA) pin, which connects to the DATA[0] input of the Cyclone III device.

After all configuration bits are received by the Cyclone III device, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10 KΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic high level. All AS configuration pins (DATA[0], DCLK, FLASH_nCE, and DATA[1]) have weak internal pull-up resistors that are always active. After configuration, these pins are set as input tri-stated and are driven high by the weak internal pull-up resistors. The CONF_DONE pin must have an external 10-KΩ pull-up resistor in order for the device to initialize.

In Cyclone III devices, the initialization clock source is either the 10 MHz (typical) internal oscillator (separate from the active serial internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone III device provides itself with enough clock cycles for proper initialization. The advantage of using the internal oscillator is you do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. Additionally, you can use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. Using the CLKUSR pin allows you to control when your device enters user mode. The device can be delayed from entering user mode for an indefinite amount of time. The **Enable user-supplied start-up clock** (**CLKUSR**) option can be turned on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. When you **Enable** the **user supplied start-up clock** option, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data is accepted and CONF_DONE goes high, Cyclone III devices require 3,185 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR f_{MAX} of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If the INIT_DONE pin is used, it will be high due to an external 10-KΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

If an error occurs during configuration, Cyclone III devices assert the nSTATUS signal low, indicating a data frame error, and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box) is turned on, the Cyclone III device resets the configuration device by pulsing FLASH_nCE, releases nSTATUS after a reset time-out period (maximum of 230 µs), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 500 ns to restart configuration.

When the Cyclone III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin should be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone III device is reset. The Cyclone III device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic high level and nSTATUS is released by the Cyclone III device, reconfiguration begins.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure CLKUSR continues to toggle during the time nSTATUS is low (a maximum of 230 µs).

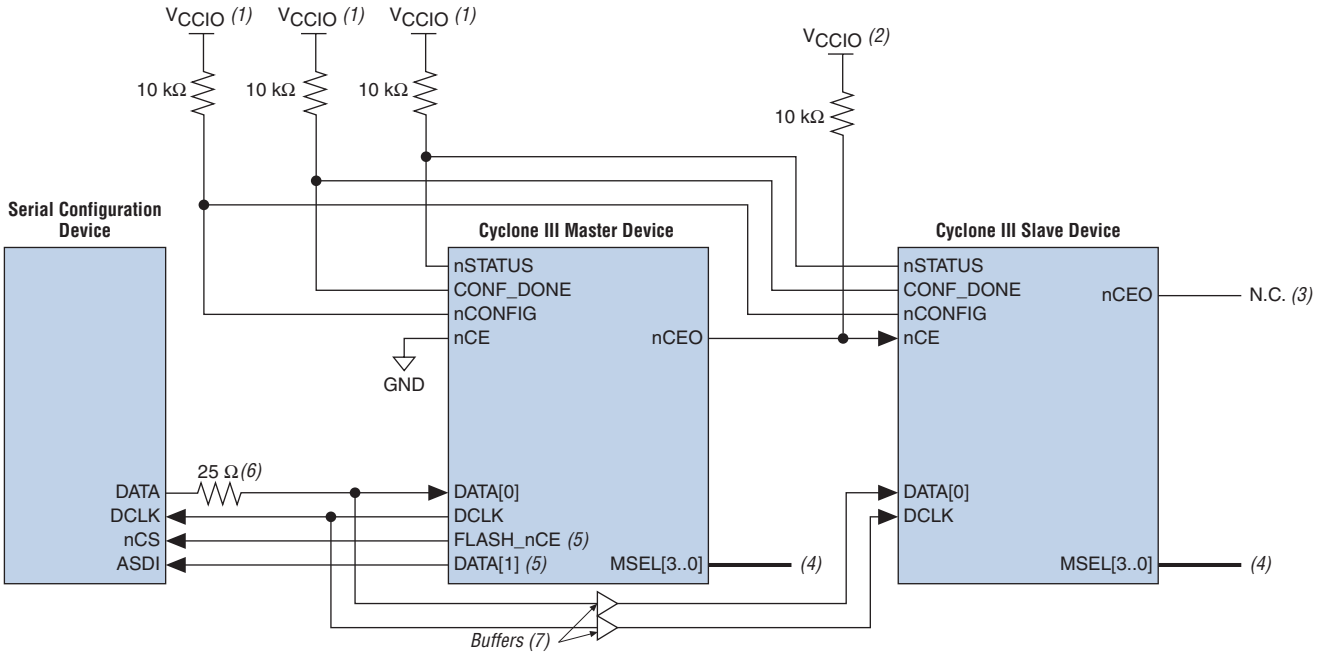
For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site at **www.altera.com**.

Multi-Device AS Configuration

You can configure multiple Cyclone III devices using a single serial configuration device. You can cascade multiple Cyclone III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in chain is a Cyclone III device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, and DATA[0] pins of each device in the chain are connected (refer to Figure 10–4).

This first Cyclone III device in the chain is the configuration master and controls configuration of the entire chain. You must connect its MSEL pins to select the AS configuration scheme. The remaining Cyclone III devices are configuration slaves and you must connect their MSEL pins to select the PS configuration scheme. Any other Altera device that supports PS configuration can also be part of the chain as a configuration slave. Figure 10–4 shows the pin connections for this setup.

Figure 10–4. Multi-Device AS Configuration



Notes to Figure 10–4:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the nCEO pin resides.

(3) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect MSEL[3..0] for the master device in AS mode, refer to Table 10–6 on page 10–9. To connect MSEL[3..0] for the slave devices in PS mode, refer to Table 10–10 on page 10–30. Connect the MSEL pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. FLASH_nCE pin functions as the nCSO pin in AS configuration scheme. DATA[1] pin functions as the ASDO pin in AS configuration scheme.

(6) Connect the series resistor at the near end of the serial configuration device.

(7) Connect the repeater buffers between the Cyclone III master and slave device(s) for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

When connecting a serial configuration device to the Cyclone III device in multi-device AS configuration, you must connect a 25 Ω series resistor at the near end of the serial configuration device for the DATA[0]. Additionally, you must connect the repeater buffers between the Cyclone III master and slave device(s) for DATA[0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

As shown in Figure 10–4, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (a maximum of 230 µs). If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The external system can pulse nCONFIG if it is under system control rather than tied to V_{CCIO}.

While you can cascade Cyclone III devices, serial configuration devices cannot be cascaded or chained together.

If the configuration bitstream size exceeds the capacity of a serial configuration device, you must select a larger configuration device, enable the compression feature or both. When configuring multiple devices, the size of the bitstream is the sum of the individual devices' configuration bitstreams.

Configuring Multiple Cyclone III Devices with the Same Design

Certain designs require you to configure multiple Cyclone III devices with the same design through a configuration bitstream or SOF. You can do this through one of two methods, as described in this section. For both methods, the serial configuration devices cannot be cascaded or chained together.

Multiple SRAM Object Files

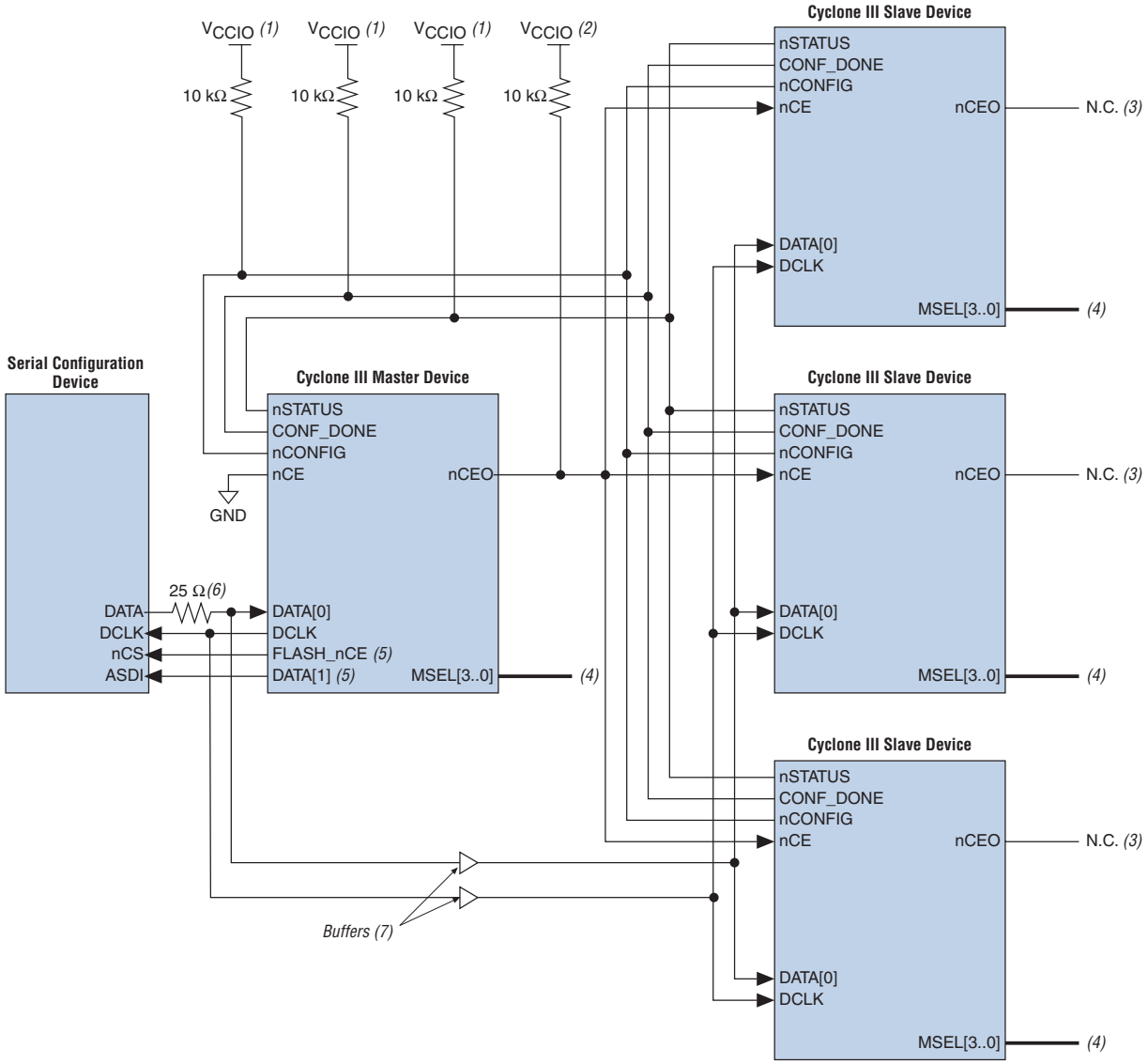
In the first method, two copies of the SRAM Object File (**.sof**) are stored in the serial configuration device. Use the first copy to configure the master Cyclone III device and the second copy to configure all remaining slave devices concurrently. All slave devices must be the same density and package. The setup is similar to Figure 10–4, in which the master is set up in active serial mode and the slave devices are set up in passive serial mode.

To configure four identical Cyclone III devices with the same SRAM Object File, you must set up the chain similar to the example shown in Figure 10–5. The first device is the master device and its MSEL pins should be set to select AS configuration. The other three slave devices are set up for concurrent configuration and its MSEL pins should be set to select PS configuration. The nCEO pin from the master device drives the nCE input pins on all three slave devices, as well as the DATA and DCLK pins connect in parallel to all four devices. During the first configuration cycle, the master device reads its configuration data from the serial configuration device while holding nCEO high. After completing its configuration cycle, the master drives nCE low and transmits the second copy of the configuration data to all three slave devices, configuring them simultaneously.

The advantage of using the setup in Figure 10–5 is that you can have a different SRAM Object File for the Cyclone III master device. However, all the Cyclone III slave devices must be configured with the same SRAM Object File. You can either compress or uncompress the SRAM Object Files in this configuration method.

You can still use this method if the master and slave Cyclone III devices use the same SRAM Object File.

Figure 10–5. Multi-Device AS Configuration in which Devices Receive the Same Data with Multiple SRAM Object Files



Notes to Figure 10–5:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank the pin resides in.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the `nCEO` pin resides.

(3) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect `MSEL[3..0]` for the master device in AS mode, refer to Table 10–6 on page 10–9. To connect `MSEL[3..0]` for the slave devices in PS mode, refer to Table 10–10 on page 10–30. Connect the `MSEL` pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. `FLASH_nCE` pin functions as the `nCSO` pin in AS configuration scheme. `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

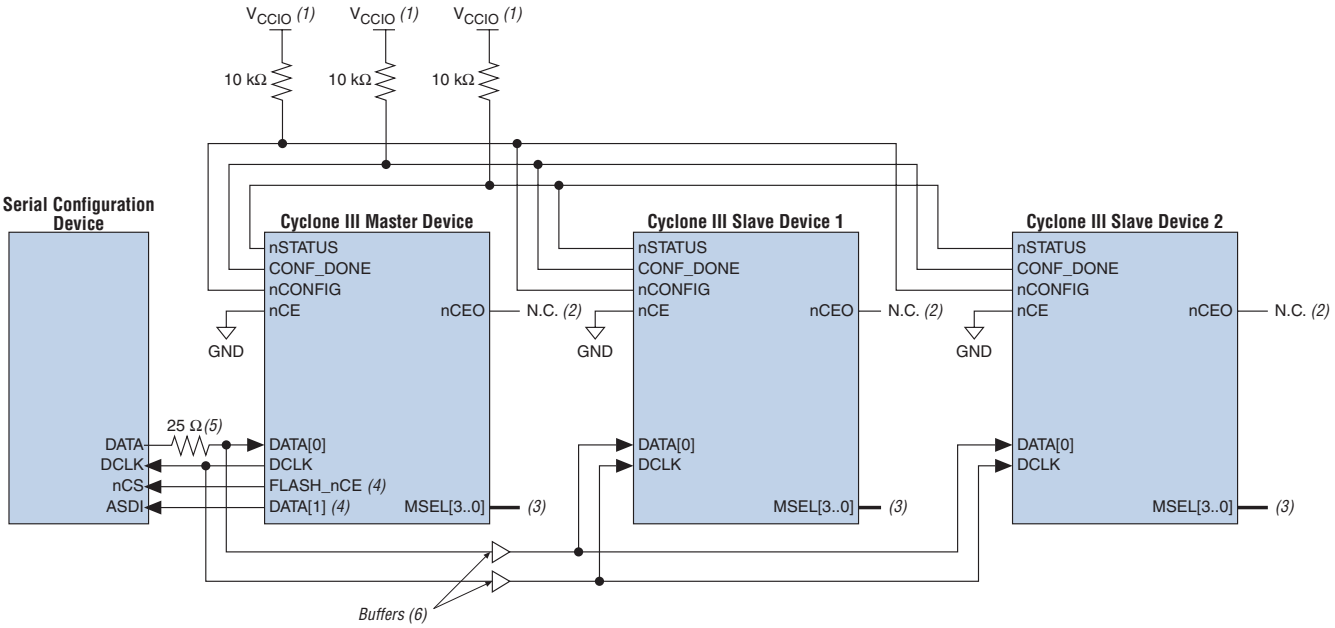
(6) Connect the series resistor at the near end of the serial configuration device.

(7) Connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

Single SRAM Object File

The second method configures both the master and slave Cyclone III devices with the same SRAM Object File. The serial configuration device stores one copy of the SRAM Object File. This setup is shown in Figure 10–6 where the master is setup in AS mode, and the slave devices are setup in PS mode. You must setup one or more slave devices in the chain. All the slave devices must be setup in the same way as shown in Figure 10–6.

Figure 10–6. Multi-Device AS Configuration in which Devices Receive the Same Data with a Single SRAM Object File



Notes to Figure 10–6:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AS mode and the slave devices in PS mode. To connect `MSEL[3..0]` for the master device in AS mode, refer to Table 10–6 on page 10–9. To connect `MSEL[3..0]` for the slave devices in PS mode, refer to Table 10–10 on page 10–30. Connect the `MSEL` pins directly to V_{CCA} or GND.

(4) These are dual-purpose I/O pins. `FLASH_nCE` pin functions as the `nCSO` pin in AS configuration scheme. `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

(5) Connect the series resistor at the near end of the serial configuration device.

(6) Connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

In this setup, all the Cyclone III devices in the chain are connected for concurrent configuration. This can reduce the AS configuration time because all the Cyclone III devices are configured in one configuration cycle. Connect the `nCE` input pins of all the Cyclone III devices to ground. You can either leave the `nCEO` output pins on all the Cyclone III devices unconnected or use the `nCEO` output pins as normal user I/O pins. The `DATA` and `DCLK` pins are connected in parallel to all the Cyclone III devices.

You should put a buffer before the `DATA` and `DCLK` output from the master Cyclone III device to avoid signal strength and signal integrity issues. The buffer should not significantly change the `DATA`-to-`DCLK` relationships or delay them with respect to other AS signals (`ASDI` and `nCS`). Also, the buffer should only drive the slave Cyclone III devices, so that the timing between the master Cyclone III device and serial configuration device is unaffected.

This configuration method supports both compressed and uncompressed SRAM Object Files. Therefore, if the configuration bitstream size exceeds the capacity of a serial configuration device, you can enable the compression feature in the SRAM Object File used or you can select a larger serial configuration device.

Estimating AS Configuration Time

Active serial configuration time is dominated by the time it takes to transfer data from the serial configuration device to the Cyclone III device. This serial interface is clocked by the Cyclone III `DCLK` output (generated from an internal oscillator). As listed in Table 10–7 on page 10–11, the `DCLK` minimum frequency when using the 40-MHz oscillator is 20 MHz (50 ns). Therefore, the maximum configuration time estimate for an EP3C10 device (3,500,000 bits of uncompressed data) is:

(1)
$$\text{RBF Size} \times \left(\frac{\text{maximum DCLK period}}{1\text{ bit}}\right) = \text{estimated maximum configuration time}$$

$$3{,}500{,}000\text{ bits} \times \left(\frac{50\text{ ns}}{1\text{ bit}}\right) = 175\text{ ms}$$

To estimate the typical configuration time, use the typical `DCLK` period as listed in Figure 10–7. With a typical `DCLK` period of 33.33 ns, the typical configuration time is 116.7 ms. Enabling compression reduces the amount of configuration data that is transmitted to the Cyclone III device, which also reduces configuration time. On average, compression reduces configuration time by 50%.

Programming Serial Configuration Devices

Serial configuration devices are non-volatile, flash-memory-based devices. You can program these devices in-system using the USB-Blaster™or ByteBlaster II™ download cable. Alternatively, you can program them using the Altera Programming Unit (APU), supported third-party programmers, or a microprocessor with the SRunner software driver.

You can perform in-system programming of serial configuration devices via the AS programming interface. During in-system programming, the download cable disables device access to the AS interface by driving the `nCE` pin high. Cyclone III devices are also held in reset by a low level on `nCONFIG`. After programming is complete, the download cable releases `nCE` and `nCONFIG`, allowing the pull-down and pull-up resistors to drive GND and V_{CC}, respectively. Figure 10–7 shows the download cable connections to the serial configuration device.

To perform in-system programming of a serial configuration device via the AS programming interface, the diodes and capacitors must be placed as close as possible to the Cyclone III device. You must ensure the diodes and capacitors maintain a maximum AC voltage of 4.1 V (refer to Figure 10–7).

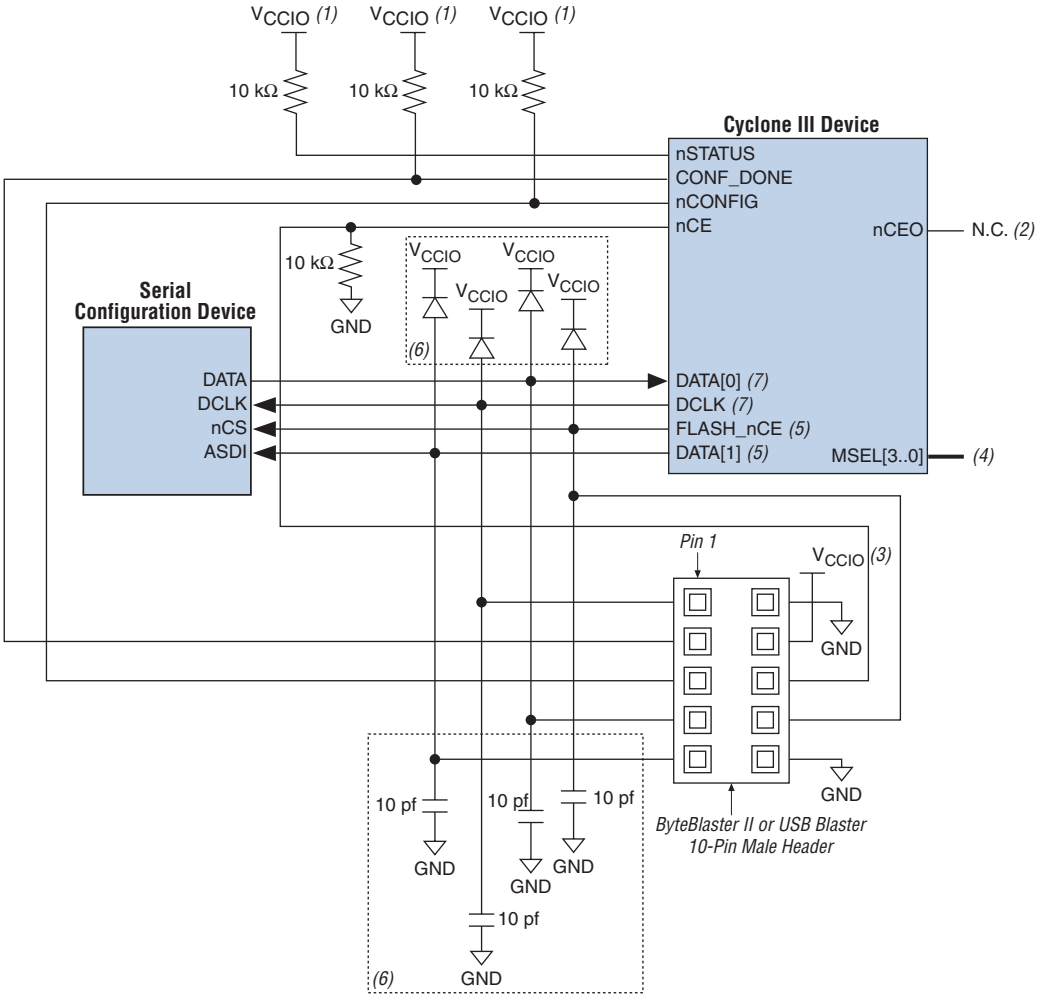
If you wish to use the same setup shown in Figure 10–7 to perform in-system programming of a serial configuration device and single- or multi-device AS configuration, you do not need a series resistor on the DATA line at the near end of the serial configuration device. The existing diodes and capacitors are sufficient.

Altera has developed the Serial FlashLoader (SFL), a JTAG-based in-system programming solution for Altera serial configuration devices. The SFL is a bridge design for the Cyclone III device that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the SFL design.

For more information about implementing the Serial FlashLoader (SFL) with Cyclone III devices, refer to "Programming Serial Configuration Devices In-System Using the JTAG Interface" on page 10–56.

For more information about the USB-Blaster download cable, refer to the *USB-Blaster Download Cable User Guide*. For more information about the ByteBlaster II cable, refer to the *ByteBlaster II Download Cable User Guide*.

Figure 10–7. In-System Programming of Serial Configuration Devices



Notes to Figure 10–7:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(3) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with the V_{CCIO} supply.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6 on page 10–9. Connect the `MSEL` pins directly to V_{CCA} or ground.

(5) These are dual-purpose I/O pins. `FLASH_nCE` pin functions as the `nCSO` pin in AS configuration scheme. `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

(6) The diodes and capacitors must be placed as close as possible to the Cyclone III device. You must ensure the diodes and capacitors maintain a maximum AC voltage of 4.1 V.

(7) When cascading Cyclone III devices in a multi-device AS configuration, connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

You can use the Quartus II software with the APU and the appropriate configuration device programming adapter to program serial configuration devices. All serial configuration devices are offered in an 8- or 16-pin small outline integrated circuit (SOIC) package.

In production environments, serial configuration devices can be programmed using multiple methods. Altera programming hardware or other third-party programming hardware can be used to program blank serial configuration devices before they are mounted onto printed circuit boards (PCBs). Alternatively, you can use an on-board microprocessor to program the serial configuration device in-system by porting the reference C-based software driver provided by Altera (that is, the SRunner software driver).

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming, which can be easily customized to fit in different embedded systems. SRunner is able to read a raw programming data (.**rpd**) file and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time with the Quartus II software.

For more information about SRunner, refer to the *AN 418: SRunner: An Embedded Solution for Serial Configuration Device Programming* application note and the source code on the Altera web site at **www.altera.com**.

For more information about programming serial configuration devices, refer to the *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* in the *Configuration Handbook*.

Active Parallel Configuration (Supported Flash Memories)

Cyclone III devices offer the AP configuration scheme for Altera's devices. In the AP configuration scheme, Cyclone III devices are configured using commodity 16-bit parallel flash memory. These external non-volatile configuration devices are industry standard microprocessor flash memories. The flash memories provide a fast interface to access configuration data. The speedup in configuration time is mainly due to the 16-bit wide parallel data bus which is used to retrieve data from the flash.

Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin. For more information, refer to Table 10–2 on page 10–3.

During device configuration, Cyclone III devices read configuration data via the parallel interface, and configure their SRAM cells. This scheme is referred to as the AP configuration scheme because the device controls the configuration interface. This scheme contrasts with the FPP configuration scheme, where the external host controls the interface.

The Cyclone III remote system upgrade feature is available when you configure your Cyclone III device using the AP configuration scheme.

Table 10–8 shows the MSEL pin settings when using the AP configuration scheme with different configuration voltage standard.

Table 10–8. Cyclone III MSEL Pin Settings for AP Configuration Schemes

Configuration Scheme	MSEL3 *(5)*	MSEL2	MSEL1	MSEL0	Configuration Voltage Standard *(4)*
Active Parallel × 16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)*	0	1	0	1	3.3 V *(6)*
Active Parallel × 16 Fast (AP Fast POR) *(1)*, *(2)*, *(3)*	0	1	1	0	1.8 V
Active Parallel × 16 (AP Standard POR) *(1)*, *(2)*, *(3)*	0	1	1	1	3.3 V *(6)*
Active Parallel × 16 (AP Standard POR) *(1)*, *(2)*, *(3)*	1	0	0	0	1.8 V
Active Parallel × 16 (AP Standard POR) *(1)*, *(2)*, *(3)*	1	0	1	1	3.0/2.5 V *(6)*

Notes to Table 10–8:

(1) These schemes support the remote system upgrade feature. Remote update mode is supported when using remote system upgrade feature. You can enable or disable remote update mode with an option setting in the Quartus II software. For more information about the remote system upgrade feature, refer to the *Remote System Upgrade With Cyclone III Devices* chapter.

(2) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme. For more information, refer to Table 10–2 on page 10–3.

(3) In the AP configuration scheme, the commodity parallel flash is used as configuration memory. For information about the supported families for the commodity parallel flash, refer to Table 10–9 on page 10–20.

(4) Configuration voltage standard applied to V_{CCIO}.

(5) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2 on page 10–3.

(6) You must follow specific requirements when interfacing Cyclone III devices with 2.5V/3.0V/3.3V configuration voltage standards. For information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 10–8.

AP Configuration Supported Flash Memories

The AP configuration controller in Cyclone III devices is designed to interface with the Intel StrataFlash® Embedded Memory P30 flash family and the Intel StrataFlash Embedded Memory P33 flash family, which are two industry standard flash families. Unlike serial configuration devices, both of the flash families supported in AP configuration scheme are designed to interface with microprocessors. By configuring from an industry standard microprocessor flash which allows access to the flash once in user mode, the AP configuration scheme allows you to combine configuration data and user data (microprocessor boot code) on the same flash memory.

The Intel P30 flash family and the P33 flash family are similar because both support a continuous synchronous burst read mode at 40 MHz DCLK frequency for reading data from the flash. Additionally, the Intel P30 and P33 flash families have identical pin-out and adopt similar protocols for data access.

☞ Cyclone III devices use a 40-MHz oscillator for the AP configuration scheme.

Table 10–9 shows the supported families of the commodity parallel flash for the AP configuration scheme.

Table 10–9. Cyclone III Supported Commodity Flash for AP Configuration Schemes *Note (1)*

Flash Memory Density	Intel P30 Flash Family *(2)*	Intel P33 Flash Family *(3)*
64 Mbit	✓	✓
128 Mbit	✓	✓
256 Mbit	✓	✓

Notes to Table 10–9:

(1) The AP configuration scheme only support flash memory speed grades of 40 MHz and above. Therefore, you must refer to the respective flash datasheets to check for the supported speed grades and package options.

(2) 3.3 V, 3.0 V, 2.5 V, and 1.8 V I/O options are supported for Intel P30 flash family.

(3) 3.3 V, 3.0 V, and 2.5 V I/O options are supported for Intel P33 flash family.

AP configuration of Cyclone III devices supports the Intel P30 and P33 family 64 Mbit, 128 Mbit and 256 Mbit flash memories. Configuring Cyclone III devices from the Intel P30 and P33 family 512 Mbit flash memory is possible, but you need to properly drive the extra address and chip select pins as required by these flash memories.

You must refer to the respective flash datasheets to check for the supported speed grades and package options. For example, the Intel P30 and P33 families have only a single speed grade at 40 MHz. However, they do not support 40 MHz on the Thin Small Outline Package (TSOP) . Therefore, the P30 and P33 FBGA packages are supported for the AP configuration scheme while the TSOP packages are not supported.

The AP configuration scheme in Cyclone III devices supports flash speed grades of 40 MHz and above. However, AP configuration for all these speed grades should be capped at 40 MHz. The advantage of the faster speed grades is realized when your design in the Cyclone III devices accesses the flash memory in user mode.

For information about the operation of the Intel StrataFlash Embedded Memory P30 flash memories, search for the keyword "P30" on the Intel web site at **www.intel.com** to obtain the P30 family datasheet.

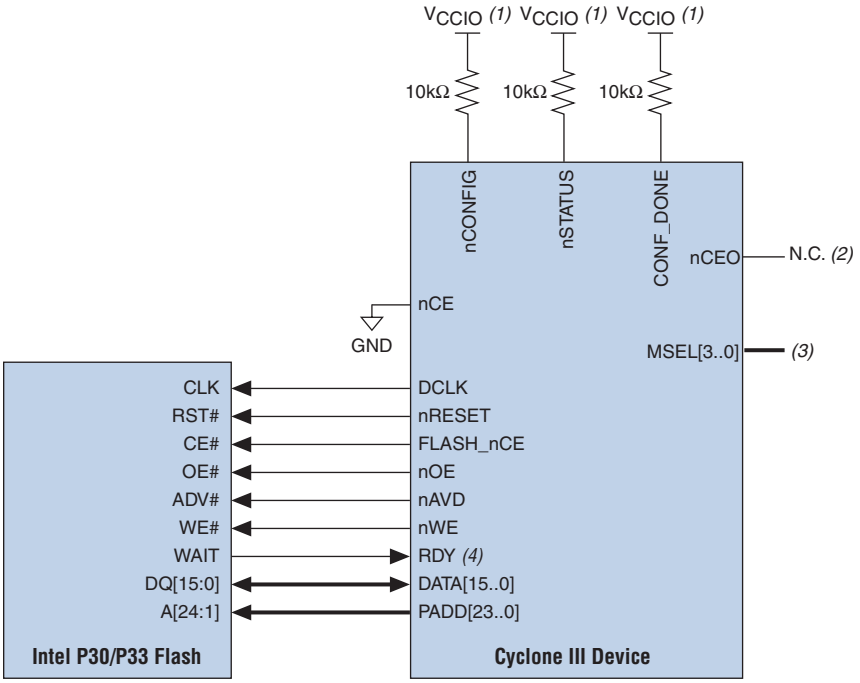
For information about the operation of the Intel StrataFlash Embedded Memory P33 flash memories, search for the keyword "P33" on the Intel web site at **www.intel.com** to obtain the P33 family datasheet.

Single Device AP Configuration

The three groups of interface pins supported in the Intel P30 and P33 flash memories are the control pins, the address pins, and the data pins. In the AP configuration scheme, both of the supported parallel flash memories accept `DCLK`, active-low reset (`RST#`), active-low chip enable (`CE#`), active-low output enable (`OE#`), active-low address valid (`ADV#`), and active-low write enable (`WE#`) as control signals from the Cyclone III device. The supported parallel flash memories output a control signal (`WAIT`) to the Cyclone III device to indicate when synchronous data is ready on the data bus. The Cyclone III device has a 24-bit address bus which connects to the address bus (`A[24:1])` of the flash memory. A 16-bit bidirectional data bus (`DATA[15..0]`) provides data transfer between the Cyclone III device and the flash memory.

The control signals from the Cyclone III device to the flash memory include `DCLK`, `nRESET`, `FLASH_nCE`, `nOE`, `nAVD`, and `nWE`. The interface for the Intel P30 flash memory and the P33 flash memory connects to Cyclone III device pins, as shown in Figure 10–8.

Figure 10–8. Single Device AP Configuration Using Intel P30/P33 Flash Memory



Notes to Figure 10–8:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–8 on page 10–20. Connect the `MSEL` pins directly to V_{CCA} or GND.

(4) The current implementation for AP configuration ignores the `RDY` pin. However, Altera recommends that you connect this pin.

In single device AP configuration, the board trace length between supported parallel flash to the Cyclone III device should be within a maximum of 6 inches.

The default read mode of the supported parallel flash memory is asynchronous, and all writes to the parallel flash memory are asynchronous. Both of the parallel flash families support a synchronous read mode, with data supplied on the positive edge of `DCLK`. `nRESET` is an active-low hard reset, `FLASH_nCE` is an active-low chip enable, `nOE` is an active-low output enable for the `DATA[15..0]` bus and `WAIT` pin, `nAVD` is an active-low address valid signal and is used to write addresses into the flash, and `nWE` is an active-low write enable and is used to write data into the flash. The `PADD[23..0]` bus is the address bus supplied to the flash. The `DATA[15..0]` bus is a bidirectional bus used to supply and read data to and from the flash, with the flash output controlled by `nOE`.

Upon power-up, the Cyclone III devices go through a POR. The POR delay is dependent on the `MSEL` pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < T_{POR} < 9 ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms, which has a lower power ramp rate. During POR, the device resets, holds `nSTATUS` and `CONF_DONE` low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

The value of the weak pull-up resistors on the I/O pins that are on before and during configuration can be found in the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. After POR, the Cyclone III devices release nSTATUS, which is pulled high by an external 10-KΩ pull-up resistor, and enters configuration mode.

☞ To begin configuration, power the V_{CCINT}, V_{CCA}, and V_{CCIO} (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

The serial clock (DCLK) generated by the Cyclone III device controls the entire configuration cycle and provides the timing for the parallel interface. Cyclone III devices use an internal oscillator to generate DCLK. Cyclone III devices use a 40-MHz oscillator for the AP configuration scheme. The oscillator is the same oscillator used in the AS configuration scheme and the active DCLK output frequency is as shown in Table 10–7 on page 10–11.

After all configuration bits are received by the Cyclone III device, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-KΩ resistor. Initialization begins only after the CONF_DONE signal reaches a logic high level. The CONF_DONE pin must have an external 10-KΩ pull-up resistor in order for the device to initialize.

In Cyclone III devices, the initialization clock source is either the 10 MHz (typical) internal oscillator (separate from the active serial internal oscillator) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone III device provides itself with enough clock cycles for proper initialization. You do not need to send additional clock cycles from an external source to the CLKUSR pin during the initialization stage. You can also use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. Using the CLKUSR pin allows you to control when your device enters user mode. The device can be delayed from entering user mode for an indefinite amount of time. The **Enable user-supplied start-up clock (CLKUSR)** option can be turned on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. When you click **Enable user-supplied start-up clock (CLKUSR)**, the CLKUSR pin is the initialization clock source. Supplying a clock on CLKUSR does not affect the configuration process. After all configuration data has been accepted and CONF_DONE goes high, Cyclone III devices require 3,185 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR f_{MAX} of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If the INIT_DONE pin is used, it will be high due to an external 10-KΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. This low-to-high transition signals that the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

If an error occurs during configuration, Cyclone III devices assert the nSTATUS signal low, indicating a data frame error, and the CONF_DONE signal stays low. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box) is turned on, the Cyclone III device resets the configuration device by pulsing FLASH_nCE, releases nSTATUS after a reset time-out period (maximum of 230 µs), and retries configuration. If this option is turned off, the system must monitor nSTATUS for errors and then pulse nCONFIG low for at least 500 ns to restart configuration.

When the Cyclone III device is in user mode, you can initiate reconfiguration by pulling the nCONFIG pin low. The nCONFIG pin should be low for at least 500 ns. When nCONFIG is pulled low, the Cyclone III device is reset. The Cyclone III device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic high level and nSTATUS is released by the Cyclone III device, reconfiguration begins.

If you use the optional CLKUSR pin and the nCONFIG pin is pulled low to restart configuration during device initialization, ensure CLKUSR continues to toggle during the time nSTATUS is low (a maximum of 230 µs).

For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site (**www.altera.com**).

Multi-Device AP Configuration

You can configure multiple Cyclone III devices using a single parallel flash. You can cascade multiple Cyclone III devices using the chip-enable (nCE) and chip-enable-out (nCEO) pins. The first device in the chain must have its nCE pin connected to GND. You must connect its nCEO pin to the nCE pin of the next device in the chain. Use an external 10-kΩ pull-up resistor to pull the nCEO signal high to its V_{CCIO} level to help the internal weak pull-up resistor. When the first device captures all of its configuration data from the bitstream, it drives the nCEO pin low, enabling the next device in the chain. You can leave the nCEO pin of the last device unconnected or use it as a user I/O pin after configuration if the last device in the chain is a Cyclone III device. The nCONFIG, nSTATUS, CONF_DONE, DCLK, DATA[15..8], and DATA[7..0] pins of each device in the chain are connected (refer to Figure 10–9 on page 10–25 and Figure 10–10 on page 10–26).

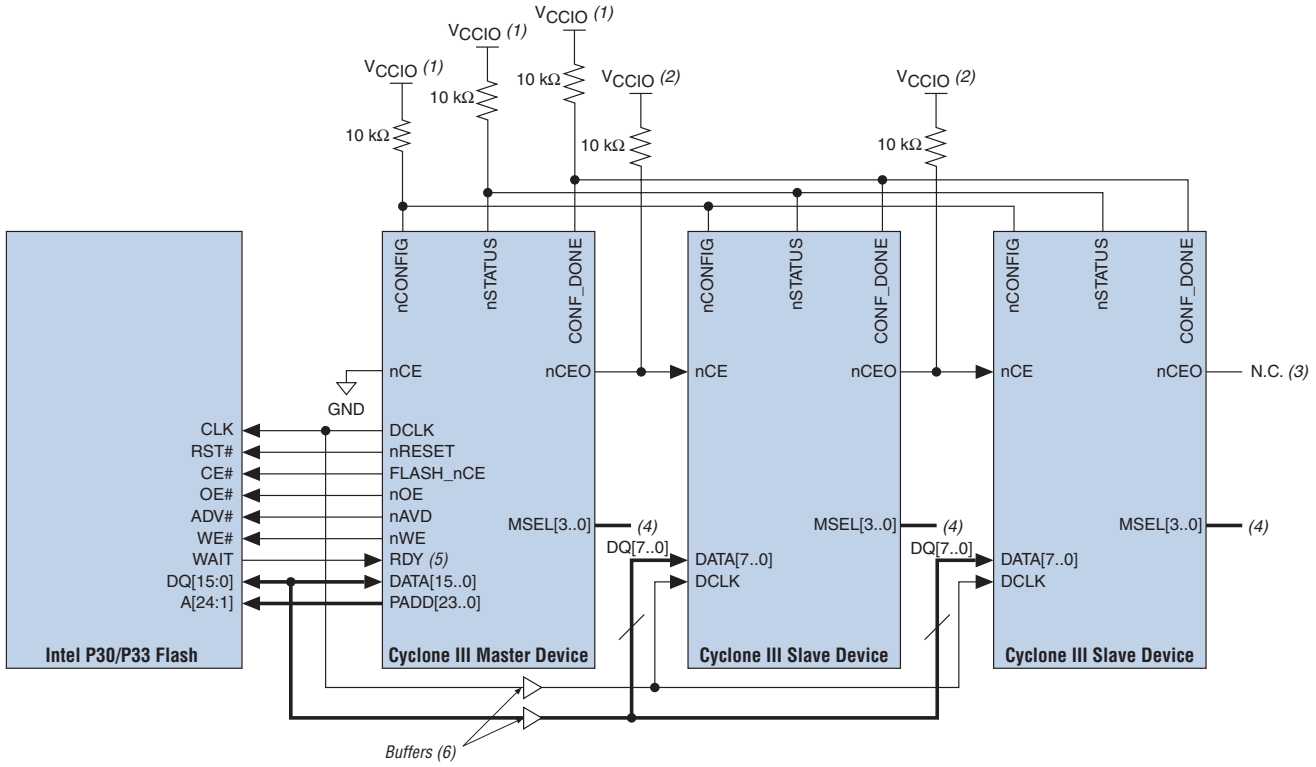
This first Cyclone III device in the chain as shown in Figure 10–9 and Figure 10–10 is the configuration master and controls configuration of the entire chain. You must connect its MSEL pins to select the AP configuration scheme. The remaining Cyclone III devices are configuration slaves and you must connect their MSEL pins to select the FPP configuration scheme. Any other Altera device that supports FPP configuration can also be part of the chain as a configuration slave.

The two configurations for the DATA[15..0] bus in multi-device AP configuration are the byte-wide multi-device AP configuration and the word-wide multi-device AP configuration.

Byte-Wide Multi-Device AP Configuration

The first method is the byte-wide multi-device AP configuration and is the simpler form. In the byte-wide multi-device AP configuration, the least significant byte DATA[7..0] from the flash and master device set to AP configuration scheme is connected to each of the slave devices set to FPP configuration scheme, as shown in Figure 10–9.

Figure 10–9. Byte-Wide Multi-Device AP Configuration



Notes to Figure 10–9:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the `nCEO` pin resides.

(3) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AP mode and the slave devices in FPP mode. To connect `MSEL[3..0]` for the master device in AP mode, refer to Table 10–8 on page 10–20. To connect `MSEL[3..0]` for the slave devices in FPP mode, refer to Table 10–12 on page 10–41. Connect the `MSEL` pins directly to V_{CCA} or GND.

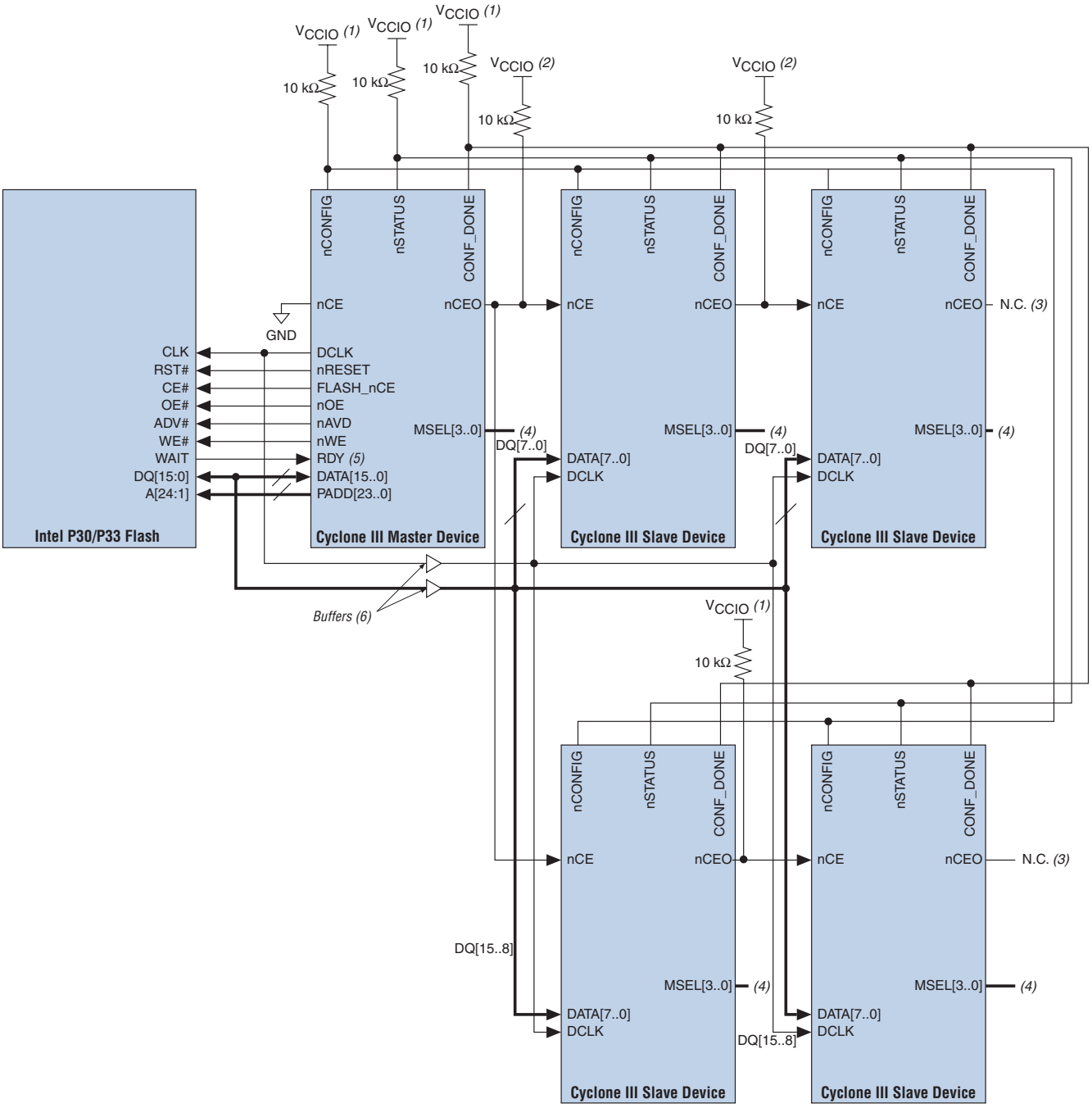
(5) The current implementation for AP configuration ignores the `RDY` pin. Altera recommends, however, that you connect this pin.

(6) Connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[15..0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

Word-Wide Multi-Device AP Configuration

The more efficient setup is one in which some of the slave devices are connected to the least significant byte `DATA[7..0]` and the remaining slave devices are connected to the most significant byte `DATA[15..8]`. In the word-wide multi-device AP configuration, the `nCEO` pin of the master device enables two separate daisy-chains of slave devices, allowing both chains to be programmed concurrently, as shown in Figure 10–10.

Figure 10–10. Word-Wide Multi-Device AP Configuration



Notes to Figure 10–10:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the `nCEO` pin resides.

(3) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. You must set the Cyclone III master device in AP mode and the slave devices in FPP mode. To connect `MSEL[3..0]` for the master device in AP mode, refer to Table 10–8 on page 10–20. To connect `MSEL[3..0]` for the slave devices in FPP mode, refer to Table 10–12 on page 10–41. Connect the `MSEL` pins directly to V_{CCA} or GND.

(5) Currently, the `RDY` pin does not listen during configuration. Altera recommends, however, that you connect this pin.

(6) Connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[15..0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

In multi-device AP configuration, the board trace length between the parallel flash to the master Cyclone III device should be within maximum of 6 inches. Additionally, you must connect the repeater buffers between the Cyclone III master and slave device(s) for DATA[15..0] and DCLK. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

As shown in Figure 10–9 and Figure 10–10, the nSTATUS and CONF_DONE pins on all target devices are connected together with external pull-up resistors. These pins are open-drain bidirectional pins on the devices. When the first device asserts nCEO (after receiving all of its configuration data), it releases its CONF_DONE pin. However, the subsequent devices in the chain keep this shared CONF_DONE line low until they have received their configuration data. When all target devices in the chain have received their configuration data and have released CONF_DONE, the pull-up resistor drives a high level on this line and all devices simultaneously enter initialization mode.

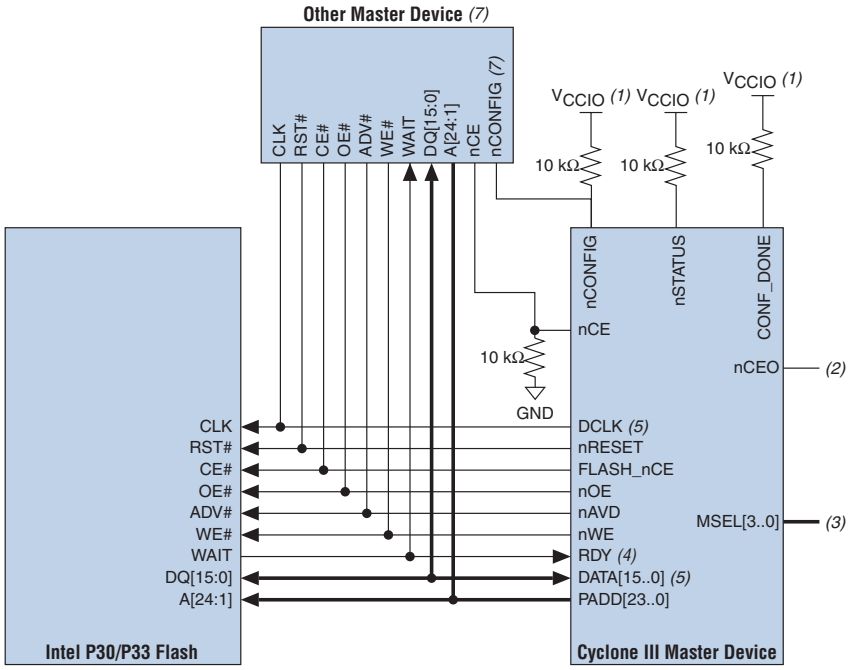
If an error occurs at any point during configuration, the nSTATUS line is driven low by the failing device. If you enable the **Auto-restart configuration after error** option, reconfiguration of the entire chain begins after a reset time-out period (a maximum of 230 µs). If the **Auto-restart configuration after error** option is turned off, the external system must monitor nSTATUS for errors and then pulse nCONFIG low to restart configuration. The external system can pulse nCONFIG if it is under system control rather than tied to V_{CCIO}.

Configuring With Multiple Bus Masters

Similar to AS configuration scheme, AP configuration scheme supports multiple bus masters for the parallel flash. For another master to take control of the AP configuration bus, it must assert nCONFIG low for at least 500 ns to reset the master Cyclone III device and override the weak 10 kΩ pull-down resistor on the nCE pin. This resets the master Cyclone III device and causes it to tri-state its AP configuration bus. The other master then takes control of the AP configuration bus. Once the other master is done, it must release the AP configuration bus, then release the nCE pin, and finally pulse nCONFIG low to restart configuration.

In the AP configuration scheme, multiple masters can share the parallel flash. Similar to the AS configuration scheme, the bus control is negotiated by the nCE pin. The AP configuration with multiple bus masters is shown in Figure 10–11.

Figure 10–11. AP Configuration with Multiple Bus Masters



Notes to Figure 10–11:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed another device's `nCE` pin.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–8 on page 10–20. Connect the `MSEL` pins directly to V_{CCA} or GND.

(4) The current implementation for AP configuration ignores the `RDY` pin. Altera recommends, however, that you connect this pin.

(5) When cascading Cyclone III devices in a multi-device AP configuration, connect the repeater buffers between the Cyclone III master and slave device(s) for `DATA[15..0]` and `DCLK`. All I/O inputs must maintain a maximum AC voltage of 4.1 V. The output resistance of the repeater buffers has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

(6) The other master device must fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

(7) The other master device can pulse `nCONFIG` if it is under system control rather than tied to V_{CCIO}.

Estimating AP Configuration Time

Active parallel configuration time is dominated by the time it takes to transfer data from the parallel flash to the Cyclone III device. This parallel interface is clocked by the Cyclone III `DCLK` output (generated from an internal oscillator). As listed in Table 10–7 on page 10–11, the `DCLK` minimum frequency when using the 40-MHz oscillator is 20MHz (50 ns). In the word-wide cascade programming, the `DATA[15..0]` bus transfers a 16-bit word and essentially cuts configuration time to approximately 1/16 that of the AS configuration time. Therefore, the maximum configuration time estimate for an EP3C10 device (3,500,000 bits of uncompressed data) is:

(2)
$$\text{RBF Size} \times \left(\frac{\text{maximum DCLK period}}{\text{16 bits per DCLK cycle}}\right) = \text{estimated maximum configuration time}$$

$$3{,}500{,}000 \text{ bits} \times \left(\frac{50 \text{ ns}}{16 \text{ bits}}\right) = 10.9 \text{ ms}$$

To estimate the typical configuration time, use the typical `DCLK` period as listed in Table 10–7 on page 10–11. With a typical `DCLK` period of 33.33 ns, the typical configuration time is 7.3 ms.

Programming Parallel Flash Memories

The supported parallel flash memories are external non-volatile configuration devices. They are industry standard microprocessor flash memories.

For information about the supported families for the commodity parallel flash, refer to Table 10–9 on page 10–20.

Cyclone III devices in a single device chain or in a multiple device chain support in-system programming of a parallel flash using the JTAG interface via the flash loader megafunction. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone III device to program the parallel flash in system, even if the host or download cable cannot access the parallel flash's configuration pins.

For more information about the Cyclone III parallel flash loader megafunction, contact Altera Technical Support.

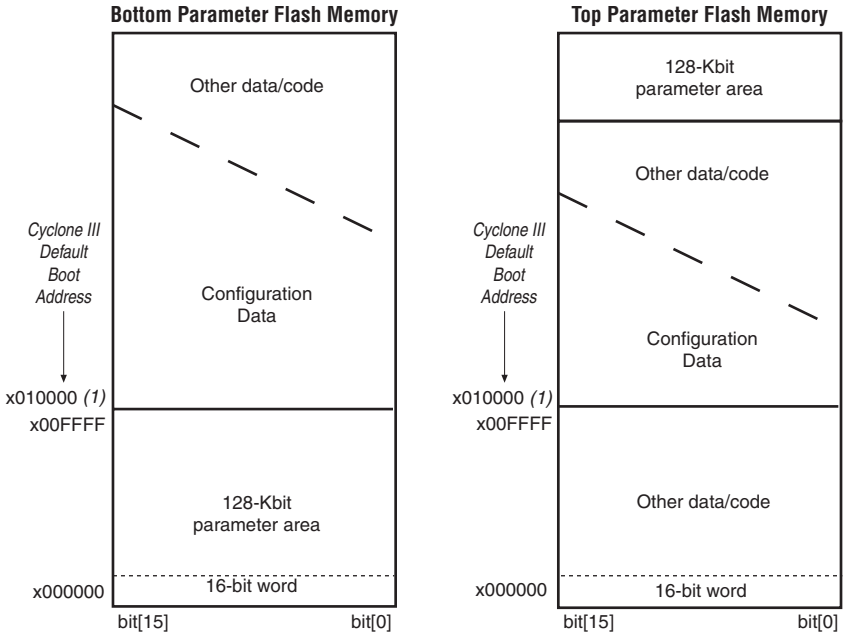
In the AP configuration scheme, the default configuration boot address is 0×010000 when represented in the 16-bit word addressing in the supported parallel flash memory (refer to Figure 10–12). In the Quartus II software, the default configuration boot address is 0x020000 because it is represented in 8-bit byte addressing. Cyclone III devices configure from word address 0x010000, which is equivalent to byte address 0x020000.

The Quartus II software uses byte addressing for the default configuration boot address. You must set the **Start address** field to "0x020000".

The default configuration boot address allows special parameter blocks within the flash memory map to be used by the system. The parameter blocks can be at the top or bottom of the memory map. The configuration boot address in the AP configuration scheme is shown in Figure 10–12. You can change the default configuration default boot address 0x010000 to any desired address using the JTAG instruction `APFC_BOOT_ADDR`.

For information about the JTAG instruction `APFC_BOOT_ADDR`, refer to "Cyclone III JTAG Instructions" on page 10–59.

Figure 10–12. Configuration Boot Address in AP Flash Memory Map



Note to Figure 10–12:
(1) The default configuration boot address is x010000 when represented in the 16-bit word addressing.

Passive Serial Configuration

You can perform PS configuration on Cyclone III devices with an external intelligent host, such as a MAX II device, microprocessor with flash memory, or a download cable. In the PS scheme, an external host controls configuration. Configuration data is clocked into the target Cyclone III device via the `DATA[0]` pin at each rising edge of `DCLK`.

The Cyclone III decompression feature is available when configuring your Cyclone III device with the PS configuration scheme.

Table 10–10 shows the `MSEL` pin settings when using the PS configuration scheme with different configuration voltage standards.

Table 10–10. Cyclone III MSEL Pin Settings for PS Configuration Schemes

Configuration Scheme	MSEL3 *(4)*	MSEL2	MSEL1	MSEL0	Configuration Voltage Standard *(2)*
Passive Serial Standard (PS Standard POR) *(1)*	0	0	0	0	3.3/2.5 V *(3)*
Passive Serial Fast (PS Fast POR) *(1)*	1	1	0	0	3.3/2.5 V *(3)*

Notes to Table 10–10:
(1) These schemes support data decompression.
(2) Configuration voltage standard applied to V_{CCIO}.
(3) You must follow specific requirements when interfacing Cyclone III devices with 2.5 V/ 3.0 V/ 3.3 V configuration voltage standards. For information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 10–8.
(4) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the `MSEL[3]` pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2 on page 10–3.

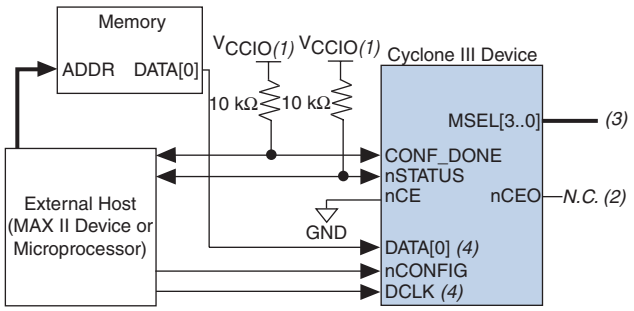
If your system already contains a common flash interface (CFI) flash memory, you can use it for the Cyclone III device configuration storage as well. The MAX II PFL feature provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone III device. Both PS and FPP configuration schemes are supported using this PFL feature.

For more information about PFL, refer to the *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

PS Configuration Using a MAX II Device as an External Host

In the PS configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device. You can store configuration data RBF, HEX, or TTF format. Figure 10–13 shows the configuration interface connections between a Cyclone III device and a MAX II device for single device configuration.

Figure 10–13. Single Device PS Configuration Using an External Host



Notes to Figure 10–13:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–10 on page 10–30. Connect the `MSEL` pins directly to V_{CCA} or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The `DATA[0]` and `DCLK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In single device PS configuration, the `DATA[0]` and `DCLK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

Upon power-up, the Cyclone III devices go through a POR. The POR delay is dependent on the `MSEL` pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < T_{POR} < 9 ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms which has a lower power ramp rate. During POR, the device resets, holds `nSTATUS` low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

For information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

The three stages of the configuration cycle are reset, configuration, and initialization. While `nCONFIG` or `nSTATUS` are low, the device is in reset. To initiate configuration, the MAX II device must generate a low-to-high transition on the `nCONFIG` pin.

To begin configuration, power the V_{CCINT}, V_{CCA}, and V_{CCIO} (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-KΩ pull-up resistor. Once nSTATUS is released, the device is ready to receive configuration data and the configuration stage begins. When nSTATUS is pulled high, the MAX II device should place the configuration data one bit at a time on the DATA[0] pin. If you are using configuration data in either an RBF, TTF, or HEX file, you must send the least significant bit (LSB) of each data byte first. For example, if the RBF contains the byte sequence 02 1B EE 01 FA, the serial bitstream you should transmit to the device is:

```
0100-0000 1101-1000 0111-0111 1000-0000 0101-1111
```

The Cyclone III devices receive configuration data on the DATA[0] pin and the clock is received on the DCLK pin. Data is latched into the device on the rising edge of DCLK. Data is continuously clocked into the target device until CONF_DONE goes high. After the device has received all configuration data successfully, it releases the open-drain CONF_DONE pin, which is pulled high by an external 10-KΩ pull-up resistor. A low-to-high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-KΩ pull-up resistor for the device to initialize.

In Cyclone III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation. Additionally, if you use the internal oscillator as the clock source, you can use the CLKUSR pin as a user I/O pin.

You also have the flexibility to synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. The **Enable user-supplied start-up clock** (**CLKUSR**) option can be turned on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. After all the configuration data is accepted and CONF_DONE goes high, CLKUSR is enabled after the time specified as t_{CD2CU}. After this time period elapses, Cyclone III devices require 3,187 clock cycles to initialize properly and enter user mode. Cyclone III devices support a CLKUSR f_{MAX} of 133 MHz.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. The **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If you use the INIT_DONE pin, it will be high due to an external 10-KΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[0] pin is available as a user I/O pin after configuration. When you choose the PS scheme in the Quartus II software, the DATA[0] pin is tri-stated, by default, in user mode and should be driven by the MAX II device. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified system frequency to ensure correct configuration (refer to Table 10–11 on page 10–36). No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box) is turned on, the Cyclone III device releases nSTATUS after a reset time-out period (maximum of 230 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but CONF_DONE or INIT_DONE have not gone high, the MAX II device must reconfigure the target device.

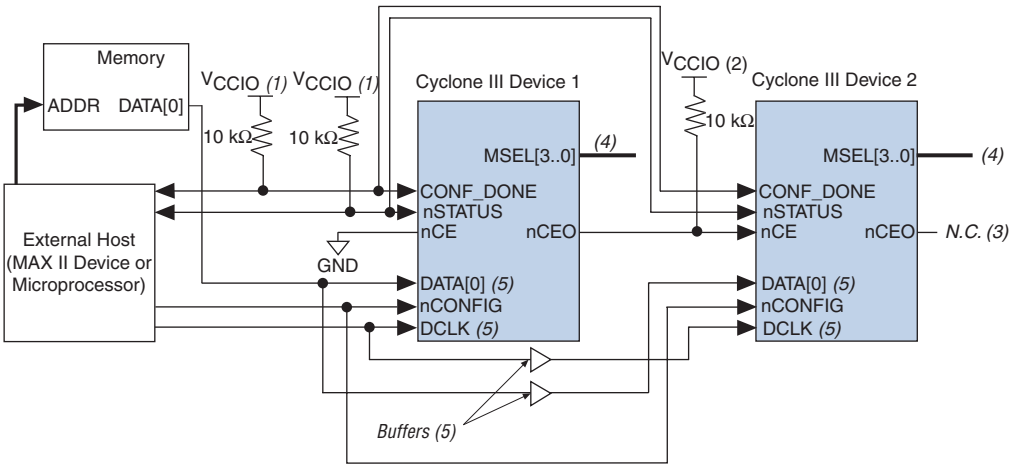
If the optional CLKUSR pin is being used and nCONFIG is pulled low to restart configuration during device initialization, you need to ensure that CLKUSR continues toggling during the time nSTATUS is low (maximum of 230 µs).

When the device is in user-mode, you can initiate a reconfiguration by transitioning the nCONFIG pin low-to-high. The nCONFIG pin must be low for at least 500 ns. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and tri-states all I/O pins. Once nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

For more information about configuration issues, refer the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site at **www.altera.com**.

Figure 10–14 shows how to configure multiple devices using a MAX II device. This circuit is similar to the PS configuration circuit for a single device, except Cyclone III devices are cascaded for multi-device configuration.

Figure 10–14. Multi-Device PS Configuration Using an External Host



Notes to Figure 10–14:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the nCEO pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–10 on page 10–30. Connect the MSEL pins directly to V_{CCA} or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The DATA[0] and DCLK has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In multi-device PS configuration, the DATA[0] and DCLK has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8. You must connect the repeater buffers between the Cyclone III master and slave device(s) for DATA[0] and DCLK.

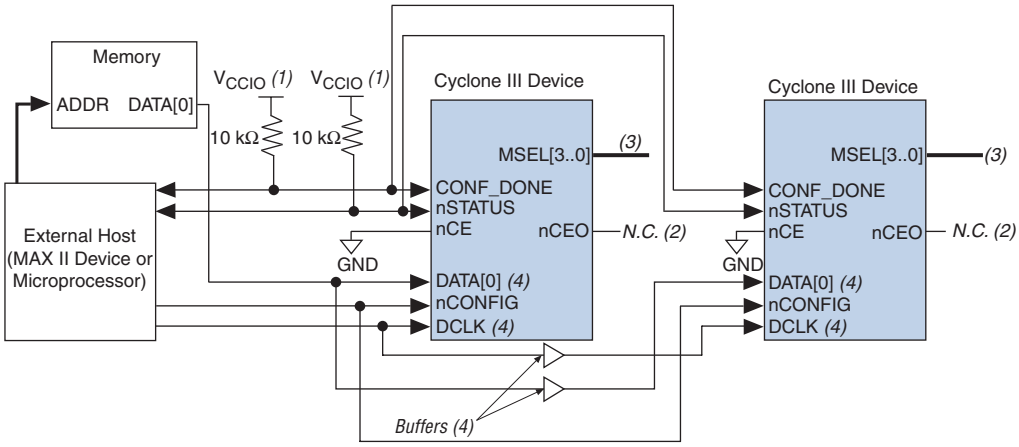
In multi-device PS configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to nCE of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle. Therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Because all device CONF_DONE pins are tied together, all devices initialize and enter user mode at the same time.

If any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured because all nSTATUS and CONF_DONE pins are tied together. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (maximum of 230 µs). After all nSTATUS pins are released and pulled high, the MAX II device can try to reconfigure the chain without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on nCONFIG to restart the configuration process.

In your system, you can have multiple devices that contain the same configuration data. To support this configuration scheme, all device nCE inputs are tied to GND, while nCEO pins are left floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[0], and CONF_DONE) are connected to every device in the chain. Configuration signals can require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be the same density and package. All devices will start and complete configuration at the same time. Figure 10–15 shows multi-device PS configuration when both Cyclone III devices are receiving the same configuration data.

Figure 10–15. Multi-Device PS Configuration When Both Devices Receive the Same Data



Notes to Figure 10–15:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The `nCEO` pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–10 on page 10–30. Connect the `MSEL` pins directly to V_{CCA} or ground.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The `DATA[0]` and `DCLK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

You can use a single configuration chain to configure Cyclone III devices with other Altera devices. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, all of the device `CONF_DONE` and `nSTATUS` pins must be tied together.

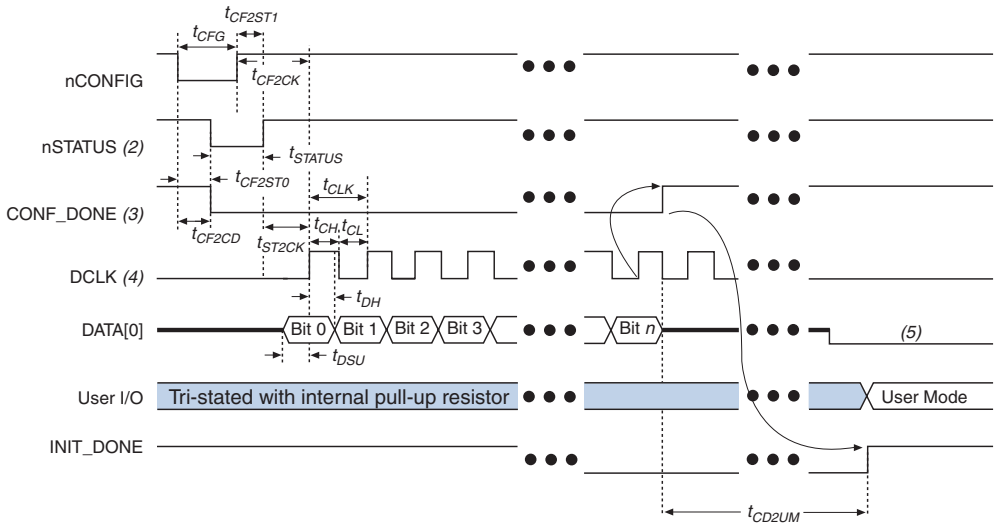
For more information about configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*.

PS Configuration Timing

A PS configuration must meet the setup and hold timing parameters and the maximum clock frequency. When using a microprocessor or another intelligent host to control the PS interface, ensure that you meet these timing requirements.

Figure 10–16 shows the timing waveform for PS configuration when using a MAX II device as an external host.

Figure 10–16. PS Configuration Timing Waveform *Note (1)*



Notes to Figure 10–16:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) Upon power-up, the Cyclone III device holds nSTATUS low for the time of the POR delay.

(3) Upon power-up, before and during configuration, CONF_DONE is low.

(4) In user mode, drive DCLK either high or low when using the PS configuration scheme, whichever is more convenient. When using the AS configuration scheme, DCLK is a Cyclone III output pin and should not be driven externally.

(5) Do not leave the DATA[0] pin floating after configuration. Drive it high or low, whichever is more convenient.

Table 10–11 defines the timing parameters for Cyclone III devices for PS configuration.

Table 10–11. PS Timing Parameters for Cyclone III Devices *Note (1)* *(Part 1 of 2)*

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	500	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	500	ns
t_{CFG}	nCONFIG low pulse width	500	—	ns
t_{STATUS}	nSTATUS low pulse width	70	230 *(2)*	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	230 *(2)*	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	230 *(2)*	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	Data setup time before rising edge on DCLK	5	—	ns
t_{DH}	Data hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	3.2	—	ns
t_{CL}	DCLK low time	3.2	—	ns
t_{CLK}	DCLK period	7.5	—	ns
f_{MAX}	DCLK frequency	—	133	MHz
t_{CD2UM}	CONF_DONE high to user mode *(3)*	300	650	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—

Table 10–11. PS Timing Parameters for Cyclone III Devices Note (1) (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (3,187 × CLKUSR period)	—	—

Notes to Table 10–11:
(1) This information is preliminary.
(2) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting the device.

For more information about device configuration options and how to create configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook*.

PS Configuration Using a Microprocessor

In the PS configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device.

All information in "PS Configuration Using a MAX II Device as an External Host" on page 10–31 is also applicable when using a microprocessor as an external host. Refer to that section for all configuration and timing information.

The MicroBlaster™ software driver enables you to configure Altera FPGAs, including Cyclone III devices, through the ByteBlaster II or ByteBlasterMV cable in PS mode. The MicroBlaster software driver supports an RBF programming input file and is targeted for embedded PS configuration. The source code is developed for the Windows NT operating system. You can customize it to run on other operating systems.

For more information about the MicroBlaster software driver, refer to the *AN 423: Configuring the MicroBlaster Passive Serial Software Driver* application note and source files on the Altera web site.

If you enable **CLKUSR** option in the Quartus II software, Cyclone III devices do not enter user mode after the MicroBlaster has transmitted all the configuration data in the RBF file. You must supply enough initialization clock cycles to the CLKUSR pin to enter user mode.

PS Configuration Using a Download Cable

In this section, the generic term "download cable" includes the Altera USB-Blaster universal serial bus (USB) port download cable, MasterBlaster™ serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlaster MV parallel port download cable.

In PS configuration with a download cable, an intelligent host (such as a PC) transfers data from a storage device to the device via the USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cable.

Upon power-up, the Cyclone III devices go through a POR. The POR delay is dependent on the MSEL pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < T_{POR} < 9 ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms, which has a lower power ramp rate. During POR, the device resets, holds nSTATUS low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

For information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter of the *Cyclone III Device Handbook*.

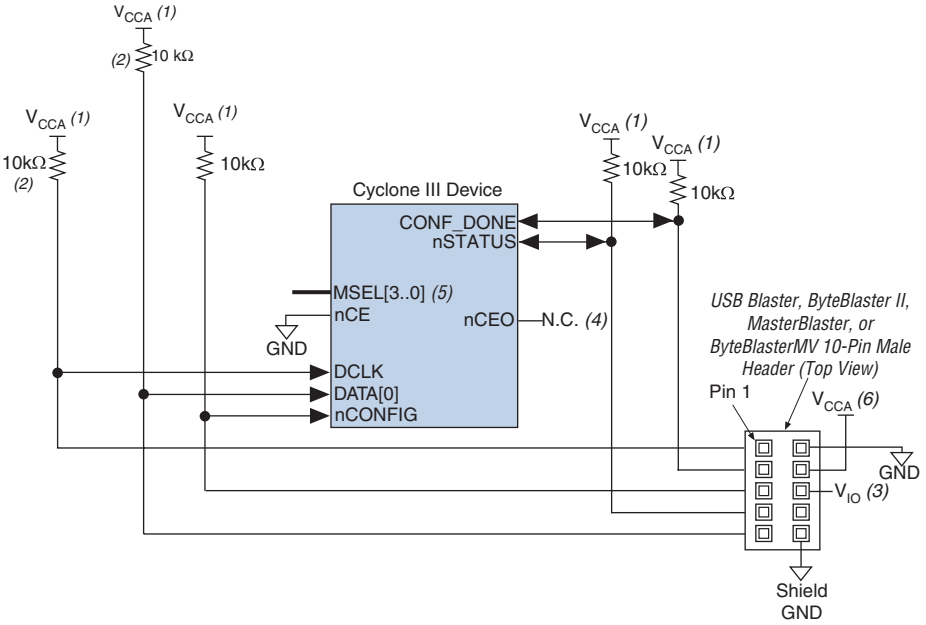
The three stages of the configuration cycle are reset, configuration, and initialization. While nCONFIG or nSTATUS are low, the device is in reset. To initiate configuration in this scheme, the download cable generates a low-to-high transition on the nCONFIG pin.

To begin configuration, power the V_{CCINT}, V_{CCA}, and V_{CCIO} (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

When nCONFIG goes high, the device comes out of reset and releases the open-drain nSTATUS pin, which is then pulled high by an external 10-KΩ pull-up resistor. Once nSTATUS is released the device is ready to receive configuration data and the configuration stage begins. The programming hardware or download cable then places the configuration data one bit at a time on the device's DATA[0] pin. The configuration data is clocked into the target device until CONF_DONE goes high. The CONF_DONE pin must have an external 10-KΩ pull-up resistor in order for the device to initialize.

When you use a download cable, setting the **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs. Additionally, the **Enable user-supplied start-up clock** (**CLKUSR**) option has no affect on the device initialization because this option is disabled in the SRAM Object File when programming the device using the Quartus II programmer and download cable. Therefore, if you turn on the CLKUSR option, you do not need to provide a clock on CLKUSR when you are configuring the device with the Quartus II programmer and a download cable. Figure 10–17 shows PS configuration for Cyclone III devices using a USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV cable.

Figure 10–17. PS Configuration Using a USB Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV Cable



Notes to Figure 10–17:

(1) The pull-up resistor should be connected to the same supply voltage as the V_{CCA} supply.

(2) The pull-up resistors on `DATA[0]` and `DCLK` are only needed if the download cable is the only configuration scheme used on your board. This is to ensure that `DATA[0]` and `DCLK` are not left floating after configuration. For example, if you are also using a configuration device, the pull-up resistors on `DATA[0]` and `DCLK` are not needed.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(5) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–10 on page 10–30 for PS Configuration Schemes. Connect the `MSEL` pins directly to V_{CCA} or GND.

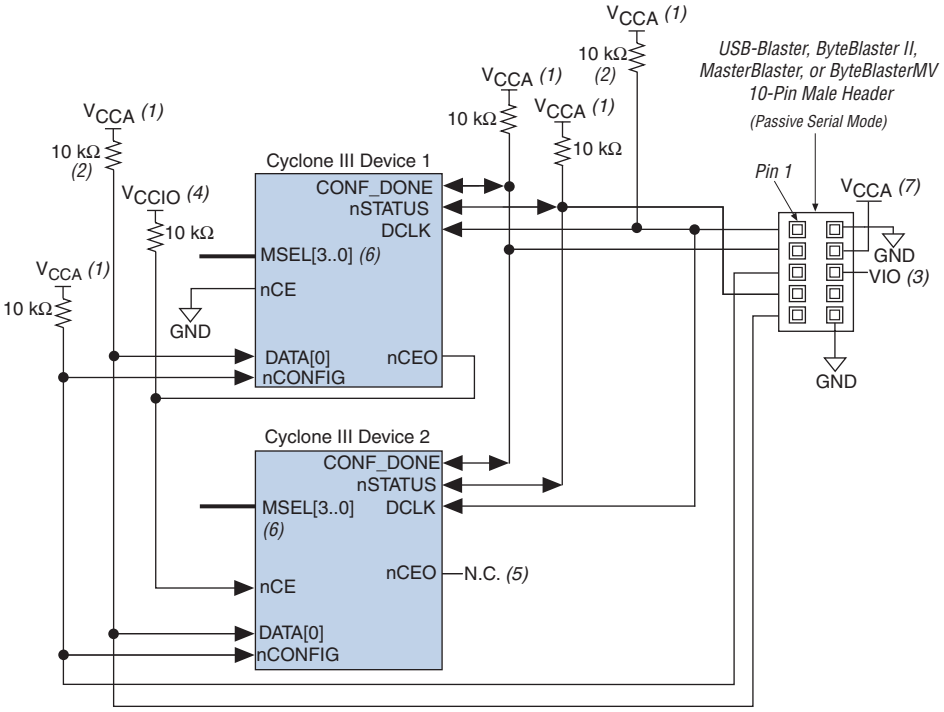
(6) Power up the ByteBlaster II, USB-Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value.

You can use a download cable to configure multiple Cyclone III devices by connecting each device's `nCEO` pin to the subsequent device's `nCE` pin. The first device's `nCE` pin is connected to GND while its `nCEO` pin is connected to the `nCE` of the next device in the chain. The last device's `nCE` input comes from the previous device, while its `nCEO` pin is left floating. All other configuration pins, `nCONFIG`, `nSTATUS`, `DCLK`, `DATA[0]`, and `CONF_DONE` are connected to every device in the chain. Because all `CONF_DONE` pins are tied together, all devices in the chain initialize and enter user mode at the same time.

In addition, the entire chain halts configuration if any device detects an error because the `nSTATUS` pins are tied together. The **Auto-restart configuration after error** option does not affect the configuration cycle because you must manually restart configuration in the Quartus II software when an error occurs.

Figure 10–18 shows how to configure multiple Cyclone III devices with a download cable.

Figure 10–18. Multi-Device PS Configuration Using a USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV Cable



Notes to Figure 10–18:

(1) The pull-up resistor should be connected to the same supply voltage as the V_{CCA} supply.

(2) The pull-up resistors on `DATA[0]` and `DCLK` are only needed if the download cable is the only configuration scheme used on your board. This is to ensure that `DATA[0]` and `DCLK` are not left floating after configuration. For example, if you are also using a configuration device, the pull-up resistors on `DATA[0]` and `DCLK` are not needed.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the `nCEO` pin resides.

(5) The `nCEO` pin of the last device in chain can be left unconnected or used as a user I/O pin.

(6) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–10 on page 10–30 for PS Configuration Schemes. Connect the `MSEL` pins directly to V_{CCA} or GND.

(7) Power up the ByteBlaster II, USB Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value.

For more information on how to use the USB Blaster, MasterBlaster, ByteBlaster II or ByteBlasterMV cables, refer to the following user guides:

- *USB-Blaster Download Cable User Guide*
- *MasterBlaster Serial/USB Communications Cable User Guide*
- *ByteBlaster II Download Cable User Guide*
- *ByteBlasterMV Download Cable User Guide*

Fast Passive Parallel Configuration

FPP configuration in Cyclone III devices is designed to meet the continuously increasing demand for faster configuration times. Cyclone III devices are designed with the capability of receiving byte-wide configuration data per clock cycle.

Table 10–12 shows the MSEL pin settings when using the FPP configuration scheme with different configuration voltage standard.

Table 10–12. Cyclone III MSEL Pin Settings for FPP Configuration Schemes

Configuration Scheme	MSEL3 *(4)*	MSEL2	MSEL1	MSEL0	Configuration Voltage Standard *(2)*
Fast Passive Parallel Fast (FPP Fast POR) *(1)*	1	1	1	0	3.3/2.5 V *(3)*
Fast Passive Parallel Fast (FPP Fast POR) *(1)*	1	1	1	1	1.8/1.5 V

Notes to Table 10–12:

(1) Some of the smaller Cyclone III devices or package options do not support the FPP configuration scheme. For more information, refer to Table 10–2.

(2) Configuration voltage standard applied to V_{CCIO}.

(3) You must follow specific requirements when interfacing Cyclone III devices with 2.5 V/ 3.0 V/ 3.3 V configuration voltage standards. For information about the requirements, refer to "Configuration and JTAG Pin I/O Requirements" on page 10–8.

(4) Some of the smaller Cyclone III devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. For information about the supported configuration schemes across device densities and package options, refer to Table 10–2 on page 10–3.

You can perform FPP configuration of Cyclone III devices with an intelligent host, such as a MAX II device or microprocessor with flash memory.

If your system already contains a CFI flash memory, you can utilize it for the Cyclone III device configuration storage as well. The MAX II PFL feature in MAX II devices provides an efficient method to program CFI flash memory devices through the JTAG interface and the logic to control configuration from the flash memory device to the Cyclone III device. Both PS and FPP configuration schemes are supported using this PFL feature.

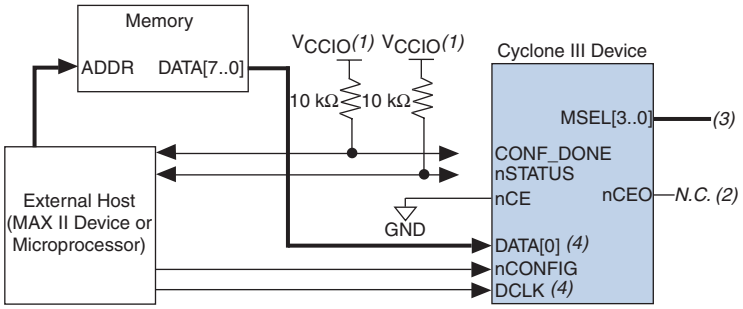
For more information about PFL, refer to *AN 386: Using the Parallel Flash Loader with the Quartus II Software*.

FPP Configuration Using a MAX II Device as an External Host

FPP configuration using an external host provides a fast method to configure Cyclone III devices. In the FPP configuration scheme, you can use a MAX II device as an intelligent host that controls the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device. You can store configuration data in RBF, HEX, or TTF format. When using a MAX II device as an intelligent host, a design that controls the configuration process, such as fetching the data from flash memory and sending it to the device, must be stored in the MAX II device.

Figure 10–19 shows the configuration interface connections between the Cyclone III device and a MAX II device for single device configuration.

Figure 10–19. Single Device FPP Configuration Using an External Host



Notes to Figure 10–19:

(1) Connect the pull-up resistor to a supply that provides an acceptable input signal for the device. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(3) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–12. Connect the `MSEL` pins directly to V_{CCA} or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The `DATA[7..0]` and `DCLK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In single device FPP configuration, the `DATA[7..0]` and `DCLK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

Upon power-up, the Cyclone III devices go through a POR. The POR delay is dependent on the `MSEL` pin settings which correspond to the configuration scheme that you select. Depending on the configuration scheme, either a fast POR time or a standard POR time is available. The fast POR time is 3 ms < T_{POR} < 9 ms for fast configuration time. The standard POR time is 50 ms < T_{POR} < 200 ms which has a lower power ramp rate. During POR, the device resets, holds `nSTATUS` low, and tri-states all user I/O pins. Once the device successfully exits POR, all user I/O pins continue to be tri-stated. The user I/O pins and dual-purpose I/O pins have weak pull-up resistors which are always enabled (after POR) before and during configuration.

For more information about the value of the weak pull-up resistors on the I/O pins that are on before and during configuration, refer to the *DC and Switching Characteristics* chapter in the *Cyclone III Device Handbook*.

The three stages in the configuration cycle are reset, configuration, and initialization. While `nCONFIG` or `nSTATUS` are low, the device is in the reset stage. To initiate configuration, the MAX II device must drive the `nCONFIG` pin from low-to-high.

To begin configuration, power the V_{CCINT}, V_{CCA}, and V_{CCIO} (for the banks in which the configuration and JTAG pins reside) voltages to the appropriate voltage levels.

When `nCONFIG` goes high, the device comes out of reset and releases the open-drain `nSTATUS` pin, which is then pulled high by an external 10-KΩ pull-up resistor. Once `nSTATUS` is released, the device is ready to receive configuration data and the configuration stage begins. When `nSTATUS` is pulled high, the MAX II device places the configuration data one byte at a time on the `DATA[7..0]` pins.

The Cyclone III devices receive configuration data on the `DATA[7..0]` pins and the clock is received on the `DCLK` pin. Data is latched into the device on the rising edge of `DCLK`. Data is continuously clocked into the target device until `CONF_DONE` goes high. The `CONF_DONE` pin goes high one byte early in FPP configuration mode. The last byte is required for serial configuration (AS and PS) modes. After the device has received the next to last byte of the configuration data successfully, it releases the open-drain `CONF_DONE` pin, which is pulled high by an external 10-KΩ pull-up resistor. A low-to-

high transition on CONF_DONE indicates configuration is complete and initialization of the device can begin. The CONF_DONE pin must have an external 10-KΩ pull-up resistor in order for the device to initialize.

In Cyclone III devices, the initialization clock source is either the internal oscillator (typically 10 MHz) or the optional CLKUSR pin. By default, the internal oscillator is the clock source for initialization. If the internal oscillator is used, the Cyclone III device provides itself with enough clock cycles for proper initialization. Therefore, if the internal oscillator is the initialization clock source, sending the entire configuration file to the device is sufficient to configure and initialize the device. Driving DCLK to the device after configuration is complete does not affect device operation. Additionally, if you use the internal oscillator as the clock source, you can use the CLKUSR pin as a user I/O pin.

You can also synchronize initialization of multiple devices or to delay initialization with the CLKUSR option. The **Enable user-supplied start-up clock** (**CLKUSR**) option can be turned on in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. Supplying a clock on CLKUSR does not affect the configuration process. The CONF_DONE pin goes high one byte early in FPP configuration mode.

The last byte is required for serial configuration (AS and PS) modes. After the CONF_DONE pin transitions high, CLKUSR is enabled after the time specified as t_{CD2CU}. After this time period elapses, Cyclone III devices require 3,187 clock cycles to initialize properly and enter user mode. Refer to Table 10–13 for the CLKUSR f_{MAX} value that the Cyclone III devices support.

An optional INIT_DONE pin is available, which signals the end of initialization and the start of user-mode with a low-to-high transition. This **Enable INIT_DONE Output** option is available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box. If the INIT_DONE pin is used, it is high because of an external 10-KΩ pull-up resistor when nCONFIG is low and during the beginning of configuration. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin goes low. When initialization is complete, the INIT_DONE pin is released and pulled high. The MAX II device must be able to detect this low-to-high transition, which signals the device has entered user mode. When initialization is complete, the device enters user mode. In user-mode, the user I/O pins no longer have weak pull-up resistors and function as assigned in your design.

To ensure DCLK and DATA[7..0] are not left floating at the end of configuration, the MAX II device must drive them either high or low, whichever is convenient on your board. The DATA[7..0] pins are available as user I/O pins after configuration. When you select the FPP scheme in the Quartus II software, these I/O pins are tri-stated in user mode by default. To change this default option in the Quartus II software, select the **Dual-Purpose Pins** tab of the **Device & Pin Options** dialog box.

The configuration clock (DCLK) speed must be below the specified frequency to ensure correct configuration. No maximum DCLK period exists, which means you can pause configuration by halting DCLK for an indefinite amount of time.

If an error occurs during configuration, the device drives its nSTATUS pin low, resetting itself internally. The low signal on the nSTATUS pin also alerts the MAX II device that there is an error. If the **Auto-restart configuration after error** option (available in the Quartus II software from the **General** tab of the **Device & Pin Options** dialog box is turned on, the device releases nSTATUS after a reset time-out period (maximum of 230 µs). After nSTATUS is released and pulled high by a pull-up resistor, the MAX II device can try to reconfigure the target device without needing to pulse nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 ns) on CONFIG to restart the configuration process.

The MAX II device can also monitor the CONF_DONE and INIT_DONE pins to ensure successful configuration. The CONF_DONE pin must be monitored by the MAX II device to detect errors and determine when programming completes. If all configuration data is sent, but the CONF_DONE or INIT_DONE signals have not gone high, the MAX II device reconfigures the target device.

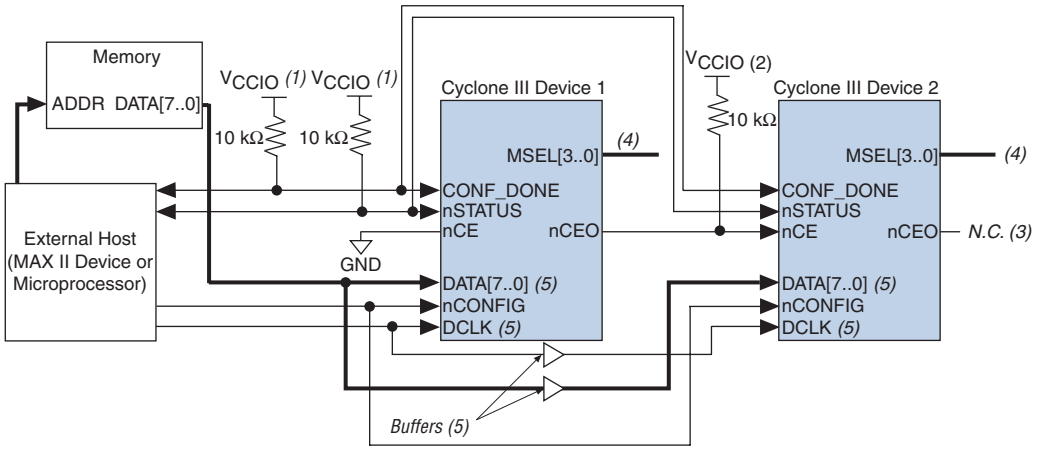
If the optional CLKUSR pin is used and nCONFIG is pulled low to restart configuration during device initialization, you must ensure CLKUSR continues toggling during the time nSTATUS is low (maximum of 230 µs).

When the device is in user mode, initiating a reconfiguration is done by transitioning the nCONFIG pin low-to-high. The nCONFIG pin should be low for at least 500 ns. When nCONFIG is pulled low, the device also pulls nSTATUS and CONF_DONE low and all I/O pins are tri-stated. When nCONFIG returns to a logic high level and nSTATUS is released by the device, reconfiguration begins.

For more information about configuration issues, refer to the *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook* and the FPGA Configuration Troubleshooter on the Altera web site at **www.altera.com**.

Figure 10–20 shows how to configure multiple devices using a MAX II device. This circuit is similar to the FPP configuration circuit for a single device, except the Cyclone III devices are cascaded for multi-device configuration.

Figure 10–20. Multi-Device FPP Configuration Using an External Host



Notes to Figure 10–20:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) Connect the pull-up resistor to the V_{CCIO} supply voltage of I/O bank in which the nCEO pin resides.

(3) The nCEO pin can be left unconnected or used as a user I/O pin when it does not feed other device's nCE pin.

(4) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12 on page 10–41. Connect the MSEL pins directly to V_{CCA} or ground.

(5) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The DATA[7..0] and DCLK has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. In multi-device FPP configuration, the DATA[7..0] and DCLK has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8. You must connect the repeater buffers between the Cyclone III master and slave device(s) for DATA[7..0] and DCLK.

In multi-device FPP configuration, the first device's nCE pin is connected to GND while its nCEO pin is connected to the nCE pin of the next device in the chain. The last device's nCE input comes from the previous device, while its nCEO pin is left floating. After the first device completes configuration in a multi-device configuration chain, its nCEO pin drives low to activate the second device's nCE pin, which prompts the second device to begin configuration. The second device in the chain begins configuration within one clock cycle; therefore, the transfer of data destinations is transparent to the MAX II device. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. The configuration signals may require

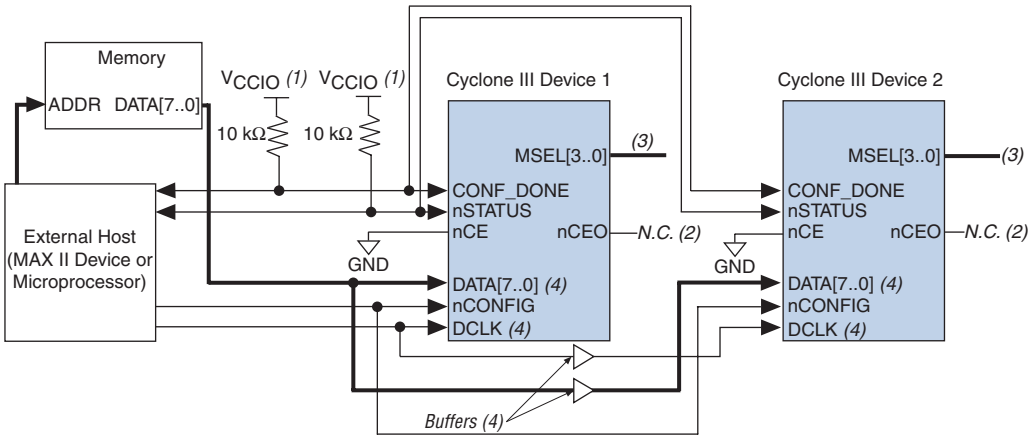
buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. All devices initialize and enter user mode at the same time because all device CONF_DONE pins are tied together.

All nSTATUS and CONF_DONE pins are tied together and if any device detects an error, configuration stops for the entire chain and the entire chain must be reconfigured. For example, if the first device flags an error on nSTATUS, it resets the chain by pulling its nSTATUS pin low. This behavior is similar to a single device detecting an error.

If the **Auto-restart configuration after error** option is turned on, the devices release their nSTATUS pins after a reset time-out period (maximum of 230 µs). After all nSTATUS pins are released and pulled high, the MAX II device can try to reconfigure the chain without pulsing nCONFIG low. If this option is turned off, the MAX II device must generate a low-to-high transition (with a low pulse of at least 500 µs) on nCONFIG to restart the configuration process.

If a system has multiple devices that contain the same configuration data, tie all device nCE inputs to GND, and leave nCEO pins floating. All other configuration pins (nCONFIG, nSTATUS, DCLK, DATA[7..0], and CONF_DONE) are connected to every device in the chain. Configuration signals may require buffering to ensure signal integrity and prevent clock skew problems. Ensure that the DCLK and DATA lines are buffered. Devices must be the same density and package. All devices start and complete configuration at the same time. Figure 10–21 shows multi-device FPP configuration when both Cyclone III devices are receiving the same configuration data.

Figure 10–21. Multi-Device FPP Configuration Using an External Host When Both Devices Receive the Same Data



Notes to Figure 10–21:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain. V_{CC} should be high enough to meet the V_{IH} specification of the I/O on the device and the external host.

(2) The nCEO pins of both devices can be left unconnected or used as user I/O pins when configuring the same configuration data into multiple devices.

(3) The MSEL pin settings vary for different configuration voltage standards and POR time. To connect MSEL[3..0], refer to Table 10–12. Connect the MSEL pins directly to V_{CCA} or GND.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. The DATA[7..0] and DCLK has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

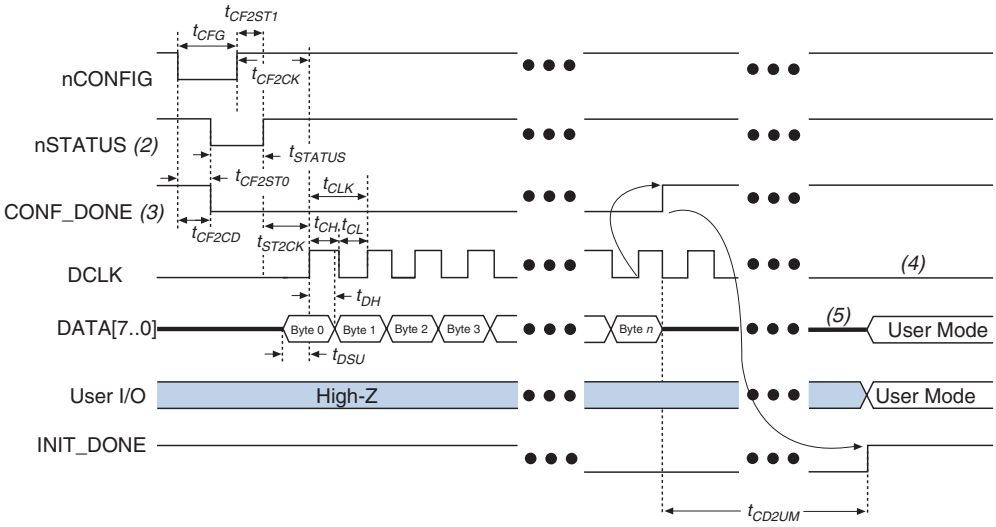
You can use a single configuration chain to configure Cyclone III devices with other Altera devices that support FPP configuration. To ensure that all devices in the chain complete configuration at the same time or that an error flagged by one device initiates reconfiguration in all devices, tie all of the device CONF_DONE and nSTATUS pins together.

For more information about configuring multiple Altera devices in the same configuration chain, refer to *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*.

FPP Configuration Timing

Figure 10–22 shows the timing waveform for FPP configuration when using a MAX II device as an external host.

Figure 10–22. FPP Configuration Timing Waveform *Note (1)*



Notes to Figure 10–22:

(1) The beginning of this waveform shows the device in user-mode. In user-mode, `nCONFIG`, `nSTATUS`, and `CONF_DONE` are at logic high levels. When `nCONFIG` is pulled low, a reconfiguration cycle begins.

(2) Upon power-up, the Cyclone III device holds `nSTATUS` low for the time of the POR delay.

(3) Upon power-up, before and during configuration, `CONF_DONE` is low.

(4) `DCLK` should not be left floating after configuration. It should be driven high or low, whichever is more convenient.

(5) `DATA[7..0]` are available as user I/O pins after configuration and the state of these pins depends on the dual-purpose pin settings.

Table 10–13 defines the timing parameters for Cyclone III devices for FPP configuration.

Table 10–13. FPP Timing Parameters for Cyclone III Devices *Note (1)* **(Part 1 of 2)**

Symbol	Parameter	Min	Max	Units
t_{CF2CD}	`nCONFIG` low to `CONF_DONE` low	—	500	ns
t_{CF2ST0}	`nCONFIG` low to `nSTATUS` low	—	500	ns
t_{CFG}	`nCONFIG` low pulse width	500	—	ns
t_{STATUS}	`nSTATUS` low pulse width	70	230 *(2)*	µs
t_{CF2ST1}	`nCONFIG` high to `nSTATUS` high	—	230 *(2)*	µs
t_{CF2CK}	`nCONFIG` high to first rising edge on `DCLK`	230 *(2)*	—	µs
t_{ST2CK}	`nSTATUS` high to first rising edge of `DCLK`	2	—	µs
t_{DSU}	Data setup time before rising edge on `DCLK`	5	—	ns
t_{DH}	Data hold time after rising edge on `DCLK`	0	—	ns
t_{CH}	`DCLK` high time	3.2	—	ns
t_{CL}	`DCLK` low time	3.2	—	ns
t_{CLK}	`DCLK` period	7.5	—	ns
f_{MAX}	`DCLK` frequency	—	100 *(4)*	MHz
t_{CD2UM}	`CONF_DONE` high to user mode *(3)*	300	650	µs

Table 10–13. FPP Timing Parameters for Cyclone III Devices Note (1) (Part 2 of 2)

Symbol	Parameter	Min	Max	Units
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} +(3,187 × CLKUSR period)	—	—

Notes to Table 10–13:
(1) This information is preliminary.
(2) This value is applicable if users do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(3) The minimum and maximum numbers apply only if the internal oscillator is chosen as the clock source for starting up the device
(4) EP3C5, EP3C10, EP3C16, EP3C25, and EP3C40 devices support a CLKUSR f_{MAX} of 133 MHz. EP3C55, EP3C80, and EP3C120 devices support a CLKUSR f_{MAX} of 100 MHz.

For more information about device configuration options and how to create configuration files, refer to the *Software Settings* section in volume 2 of the *Configuration Handbook.*

FPP Configuration Using a Microprocessor

In the FPP configuration scheme, a microprocessor can control the transfer of configuration data from a storage device, such as flash memory, to the target Cyclone III device.

All information in "FPP Configuration Using a MAX II Device as an External Host" on page 10–41 is also applicable when using a microprocessor as an external host. Refer to that section for all configuration and timing information.

JTAG Configuration

JTAG has developed a specification for boundary-scan testing. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing. The BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. You can also use the JTAG circuitry to shift configuration data into the device. The Quartus II software automatically generates SRAM Object Files that can be used for JTAG configuration with a download cable in the Quartus II software programmer.

For more information about JTAG boundary-scan testing, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook.*

Cyclone III devices are designed such that JTAG instructions have precedence over any device configuration modes. Therefore, JTAG configuration can take place without waiting for other configuration modes to complete. For example, if you attempt JTAG configuration of Cyclone III devices during PS configuration, PS configuration terminates and JTAG configuration begins. If the Cyclone III MSEL pins are set to AS mode, the Cyclone III device does not output a DCLK signal when JTAG configuration takes place.

You cannot use the Cyclone III decompression feature if you are configuring your Cyclone III device when using JTAG-based configuration.

The four required pins for a device operating in JTAG mode are TDI, TDO, TMS, and TCK. The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have weak internal pull-up resistors (typically 25 kΩ). The TDO output pin is powered by V_{CCIO} in I/O bank 1. All of the JTAG input pins are powered by the V_{CCIO} pin. All the JTAG pins support only LVTTL I/O standard. All user I/O pins are tri-stated during JTAG configuration. Table 10–14 explains each JTAG pin's function.

The TDO output is powered by the V_{CCIO} power supply of I/O bank 1.

For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*.

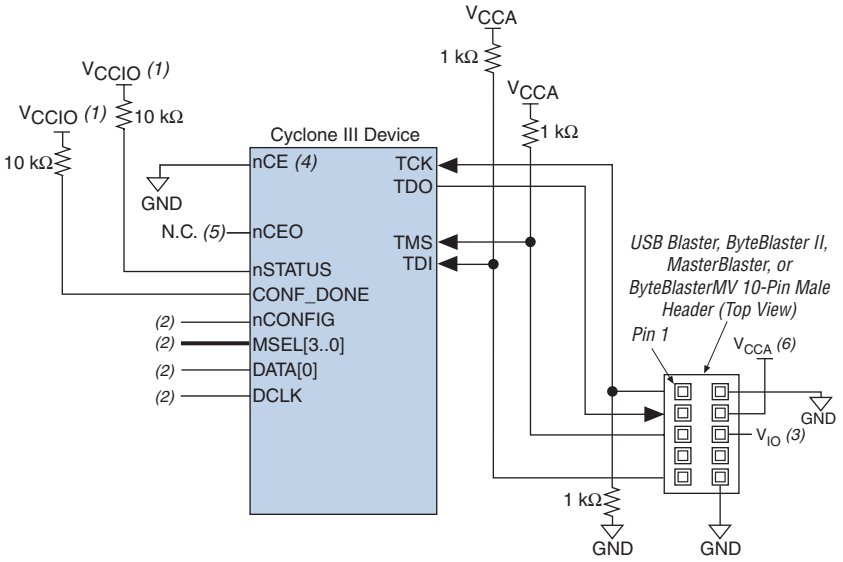
Table 10–14. Dedicated JTAG Pins

Pin Name	Pin Type	Description
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to VCC.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to GND.

You can download data to the device on the PCB through the USB Blaster, MasterBlaster, ByteBlaster II, or ByteBlasterMV download cable during JTAG configuration. Configuring devices using a cable is similar to programming devices in-system. Figure 10–23 on page 10–49 and Figure 10–24 on page 10–50 show JTAG configuration of a single Cyclone III device.

For device V_{CCIO} of 2.5 V, 3.0 V or 3.3 V, refer to Figure 10–23. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using V_{CCIO} of 2.5 V, 3.0 V, or 3.3 V, you must power up the download cable's V_{CC} with a 2.5 V supply from V_{CCA}. For device V_{CCIO} of 1.2 V, 1.5 V, or 1.8 V, refer to Figure 10–24 on page 10–50. You can power up the download cable's V_{CC} with the supply from V_{CCIO}.

Figure 10–23. JTAG Configuration of a Single Device Using a Download Cable (2.5 V, 3.0 V, or 3.3 V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 10–23:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If only a JTAG configuration is used, connect the `nCONFIG` pin to V_{CC}, and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

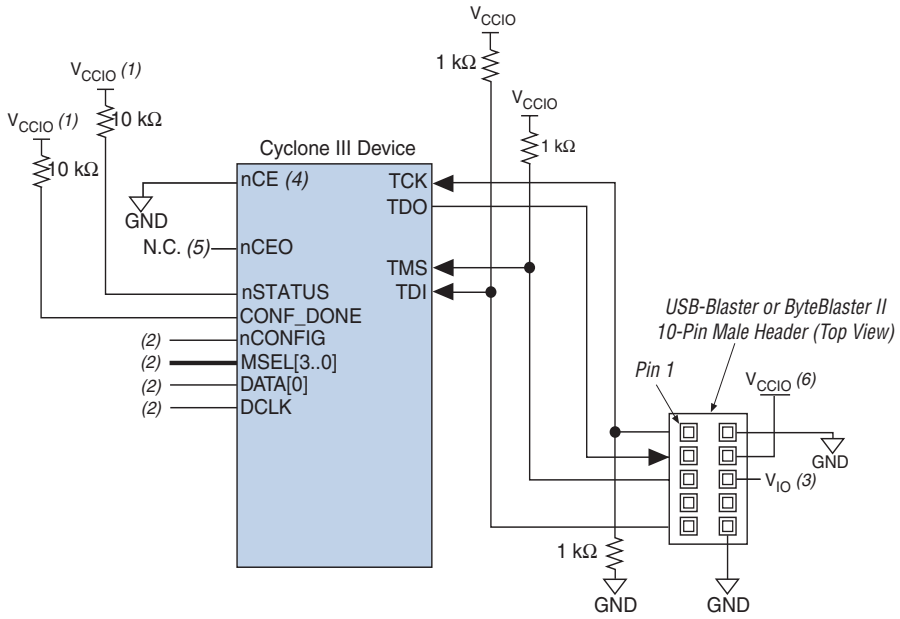
(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(6) Power up the ByteBlaster II, USB Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value.

Figure 10–24. JTAG Configuration of a Single Device Using a Download Cable (1.2 V, 1.5 V, or 1.8 V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 10–24:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the `nCONFIG` pin to V_{CC}, and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming; otherwise it is a no connect.

(4) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(6) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with supply from V_{CCIO}. The ByteBlaster II and USB Blaster cables do not support a target supply voltage of 1.2 V. Refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide* for the target supply voltage value.

To configure a single device in a JTAG chain, the programming software places all other devices in bypass mode. In bypass mode, devices pass programming data from the `TDI` pin to the `TDO` pin through a single bypass register without being affected internally. This scheme enables the programming software to program or verify the target device. Configuration data driven into the device appears on the `TDO` pin one clock cycle later.

The Quartus II software verifies successful JTAG configuration upon completion. At the end of configuration, the software checks the state of `CONF_DONE` through the JTAG port. When Quartus II generates a (.**jam**) file for a multi-device chain, it contains instructions so that all the devices in the chain are initialized at the same time. If `CONF_DONE` is not high, the Quartus II software indicates that configuration has failed. If `CONF_DONE` is high, the software indicates that configuration was successful. After the configuration bitstream is transmitted serially via the JTAG `TDI` port, the `TCK` port is clocked an additional 3,180 cycles to perform device initialization.

Cyclone III devices have dedicated JTAG pins that always function as JTAG pins. Not only can you perform JTAG testing on Cyclone III devices before and after, but also during configuration. Cyclone III devices support the `BYPASS`, `IDCODE`, and `SAMPLE` instructions during configuration without interrupting configuration. All other JTAG instructions may only be issued by first interrupting configuration and reprogramming I/O pins using the `ACTIVE_DISENGAGE` and `CONFIG_IO` instructions.

The `CONFIG_IO` instruction allows I/O buffers to be configured via the JTAG port and when issued after the `ACTIVE_DISENGAGE` instruction, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device or waiting for a configuration

device to complete configuration. In Cyclone III devices, prior to issuing the CONFIG_IO instruction, you must issue the ACTIVE_DISENGAGE instruction. This is because in Cyclone III devices, the CONFIG_IO instruction does not hold nSTATUS low until reconfiguration, so you must disengage the active configuration mode controller when active configuration is interrupted. The ACTIVE_DISENGAGE instruction places the active configuration mode controllers in an idle state prior to JTAG programming. Additionally, the ACTIVE_ENGAGE instruction allows you to re-engage an already disengaged active configuration mode controller.

☞ You must follow a specific flow when executing the CONFIG_IO, ACTIVE_DISENGAGE, and ACTIVE_ENGAGE JTAG instructions in Cyclone III devices. For information about the instruction flow, refer to "Cyclone III JTAG Instructions" on page 10–59.

The chip-wide reset (DEV_CLRn) and chip-wide output enable (DEV_OE) pins on Cyclone III devices do not affect JTAG boundary-scan or programming operations. Toggling these pins does not affect JTAG operations (other than the usual boundary-scan operation).

When designing a board for JTAG configuration of Cyclone III devices, consider the dedicated configuration pins. Table 10–15 shows how these pins should be connected during JTAG configuration.

Table 10–15. Dedicated Configuration Pin Connections During JTAG Configuration

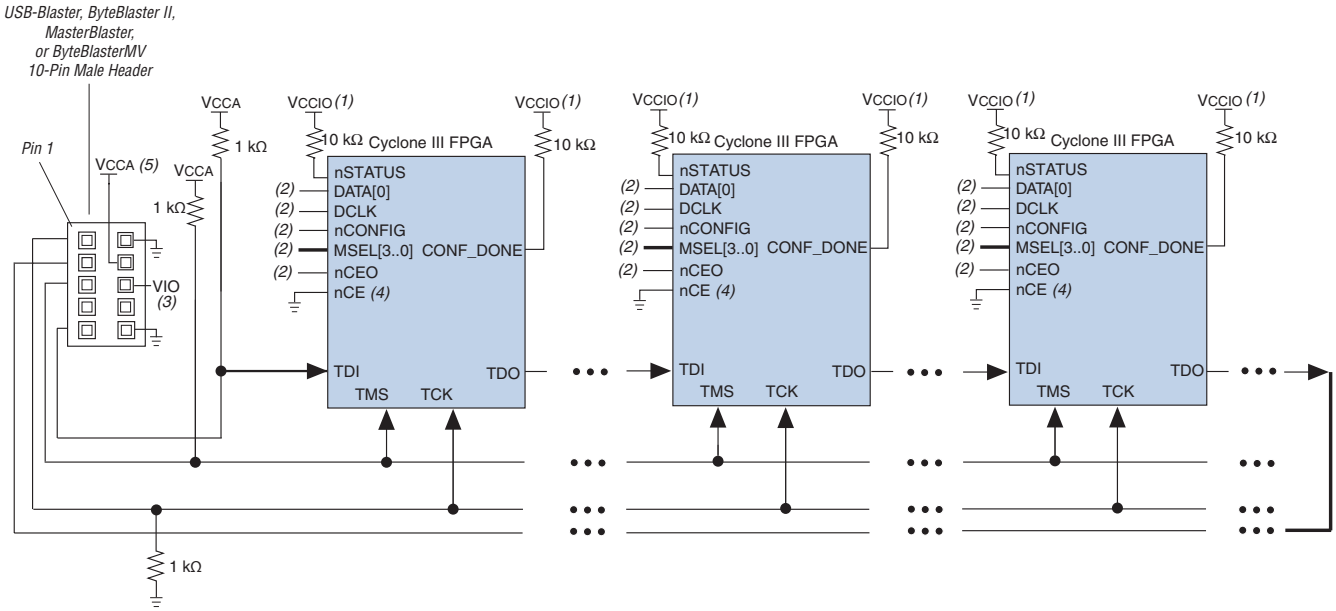
Signal	Description
nCE	On all Cyclone III devices in the chain, nCE should be driven low by connecting it to ground, pulling it low via a resistor, or driving it by some control circuitry. For devices that are also in multi-device AS, AP, PS, or FPP configuration chains, the nCE pins should be connected to GND during JTAG configuration or JTAG configured in the same order as the configuration chain.
nCEO	On all Cyclone III devices in the chain, nCEO can be left floating or connected to the nCE of the next device.
MSEL[3..0]	These pins must not be left floating. These pins support whichever non-JTAG configuration is used in production. If only JTAG configuration is used, tie these pins to GND.
nCONFIG	Driven high by connecting to V_{CC}, pulling up via a resistor, or driven high by some control circuitry.
nSTATUS	Pull to V_{CC} via a 10 KΩ resistor. When configuring multiple devices in the same JTAG chain, each nSTATUS pin should be pulled up to V_{CC} individually.
CONF_DONE	Pull to V_{CC} via a 10 KΩ resistor. When configuring multiple devices in the same JTAG chain, each CONF_DONE pin should be pulled up to V_{CC} individually. CONF_DONE going high at the end of JTAG configuration indicates successful configuration.
DCLK	Should not be left floating. Drive low or high, whichever is more convenient on your board.

When programming a JTAG device chain, one JTAG-compatible header is connected to several devices. The number of devices in the JTAG chain is limited only by the drive capability of the download cable. When four or more devices are connected in a JTAG chain, Altera recommends buffering the TCK, TDI, and TMS pins with an on-board buffer.

JTAG-chain device programming is ideal when the system contains multiple devices, or when testing your system using JTAG BST circuitry. Figure 10–25 and Figure 10–26 show a multi-device JTAG configuration.

For device V_{CCIO} of 2.5 V, 3.0 V, or 3.3 V, you must refer to Figure 10–25. All I/O inputs must maintain a maximum AC voltage of 4.1 V. Because JTAG pins do not have the internal PCI clamping diodes to prevent voltage overshoot when using V_{CCIO} of 2.5 V, 3.0 V, or 3.3 V, you must power up the download cable's V_{CC} with a 2.5 V supply from V_{CCA}. For device V_{CCIO} of 1.2 V, 1.5 V, or 1.8 V, refer to Figure 10–26. You can power up the download cable's V_{CC} with the supply from V_{CCIO}.

Figure 10–25. JTAG Configuration of Multiple Devices Using a Download Cable (2.5 V, 3.0 V, or 3.3 V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 10–25:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

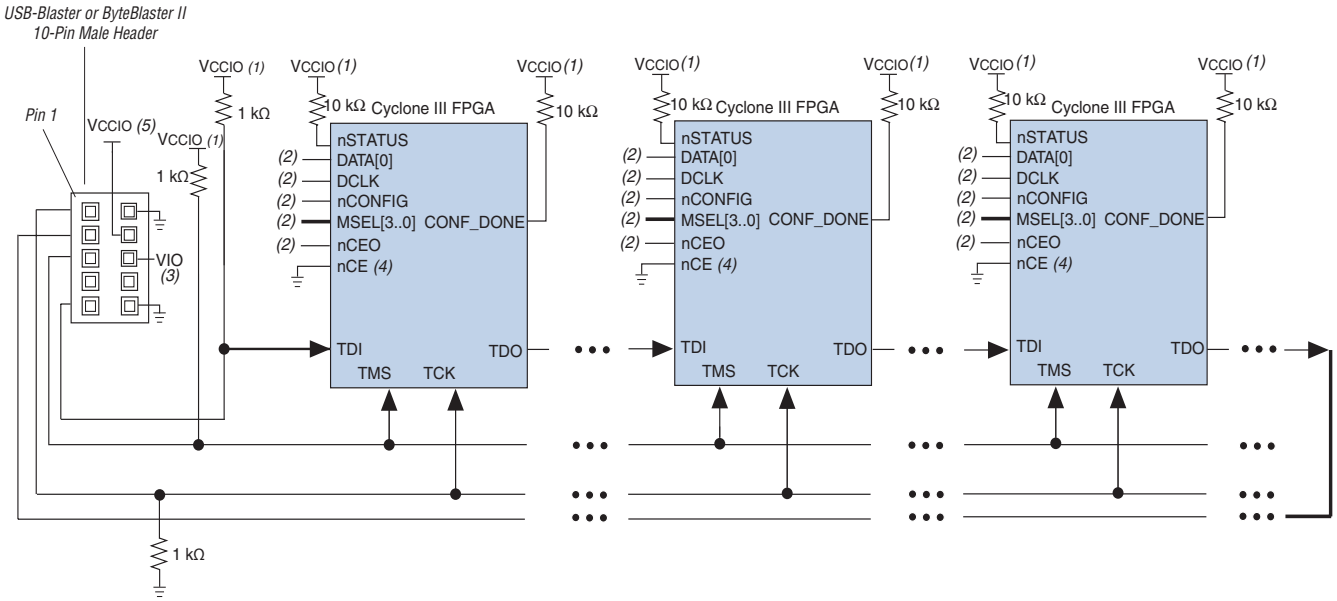
(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the `nCONFIG` pin to V_{CC}, and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV cable, this pin is a no connect. In the USB-Blaster and ByteBlaster II cable, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) `nCE` must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the ByteBlaster II, USB Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications User Guide* for this value.

Figure 10–26. JTAG Configuration of Multiple Devices Using a Download Cable (1.2 V, 1.5 V, or 1.8 V V_{CCIO} Powering the JTAG Pins)



Notes to Figure 10–26:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the `nCONFIG` pin to V_{CC}, and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) In the USB-Blaster and ByteBlaster II cable, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) `nCE` must be connected to ground or driven low for successful JTAG configuration.

(5) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with supply from V_{CCIO}. The ByteBlaster II and USB Blaster cables do not support a target supply voltage of 1.2 V. Refer to the *ByteBlaster II Download Cable User Guide* and the *USB-Blaster Download Cable User Guide* for the target supply voltage value.

All I/O inputs must maintain a maximum AC voltage of 4.1V. If a non-Cyclone III device is cascaded in the JTAG-chain, `TDO` of the non-Cyclone III device driving into `TDI` of Cyclone III has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

The `nCE` pin must be connected to GND or driven low during JTAG configuration. In multi-device AS, AP, PS, and FPP configuration chains, the first device's `nCE` pin is connected to GND while its `nCEO` pin is connected to the `nCE` pin of the next device in the chain. The last device's input for the `nCE` pin comes from the previous device, while its `nCEO` pin is left floating. In addition, the `CONF_DONE` and `nSTATUS` signals are all shared in multi-device AS, AP, PS, and FPP configuration chains so the devices can enter user mode at the same time after configuration is complete. When the `CONF_DONE` and `nSTATUS` signals are shared among all the devices, every device must be configured when JTAG configuration is performed.

If you only use JTAG configuration, Altera recommends that you connect the circuitry as shown in Figure 10–25 or Figure 10–26, where each of the `CONF_DONE` and `nSTATUS` signals are isolated so that each device can enter user mode individually.

After the first device completes configuration in a multi-device configuration chain, its `nCEO` pin drives low to activate the second device's `nCE` pin, which prompts the second device to begin configuration. Therefore, if these devices are also in a JTAG chain, make sure the `nCE` pins are connected to GND during JTAG configuration or that the devices are JTAG configured in the same order as the configuration chain. As long as the devices are JTAG configured in the same order as the multi-device configuration chain, the `nCEO` of the previous device drives the `nCE` pin of the next device low when it has successfully been JTAG configured.

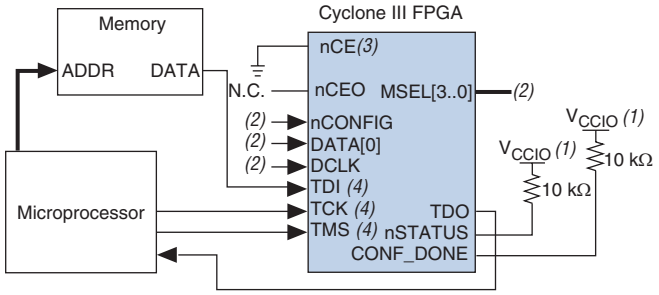
You can place other Altera devices that have JTAG support in the same JTAG chain for device programming and configuration.

JTAG configuration allows an unlimited number of Cyclone III devices to be cascaded in a JTAG chain.

For more information about configuring multiple Altera devices in the same configuration chain, refer to the *Configuring Mixed Altera Device Chains* chapter in volume 2 of the *Configuration Handbook*.

Figure 10–27 shows JTAG configuration of a Cyclone III device with a microprocessor.

Figure 10–27. JTAG Configuration of a Single Device Using a Microprocessor



Notes to Figure 10–27:

(1) The pull-up resistor should be connected to a supply that provides an acceptable input signal for all devices in the chain.

(2) Connect the `nCONFIG` and `MSEL[3..0]` pins to support a non-JTAG configuration scheme. If only JTAG configuration is used, connect the `nCONFIG` pin to V_{CC}, and the `MSEL[3..0]` pins to ground. In addition, pull `DCLK` and `DATA[0]` to either high or low, whichever is convenient on your board.

(3) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(4) All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into `TDI`, `TMS`, and `TCK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

All I/O inputs must maintain a maximum AC voltage of 4.1 V. Signals driving into `TDI`, `TMS`, and `TCK` has to fit the maximum overshoot equation outlined in "Configuration and JTAG Pin I/O Requirements" on page 10–8.

Jam STAPL

Jam STAPL, JEDEC standard JESD-71, is a standard file format for in-system programmability (ISP) purposes. Jam STAPL supports programming or configuration of programmable devices and testing of electronic systems, using the IEEE 1149.1 JTAG interface. Jam STAPL is a freely licensed open standard.

The Jam Player provides an interface for manipulating the IEEE Std. 1149.1 JTAG TAP state machine.

For more information about JTAG and Jam STAPL in embedded environments, refer to the *AN 122: Using Jam STAPL for ISP and ICR via an Embedded Processor*. To download the jam player, visit the Altera web site at **www.altera.com.**

Configuring Cyclone III Devices with JRunner

The JRunner software driver supports the EP3C25 device. The support for other Cyclone III devices will be available soon. Contact Altera Technical Support for more information.

JRunner is a software driver that allows you to configure Cyclone III devices through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in RBF format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II

software. JRunner is targeted for embedded JTAG configuration. The source code has been developed for the Windows NT operating system (OS). You can customize the code to make it run on your embedded platform.

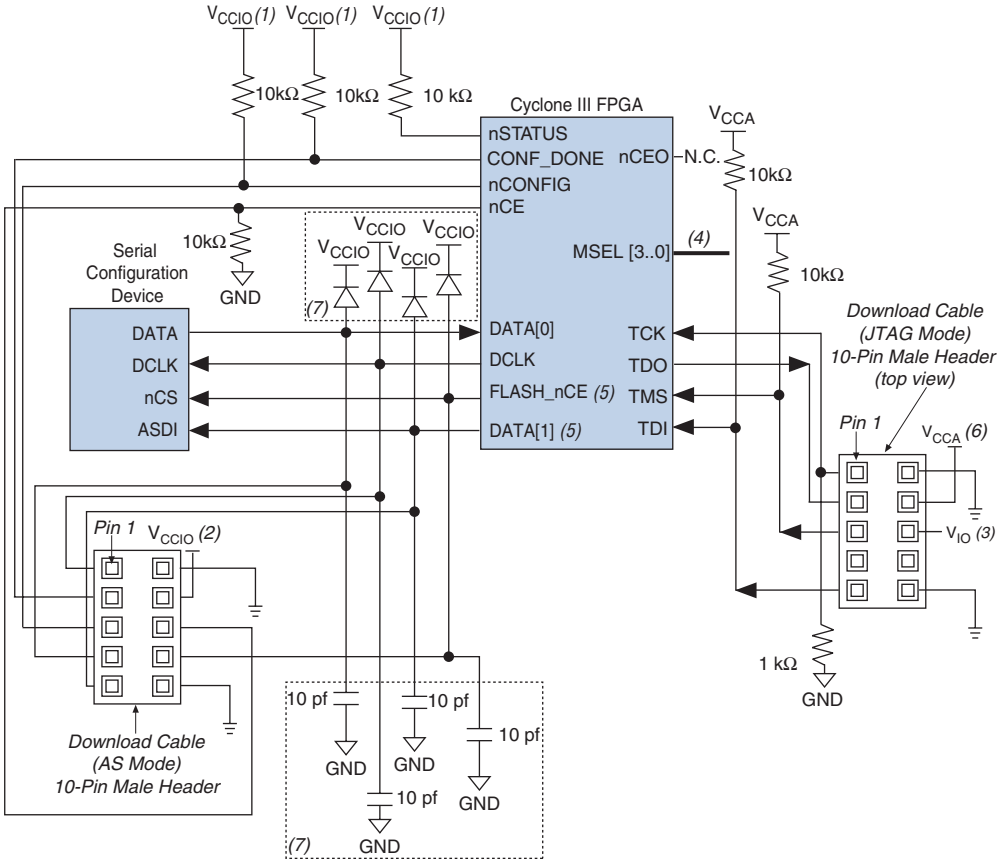
The RBF used by the JRunner software driver can not be a compressed RBF because JRunner uses JTAG-based configuration. During JTAG-based configuration, the real-time decompression feature is not available.

For more information about the JRunner software driver, refer to the *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration* application note and the source files on the Altera web site at **www.altera.com**.

Combining JTAG and Active Serial Configuration Schemes

You can combine the AS configuration scheme with JTAG-based configuration (Figure 10–28). This setup uses two 10-pin download cable headers on the board. One download cable is used in JTAG mode to configure the Cyclone III device directly via the JTAG interface. The other download cable is used in AS mode to program the serial configuration device in-system via the AS programming interface. The `MSEL[3..0]` pins should be set to select the AS configuration mode (refer to Table 10–6 on page 10–9). If you try configuring the device using both schemes simultaneously, JTAG configuration takes precedence and AS configuration terminates.

Figure 10–28. Combining JTAG and AS Configuration Schemes



Notes to Figure 10–28:

(1) Connect these pull-up resistors to the V_{CCIO} supply of the bank in which the pin resides.

(2) Power up the ByteBlaster II or USB Blaster cable's V_{CC} with the V_{CCIO} supply.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6 on page 10–9 for AS Configuration Schemes. Connect the `MSEL` pins directly to V_{CCA} or GND.

(5) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

(6) Power up the ByteBlaster II, USB Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value.

(7) The diodes and capacitors must be placed as close as possible to the Cyclone III device.

Programming Serial Configuration Devices In-System Using the JTAG Interface

Cyclone III devices in a single device chain or in a multiple device chain support in-system programming of a serial configuration device using the JTAG interface via the serial flash loader design. The board's intelligent host or download cable can use the four JTAG pins on the Cyclone III device to program the serial configuration device in system, even if the host or download cable cannot access the configuration device's configuration pins (`DCLK`, `DATA`, `ASDI`, and `nCS` pins).

The serial flash loader design is a JTAG-based in-system programming solution for Altera serial configuration devices. The serial flash loader is a bridge design for the Cyclone III device that uses its JTAG interface to access the EPCS JIC (JTAG Indirect Configuration Device Programming) file and then uses the AS interface to program the EPCS device. Both the JTAG interface and AS interface are bridged together inside the serial flash loader design.

In a multiple device chain, you only need to configure the master Cyclone III device which is controlling the serial configuration device. The slave devices in the multiple device chain which are configured by the serial configuration device do not need to be configured when using this feature. To use this feature successfully, set the `MSEL[3..0]` pins of the master Cyclone III device to select the AS configuration scheme (refer to Table 10–6).

The serial configuration device in-system programming through the Cyclone III JTAG interface has three stages, which are described in the following sections.

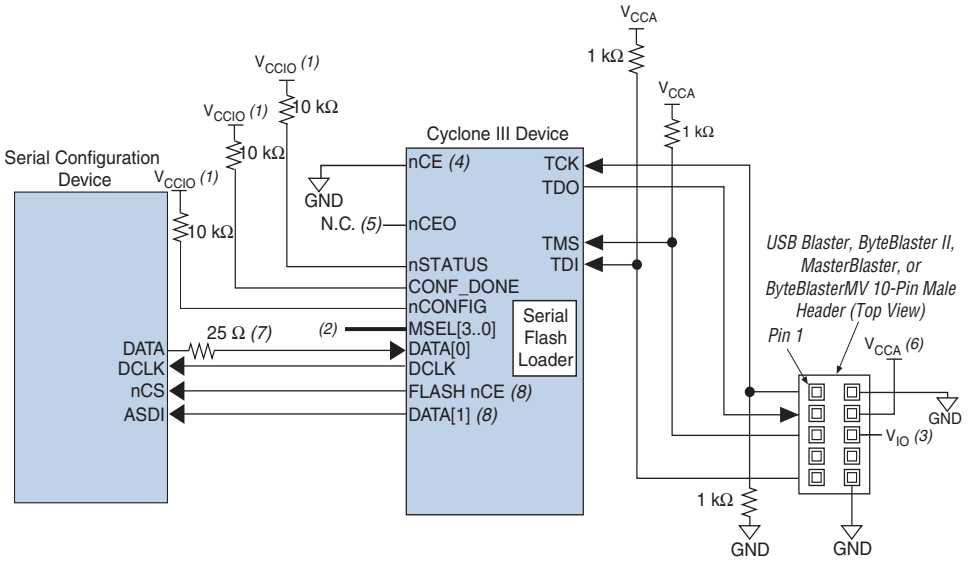
Loading the Serial Flash Loader Design

The serial flash loader design is a design inside the Cyclone III device that bridges the JTAG interface and AS interface inside the Cyclone III device using glue logic.

The intelligent host uses the JTAG interface to configure the master Cyclone III device with a serial flash loader design. The serial flash loader design allows the master Cyclone III device to control the access of four serial configuration device pins, also known as the Active Serial Memory Interface (ASMI) pins, through the JTAG interface. The `ASMI` pins are serial clock input (`DCLK`), serial data output (`DATA`), AS data input (`ASDI`), and active-low chip select (`nCS`) pins.

If you configure a master Cyclone III device with a serial flash loader design, the master Cyclone III device can enter user mode even though the slave devices in the multiple device chain are not being configured. The master Cyclone III device can enter user mode with a serial flash loader design even though the `CONF_DONE` signal is externally held low by the other slave devices in chain. Figure 10–29 shows the JTAG configuration of a single Cyclone III device with a serial flash loader design.

Figure 10–29. Programming Serial Configuration Devices In-System Using the JTAG Interface



Notes to Figure 10–29:

(1) Connect the pull-up resistors to V_{CCIO} supply of the bank in which the pin resides.

(2) The `MSEL` pin settings vary for different configuration voltage standards and POR time. To connect `MSEL[3..0]`, refer to Table 10–6 on page 10–9 for AS Configuration Schemes. Connect the `MSEL` pins directly to V_{CCA} or GND.

(3) Pin 6 of the header is a V_{IO} reference voltage for the MasterBlaster output driver. V_{IO} should match the device's V_{CCA}. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value. In the ByteBlasterMV, this pin is a no connect. In the USB-Blaster and ByteBlaster II, this pin is connected to `nCE` when it is used for AS programming, otherwise it is a no connect.

(4) `nCE` must be connected to GND or driven low for successful JTAG configuration.

(5) The `nCEO` pin can be left unconnected or used as a user I/O pin when it does not feed other device's `nCE` pin.

(6) Power up the ByteBlaster II, USB Blaster, or ByteBlasterMV cable's V_{CC} with a 2.5 V supply from V_{CCA}. Third-party programmers must switch to 2.5 V. Pin 4 of the header is a V_{CC} power supply for the MasterBlaster cable. The MasterBlaster cable can receive power from either 5.0- or 3.3-V circuit boards, DC power supply, or 5.0 V from the USB cable. Refer to the *MasterBlaster Serial/USB Communications Cable User Guide* for this value.

(7) Connect the series resistor at the near end of the serial configuration device.

(8) These are dual-purpose I/O pins. The `FLASH_nCE` pin functions as the `nCSO` pin in AS configuration scheme. The `DATA[1]` pin functions as the `ASDO` pin in AS configuration scheme.

ISP of Serial Configuration Device

In the second stage, the serial flash loader design in the master Cyclone III device allows you to write the configuration data for the device chain into the serial configuration device by using the Cyclone III JTAG interface. The JTAG interface sends the programming data for the serial configuration device to the Cyclone III device first. The Cyclone III device then uses the `ASMI` pins to transmit the data to the serial configuration device.

Reconfiguration

After all the configuration data is written into the serial configuration device successfully, the Cyclone III device does not reconfigure by itself. The intelligent host issues the `PULSE_NCONFIG` JTAG instruction to initialize the reconfiguration process. During reconfiguration, the master Cyclone III device is reset and the serial flash loader design no longer exists in the Cyclone III device and the serial configuration device configures all the devices in the chain with your user design.

For more information about the Serial FlashLoader (SFL), refer to the *AN 370: Using the Serial FlashLoader with Quartus II Software* application note on the Altera web site at **www.altera.com**.

Cyclone III JTAG Instructions

This section describes some JTAG instructions for Cyclone III devices. These instructions are CONFIG_IO, ACTIVE_DISENGAGE, ACTIVE_ENGAGE, EN_ACTIVE_CLK, DIS_ACTIVE_CLK, and APFC_BOOT_ADDR.

For information about the JTAG binary instruction code, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook.*

I/O Reconfiguration

The CONFIG_IO instruction is used to reconfigure the I/O configuration shift register (IOCSR) chain. This instruction allows you to perform board-level testing prior to configuring the Cyclone III device or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG testing is complete, the part must be reconfigured via JTAG (PULSE_NCONFIG instruction) or by pulsing nCONFIG pin low.

You can issue the CONFIG_IO instruction any time during user mode. The CONFIG_IO instruction cannot be issued while nCONFIG pin is asserted low (during power up) or immediately after issuing a JTAG instruction that triggers reconfiguration. Refer to Table 10–16 on page 10–59 on the wait-time for issuing the CONFIG_IO instruction.

You must meet the following timing restrictions when using CONFIG_IO instruction:

- CONFIG_IO instruction cannot be issued during nCONFIG pin low
- Must observe 230 µs minimum wait time after, either one of the following conditions:
  - nCONFIG pin goes high
  - issuing PULSE_NCONFIG instruction
  - issuing ACTIVE_ENGAGE instruction, before issuing CONFIG_IO instruction
- Must wait 230 µs after power up, with nCONFIG pin high before issuing CONFIG_IO instruction (or wait for nSTATUS pin goes high).

Table 10–16. Wait Time for Issuing CONFIG_IO Instruction

Wait Time	TIme
Wait time after nCONFIG pin is released.	230 µs
Wait time after PULSE_NCONFIG or ACTIVE_ENGAGE is issued	230 µs

The ACTIVE_DISENGAGE instruction can be used together with CONFIG_IO instruction to interrupt configuration. Table 10–17 shows the sequence of instructions to use for various CONFIG_IO usage scenarios.

Table 10–17. JTAG CONFIG_IO (Without JTAG_PROGRAM) Instruction Flows Note (1) (Part 1 of 2)

JTAG Instruction	Configuration scheme and current state of the Cyclone III device											
	Prior to user mode (interrupting configuration)				User mode				Power up			
	PS	FPP	AS	AP	PS	FPP	AS	AP	PS	FPP	AS	AP
ACTIVE_DISENGAGE	O	O	O	O	O	O	O	O	-	-	-	-
CONFIG_IO	R	R	R	R	R	R	R	R	NA	NA	NA	NA
JTAG Boundary Scan Instructions (no JTAG_PROGRAM)	O	O	O	O	O	O	O	O	-	-	-	-
ACTIVE_ENGAGE	A	A	R *(2)*	R *(2)*	A	A	R *(2)*	R *(2)*	-	-	-	-
PULSE_NCONFIG			A *(3)*	A *(3)*			O	O	-	-	-	-
Pulse nCONFIG pin			A *(3)*	A *(3)*			O	O	-	-	-	-

Table 10–17. JTAG CONFIG_IO (Without JTAG_PROGRAM) Instruction Flows Note (1) (Part 2 of 2)

JTAG Instruction	Configuration scheme and current state of the Cyclone III device											
	Prior to user mode (interrupting configuration)				User mode				Power up			
	PS	FPP	AS	AP	PS	FPP	AS	AP	PS	FPP	AS	AP
JTAG TAP Reset	R	R	R	R	R	R	R	R	-	-	-	-

Notes to Table 10–17:

(1) "R" indicates required, "O" indicates optional, "A" indicates any of these instructions, and "NA" indicates not allowed.

(2) Required if ACTIVE_DISENGAGE is used.

(3) Neither of the instructions is required if ACTIVE_ENGAGE is used.

The instructions ACTIVE_DISENGAGE and ACTIVE_ENGAGE are unique to Cyclone III devices, and are related to the change to CONFIG_IO instruction. Since in Cyclone III devices, the CONFIG_IO instruction does not hold nSTATUS pin low until reconfiguration, you must disengage the active configuration (AS, and AP) controllers when active configuration is interrupted. You must issue the ACTIVE_DISENGAGE instruction alone or prior to CONFIG_IO instruction if the JTAG_PROGRAM instruction is to be issued later (refer to Table 10–18). This puts the active configuration controllers into the idle state. The active configuration controller will be re-engaged once user mode is reached via JTAG programming (refer to Table 10–18).

While executing the CONFIG_IO instruction, all user IOs are tri-stated.

If reconfiguration after interruption will be done using configuration modes (rather than using JTAG_PROGRAM), then it is not necessary to issue ACTIVE_DISENGAGE instruction prior to CONFIG_IO. You can initiate reconfiguration by either pulling nCONFIG pin low for at least 500 ns, or issuing PULSE_NCONFIG instruction. In the case ACTIVE_DISENGAGE instruction was issued and JTAG_PROGRAM instruction is unsuccessful to user mode, you must issue the ACTIVE_ENGAGE instruction to reactivate the active configuration (AS, and AP) controller. Issuing ACTIVE_ENGAGE instruction will also trigger reconfiguration in configuration modes; therefore, it is not necessary to pull nCONFIG pin low or issue PULSE_NCONFIG instruction.

ACTIVE_DISENGAGE

The ACTIVE_DISENGAGE is a unique JTAG instruction on Cyclone III devices that places the active configuration (AS, and AP) controllers into an idle state prior to JTAG programming. The active configuration controllers are the AS controller when the MSEL pins are set to AS configuration scheme, and the AP controller when the MSEL pins are set to AP configuration scheme. The two purposes of placing the active controllers in an idle state is to ensure that they are not trying to configure the device in their respective configuration modes during JTAG programming and to allow the controllers to properly recognize a successful JTAG programming that results in the device reaching user mode.

The ACTIVE_DISENGAGE instruction is required before JTAG programming regardless of the current state of the Cyclone III device if the MSEL pins are set to an active configuration scheme (AS or AP). The ACTIVE_DISENGAGE instruction can be issued during a passive configuration scheme (PS, or FPP), it will just have no effect on the Cyclone III device. Similarly, the CONFIG_IO instruction can be issued after an ACTIVE_DISENGAGE instruction, but is no longer required to properly halt configuration. Refer to Table 10–18 for a summary of the required, recommended and optional instructions for each configuration mode. The ordering of the required instructions is a hard requirement and must be met to ensure functionality.

Table 10–18. JTAG Programming Instruction Flows Note (1)

JTAG Instruction	Configuration scheme and current state of the Cyclone III device											
	Prior to user mode (interrupting configuration)				User mode				Power up			
	PS	FPP	AS	AP	PS	FPP	AS	AP	PS	FPP	AS	AP
ACTIVE_DISENGAGE	O	O	R	R	O	O	O	R	O	O	R	R
CONFIG_IO	Rc	Rc	O	O	O	O	O	O	NA	NA	NA	NA
Other JTAG instructions	O	O	O	O	O	O	O	O	O	O	O	O
JTAG_PROGRAM	R	R	R	R	R	R	R	R	R	R	R	R
CHECK_STATUS	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc	Rc
JTAG_STARTUP	R	R	R	R	R	R	R	R	R	R	R	R
JTAG TAP Reset/ other instruction	R	R	R	R	R	R	R	R	R	R	R	R

Note to Table 10–18:
(1) "R" indicates required, "O" indicates optional, "Rc" indicates recommended, and "NA" indicates not allowed.

The effect of the ACTIVE_DISENGAGE instruction is similar to the AS and AP controllers. In AS or AP configuration scheme, the ACTIVE_DISENGAGE instruction will put the active configuration controllers into the idle state. If a successful JTAG programming is executed, the active controllers will automatically be re-engaged once user mode is reached via JTAG programming. This causes the active controllers to transition to their respective user mode states.

If JTAG programming is not successful in getting the Cyclone III device to user mode, and re-engage the active programming, the methods available to achieve this are different for AS and AP configuration schemes. When in AS configuration scheme, you can re-engage the AS controller either by moving the JTAG TAP controller to the reset state, or by issuing the ACTIVE_ENGAGE instruction. When in AP configuration scheme, the only way to re-engage the AP controller is to issue the ACTIVE_ENGAGE instruction. In this case, asserting the nCONFIG pin will not re-engage either active controller.

ACTIVE_ENGAGE

The ACTIVE_ENGAGE instruction enables you to re-engage an already disengaged active controller. You can issue this instruction any time during configuration or user mode to re-engage an already disengaged active controller as well as trigger reconfiguration of the Cyclone III device in active configuration scheme specified by MSEL pin settings.

The ACTIVE_ENGAGE instruction functions as PULSE_NCONFIG instruction when the device is in passive configuration schemes (PS, or FPP). The nCONFIG pin is disabled when the ACTIVE_ENGAGE instruction is issued.

You should never have to use the ACTIVE_ENGAGE instruction but it is provided as a fail-safe instruction for re-engaging the active configuration (AS, and AP) controllers.

Overriding the Internal Oscillator

This feature allows you to override the internal oscillator during active configuration scheme. The active configuration (AS, and AP) controllers use the internal oscillator as the clock source. You can change the clock source to CLKUSR through JTAG instruction.

The JTAG instructions EN_ACTIVE_CLK and DIS_ACTIVE_CLK will toggle on or off whether the active clock is sourced from the CLKUSR pin or the internal configuration oscillator. To source the active clock from the CLKUSR pin, you can issue the EN_ACTIVE_CLK instruction. This will cause the CLKUSR pin to become the active clock source. When using the EN_ACTIVE_CLK instruction, the internal oscillator must be enabled for the clock change to occur. The internal oscillator is enabled by either one of the following conditions:

- a reconfiguration event (for example driving nCONFIG low)
- remote update is enabled
- error detection is enabled

You must clock the CLKUSR pin at 2 times the expected DCLK frequency. The CLKUSR pin allows a maximum frequency of 80 MHz (40 MHz DCLK). Normally, test instruments use the CLKUSR pin when it wants to drive its own clock to control the AS state machine.

To revert the clock source back to the configuration oscillator, you can issue the DIS_ACTIVE_CLK instruction. After the DIS_ACTIVE_CLK instruction is issued, you must continue to clock the CLKUSR pin for 10 clock cycles. Otherwise, even toggling the nCONFIG pin will not revert the clock source and reconfiguration will not occur. Consequently, a power-on reset (POR) will revert the clock source back to the configuration oscillator. Toggling the nCONFIG pin or driving the JTAG state machine to the reset state will not revert the clock source.

EN_ACTIVE_CLK

The EN_ACTIVE_CLK instruction causes the CLKUSR pin signal to replace the internal oscillator as the source of clock. When using the EN_ACTIVE_CLK instruction, the internal oscillator must be enabled in order for the clock change to occur. After this instruction is issued, other JTAG instructions can be issued while CLKUSR pin signal remains as the clock source. The clock source is only reverted back to the internal oscillator by issuing the DIS_ACTIVE_CLK instruction or a power-on reset (POR).

DIS_ACTIVE_CLK

The DIS_ACTIVE_CLK instruction breaks the CLKUSR enable latch set by EN_ACTIVE_CLK instruction and cause the clock source to revert back to the internal oscillator. After the DIS_ACTIVE_CLK instruction is issued, you must continue to clock the CLKUSR pin for 10 clock cycles.

☞ The CLKUSR pin must be clocked at 2 times the expected DCLK frequency. The CLKUSR pin allows a maximum frequency of 80 MHz (40 MHz DCLK).

Changing the Start Boot Address of AP Flash

In AP configuration scheme, you can change the default configuration boot address of the parallel flash memory to any desired address using the JTAG instruction APFC_BOOT_ADDR.

APFC_BOOT_ADDR

The APFC_BOOT_ADDR instruction defines a start boot address for the parallel flash memory in the AP configuration scheme.

This instruction shifts in a start boot address for the AP flash. When this instruction becomes the active instruction, TDI and TDO are connected through a 22-bit active boot address shift register. The shifted in boot address bits get loaded into the 22-bit AP boot address update register, which feeds into the AP controller. The content of the AP boot address update register can be captured, and shifted out of the active boot address shift register from TDO.

The boot address in the boot address shift register and update register are shifted to the right (towards LSB direction) by two bits versus intended boot address. The reason for this is that the two LSB of the address are not accessible. When this boot address is fed into the AP controller, two 0's are attached in the end as least significant bits therefore pushing the shifted-in boot address to the left by two bits, which becomes the actual AP boot address the AP controller gets.

When the remote update feature is enabled, the `APFC_BOOT_ADDR` instruction sets the boot address for the factory configuration only.

The `APFC_BOOT_ADDR` instruction is retained after reconfiguration while the system board is still powered on. However, you must reprogram the instruction whenever you restart the system board.

Device Configuration Pins

The following tables describe the connections and functionality of all the configuration related pins on the Cyclone III devices. Table 10–19 summarizes the Cyclone III pin configuration.

Table 10–19. Cyclone III Configuration Pin Summary (Part 1 of 2)

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
1	FLASH_nCE, nCSO	Output		V_{CCIO}	AS, AP
6	CRC_ERROR	Output		V_{CCIO}	Optional, all modes
1	DATA[0]	Input	Yes	V_{CCIO}	PS, FPP, AS
		Bidirectional		V_{CCIO}	AP
1	DATA[1], ASDO	Input		V_{CCIO}	FPP
		Output		V_{CCIO}	AS
		Bidirectional		V_{CCIO}	AP
8	DATA[7..2]	Input		V_{CCIO}	FPP
		Bidirectional		V_{CCIO}	AP
8	DATA[15..8]	Bidirectional		V_{CCIO}	AP
6	INIT_DONE	Output		Pull-up	Optional, all modes
1	nSTATUS	Bidirectional	Yes	Pull-up	All modes
1	nCE	Input	Yes	V_{CCIO}	All modes
1	DCLK	Input	Yes	V_{CCIO}	PS, FPP
		Output		V_{CCIO}	AS, AP
6	CONF_DONE	Bidirectional	Yes	Pull-up	All modes
1	TDI	Input	Yes	V_{CCIO}	JTAG
1	TMS	Input	Yes	V_{CCIO}	JTAG
1	TCK	Input	Yes	V_{CCIO}	JTAG
1	nCONFIG	Input	Yes	V_{CCIO}	All modes
6	CLKUSR	Input		V_{CCIO}	Optional
6	nCEO	Output		V_{CCIO}	Optional, all modes
6	MSEL[3..0]	Input	Yes	V_{CCINT}	All modes
1	TDO	Output	Yes	V_{CCIO}	JTAG
7	PADD[14..0]	Output		V_{CCIO}	AP
8	PADD[19..15]	Output		V_{CCIO}	AP
6	PADD[23..20]	Output		V_{CCIO}	AP
1	nRESET	Output		V_{CCIO}	AP
6	nAVD	Output		V_{CCIO}	AP

Table 10–19. Cyclone III Configuration Pin Summary (Part 2 of 2)

Bank	Description	Input/Output	Dedicated	Powered By	Configuration Mode
6	nOE	Output		V_{CCIO}	AP
6	nWE	Output		V_{CCIO}	AP
6	RDY	Input		V_{CCIO}	AP
5	DEV_OE	Input		V_{CCIO}	Optional, AP
5	DEV_CLRn	Input		V_{CCIO}	Optional, AP

Table 10–20 describes the dedicated configuration pins, which are required to be connected properly on your board for successful configuration. Some of these pins may not be required for your configuration schemes.

Table 10–20. Dedicated Configuration Pins on the Cyclone III Device (Part 1 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
MSEL[3..0]	N/A	All	Input	4-bit configuration input that sets the Cyclone III device configuration scheme. Some of the smaller devices or package options do not support the AP configuration scheme and do not have the MSEL[3] pin. Refer to Table 10–1 for the appropriate connections. These pins must be hard-wired to V_{CCA} or GND. The MSEL[3..0] pins have internal 5-kΩ pull-down resistors that are always active.
nCONFIG	N/A	All	Input	Configuration control input. Pulling this pin low during user-mode will cause the Cyclone III device to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate a reconfiguration.
nSTATUS	N/A	All	Bidirectional open-drain	The Cyclone III device drives nSTATUS low immediately after power-up and releases it after the POR time. Status output. If an error occurs during configuration, nSTATUS is pulled low by the target device. Status input. If an external source (for example, another Cyclone III device) drives the nSTATUS pin low during configuration or initialization, the target device enters an error state. Driving nSTATUS low after configuration and initialization does not affect the configured device. If a configuration device is used, driving nSTATUS low will cause the configuration device to attempt to configure the device, but since the device ignores transitions on nSTATUS in user-mode, the device does not reconfigure. To initiate a reconfiguration, nCONFIG must be pulled low.

Table 10–20. Dedicated Configuration Pins on the Cyclone III Device (Part 2 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
CONF_DONE	N/A	All	Bidirectional open-drain	Status output. The target Cyclone III device drives the CONF_DONE pin low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, the target device releases CONF_DONE. Status input. After all data is received and CONF_DONE goes high, the target device initializes and enters user mode. The CONF_DONE pin must have an external 10-KΩ pull-up resistor in order for the device to initialize. Driving CONF_DONE low after configuration and initialization does not affect the configured device.
nCE	N/A	All	Input	Active-low chip enable. The nCE pin activates the Cyclone III device with a low signal to allow configuration. The nCE pin must be held low during configuration, initialization, and user-mode. In single device configuration, it should be tied low. In multi-device configuration, nCE of the first device is tied low while its nCEO pin is connected to nCE of the next device in the chain. The nCE pin must also be held low for successful JTAG programming of the device.
nCEO	N/A if option is on. I/O if option is off.	All	Output	Output that drives low when Cyclone III device configuration is complete. In single device configuration, you can leave this pin floating or use it as a user I/O pin after configuration. In multi-device configuration, this pin feeds the next device's nCE pin. The nCEO of the last device in the chain can be left floating or used as a user I/O pin after configuration. If you use the nCEO pin to feed next device's nCE pin, use an external 10-kΩ pull-up resistor to pull the nCEO pin high to the V_{CCIO} voltage of its I/O bank to help the internal weak pull-up resistor. Use the Quartus II software to make this pin a user I/O pin.
FLASH_nCE, nCSO	N/A in AS or AP modes. I/O in other modes	AS, AP	Output	Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE pin functions as the nCSO pin in AS mode. Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash. Connects to the CE# pin on the Intel P30 or P33 flash. In AS or AP mode, FLASH_nCE has an internal pull-up resistor that is always active.

Table 10–20. Dedicated Configuration Pins on the Cyclone III Device (Part 3 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DCLK	N/A	PS, FPP, AS, AP	Input (PS, FPP). Output (AS, AP)	In PS and FPP configuration, DCLK is the clock input used to clock data from an external source into the target Cyclone III device. Data is latched into the device on the rising edge of DCLK. In AS and AP mode, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. Optionally, in AS and AP mode, DCLK can be controlled by the core in user-mode. In AS mode, DCLK has an internal pull-up resistor (typically 25 kΩ) that is always active. After configuration, this pin is tri-stated. In schemes that use a configuration device, DCLK will be driven low after configuration is done. In schemes that use a control host, DCLK should be driven either high or low, whichever is more convenient. Toggling this pin after configuration does not affect the configured device.
DATA[0]	N/A in AS or AP modes. I/O in other modes.	PS, FPP, AS, AP	Input (PS, FPP, AS). Bidirectional open-drain (AP)	Data input. In serial configuration modes, bit-wide configuration data is presented to the target Cyclone III device on the DATA[0] pin. In AS mode, DATA[0] has an internal pull-up resistor that is always active. After AS configuration, DATA[0] is a dedicated input pin with optional user control. After PS or FPP configuration, DATA[0] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings. After AP configuration, DATA[0] is a dedicated bidirectional pin with optional user control.
DATA[1], ASDO	N/A in AS or AP modes. I/O in other modes.	FPP, AS, AP	Input (FPP). Output (AS). Bidirectional open-drain (AP)	Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0] respectively. Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. The DATA[1] pin functions as the ASDO pin in AS mode. In AS mode, DATA[1] has an internal pull-up resistor that is always active. After AS configuration, DATA[1] is a dedicated output pin with optional user control. In PS configuration scheme, DATA[1] functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA[1] is available as a user I/O pin and the state of this pin depends on the **Dual-Purpose Pin** settings. After AP configuration, DATA[1] is a dedicated bidirectional pin with optional user control.

Table 10–20. Dedicated Configuration Pins on the Cyclone III Device (Part 4 of 4)

Pin Name	User Mode	Configuration Scheme	Pin Type	Description
DATA[7..2]	N/A in AP mode. I/O in other modes.	FPP, AP	Inputs (FPP). Bidirectional open-drain (AP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target Cyclone III device on DATA[7..0] or DATA[15..0] respectively. In AS or PS configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pin depends on the **Dual-Purpose Pin** settings. After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control.
DATA[15..8]	N/A in AP mode. I/O in other modes.	AP	Bidirectional open-drain	Data inputs. Word-wide configuration data is presented to the target Cyclone III device on DATA[15..0]. In PS, FPP or AS configuration schemes, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15:8] are dedicated bidirectional pins with optional user control.
PADD[23..0]	N/A in AP mode. I/O in other modes	AP	Output	24-bit address bus from the Cyclone III device to the parallel flash in AP mode. Connects to the A[24:1] bus on the Intel P30 or P33 flash.
nRESET	N/A in AP mode. I/O in other modes	AP	Output	Active-low reset output. Driving the nRESET pin low resets the parallel flash. Connects to the RST# pin on the Intel P30 or P33 flash.
nAVD	N/A in AP mode. I/O in other modes	AP	Output	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus. Connects to the ADV# pin on the Intel P30 or P33 flash.
nOE	N/A in AP mode. I/O in other modes	AP	Output	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0] and RDY). Connects to the OE# pin on the Intel P30 or P33 flash.
nWE	N/A in AP mode. I/O in other modes	AP	Output	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid. Connects to the WE# pin on the Intel P30 or P33 flash.
RDY	N/A in AP mode. I/O in other modes	AP	Input	The current implementation for AP configuration ignores the RDY pin. However, it is recommended that you connect this pin. Connects to the WAIT pin on the Intel P30 or P33 flash.

Table 10–21 describes the optional configuration pins. If these optional configuration pins are not enabled in the Quartus II software, they are available as general-purpose user I/O pins. Therefore, during configuration, these pins function as user I/O pins and are tri-stated with weak pull-up resistors.

Table 10–21. Optional Configuration Pins

Pin Name	User Mode	Pin Type	Description
CLKUSR	N/A if option is on. I/O if option is off.	Input	Optional user-supplied clock input synchronizes the initialization of one or more devices. This pin is enabled by turning on the **Enable user-supplied start-up clock** (**CLKUSR**) option in the Quartus II software.
INIT_DONE	N/A if option is on. I/O if option is off.	Output open-drain	Status pin can be used to indicate when the device has initialized and is in user-mode. When nCONFIG is low and during the beginning of configuration, the INIT_DONE pin is tri-stated and pulled high due to an external 10-KΩ pull-up resistor. Once the option bit to enable INIT_DONE is programmed into the device (during the first frame of configuration data), the INIT_DONE pin will go low. When initialization is complete, the INIT_DONE pin will be released and pulled high and the device enters user-mode. Thus, the monitoring circuitry must be able to detect a low-to-high transition. This pin is enabled by turning on the **Enable INIT_DONE output** option in the Quartus II software.
DEV_OE	N/A if option is on. I/O if option is off.	Input	Optional pin that allows the user to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as programmed. This pin is enabled by turning on the **Enable device-wide output enable** (**DEV_OE**) option in the Quartus II software.
DEV_CLRn	N/A if option is on. I/O if option is off.	Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the **Enable device-wide reset** (**DEV_CLRn**) option in the Quartus II software.

Table 10–22 describes the dedicated JTAG pins. JTAG pins must be kept stable before and during configuration to prevent accidental loading of JTAG instructions. The TDI and TMS have weak internal pull-up resistors, while TCK has a weak internal pull-down resistor. If you plan to use the SignalTap® II Embedded Logic Array Analyzer, you need to connect the JTAG pins of the Cyclone III device to a JTAG header on your board.

Table 10–22. Dedicated JTAG Pins (Part 1 of 2)

Pin Name	User Mode	Pin Type	Description
TDI	N/A	Input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK. The TDI pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TDO	N/A	Output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device. The TDO pin is powered by V_{CCIO} in I/O bank 1. For recommendations on connecting a JTAG chain with multiple voltages across the devices in the chain, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by leaving this pin unconnected.

Table 10–22. Dedicated JTAG Pins (Part 2 of 2)

Pin Name	User Mode	Pin Type	Description
TMS	N/A	Input	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur on the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. The TMS pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting this pin to V_{CC}.
TCK	N/A	Input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. The TCK pin is powered by the V_{CCIO} supply. If the JTAG interface is not required on the board, the JTAG circuitry can be disabled by connecting TCK to GND.

Conclusion

Cyclone III devices can be configured in a number of different schemes to fit your system's need. In addition, configuration data decompression and remote system upgrade support supplement the Cyclone III configuration solution.

Referenced Documents

This chapter references the following documents:

- *Serial Configuration Devices (EPCS1, EPCS4, EPCS16 and EPCS64) Data Sheet* chapter in volume 2 of the *Configuration Handbook*
- *Remote System Upgrade* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Software Settings* section in volume 2 of the *Configuration Handbook*
- *Hot Socketing and Power-On Reset* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Debugging Configuration Problems* chapter in volume 2 of the *Configuration Handbook*
- *USB-Blaster Download Cable User Guide*
- *ByteBlaster II Download Cable User Guide*
- *AN 418: SRunner: An Embedded Solution for Serial Configuration Device Programming*
- *AN 386: Using the Parallel Flash Loader with the Quartus II Software*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*
- *Configuring Mixed Altera FPGA Chains* in volume 2 of the *Configuration Handbook*
- *AN 423: Configuring the MicroBlaster Passive Serial Software Driver*
- *MasterBlaster Serial/USB Communications Cable User Guide*
- *ByteBlasterMV Download Cable User Guide*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing* chapter in volume 1 of the *Cyclone III Device Handbook*
- *AN 122: Using Jam STAPL for ISP and ICR via an Embedded Processor*
- *AN 414: JRunner Software Driver: An Embedded Solution for PLD JTAG Configuration*
- *AN 370: Using the Serial FlashLoader with the Quartus II Software*

Document Revision History

Table 10–23 shows the revision history for this document.

Table 10–23. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "Configuration Devices" section. • Removed references to Spansion in Table 10–1, Table 10–4, Table 10–5, Table 10–8, Table 10–9, Table 10–20, "AP Configuration Supported Flash Memories", "Single Device AP Configuration", and "Programming Parallel Flash Memories" sections. • Changed V_{CCIO} to V_{CCA} for MSEL pin connection in "Configuration Schemes" section, in footnotes to Table 10–1, Figure 10–3, Figure 10–4, Figure 10–5, Figure 10–6, Figure 10–7, Figure 10–8, Figure 10–9, Figure 10–10, Figure 10–11, Figure 10–14, Figure 10–15, Figure 10–17, Figure 10–18, Figure 10–19, Figure 10–20, Figure 10–21, Figure 10–28, Figure 10–29, and in MSEL[3..0] row in Table 10–20. • Updated "Configuration Schemes" section. • Updated Table 10–6 with *Note (5)*. • Updated "Programming Serial Configuration Devices" section. • Updated *Note (6)* to Figure 10–7. • Updated Figure 10–8. • Deleted version 1.0 Figure10-9. • Updated Figure 10–9. • Updated "Word-Wide Multi-Device AP Configuration" section. • Updated Figure 10–10 and Figure 10–11. • Updated "Programming Parallel Flash Memories" section. • Updated Figure 10–12 and added *Note (1)*. • Added *Note (4)* to Table 10–10. • Added *Note (4)* to Table 10–12. • Updated "JTAG Configuration" section. • Added Figure 10–24 and Figure 10–26. • Updated Figure 10–25. • Updated "Configuring Cyclone III Devices with JRunner" section. • Aded new "Programming Serial Configuration Devices In-System Using the JTAG Interface" section with Figure 10–29. • Updated Table 10–17. • Added chapter TOC and "Referenced Documents" section.	• Removed support for Spansion S29WS-N flash memory. • Added information about the default AP configuration boot address in Quartus II software. • Added information about JTAG configuration. When using different VCCIO voltages, user must power up the download cable's VCC with the specific recommended voltage. • Added information about programming serial configuration devices in-system using the JTAG interface (SFL approach). • Changed V_{CCIO} to V_{CCA} for MSEL pin connection.
March 2007 v1.0	Initial Release.	N/A

11. Hot Socketing and Power-On Reset in Cyclone III Devices

CIII51011-1.1

Introduction

Cyclone® III devices offer hot socketing, also known as hot plug-in, hot insertion, or hot swap, and power sequencing support without the use of any external devices. You can insert or remove a Cyclone III board in a system during system operation without causing undesirable effects to the board or to the running system bus.

The hot socketing feature removes complexity when using Cyclone III devices on printed circuit boards (PCBs) containing a mixture of 3.0, 3.3, 2.5, 1.8, 1.5, and 1.2 V devices. With the Cyclone III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

The Cyclone III hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter also discusses the power-on reset (POR) circuitry in Cyclone III devices. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

This chapter contains the following sections:

- "Cyclone III Hot-Socketing Specifications" on page 11–1
- "Hot-Socketing Feature Implementation in Cyclone III Devices" on page 11–2
- "Power-On Reset Circuitry" on page 11–4

Cyclone III Hot-Socketing Specifications

Cyclone III devices offer hot-socketing capability with all three features listed above without any external components or special design requirements. The hot-socketing feature in Cyclone III devices offers the following:

- The device can be driven before power-up without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.

Devices Can Be Driven Before Power-Up

You can drive signals into the I/O pins, dedicated input pins, and dedicated clock pins of Cyclone III devices before or during power-up or power-down without damaging the device. Cyclone III devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design.

I/O Pins Remain Tri-Stated During Power-Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot-socketing situation, the output buffers of the Cyclone III device are turned off during system power-up or power-down. A Cyclone III device also does not drive out until the device is configured and has attained proper operating conditions. The I/O pins are tri-stated until the device enters user mode with a weak pull-up resistor (R) to V_{CCIO}. Refer to Figure 11–1 for more information.

You can power up or power down the V_{CCIO}, V_{CCA}, and V_{CCINT} pins in any sequence. The V_{CCIO}, V_{CCA}, and V_{CCINT} must have monotonic rise to their steady state levels. (Refer to Figure 11–3 for more information.) The maximum power ramp rate for fast POR time is 3 ms, and 50 ms for standard POR time, respectively. The minimum power ramp rate is 50 µs. V_{CCIO} for all I/O banks should be powered-up during device operation. All V_{CCA} pins must be powered to 2.5-V (even when PLLs are

not used), and must be powered-up and powered-down at the same time. V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Cyclone III devices meet the following hot socketing specification:

- The hot-socketing DC specification is $| I_{IOPIN} | < 300$ uA.
- The hot-socketing AC specification is $| I_{IOPIN} | < 8$ mA for the ramp rate of 10 ns or more.

For ramp rates faster than 10 ns on I/O pins, $|I_{IOPIN}|$ can be obtained with the equation I = C dv/dt, where C is the I/O pin capacitance and dv/dt is the slew rate. The hot-socketing specification takes into account the pin capacitance but not board trace and external loading capacitance. You must consider additional or separate capacitance for trace, connector, and loading.

I_{IOPIN} is the current for any user I/O pin on the device. The DC specification applies when all V_{CC} supplied to the device is stable in the powered-up or powered-down conditions.

A possible concern for semiconductor devices in general regarding hot socketing is the potential for latch-up. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins may be connected and driven by the active system before the power supply can provide current to the device's V_{CC} and ground planes. This condition can lead to latch-up and cause a low-impedance path from V_{CC} to ground within the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

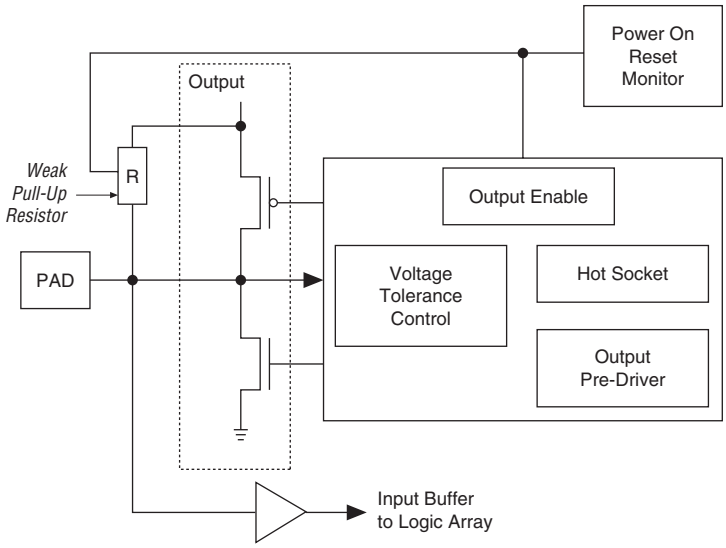
By design of the I/O buffers and hot socketing circuitry, Altera® ensures that Cyclone III devices are immune to latch-up during hot socketing.

Hot-Socketing Feature Implementation in Cyclone III Devices

The hot-socketing feature disables the output buffer during power-up (either V_{CCINT} or V_{CCIO} supplies) or power-down. The hot-socket circuit generates an internal `HOTSCKT` signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage. Designs cannot use the `HOTSCKT` signal for other purposes. The `HOTSCKT` signal cuts off the output buffer to ensure that no DC current (except for weak pull-up leakage current) leaks through the pin. When V_{CC} ramps up slowly, V_{CC} is still relatively low, even after the internal `POR` signal (not available to the FPGA fabric used by customer designs) is released and the configuration is finished. The `CONF_DONE`, `nCEO`, and `nSTATUS` pins would fail to respond, as the output buffer cannot drive out because the hot-socketing circuitry keeps the I/O pins tri-stated at this low V_{CC} voltage. Therefore, the hot-socketing circuit has been removed on these configuration output or bidirectional pins to ensure that they are operational during configuration. These pins are expected to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 11–1.

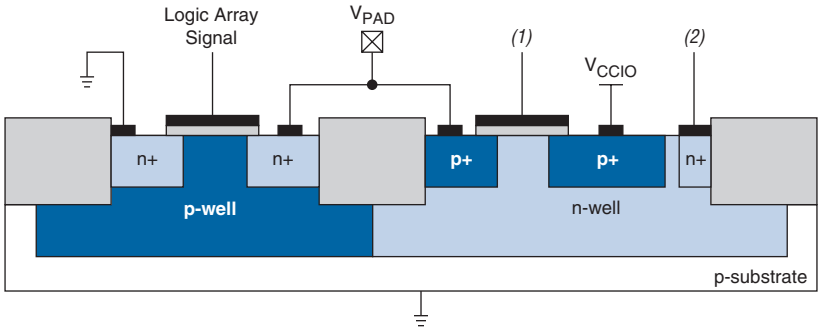
Figure 11–1. Hot Socketing Circuit Block Diagram for Cyclone III Devices



The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCA}. voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} keeps the I/O pins from floating. The voltage tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

Figure 11–2 shows a transistor level cross section of the Cyclone III device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot socketing. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} during hot socketing. The V_{PAD} leakage current charges the voltage tolerance control circuit capacitance.

Figure 11–2. Transistor Level Diagram of FPGA Device I/O Buffers



Note to Figure 11–2:

(1) This is the logic array signal or the larger of either the V_{CCIO} or V_{PAD} signal.

(2) This is the larger of either the V_{CCIO} or V_{PAD} signal.

Power-On Reset Circuitry

Cyclone III devices contain POR circuitry to keep the device in a reset state until the power supply voltage levels have stabilized during power-up. The POR circuit monitors the V_{CCINT}, V_{CCIO}, and V_{CCA} pin and tri-states all user I/O pins until the V_{CC} reaches the recommended operating levels. In addition, the POR circuitry also ensures the V_{CCIO} level of I/O banks 1, 6, 7, and 8 that contains configuration pins reach an acceptable level before configuration is triggered.

After the Cyclone III device enters user mode, the POR circuit continues to monitor the V_{CCINT} and V_{CCA} pin so that a brown-out condition during user mode can be detected. If the V_{CCINT} and V_{CCA} voltage sags below the POR trip point during user mode, the POR circuit resets the device. If the V_{CCIO} voltage sags during user mode, the POR circuit does not reset the device.

Wake-Up Time for Cyclone III Devices

In some applications, it may be necessary for a device to wake up very quickly in order to begin operation. The Cyclone III device offers the Fast-On feature to support fast wake-up time applications. For Cyclone III devices, `MSEL[3..0]` pin settings determine the POR time (t_{POR}) of the device. The fast POR ranges from 3 ms to 9 ms while the standard POR ranges from 50 ms to 200 ms.

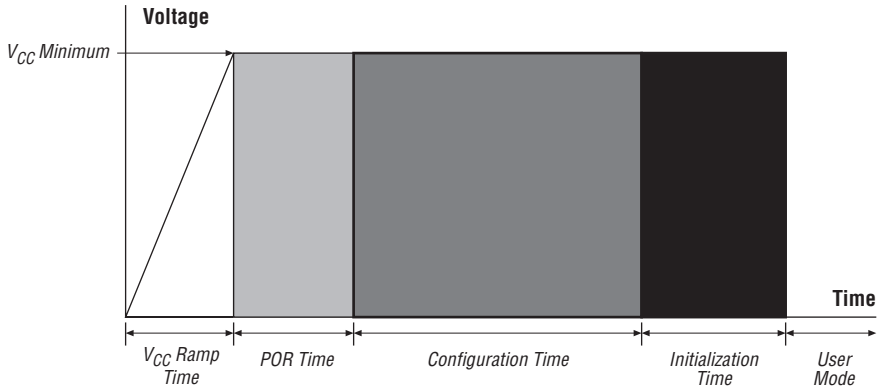
For more information about the `MSEL[3..0]` pin settings, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

For Cyclone III devices, wake-up time consists of power-up, POR, configuration, and initialization. The device must properly go through all four stages to configure correctly and begin operation. You can calculate wake-up time using equation 1:

$$\text{Wake-up Time} = V_{CC}\ \text{Ramp Time} + POR\ \text{Time} + \text{Configuration Time} + \text{Initialization Time} \quad (1)$$

Figure 11–3 illustrates the components of wake-up time.

Figure 11–3. Cyclone III Wake-Up Time



Note to Figure 11–3:
(1) V_{CC} ramp must be monotonic.

The V_{CC} ramp time and POR time depend on the power supply used in your system and the device `MSEL[3..0]` pin settings.

Configuration time depends on the configuration scheme you chose and the configuration file size. You can calculate configuration time by multiplying the number of bits in the configuration file with the period of the configuration clock. For fast configuration times, you should either use a fast passive parallel (FPP) configuration scheme with maximum DCLK frequency of 100 MHz or an active parallel (AP) configuration scheme with maximum DCLK frequency of 40 MHz. In addition, you can

use passive serial (PS) with compression to reduce the configuration file size and speed up the configuration time. Passive parallel configuration mode does not support compression. The t_{CD2UM} or t_{CD2UMC} parameters determine the initialization time.

For more information about the t_{CD2UM} or t_{CD2UMC} parameters and configuration schemes, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

If you cannot meet the maximum V_{CC} ramp time requirement, you must use an external component to hold `nCONFIG` low until the power supplies have reached their minimum recommended operating levels. Otherwise, the device may not properly configure and enter user mode.

Conclusion

Cyclone III devices offer hot socketing allowing the device to power-up successfully without any power-sequencing. The POR circuitry keeps the devices in the reset state until the V_{CC} is within operating range.

Referenced Documents

This chapter references the following document:

- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 11–1 shows the revision history for this document.

Table 11–1. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "I/O Pins Remain Tri-Stated During Power-Up" section. • Updated Figure 11–3. • Added chapter TOC and "Referenced Documents" section.	Added information that the power supply voltages must rise monotonically to their steady state levels.
March 2007 v1.0	Initial Release.	—

12. Remote System Upgrade With Cyclone III Devices

CIII51012-1.1

Introduction

System designers face difficult challenges such as shortened design cycles, evolving standards, and system deployments in remote locations. Cyclone® III devices help overcome these challenges with their inherent re-programmability and dedicated circuitry to perform remote system upgrades. Remote system upgrades help deliver feature enhancements and bug fixes without costly recalls, reduce time-to-market, and extend product life.

Cyclone III devices feature dedicated remote system update circuitry. Soft logic (either the Nios II® embedded processor or user logic) implemented in a Cyclone III device can download a new configuration image from a remote location, store it in configuration memory (such as a serial configuration device), and direct the dedicated remote system update circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to Cyclone III devices and helps to avoid system downtime.

Remote system upgrade is supported in Cyclone III active serial (AS) and active parallel (AP) configuration schemes. Remote system upgrade can also be implemented in conjunction with advanced Cyclone III features such as real-time decompression of configuration data in an AS configuration scheme.

This chapter describes the functionality and implementation of the dedicated remote system upgrade circuitry. It also defines several concepts related to remote system upgrade, including factory configuration, application configuration, remote update mode, and user watchdog timer.

This chapter contains the following sections:

- "Functional Description" on page 12–1
- "Enabling Remote Update" on page 12–3
- "Remote System Upgrade Mode" on page 12–4
- "Dedicated Remote System Upgrade Circuitry" on page 12–6
- "Quartus II Software Support" on page 12–12

Functional Description

The dedicated remote system upgrade circuitry in Cyclone III devices manages remote configuration and provides error detection, recovery, and status information. User logic or a Nios II processor implemented in the Cyclone III device logic array provides access to the remote configuration data source and an interface to the system's configuration memory.

The Cyclone III device's remote system upgrade process involves the following steps:

1. A Nios II processor (or user logic) implemented in the Cyclone III device logic array receives new configuration data from a remote location. The connection to the remote source is a communication protocol such as the transmission control protocol/Internet protocol (TCP/IP), peripheral component interconnect (PCI), user datagram protocol (UDP), universal asynchronous receiver/transmitter (UART), or a proprietary interface.

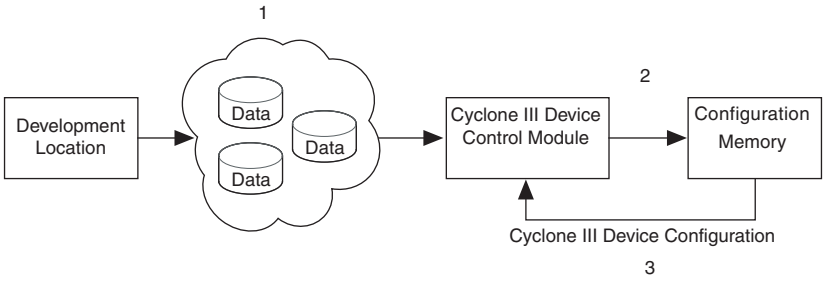
2. The Nios II processor (or user logic) writes this new configuration data into a non-volatile configuration memory. The non-volatile configuration memory can be the serial configuration device (in the AS configuration scheme), or the supported parallel flash memory (in the AP configuration scheme).

3. The Nios II processor (or user logic) initiates a reconfiguration cycle with the new or updated configuration data.

4. The dedicated remote system upgrade circuitry detects and recovers from any error that might occur during or after the reconfiguration cycle, and provides error status information to the user design.

Figure 12–1 shows the steps required for performing remote configuration updates. (The numbers in the figure below coincide with the steps above.)

Figure 12–1. Functional Diagram of Cyclone III Remote System Upgrade

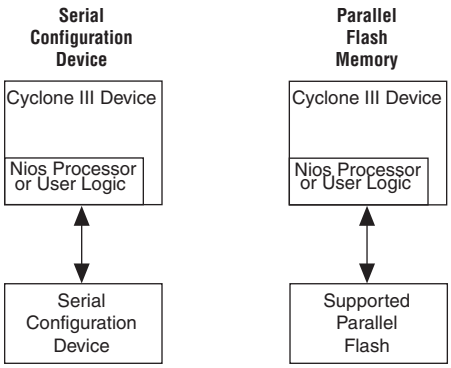


Cyclone III devices only support remote system upgrade in the AS and AP configuration schemes.

- The serial configuration device uses the AS configuration scheme to configure the Cyclone III device.
- The supported parallel flash uses the AP configuration scheme to configure the Cyclone III device.

Figure 12–2 shows the block diagrams for implementing remote system upgrade with the Cyclone III AS and AP configuration schemes.

Figure 12–2. Remote System Upgrade Block Diagrams for Cyclone III AS and AP Configuration Schemes



Remote system upgrade only supports single device configuration.

For information about programming the serial configuration device or programming the supported parallel flash memory, refer to the *Configuring Cyclone III Devices* chapter of the *Cyclone III Device Handbook*.

You must set the mode select pins (`MSEL[3..0]`) to the AS or AP configuration scheme to use the remote system upgrade in your system. The `MSEL` pin settings in remote system upgrade mode is the same as in the standard configuration mode. Standard configuration mode refers to normal Cyclone III device configuration mode with no support for remote system upgrades, and the remote

system upgrade circuitry is disabled. When using remote system upgrade in Cyclone III devices, you must enable the remote update mode option setting in the Quartus® II software. Refer to"Enabling Remote Update" on page 12–3.

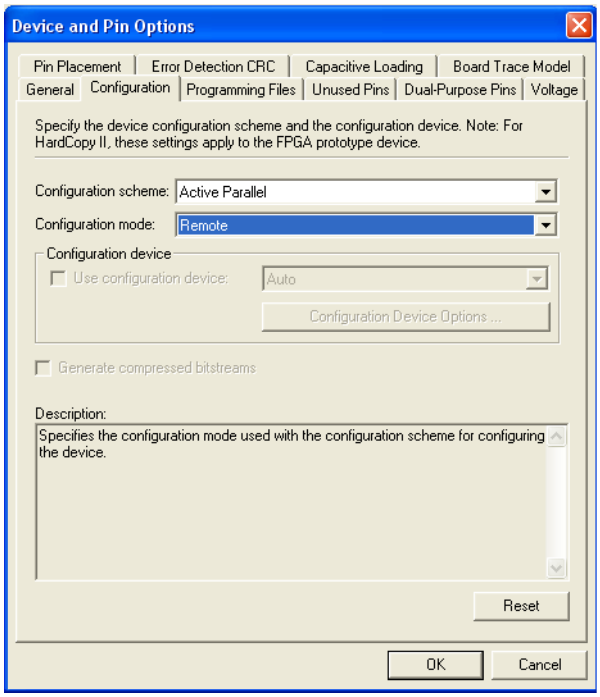
For more information about standard configuration schemes supported in Cyclone III devices, refer to the *Configuring Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

Enabling Remote Update

You can enable or disable remote update for Cyclone III devices in the Quartus II software before design compilation (in the Compiler Settings menu). To enable remote update in the project's compiler settings, perform the following steps in the Quartus II software:

1. On the Assignments menu, click **Device**. The **Settings** dialog box appears.
2. Click **Device & Pin Options**. The **Device & Pin Options** dialog box appears.
3. Click the **Configuration** tab.
4. From the **Configuration Mode** list, select **Remote** (Figure 12–3).
5. Click **OK**.
6. In the Settings dialog box, click **OK**.

Figure 12–3. Enabling Remote Update for Cyclone III Devices in Compiler Settings



Configuration Image Types

When using remote system upgrade, Cyclone III device configuration bitstreams are classified as factory configuration images or application configuration images. An image, also referred to as a configuration, is a design loaded into the device that performs certain user-defined functions. Each device in your system requires one factory image or with addition of one or more application images. The factory image is a user-defined fall-back, or safe, configuration and is responsible for

administering remote updates in conjunction with the dedicated circuitry. Application images implement user-defined functionality in the target Cyclone III device. You may include the default application image functionality in the factory image.

A remote system update involves storing a new application configuration image or updating an existing one via the remote communication interface. After an application configuration image is stored or updated remotely, the user design in the Cyclone III device initiates a reconfiguration cycle with the new image. Any errors during or after this cycle are detected by the dedicated remote system upgrade circuitry, and cause the device to automatically revert to the factory image. The factory image then performs error processing and recovery. While error processing functionality is limited to the factory configuration, both factory and application configurations can download and store remote updates and initiate system reconfiguration.

Remote System Upgrade Mode

The remote update mode allows you to determine the functionality of your system upon power up and offer various features.

Overview

In remote update mode, the Cyclone III device loads the factory configuration image upon power up. The user-defined factory configuration determines which application configuration is to be loaded and triggers a reconfiguration cycle. The factory configuration can also contain application logic.

When used with serial configuration devices or with supported parallel flash memories, the remote update mode allows an application configuration to start at any flash sector boundary. Additionally, the remote update mode features a user watchdog timer that can detect functional errors in an application configuration.

Remote Update Mode

When a Cyclone III device is first powered up in remote update in the AS configuration scheme, it loads the factory configuration located at address `boot_address[23:0] = 24b'0`. You should always store the factory configuration image for your system at boot address `24b'0` when using the AS configuration scheme. A factory configuration image is a bitstream for the Cyclone III device(s) in your system that is programmed during production and is the fall-back image when an error occurs. This image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the start address location 0x000000 in the serial configuration device.

Upon power up in remote update in the AP configuration scheme, the Cyclone III device loads the default factory configuration located at address:

```
boot_address[23:0] = 24'h010000 = 24'b1 0000 0000 0000 0000
```

You can change the default factory configuration address to any desired address using the JTAG instruction `APFC_BOOT_ADDR`. The factory configuration image is stored in non-volatile memory and is never updated or modified using remote access. This corresponds to the default start address location 0x010000 represented in 16-bit word addressing (or the updated address if the default address is changed) in the supported parallel flash memory.

For information about the application of the JTAG instruction `APFC_BOOT_ADDR` in AP configuration scheme, refer to the *Configuring Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

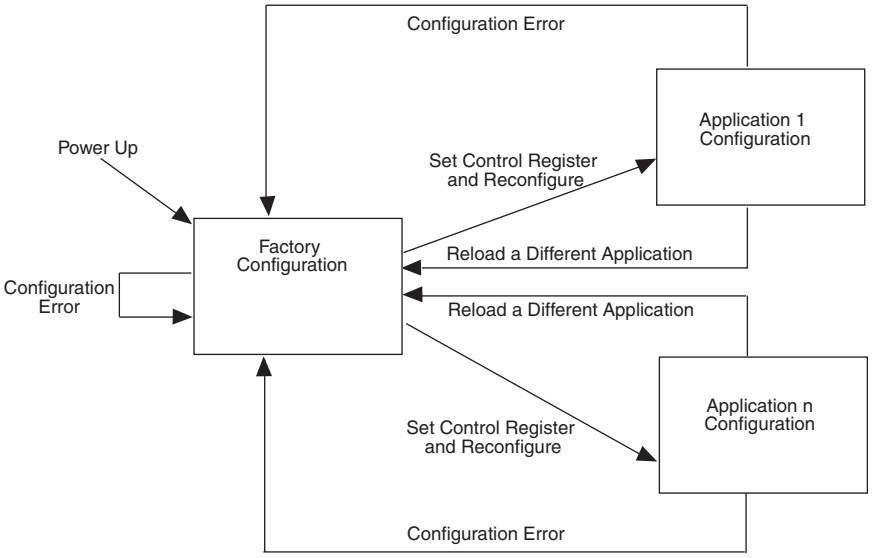
The factory configuration image is user designed and contains soft logic to:

- Process any errors based on status information from the dedicated remote system upgrade circuitry
- Communicate with the remote host and receive new application configurations, and store this new configuration data in the local non-volatile memory device
- Determine which application configuration is to be loaded into the Cyclone III device
- Enable or disable the user watchdog timer and load its time-out value (optional).

- Instruct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle

Figure 12–4 shows the transitions between the factory and application configurations in remote update mode.

Figure 12–4. Transitions Between Configurations in Remote Update Mode



After power up or a configuration error, the factory configuration logic writes the remote system upgrade control register to specify the address of the application configuration to be loaded. The factory configuration also specifies whether or not to enable the user watchdog timer for the application configuration and, if enabled, specify the timer setting.

The user watchdog timer ensures that the application configuration is valid and functional. After confirming the system is healthy, the user-designed application configuration must reset the timer periodically during user-mode operation of an application configuration. This timer reset logic should be a user-designed hardware and/or software health monitoring signal that indicates error-free system operation. If the user application configuration detects a functional problem or if the system hangs, the timer is not reset in time and the dedicated circuitry updates the remote system upgrade status register, triggering the device to load the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

☞ Only valid application configurations designed for remote update mode include the logic to reset the timer in user mode.

For more information about the user watchdog timer, refer to the "User Watchdog Timer" on page 12–11.

If there is an error while loading the application configuration, the remote system upgrade status register is written by the Cyclone III device's dedicated remote system upgrade circuitry, specifying the cause of the reconfiguration. The following actions cause the remote system upgrade status register to be written:

- `nSTATUS` driven low externally
- Internal `CRC` error
- User watchdog timer timeout
- A configuration reset (logic array `nCONFIG` signal or external `nCONFIG` pin assertion)

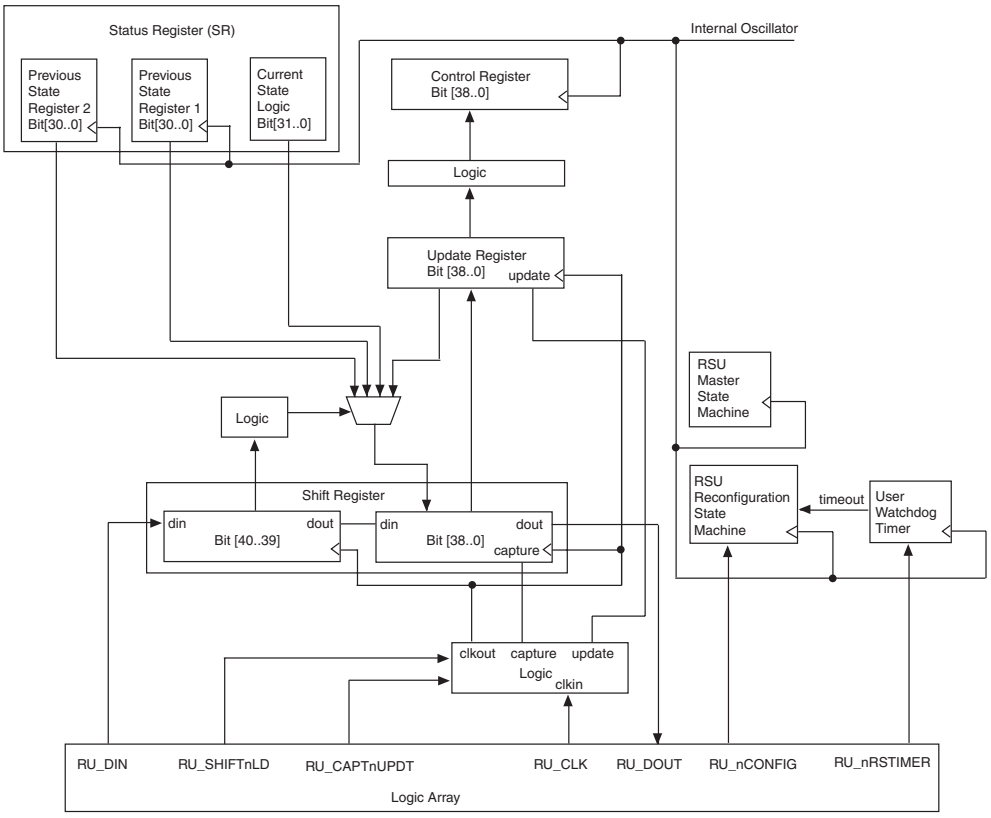
Cyclone III devices automatically load the factory configuration located at address `boot_address[23:0] = 24'b0` for the AS configuration scheme, and default address `boot_address[23:0] = 24'h010000` (or the updated address if the default address is changed) for the AP configuration scheme. This user-designed factory configuration reads the remote system upgrade status register to determine the reason for reconfiguration. Then the factory configuration takes the appropriate error recovery steps and writes to the remote system upgrade control register to determine the next application configuration to be loaded.

When Cyclone III devices successfully load the application configuration, they enter into user mode. In user mode, the soft logic (Nios II processor or state machine and the remote communication interface) assists the Cyclone III device in determining when a remote system update is arriving. When a remote system update arrives, the soft logic receives the incoming data, writes it to the configuration memory device, and triggers the device to load the factory configuration. The factory configuration reads the remote system upgrade status register, determines the valid application configuration to load, writes the remote system upgrade control register accordingly, and initiates system reconfiguration.

Dedicated Remote System Upgrade Circuitry

This section explains the implementation of the Cyclone III remote system upgrade dedicated circuitry. The remote system upgrade circuitry is implemented in hard logic. This dedicated circuitry interfaces to the user-defined factory application configurations implemented in the Cyclone III device logic array to provide the complete remote configuration solution. The remote system upgrade circuitry contains the remote system upgrade registers, a watchdog timer, and state machines that control those components. Figure 12–5 shows the remote system upgrade block's data path.

Figure 12–5. Remote System Upgrade Circuit Data Path *Note (1)*



Note to Figure 12–5:

(1) `RU_DOUT`, `RU_SHIFTnLD`, `RU_CAPTnUPDT`, `RU_CLK`, `RU_DIN`, `RU_nCONFIG`, and `RU_nRSTIMER` signals are internally controlled by the altremote_update megafunction.

Remote System Upgrade Registers

The remote system upgrade block contains a series of registers that store the configuration addresses, watchdog timer settings, and status information. These registers are detailed in Table 12–1.

Table 12–1. Remote System Upgrade Registers

Register	Description
Shift register	This register is accessible by the logic array and allows the update, status, and control registers to be written and sampled by user logic. Write access is enabled in remote update mode for factory configurations to allow writes to the update register. Write access is disabled for all application configurations in remote update mode.
Control register	This register contains the current configuration address, the user watchdog timer settings, one option bit for checking early `CONF_DONE`, and one option bit for selecting the internal oscillator as the startup state machine clock. During a read operation in an application configuration, this register is read into the shift register. When a reconfiguration cycle is initiated, the contents of the update register are written into the control register.
Update register	This register contains data similar to that in the control register. However, it can only be updated by the factory configuration by shifting data into the shift register and issuing an update operation. When a reconfiguration cycle is triggered by the factory configuration, the control register is updated with the contents of the update register. During a read in a factory configuration, this register is read into the shift register.
Status register	This register is written to by the remote system upgrade circuitry on every reconfiguration to record the cause of the reconfiguration. This information is used by the factory configuration to determine the appropriate action following a reconfiguration. During a capture cycle, this register is read into the shift register.

The remote system upgrade control and status registers are clocked by the 10-MHz internal oscillator (the same oscillator that controls the user watchdog timer). However, the remote system upgrade shift and update registers are clocked by the user clock input (`RU_CLK`).

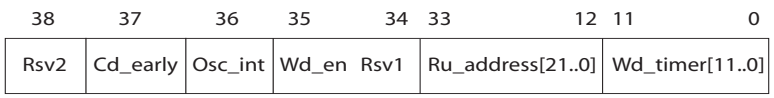
Remote System Upgrade Control Register

The remote system upgrade control register stores the application configuration address, the user watchdog timer settings, and option bits for application configuration. In remote update mode for the AS configuration scheme, the control register address bits are set to all zeros (`24'b0`) at power up to load the AS factory configuration. In remote update mode for the AP configuration scheme, the control register address bits are set to `24'h010000` (24'b1 0000 0000 0000 0000) at power up to load the AP default factory configuration. However, for the AP configuration scheme, you can change the default factory configuration address to any desired address using the JTAG instruction `APFC_BOOT_ADDR`. Additionally, a factory configuration in remote update mode has write access to this register.

For information about the application of the JTAG instruction `APFC_BOOT_ADDR` in the AP configuration scheme, refer to the *Configuring Cyclone III Devices* chapter in the *Cyclone III Device Handbook*.

The control register bit positions are shown in Figure 12–6 and defined in Table 12–2. In the figure, the numbers show the bit position of a setting within a register. For example, bit number 35 is the enable bit for the watchdog timer.

Figure 12–6. Remote System Upgrade Control Register



The early CONF_DONE check (Cd_early) option bit, when enabled, ensures that there is a valid configuration at the boot address specified by the factory configuration and that it is of the proper size. The internal oscillator as startup state machine clock (Osc_int) option bit, when enabled, ensures a functional startup clock to eliminate the hanging of startup. When all option bits are turned on, they provide complete coverage for the programming and startup portions of the application configuration. It is strongly recommended that you turn on both the Cd_early and Osc_int option bits.

☞ The Cd_early and Osc_int option bits for the application configuration should be turned on by the factory configuration.

Table 12–2. Remote System Upgrade Control Register Contents

Control Register Bit	Value	Definition
Wd_timer[11..0]	12'b000000000000	User watchdog time-out value (most significant 12 bits of 29-bit count value: {Wd_timer[11..0],17'b0})
Ru_address[21..0]	22'b0000000000000000000000	AS and AP configuration address (most significant 22 bits of 24-bit boot address value: boot_address[23:0] = {Ru_address[21..0],2'b0})
Rsv1	1'b0	Reserved bit
Wd_en	1'b1	User watchdog timer enable bit
Osc_int *(1)*	1'b1	Internal oscillator as startup state machine clock enable bit
Cd_early *(1)*	1'b1	Early CONF_DONE check
Rsv2	1'b1	Reserved bit

Note to Table 12–2:
(1) Option bit for the application configuration.

Remote System Upgrade Status Register

The remote system upgrade status register specifies the reconfiguration trigger condition. The various trigger and error conditions include:

- CRC (cyclic redundancy check) error during application configuration
- nSTATUS assertion by an external device due to an error
- Cyclone III device logic array triggered a reconfiguration cycle, possibly after downloading a new application configuration image
- External configuration reset (nCONFIG) assertion
- User watchdog timer time out

Table 12–3 describes the contents of the current state logic in the status register, when the RSU master state machine is in factory configuration accessing the factory information, and the MSEL pin settings are set to AS or AP scheme. The status register bit in the table shows the bit positions within a 32-bit logic.

Table 12–3. Remote System Upgrade Current State Logic (Factory Information) Contents In Status Register Notes (1), (2)

Status Register Bit	Definition	Description
31:30	Master State Machine current state	The current state of the RSU master state machine
29:24	Reserved bits	Padding bits that are set to all 0's
23:0	Boot address	The current 24-bit boot address that was used by the AS or AP configuration scheme as the start address to load the current configuration

Notes to Table 12–3:
(1) The RSU master state machine is in factory configuration.
(2) The MSEL pin settings are in the AS or AP configuration scheme.

Table 12–4 describes the contents of the current state logic in the status register when the RSU master state machine is in application configuration accessing the application information 1, and the MSEL pin settings are set to AS or AP scheme. The status register bit in the table shows the bit positions within a 32-bit logic.

Table 12–4. Remote System Upgrade Current State Logic (Application Information 1) Contents In Status Register Notes (1), (2)

Status Register Bit	Definition	Description
31:30	Master State Machine current state	The current state of the RSU master state machine
29	User watchdog timer enable bit	The current state of the user watchdog enable, which is active high
28:0	User watchdog timer time-out value	The current, entire 29-bit watchdog time-out value

Notes to Table 12–4:
(1) The RSU master state machine is in application configuration.
(2) The MSEL pin settings are in the AS or AP configuration scheme.

Table 12–5 describes the contents of the current state logic in the status register when the RSU master state machine is in application configuration accessing the application information 2, and the MSEL pin settings are set to AS or AP scheme. The status register bit in the table shows the bit positions within a 32-bit logic.

Table 12–5. Remote System Upgrade Current State Logic (Application Information 2) Contents In Status Register Notes (1), (2)

Status Register Bit	Definition	Description
31:30	Master State Machine current state	The current state of the RSU master state machine.
29:24	Reserved bits	Padding bits that are set to all 0's.
23:0	Boot address	The current 24-bit boot address that was used by the AS or AP configuration scheme as the start address to load the current configuration.

Notes to Table 12–5:
(1) The RSU master state machine is in application configuration.
(2) The MSEL pin settings are in the AS or AP configuration scheme.

The previous two application configurations are available in the previous state registers (previous state register 1 and previous state register 2), but only for debug purposes. Table 12–6 describes the contents of the previous state register 1 in the status register when the MSEL pin settings are set to AS or AP scheme. The status register bit in the table shows the bit positions within a 31-bit register.

Table 12–6. Remote System Upgrade Previous State Register 1 Contents In Status Register Note (1)

Status Register Bit	Definition	Description
30	nCONFIG source	One-hot, active high field that describes the reconfiguration source that caused the Cyclone III device to leave the previous application configuration. In the event of a tie, the higher bit order indicates precedence. For example, if nCONFIG and RSU nCONFIG reach the reconfiguration state machine at the same time, the nCONFIG precedes the RSU nCONFIG.
29	CRC error source	
28	nSTATUS source	
27	User watchdog timer source	
26	RSU nCONFIG source	
25:24	Master State Machine current state	The state of the master state machine when the reconfiguration event occurred that caused the Cyclone III device to leave the previous application configuration.
23:0	Boot address	The address used by the AS or AP configuration scheme to load the previous application configuration.

Note to Table 12–6:
(1) The MSEL pin settings are in the AS or AP configuration scheme.

Table 12–7 describes the contents of the previous state register 2 in the status register when the MSEL pin settings are set to AS or AP scheme. The status register bit in the table shows the bit positions within a 31-bit register. Table 12–7 has the same bit definitions as Table 12–6, except all fields reflect the current state when a reconfiguration source caused the Cyclone III device to leave the application configuration before the previous application configuration.

Table 12–7. Remote System Upgrade Previous State Register 2 Contents In Status Register Notes (1), (2)

Status Register Bit	Definition	Description
30	nCONFIG source	One-hot, active high field that describes the reconfiguration source that caused the Cyclone III device to leave the previous application configuration. In the event of a tie, the higher bit order indicates precedence. For example, if nCONFIG and RSU nCONFIG reach the reconfiguration state machine at the same time, the nCONFIG precedes the RSU nCONFIG.
29	CRC Error source	
28	nSTATUS source	
27	User watchdog timer source	
26	RSU nCONFIG source	
25:24	Master State Machine current state	The state of the master state machine when the reconfiguration event occurred that caused the Cyclone III device to leave the previous application configuration.
23:0	Boot address	The address used by the AS or AP configuration scheme to load the previous application configuration.

Notes to Table 12–7:
(1) The MSEL pin settings are in the AS or AP configuration scheme.
(2) Bit definitions are the same as previous state register 1, except all fields reflect the current state when a reconfiguration source caused the Cyclone III device to leave the application configuration before the previous application configuration.

If a capture is done inappropriately, for example capturing a previous state before the system has entered remote update application configuration for the first time, a value will be output from the shift register to indicate that capture was incorrectly called.

Remote System Upgrade State Machine

The remote system upgrade control and update registers have identical bit definitions, but serve different roles (refer to Table 12–1). While both registers can only be updated when the device is loaded with a factory configuration image, the update register writes are controlled by the user logic, and the control register writes are controlled by the remote system upgrade state machine.

In factory configurations, the user logic should send the option bits (`Cd_early` and `Osc_int`), the configuration address, and watchdog timer settings for the next application configuration bit to the update register. When the logic array configuration reset (`RU_nCONFIG`) goes high, the remote system upgrade state machine updates the control register with the contents of the update register and initiates system reconfiguration from the new application page.

In the event of an error or reconfiguration trigger condition, the remote system upgrade state machine directs the system to load a factory or application configuration (based on mode and error condition) by setting the control register accordingly. Table 12–8 lists the contents of the control register after such an event occurs for all possible error or trigger conditions.

The remote system upgrade status register is updated by the dedicated error monitoring circuitry after an error condition but before the factory configuration is loaded.

Table 12–8. Control Register Contents After an Error or Reconfiguration Trigger Condition

Reconfiguration Error/Trigger	Control Register Setting In Remote Update
`nCONFIG` reset	All bits are 0
`nSTATUS` error	All bits are 0
CORE triggered reconfiguration	Update register
CRC error	All bits are 0
Wd time out	All bits are 0

Read operations during factory configuration access the contents of the update register. This feature is used by the user logic to verify that the configuration address and watchdog timer settings were written correctly. Read operations in application configurations access the contents of the control register. This information is used by the user logic in the application configuration.

User Watchdog Timer

The user watchdog timer prevents a faulty application configuration from stalling the device indefinitely. The system uses the timer to detect functional errors after an application configuration is successfully loaded into the Cyclone III device.

The user watchdog timer is a counter that counts down from the initial value loaded into the remote system upgrade control register by the factory configuration. The counter is 29 bits wide and has a maximum count value of 2^{29}. When specifying the user watchdog timer value, specify only the most significant 12 bits. The granularity of the timer setting is 2^{17} cycles. The cycle time is based on the frequency of the 10-MHz internal oscillator. Table 12–9 specifies the operating range of the 10-MHz internal oscillator.

Table 12–9. 10-MHz Internal Oscillator Specifications Note (1)

Minimum	Typical	Maximum	Units
5	6.5	10	MHz

Note to Table 12–9:
(1) These values are preliminary.

The user watchdog timer begins counting once the application configuration enters device user mode. This timer must be periodically reloaded or reset by the application configuration before the timer expires by asserting `RU_nRSTIMER`. If the application configuration does not reload the user watchdog timer before the count expires, a time-out signal is generated by the remote system upgrade dedicated circuitry. The timeout signal tells the remote system upgrade circuitry to set the user watchdog timer status bit (`Wd`) in the remote system upgrade status register and reconfigures the device by loading the factory configuration.

The user watchdog timer is not enabled during the configuration cycle of the device. Errors during configuration are detected by the CRC engine. Also, the timer is disabled for factory configurations. Functional errors should not exist in the factory configuration since it is stored and validated during production and is never updated remotely.

☞ The user watchdog timer is disabled in factory configurations and during the configuration cycle of the application configuration. It is enabled after the application configuration enters user mode.

Quartus II Software Support

Implementation in your design requires a remote system upgrade interface between the Cyclone III device logic array and remote system upgrade circuitry. You also need to generate configuration files for production and remote programming of the system configuration memory. The Quartus II software provides these features.

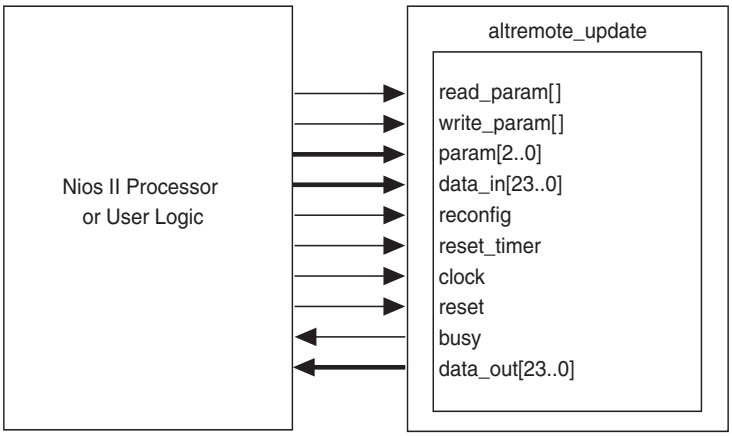
The two implementation options, altremote_update megafunction and remote system upgrade atom, are for the interface between the remote system upgrade circuitry and the device logic array interface. Using the megafunction block instead of creating your own logic saves design time and offers more efficient logic synthesis and device implementation.

altremote_update Megafunction

The altremote_update megafunction provides a memory-like interface to the remote system upgrade circuitry and handles the shift register read/write protocol in Cyclone III device logic. This implementation is suitable for designs that implement the factory configuration functions using a Nios II processor in the device.

Figure 12–7 shows the interface signals between the altremote_update megafunction and the Nios II processor/user logic.

Figure 12–7. interface Signals Between the altremote_update Megafunction and the Nios II Processor



For more information about the altremote_update megafunction and the description of ports listed in Figure 12–7, refer to the *altremote_update Megafunction User Guide*.

Conclusion

Cyclone III devices offer remote system upgrade capability, where you can upgrade a system in real-time through any network. Remote system upgrade helps to deliver feature enhancements and bug fixes without costly recalls, reduces time to market, and extends product life cycles. The dedicated remote system upgrade circuitry in Cyclone III devices provides error detection, recovery, and status information to ensure reliable reconfiguration.

Referenced Documents

This chapter references the following documents:

- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *altremote_update Megafunction User Guide*

Document Revision History

Table 12–10 shows the revision history for this document.

Table 12–10. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "Functional Description" section. • Added new "Enabling Remote Update" section with Figure 12–3. • Deleted Table 12-1. • Updated "Configuration Image Types" section. • Added *Note (1)* to Figure 12–5. • Updated "Remote System Upgrade Mode" section. • Deleted "Interface Signals between Remote System Upgrade Circuitry and Cyclone III Device Logic Array" section. • Deleted "Remote System Upgrade Atom" section. • Added new Figure 12–7. • Added chapter TOC and "Referenced Documents" section.	• Added new section on how to enable remote update in the Quartus II software. This section replaces information in Table 12-1. • Replaced duplicate information about the altremote_update megafunction with updated information.
March 2007 v1.0	Initial Release.	—

13. SEU Mitigation in Cyclone III Devices

CIII51013- 1.1

Introduction

In critical applications used in the fields of avionics, telecommications, system control, medical, and military applications, it is important to be able to:

- Confirm the accuracy of the configuration data stored in an FPGA device
- Alert the system to an occurrence of a configuration error

Dedicated circuitry built into Cyclone® III devices consists of a cyclic redundancy check (CRC) error detection feature that can optionally check for a single event upset (SEU) continuously and automatically.

This chapter describes how to:

- Activate and use the error detection CRC feature in user mode
- Recover from configuration errors caused by CRC errors

This chapter contains the following sections:

- "Error Detection Fundamentals" on page 13–1
- "Configuration Error Detection" on page 13–2
- "User Mode Error Detection" on page 13–2
- "Automated Single Event Upset Detection" on page 13–3
- "Error Detection Pin Description" on page 13–3
- "CRC_ERROR Pin" on page 13–3
- "Error Detection Block" on page 13–3
- "Error Detection Timing" on page 13–4
- "Software Support" on page 13–5
- "Recovering from CRC Errors" on page 13–6

For Cyclone III devices, use of the error detection CRC feature is provided in the Quartus® II software, starting with version 6.1.

Using CRC error detection for the Cyclone III family does not impact fitting or performance.

Information about SEU is located in the Products page on the Altera® web site (**www.altera.com**).

Error Detection Fundamentals

Error detection determines if the data received through an input device has been corrupted during transmission. In validating the data, the transmitter uses a function to calculate a checksum value for the data and appends the checksum to the original data frame. The receiver uses the same calculation methodology to generate a checksum for the received data frame and compares the received checksum to the transmitted checksum. If the two checksum values are equal, the received data frame is correct and no data corruption occurred during transmission or storage.

The error detection CRC feature in Cyclone III devices puts theory into practice. In user mode, a Cyclone III device's error detection CRC feature ensures the integrity of the configuration data.

There are two CRC error checks:

- One always during configuration
- A second optional CRC error check runs in the background in user mode

For more information, refer to "Configuration Error Detection" on page 13–2 and "User Mode Error Detection" on page 13–2.

Configuration Error Detection

In configuration mode, a frame-based CRC is stored within the configuration data and contains the CRC value for each data frame.

During configuration, the FPGA calculates the CRC value based on the frame of data that is received and compares it against the frame CRC value in the data stream. Configuration continues until either the device detects an error or all the values are calculated.

For Cyclone III devices, the CRC is computed by the Quartus II software and downloaded into the device as part of the configuration bit stream. These devices store the CRC in the 32-bit storage register at the end of the configuration mode.

User Mode Error Detection

Soft errors are changes in a configuration random-access memory (CRAM) bit state due to an ionizing particle. All Cyclone series devices have built-in error detection circuitry to detect data corruption by soft errors in the CRAM cells.

This error detection capability continuously computes the CRC of the configured CRAM bits based on the contents of the device and compares it with the pre-calculated CRC value obtained at the end of the configuration. If the CRCs match, there is no error in the current configuration CRAM bits. The process of error detection continues until the device is reset (by setting `nCONFIG` to low).

The Cyclone III device error detection feature does not check memory blocks and I/O buffers. These device memory blocks support parity bits that are used to check the contents of memory blocks for any error. The I/O buffers are not verified during error detection because these bits use flip-flops as storage elements that are more resistant to soft errors. Similar flip-flops are used to store the pre-calculated CRC and other error detection circuitry option bits.

The error detection circuitry in Cyclone III devices uses a 32-bit CRC IEEE 802 standard and 32-bit polynomial as the CRC generator. Therefore, a single 32-bit CRC calculation is performed by the device. If a soft error does not occur, the resulting 32-bit signature value is `0x000000`, which results in a `0` on the output signal `CRC_ERROR`. If a soft error occurs within the device, the resulting signature value is non-zero and the `CRC_ERROR` output signal is `1`.

You can inject a soft error by changing the 32-bit CRC storage register in the CRC circuitry. After verifying the failure induced, you can restore the 32-bit CRC value to the correct CRC value using the same instruction and inserting the correct value. Be sure to read out the correct value first before updating it with a known bad value.

Cyclone III devices, when in user mode, support the `CHANGE_EDREG` Joint Test Action Group (JTAG) instruction, which allows you to write to the 32-bit storage register. You can use Jam files (**.jam**) to automate the testing and verification process. This is a powerful design feature that enables you to dynamically verify the CRC functionality in-system without having to reconfigure the device. You can then switch to use the CRC circuit to check for real errors induced by an SEU. You can only execute the `CHANGE_EDREG` JTAG instruction when the device is in user mode.

Table 13–1. CHANGE_EDREG JTAG Instruction

JTAG Instruction	Instruction Code	Description
`CHANGE_EDREG`	00 0001 0101	This instruction connects the 32-bit CRC storage register between `TDI` and `TDO`. Any precomputed CRC is loaded into the CRC storage register to test the operation of the error detection CRC circuitry at the `CRC_ERROR` pin.

☞ After the test completes, Altera recommends that you reconfigure the device.

Automated Single Event Upset Detection

Cyclone III devices offer on-chip circuitry for automated checking of SEU detection. Applications that require the device to operate error-free at high elevations or in close proximity to earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy code feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Cyclone III devices, eliminating the need for external logic. The CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. The `CRC_ERROR` pin reports a soft error when configuration CRAM data is corrupted, and you have to decide whether to reconfigure the FPGA by strobing the `nCONFIG` pin low or ignore the error.

Error Detection Pin Description

A specific error detection pin, `CRC_ERROR`, is required to monitor the results of the error detection circuitry during user mode.

CRC_ERROR Pin

Table 13–2 describes the `CRC_ERROR` pin.

Table 13–2. CRC_ERROR Pin Description

Pin Name	Pin Type	Description
`CRC_ERROR`	I/O, output	This is an active high signal that indicates that the error detection circuit has detected errors in the configuration CRAM bits. This pin is optional and is used when the error detection CRC circuit is enabled. When the error detection CRC circuit is disabled, it is a user I/O pin. The CRC error output, when using the WYSIWYG function, is a dedicated path to the `CRC_ERROR` pin. The `CRC_ERROR` pin does not support open-drain or inversion.

The `CRC_ERROR` pin information for Cyclone III devices is reported in the Device Pin-Outs on the **Literature** page of the Altera web site (**www.altera.com**).

Error Detection Block

You can enable the Cyclone III device error detection block in the Quartus II software (refer to "Software Support" on page 13–5). This block contains the logic necessary to calculate the 32-bit CRC signature for the configuration CRAM bits in the device.

The CRC circuit continues running even if an error occurs. When a soft error occurs, the device sets the `CRC_ERROR` pin high. There are two types of CRC detection to check the configuration bits:

- CRAM error checking ability (32-bit CRC) during user mode, for use by the `CRC_ERROR` pin.

  There is only one 32-bit CRC value and this 32-bit CRC value covers all of the CRAM data.

- 16-bit CRC embedded in every configuration data frame.

  During configuration, after a frame of data has loaded into the device, the pre-computed CRC is shifted into the CRC circuitry. Simultaneously, the CRC value for the data frame shifted-in is calculated. If the pre-computed CRC and calculated CRC values do not match, `nSTATUS` is set low. Every data frame has a 16-bit CRC, and therefore, there are many 16-bit CRC values for the whole configuration bit stream. Every device has a different length of the configuration data frame.

This section focuses on the first type, the 32-bit CRC when the device is in user mode.

Error Detection Registers

There are two sets of 32-bit registers in the error detection circuitry that store the computed CRC signature and precalculated CRC value. A non-zero value on the signature register causes the CRC_ERROR pin to set high. Figure 13–1 shows the block diagram of the error detection block and the two related 32-bit registers: the signature register and the storage register.

Figure 13–1. Error Detection Block Diagram

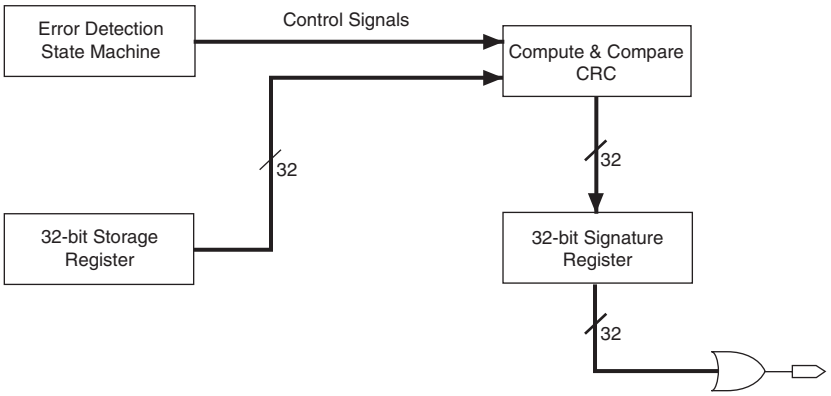


Table 13–3 defines the registers shown in Figure 13–1.

Table 13–3. Error Detection Registers

Register	Function
32-bit signature register	This register contains the CRC signature. The signature register contains the result of the user mode calculated CRC value compared against the pre-calculated CRC value. If no errors are detected, the signature register is all zeros. A non-zero signature register indicates an error in the configuration CRAM contents. The CRC_ERROR signal is derived from the contents of this register.
32-bit storage register	This register is loaded with the 32-bit pre-computed CRC signature at the end of the configuration stage. The signature is then loaded into the 32-bit CRC circuit (called the Compute & Compare CRC block, as shown in Figure 13–1) during user mode to calculate the CRC error. This register forms a 32-bit scan chain during execution of the CHANGE_EDREG JTAG instruction. The CHANGE_EDREG JTAG instruction can change the content of the storage register. Therefore, the functionality of the error detection CRC circuitry is checked in-system by executing the instruction to inject an error during the operation. The operation of the device is not halted when issuing the CHANGE_EDREG instruction.

Error Detection Timing

When the error detection CRC feature is enabled through the Quartus II software, the device automatically activates the CRC process upon entering user mode, after configuration and initialization is complete.

The CRC_ERROR pin is driven low until the error detection circuitry has detected a corrupted bit in the previous CRC calculation. Once the pin goes high, it remains high during the next CRC calculation. This pin does not log the previous CRC calculation. If the new CRC calculation does not contain any corrupted bits, the CRC_ERROR pin is driven low. The error detection runs until the device is reset.

The error detection circuitry runs off an internal configuration oscillator with a divisor that sets the maximum frequency. Table 13–4 shows the minimum and maximum error detection frequencies.

Table 13–4. Minimum and Maximum Error Detection Frequencies

Device Type	Error Detection Frequency	Maximum Error Detection Frequency	Minimum Error Detection Frequency	Valid Divisors (2^n)
Cyclone III	80 MHz/2^n	80 MHz	312.5 kHz	0, 1, 2, 3, 4, 5, 6, 7, 8

You can set a lower clock frequency by specifying a division factor in the Quartus II software (refer to "Software Support" on page 13–5). The divisor is a power of two (2), where n is between 0 and 8. The divisor ranges from 1 through 256. Refer to equation 1:

$$\text{Error detection frequency} = \frac{80\ \text{MHz}}{2^n} \quad (1)$$

CRC calculation time depends on the device and the error detection clock frequency. Table 13–5 shows the estimated time for each CRC calculation with minimum and maximum clock frequencies for Cyclone III devices.

Table 13–5. CRC Calculation Time

Device	Minimum Time (ms) *(1)*	Maximum Time (s) *(2)*
EP3C5	5	2.29
EP3C10	5	2.29
EP3C16	7	3.17
EP3C25	9	4.51
EP3C40	15	7.48
EP3C55	23	11.77
EP3C80	31	15.81
EP3C120	45	22.67

Notes to Table 13–5:

(1) The minimum time corresponds to the maximum error detection clock frequency and may vary with different processes, voltages, and temperatures.

(2) The maximum time corresponds to the minimum error detection clock frequency and may vary with different processes, voltages, and temperatures.

Software Support

Starting with version 6.1, Quartus II software supports the error detection CRC feature. Enabling this feature generates the `CRC_ERROR` output to the optional dual purpose `CRC_ERROR` pin.

The error detection CRC feature is controlled by the **Device & Pin Options** dialog box in the Quartus II software.

Enable the error detection feature using CRC by performing the following steps:

1. Open the Quartus II software and load a project using a Stratix or Cyclone series device.
2. On the Assignments menu, click **Settings**. The **Settings** dialog box appears.
3. In the Category list, select **Device**. The **Device** page appears.
4. Click **Device & Pin Options**, as shown in Figure 13–2.
5. In the **Device & Pin Options** dialog box, click the **Error Detection CRC** tab.

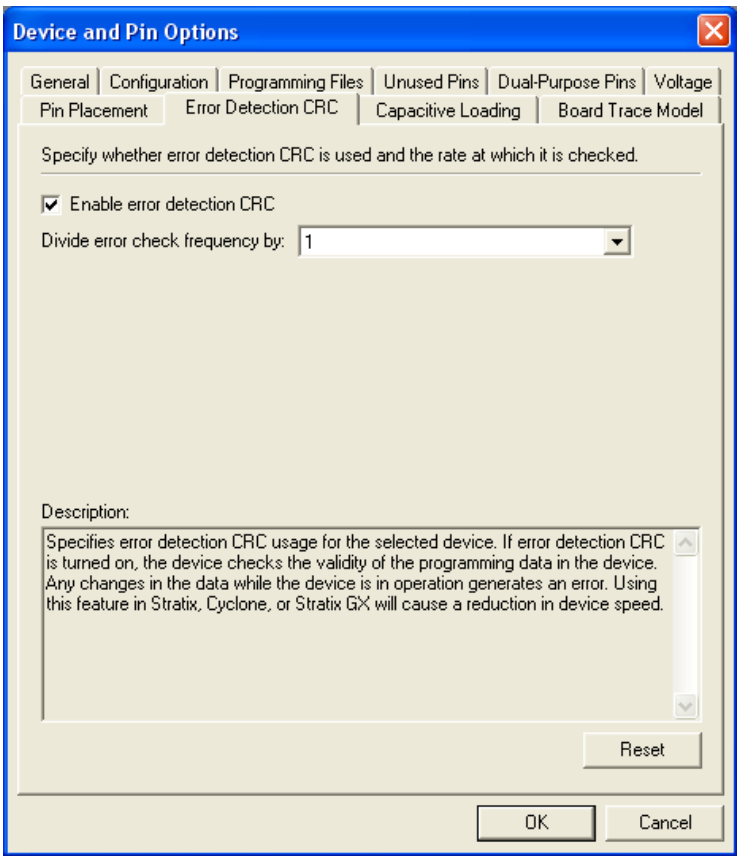
6. Turn on **Enable error detection CRC**.

7. In the **Divide error check frequency by** box, enter a valid divisor as documented in Table 13–4.

☞ The divisor value divides down the frequency of the configuration oscillator output clock that measures the CRC circuitry.

8. Click **OK**.

Figure 13–2. Enabling the Error Detection CRC Feature in the Quartus II Software



Recovering from CRC Errors

The system that the Altera FPGA resides in must control device reconfiguration. After detecting an error on the `CRC_ERROR` pin, strobing the `nCONFIG` low directs the system to perform the reconfiguration at a time when it is safe for the system to reconfigure the FPGA.

When the data bit is rewritten with the correct value by reconfiguring the device, the device functions correctly.

While soft errors are uncommon in Altera devices, certain high-reliability applications may require a design to account for these errors.

Conclusion

The purpose of the error detection CRC feature is to detect a flip in any of the configuration CRAM bits in Cyclone III devices due to a soft error. By using the error detection circuitry, you can continuously verify the integrity of the configuration CRAM bits.

Document Revision History

Table 13–6 shows the revision history for this document.

Table 13–6. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.0	Added chapter TOC to document.	—
March 2007 v1.0	Initial Release.	—

14. IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices

CIII5014-1.1

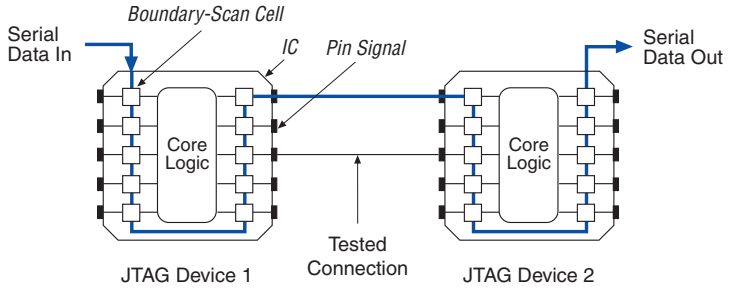
Introduction

As PCBs become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (such as external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions increase the cost for traditional testing methods.

In the 1980s, the JTAG developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the ability to efficiently test components on PCBs with tight lead spacing.

BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 14–1 illustrates the concept of BST.

Figure 14–1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in Cyclone® III devices and contains the following sections:

- "IEEE Std. 1149.1 BST Architecture" on page 14–2
- "IEEE Std. 1149.1 Boundary-Scan Register" on page 14–4
- "IEEE Std. 1149.1 BST Operation Control" on page 14–6
- "I/O Voltage Support in JTAG Chain" on page 14–14
- "Using IEEE Std. 1149.1 BST Circuitry" on page 14–15
- "BST for Configured Devices" on page 14–15
- "Disabling IEEE Std. 1149.1 BST Circuitry" on page 14–15
- "Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing" on page 14–16
- "Boundary-Scan Description Language (BSDL) Support" on page 14–16

In addition to BST, you can use the IEEE Std. 1149.1 controller for Cyclone III device in-circuit reconfiguration (ICR). However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For information about configuring Cyclone III devices via the IEEE Std. 1149.1 circuitry, refer to the *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*.

IEEE Std. 1149.1 BST Architecture

A Cyclone III device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS and TCK. The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have weak internal pull-up resistors. The TDO output pin and all the JTAG input pins are powered by the 2.5-V/3.0-V V_{CCIO} supply. All user I/O pins are tri-stated during JTAG configuration.

For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to "I/O Voltage Support in JTAG Chain" on page 14–14.

Table 14–1 summarizes the functions of each of these pins.

Table 14–1. IEEE Std. 1149.1 Pin Descriptions

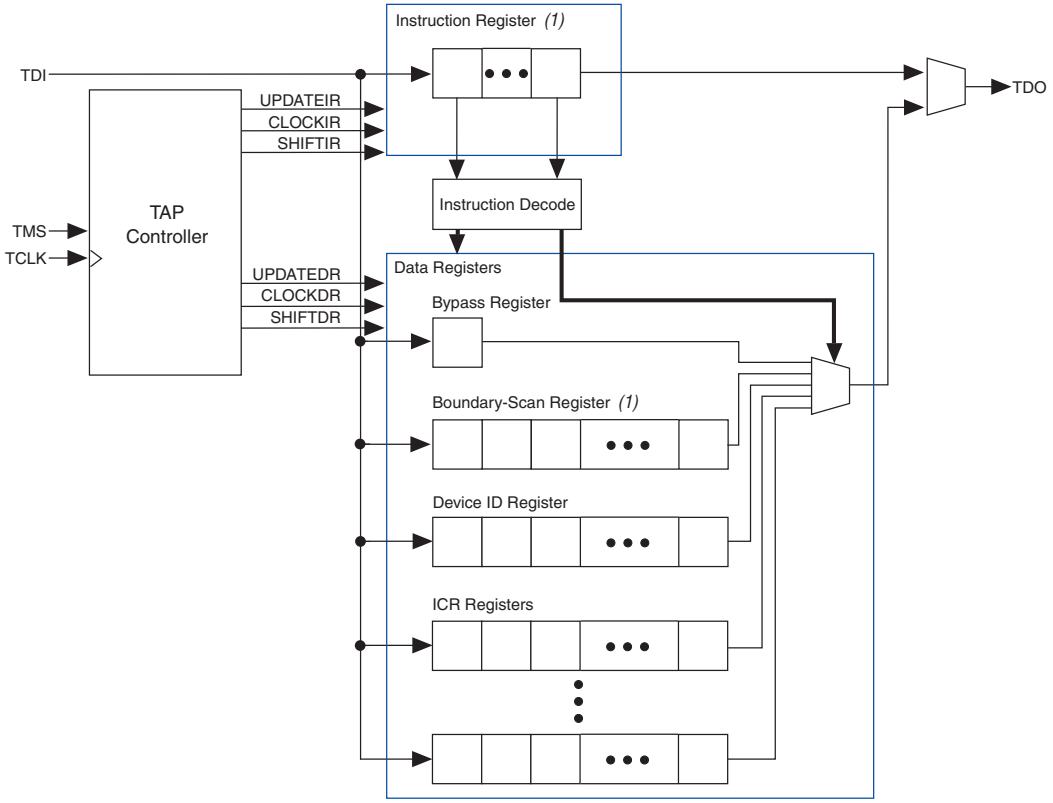
Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. A signal applied to TDI is expected to change state at the falling edge of TCK. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the Test Access Port (TAP) controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. During non-JTAG operation, TMS is recommended to be driven high.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a 1-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 14–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 14–2. IEEE Std. 1149.1 Circuitry



Note to Figure 14–2:
(1) For register lengths, refer to Table 14–2 on page 14–4.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information about the TAP controller, refer to the "IEEE Std. 1149.1 BST Operation Control" section. The `TMS` and `TCK` pins operate the TAP controller, and the `TDI` and `TDO` pins provide the serial path for the data registers. The `TDI` pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Cyclone III I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.

Figure 14–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 14–3. Boundary-Scan Register

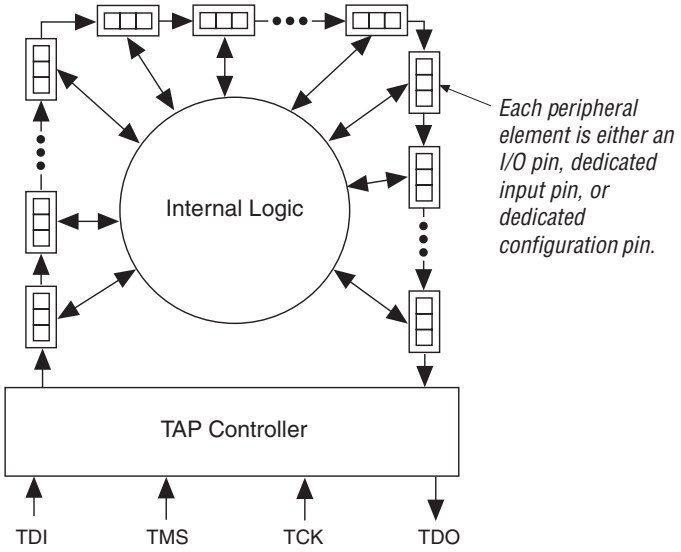


Table 14–2 shows the boundary-scan register length for Cyclone III devices.

Table 14–2. Cyclone III Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP3C5	603
EP3C10	603
EP3C16	1080
EP3C25	732
EP3C40	1632
EP3C55	1164
EP3C80	1314
EP3C120	1620

Boundary-Scan Cells of a Cyclone III Device I/O Pin

The Cyclone III device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ, OEJ, and PIN_IN signals, while the update registers connect to external data through the PIN_OUT, and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (such as shift, clock, and update) are generated internally by the TAP controller. The MODE signal is generated by a decode of the instruction register. The HIGHZ signal is high when executing the HIGHZ instruction. The data signal path for the boundary-scan register runs from the SDI signal to the SDO signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 14–4 shows the Cyclone III device's user I/O boundary-scan cell.

Figure 14–4. Cyclone III Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

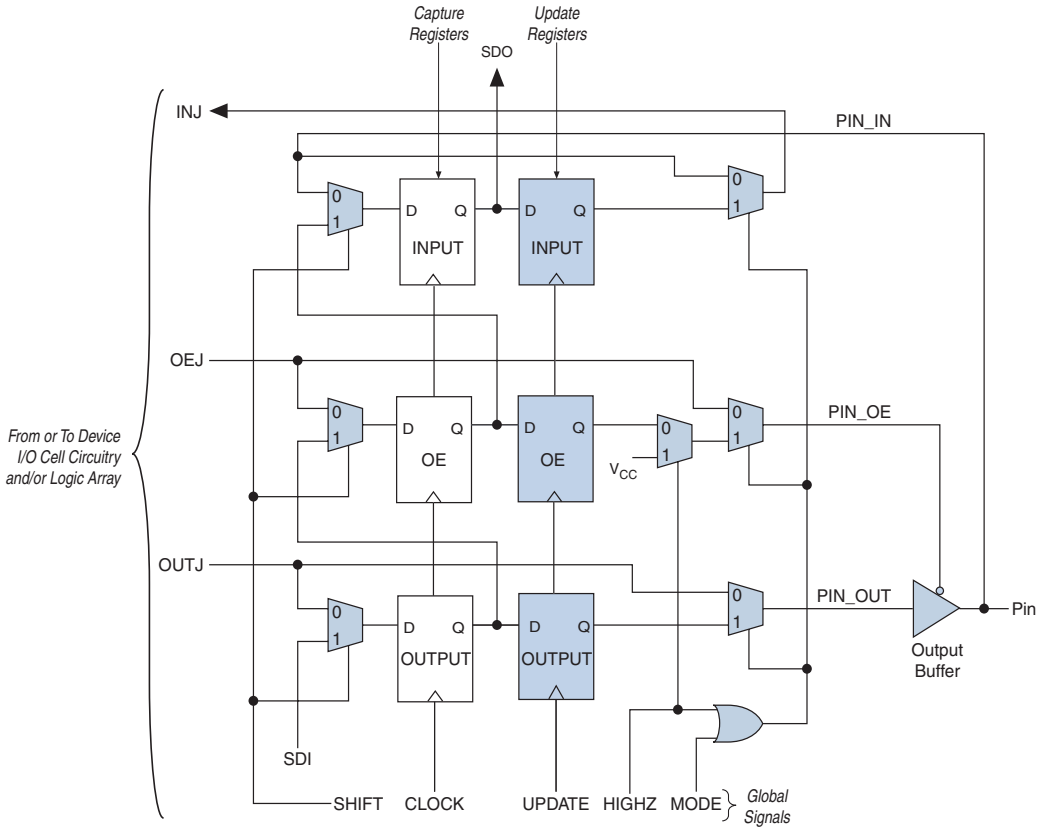


Table 14–3 describes the capture and update register capabilities of all boundary-scan cells within Cyclone III devices.

Table 14–3. Cyclone III Device Boundary Scan Cell Descriptions Note (1)

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	—
Dedicated clock input	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to clock network or logic array
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to control logic
Dedicated bidirectional (open drain) *(4)*	0	OEJ	PIN_IN	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	PIN_IN drives to configuration control
Dedicated output	OUTJ	0	0	N.C. *(2)*	N.C. *(2)*	N.C. *(2)*	OUTJ drives to output buffer

Notes to Table 14–3:

(1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types do not have BSCs.
(2) No Connect (N.C.).
(3) This includes pins nCONFIG, MSEL0, MSEL1, MSEL2, MSEL3, and nCE.
(4) This includes pins CONF_DONE and nSTATUS.

IEEE Std. 1149.1 BST Operation Control

Cyclone III devices support the IEEE Std. 1149.1 (JTAG) instructions shown in Table 14–4.

Table 14–4. Cyclone III JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. IDCODE is the default instruction at power up and in TAP RESET state.
HIGHZ	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions	—	Used when configuring a Cyclone III device via the JTAG port with a USB Blaster™ ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File, or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO *(2)*	00 0000 1101	Allows I/O reconfiguration through JTAG ports using the IOCSR for JTAG testing. Can be executed after or during configurations. nSTATUS pin must go high before you can issue the CONFIG_IO instruction.
EN_ACTIVE_CLK *(2)*	01 1110 1110	Allows CLKUSR pin signal to replace the internal oscillator as the configuration clock source.
DIS_ACTIVE_CLK *(2)*	10 1110 1110	Allows you to revert the configuration clock source from CLKUSR pin signal set by EN_ACTIVE_CLK back to the internal oscillator.
ACTIVE_DISENGAGE *(2)*	10 1101 0000	Places the active configuration mode controllers into idle state prior to CONFIG_IO to configure the IOCSR or perform board level testing.
ACTIVE_ENGAGE *(2)*	10 1011 0000	This instruction may need to be used in AS and AP configuration schemes to re-engage the active controller.
APFC_BOOT_ADDR *(2)*	10 0111 0000	Places the 22-bit active boot address register between the TDI and TDO pins, allowing a new active boot address to be serially shifted into TDI and into the active parallel (AP) flash controller. In remote system upgrade, the APFC_BOOT_ADDR instruction sets the boot address for the factory configuration.

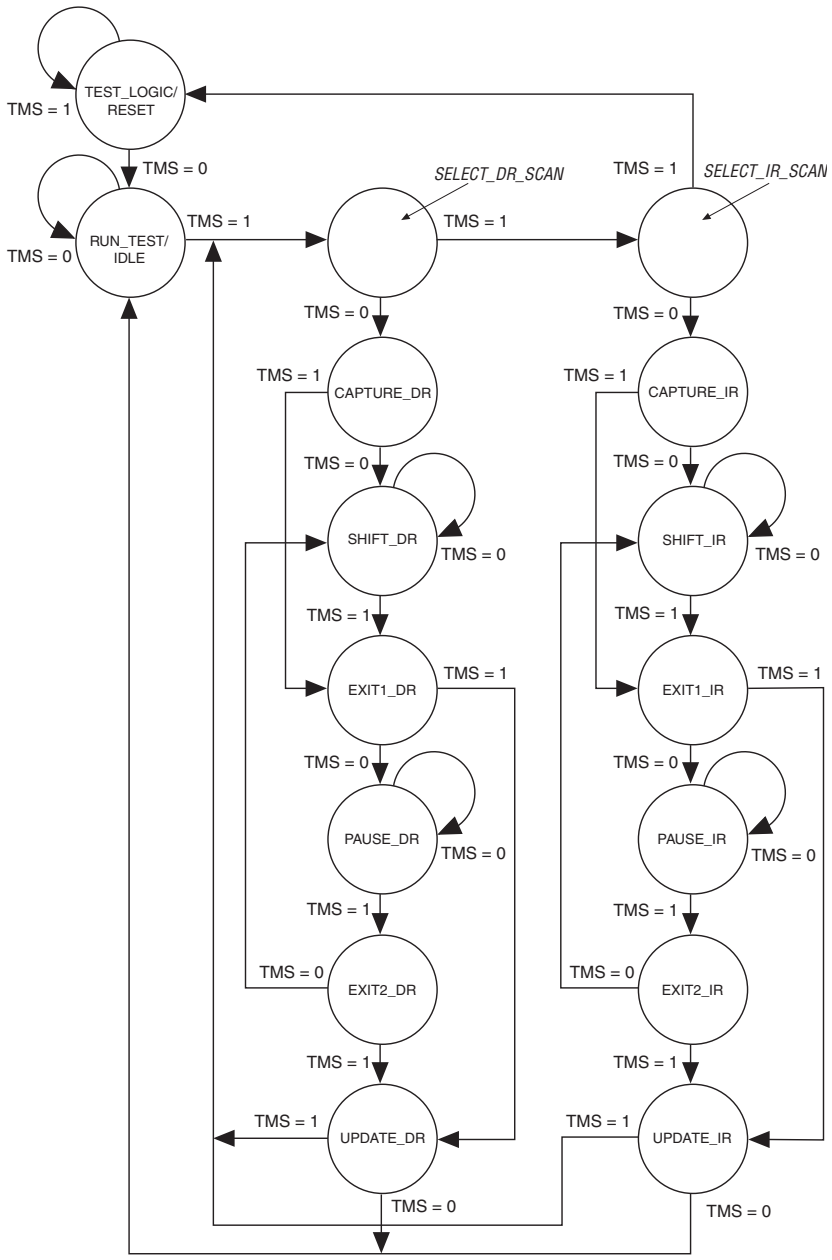
Notes to Table 14–4:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

(2) For more information on how to use CONFIG_IO, EN_ACTIVE_CLK, DIS_ACTIVE_CLK, ACTIVE_DISENGAGE, ACTIVE_ENGAGE and APFC_BOOT_ADDR instructions for Cyclone III devices, refer to *Configuring Cyclone III Devices* chapter of the *Cyclone III Device Handbook*.

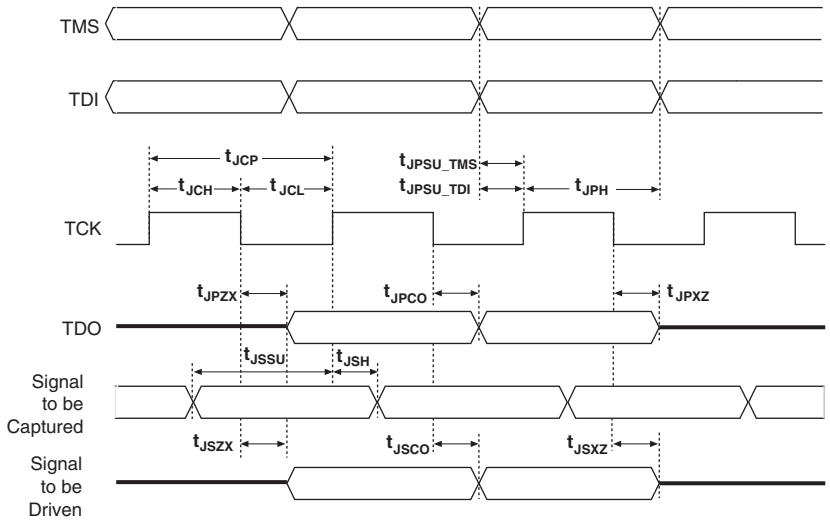
The IEEE Std. 1149.1 TAP controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 14–5 shows the TAP controller state machine.

Figure 14–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the `TEST_LOGIC/RESET` state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with `IDCODE` as the initial instruction. At device power-up, the TAP controller starts in this `TEST_LOGIC/RESET` state. In addition, forcing the TAP controller to the `TEST_LOGIC/RESET` state is done by holding `TMS` high for five `TCK` clock cycles. Once in the `TEST_LOGIC/RESET` state, the TAP controller remains in this state as long as `TMS` is held high (while `TCK` is clocked). Figure 14–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 14–6. IEEE Std. 1149.1 Timing Waveforms Note (1)

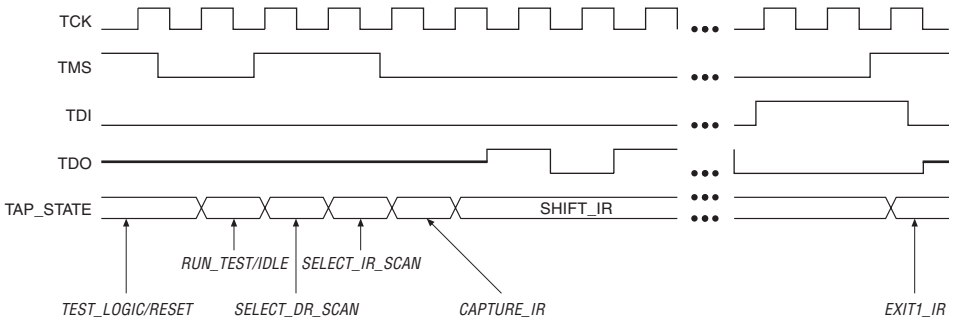


Note to Figure 14–6:

(1) For JTAG timing parameters, refer to the *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*.

To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (`SHIFT_IR`) state and shift in the appropriate instruction code on the `TDI` pin. The waveform diagram in Figure 14–7 represents the entry of the instruction code into the instruction register. Figure 14–7 shows the values of `TCK`, `TMS`, `TDI`, `TDO`, and the states of the TAP controller. From the `RESET` state, `TMS` is clocked with the pattern `01100` to advance the TAP controller to `SHIFT_IR`.

Figure 14–7. Selecting the Instruction Mode



The `TDO` pin is tri-stated in all states except in the `SHIFT_IR` and `SHIFT_DR` states. The `TDO` pin is activated at the first falling edge of `TCK` after entering either of the shift states and is tri-stated at the first falling edge of `TCK` after leaving either of the shift states.

When the `SHIFT_IR` state is activated, `TDO` is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of `TCK`. The first 10 bits shifted out from the instruction register are 1010101010. `TDO` continues to shift out the contents of the instruction register as long as the `SHIFT_IR` state is active. The TAP controller remains in the `SHIFT_IR` state as long as `TMS` remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code is clocked at the same time that the next state, EXIT1_IR, is activated. Set TMS to high to activate the EXIT1_IR state. Once in the EXIT1_IR state, TDO becomes tri-stated again. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of three modes. The three serial shift test data instruction modes are:

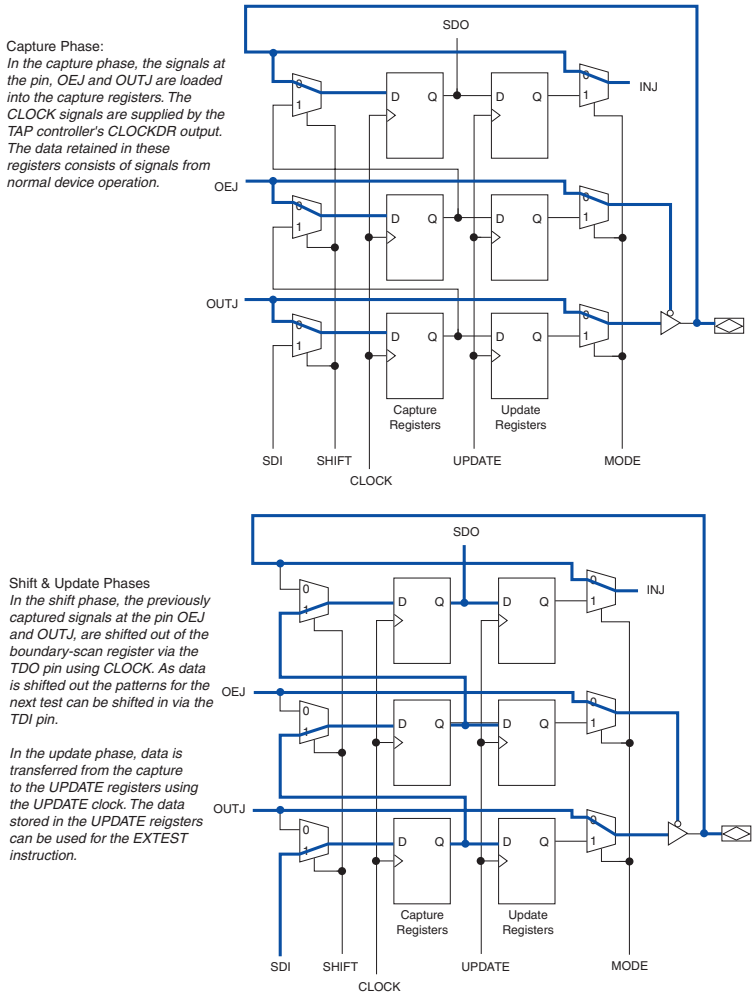
- SAMPLE/PRELOAD Instruction Mode
- EXTEST Instruction Mode
- BYPASS Instruction Mode

These three modes will be discussed in greater detail in the following three sections.

SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, this instruction is most often used to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 14–8 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

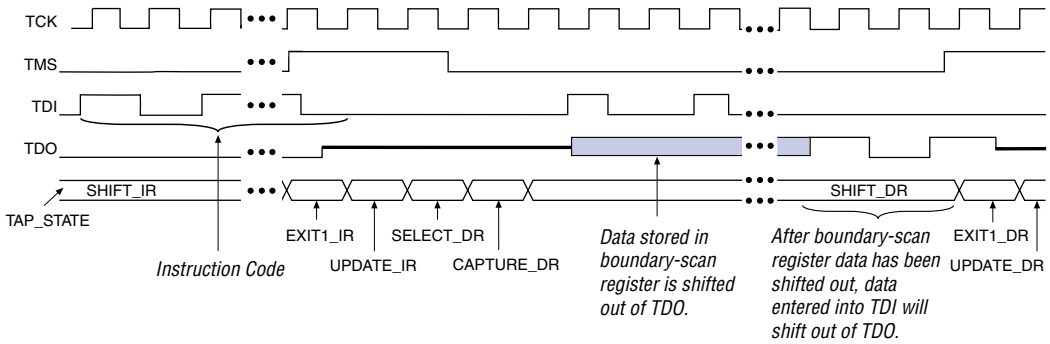
Figure 14–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode



During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. Refer to the "EXTEST Instruction Mode"section for more information.

Figure 14–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 14–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

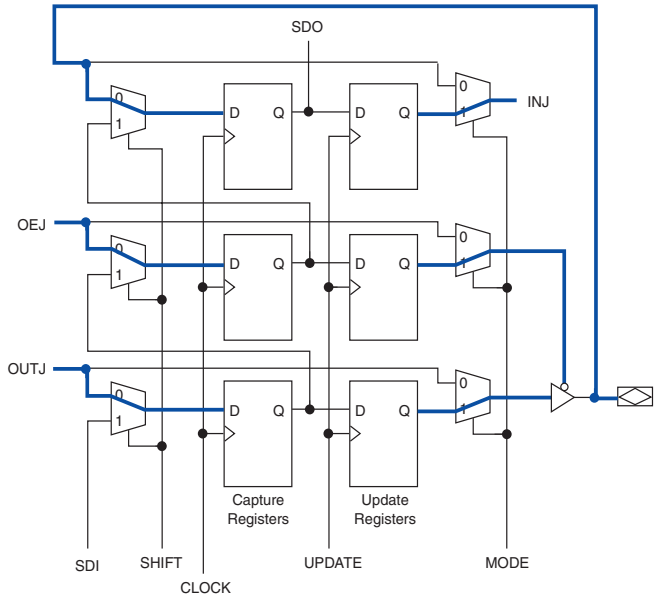
Figure 14–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 14–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_OUT, INJ and allows the I/O pin to tri-state or drive a signal out.

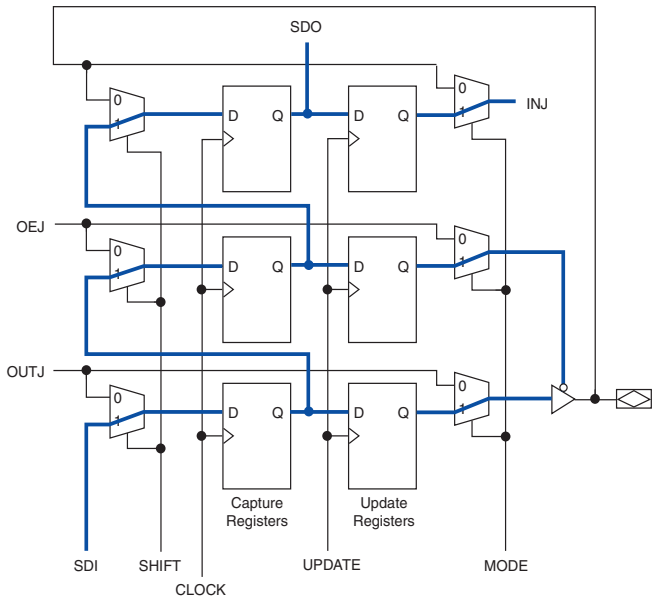
A "1" in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

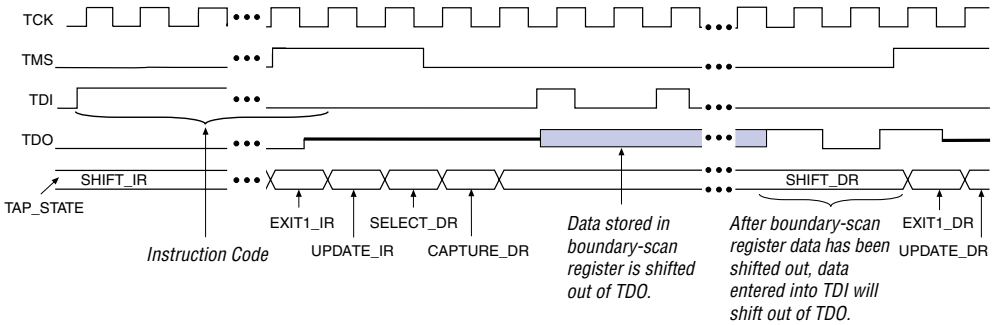
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_IN, INU, and allow the I/O pin to tri-state or drive a signal out.



`EXTEST` selects data differently than `SAMPLE/PRELOAD`. `EXTEST` chooses data from the update registers as the source of the output and output enable signals. Once the `EXTEST` instruction code is entered, the multiplexers select the update register data. Thus, data stored in these registers from a previous `EXTEST` or `SAMPLE/PRELOAD` test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of `TDO` during the shift phase. New test data can then be stored in the update registers during the update phase.

The `EXTEST` waveform diagram in Figure 14–11 resembles the `SAMPLE/PRELOAD` waveform diagram, except for the instruction code. The data shifted out of `TDO` consists of the data that was present in the capture registers after the capture phase. New test data shifted into the `TDI` pin appears at the `TDO` pin after being clocked through the entire boundary-scan register.

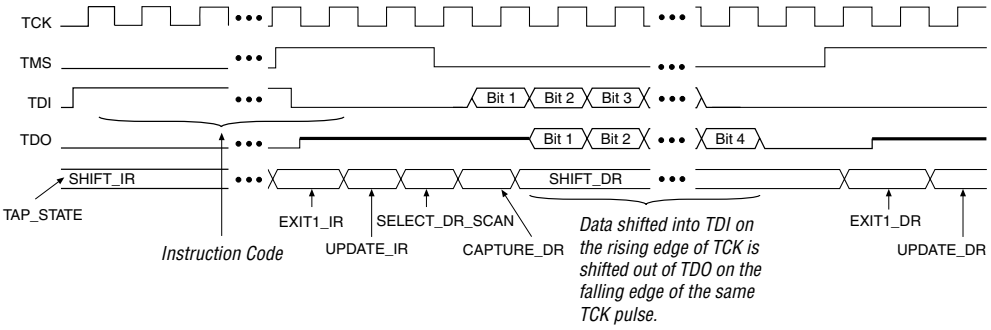
Figure 14–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all ones is loaded in the instruction register. This mode allows the boundary scan data to pass the selected device synchronously to adjacent devices when no test operation of the device is needed at the board level. The waveforms in Figure 14–12 show how scan data passes through a device once the TAP controller is in the `SHIFT_DR` state. In this state, data signals are clocked into the bypass register from `TDI` on the rising edge of `TCK` and out of `TDO` on the falling edge of the same clock pulse.

Figure 14–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

The `IDCODE` instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When `IDCODE` is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the `TDI` and `TDO` ports, and the device `IDCODE` is shifted out.

Table 14–5 shows the `IDCODE` information for Cyclone III devices.

Table 14–5. 32-Bit Cyclone III Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP3C5	0000	0010 0000 1111 0001	000 0110 1110	1
EP3C10	0000	0010 0000 1111 0001	000 0110 1110	1
EP3C16	0000	0010 0000 1111 0010	000 0110 1110	1
EP3C25	0000	0010 0000 1111 0011	000 0110 1110	1
EP3C40	0000	0010 0000 1111 0100	000 0110 1110	1
EP3C55	0000	0010 0000 1111 0101	000 0110 1110	1
EP3C80	0000	0010 0000 1111 0110	000 0110 1110	1
EP3C120	0000	0010 0000 1111 0111	000 0110 1110	1

Notes to Table 14–5:
(1) The most significant bit (MSB) is on the left.
(2) The `IDCODE`'s least significant bit (LSB) is always 1.

USERCODE Instruction Mode

The `USERCODE` instruction mode is used to examine the UES within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the `TDI` and `TDO` ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit `USERCODE` register. The UES is then shifted out through the device ID register.

The UES value is not user defined until after the device is configured. This is because the value is stored in the POF file and only loaded to the device during configuration. Before configuration, the UES value is set to the default value.

CLAMP Instruction Mode

The `CLAMP` instruction mode is used to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the `TDI` and `TDO` ports. The state of all signals driven from the pins are completely defined by the data held in the boundary-scan register.

If you are testing after configuring the device, the programmable weak pull-up resistor or the bus hold feature overrides the `CLAMP` value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The `HIGHZ` instruction mode sets all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the `TDI` and `TDO` ports.

If you are testing after configuring the device, the programmable weak pull-up resistor or the bus hold feature overrides the `HIGHZ` value at the pin.

CONFIG_IO Instruction Mode

The CONFIG_IO instruction allows you to perform I/O reconfiguration through JTAG ports using the I/O configuration shift register (IOCSR). IOCSR is a chain of I/O element (IOE) registers, which contains configuration bits to control the IOE characteristics. Thus, you can perform I/O reconfiguration by shifting new configuration data into the IOCSR. CONFIG_IO instruction needs to be used together with ACTIVE_DISENGAGE instruction to interrupt active configuration. CONFIG_IO also drives the nSTATUS pin low and releases it when the CONFIG_IO instruction is no longer active.

☞ The nCONFIG pin must not be low and nSTATUS pin must go high before you can issue the CONFIG_IO instruction.

I/O Voltage Support in JTAG Chain

A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone III devices, the TDO pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

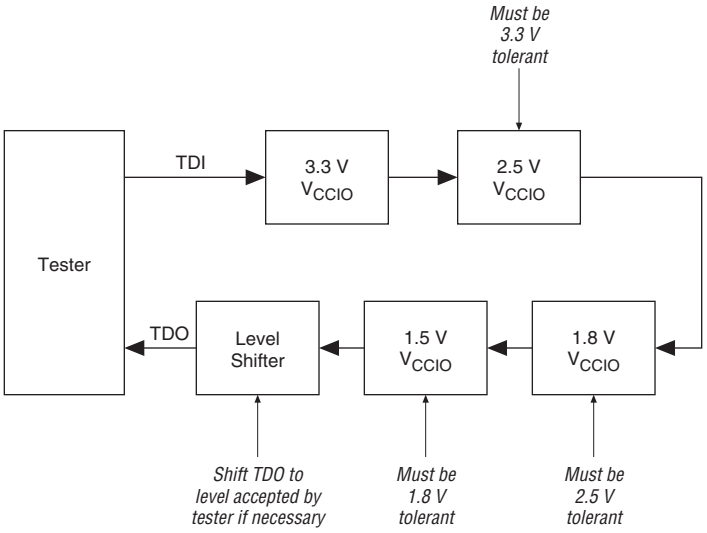
Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone III devices can support 2.5-V or 3.3-V input levels.

☞ For multiple devices in a JTAG chain with 3.0-V/ 3.3-V I/O standard, you need to connect a 25 Ω series resistor on a TDO pin driving a TDI pin.

For more information about MultiVolt™ I/O support, refer to the *Cyclone III Device I/O Feature* chapter in volume 1 of the *Cyclone III Device Handbook*.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 14–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 14–13. JTAG Chain of Mixed Voltages



Using IEEE Std. 1149.1 BST Circuitry

Cyclone III devices have dedicated JTAG pins and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. Not only can you perform BST on Cyclone III FPGAs before and after, but also during configuration. Cyclone III FPGAs support the `BYPASS`, `IDCODE` and `SAMPLE` instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the `CONFIG_IO` instruction except for active configuration schemes where `ACTIVE_DISENGAGE` instruction is used instead.

The `CONFIG_IO` instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone III FPGA or you can wait for the configuration device to complete configuration. Once configuration is interrupted and JTAG BST is complete, you must reconfigure the part via JTAG (`PULSE_NCONFIG` instruction) or by pulsing `nCONFIG` low.

When you perform JTAG boundary-scan testing before configuration, the `nCONFIG` pin must be held low.

When you design a board for JTAG configuration of Cyclone III devices, you need to consider the connections for the dedicated configuration pins.

For more information on using the IEEE Std.1149.1 circuitry for device configuration, refer to the *Configuring Cyclone III Devices* chapter of the *Cyclone III Device Handbook*.

BST for Configured Devices

If you are performing BST for a configured device, a post configuration BSDL file is required. Use the BSDL Customizer script that is available on the Altera web site at **www.altera.com** to generate a post-configuration BSDL file that is customized to your design.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Cyclone III devices is enabled upon device power-up. Because the IEEE Std. 1149.1 BST circuitry is used for BST or in-circuit reconfiguration, you must enable the circuitry only at specific times as mentioned in "Using IEEE Std. 1149.1 BST Circuitry".

If you are not using the IEEE Std. 1149.1 circuitry in Cyclone III, then you should permanently disable the circuitry to ensure that you do not inadvertently enable when it is not required.

Table 14–6 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Cyclone III devices.

Table 14–6. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*	Connection for Disabling
`TMS`	VCC
`TCK`	GND
`TDI`	VCC
`TDO`	Leave open

Note to Table 14–6:
(1) There is no software option to disable JTAG in Cyclone III devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the 10 bit checkerboard pattern (1010101010) does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
  - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.
- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when you enter the EXTEST mode. If the OEJ update register contains a 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during ICR. This instruction is supported before or after ICR, but not during ICR. Use the CONFIG_IO instruction to interrupt configuration and then perform testing, or wait for configuration to complete.
- If performing testing before configuration, hold nCONFIG pin low.
- The following private instructions must not be used as they may render the device inoperable:
  1000010000
  1001000000
  1011100000
  You should take precautions not to invoke these instructions at any time.

For more information about boundary scan testing, contact mySupport at www.altera.com.

Boundary-Scan Description Language (BSDL) Support

BSDL, a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, and failure diagnostics.

For more information about BSDL files for IEEE Std. 1149.1-compliant Cyclone III devices and the BSDLCustomizer script, visit the Altera web site at **www.altera.com**.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Cyclone III devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Referenced Documents

This chapter references the following documents:

- *Cyclone III Device I/O Features* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Cyclone III Device Datasheet: DC and Switching Characteristics* chapter in volume 2 of the *Cyclone III Device Handbook*

Document Revision History

Table 14–7 shows the revision history for this document.

Table 14–7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	• Updated "IEEE Std. 1149.1 Boundary-Scan Register" section. • Updated `IDCODE` information and removed SignalTap II instructions in Table 14–4. • Updated "BST for Configured Devices" section. • Added a guideline to "Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing" section. • Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release.	—

Section 4. Packaging Information

This section includes the following chapter:

- Chapter 15, Package Information for Cyclone III Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

15. Package Information for Cyclone III Devices

CIII51015-1.1

Introduction

This chapter provides package information for Altera® Cyclone® III devices, and contains the following sections:

- "Thermal Resistance" on page 15–2
- "Package Outlines" on page 15–2

Table 15–1 shows Cyclone III device package options.

Table 15–1. Cyclone III Device Package Options (Part 1 of 2)

Device	Package *(2)*	Pins
EP3C5	Plastic Enhanced Quad Flat Pack (EQFP) – Wire Bond	144 *(1)*
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	256
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	256
EP3C10	Plastic Enhanced Quad Flat Pack (EQFP) – Wire Bond	144 *(1)*
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	256
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	256
EP3C16	Plastic Enhanced Quad Flat Pack (EQFP) – Wire Bond	144 *(1)*
	Plastic Quad Flat Pack (PQFP) – Wire Bond	240
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	256
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	256
	FineLine Ball-Grid Array (FBGA) – Option 3 – Wire Bond	484
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	484
EP3C25	Plastic Enhanced Quad Flat Pack (EQFP) – Wire Bond	144 *(1)*
	Plastic Quad Flat Pack (PQFP) – Wire Bond	240
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	256
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	256
	FineLine Ball-Grid Array (FBGA) – Wire Bond	324
EP3C40	Plastic Quad Flat Pack (PQFP) – Wire Bond	240
	FineLine Ball-Grid Array (FBGA) – Wire Bond	324
	FineLine Ball-Grid Array (FBGA) – Option 3 – Wire Bond	484
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	484
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	780
EP3C55	FineLine Ball-Grid Array (FBGA) – Option 3 – Wire Bond	484
	Ultra FineLine Ball-Grid Array (UBGA) – Wire Bond	484
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	780
EP3C80	FineLine Ball-Grid Array (FBGA) – Option 3 – Wire Bond	484
	Ultra FineLine Ball-Grid Array (UBGA) - Wire Bond	484
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	780

Table 15–1. Cyclone III Device Package Options (Part 2 of 2)

Device	Package *(2)*	Pins
EP3C120	FineLine Ball-Grid Array (FBGA) – Option 3 – Wire Bond	484
	FineLine Ball-Grid Array (FBGA) – Option 2 – Wire Bond	780

Notes to Table 15–1:

(1) The E144 package has an exposed pad at the bottom of the package. This exposed pad is a ground pad that must be connected to the ground plane on your PCB. This exposed pad is used for electrical connectivity and not for thermal purposes.

(2) The package type entries with "Option #" refer to instances where multiple package options exist for a given package type and pin count. The Option number identifies the specific type used by the corresponding device density.

Thermal Resistance

For thermal resistance specifications for Cyclone III devices, refer to the *Cyclone Series Device Thermal Resistance Data Sheet*.

Package Outlines

Cyclone III device package outlines can be downloaded from the *Device Packaging Specifications* web page.

Referenced Documents

This chapter references the following document:

- *Cyclone Series Device Thermal Resistance Data Sheet*

Document Revision History

Table 15–2 shows the revision history for this document.

Table 15–2. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	Added chapter TOC and "Referenced Documents" section.	—
March 2007 v1.0	Initial Release	—

Cyclone III Device Handbook, Volume 2

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CIII5V2-1.3

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I.S. EN ISO 9001

Chapter Revision Dates

Chapter 1. Cyclone III Device Datasheet: DC and Switching Characteristics
Revised: *July 2007*
Part number: *CIII52001-1.3*

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About this Handbook

This handbook provides comprehensive information about the Altera® Cyclone® III family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Altera literature services	Email	literature@altera.com
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.

Visual Cue	Meaning
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
WARNING	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Section 1. Cyclone III Device Datasheet

This section includes the following chapter:

- Chapter 1, Cyclone III Device Datasheet: DC and Switching Characteristics

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

1. Cyclone III Device Datasheet: DC and Switching Characteristics

CIII52001-1.3

Electrical Characteristics

Operating Conditions

When Cyclone® III devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone III devices, system designers must consider the operating requirements within this document. Cyclone III devices are offered in both commercial and industrial grades. Commercial devices are offered in –6 (fastest), –7, and –8 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone III devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Conditions beyond those listed in Table 1–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device. All parameters representing voltages are measured with respect to ground.

Table 1–1. Cyclone III Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	–0.5	1.8	V
V_{CCIO}	Supply voltage for output buffers	–0.5	3.9	V
V_{CCA}	Supply (analog) voltage for PLL regulator	–0.5	3.75	V
V_{CCD_PLL}	Supply (digital) voltage for PLL	–0.5	1.8	V
V_I	DC input voltage	–0.5	3.95	V
I_{OUT}	DC output current, per pin	–25	40	mA
V_{ESDHBM}	Electrostatic discharge voltage using the human body model	NA	±2000	V
V_{ESDCDM}	Electrostatic discharge voltage using the charged device model	NA	±500	V
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins, not at the power supply.

Maximum Allowed Overshoot/Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for input currents less than 100 mA and for periods shorter than 20 ns.

Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as percentage of high-time over the lifetime of the device.

A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.2 V can only be at 4.2 V for 10.74% over the lifetime of the device; for device lifetime of 10 years, this amounts to 10.74/10ths of a year. Figure 1–1 shows the way to determine the overshoot duration.

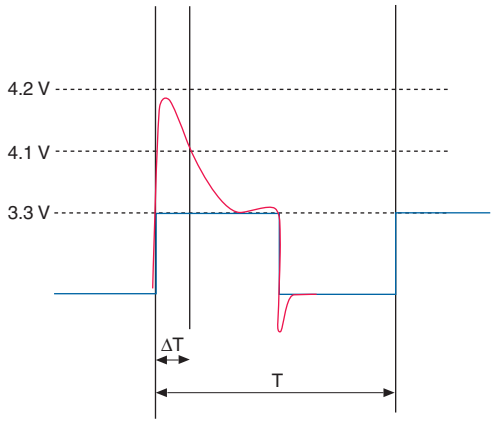
Table 1–2. Maximum Allowed Overshoot During Transitions over 10-Year Time Frame

Symbol	Parameter	Condition	Overshoot Duration as % of High Time	Unit
Vi	AC Input Voltage	V_I = 3.95 V	100	%
		V_I = 4.0 V	95.67	%
		V_I = 4.05 V	55.24	%
		V_I = 4.10 V	31.97	%
		V_I = 4.15 V	18.52	%
		V_I = 4.20 V	10.74	%
		V_I = 4.25 V	6.23	%
		V_I = 4.30 V	3.62	%
		V_I = 4.35 V	2.1	%
		V_I = 4.40 V	1.22	%
		V_I = 4.45 V	0.71	%
		V_I = 4.50 V	0.41	%
		V_I = 4.60 V	0.14	%
		V_I = 4.70 V	0.047	%

Note to Table 1–2:

(1) Figure 1–1 shows the methodology to determine the overshoot duration. In the example in Figure 1–1, overshoot voltage is shown in red and is present on the Cyclone III input pin at over 4.1 V but below 4.2 V. From Table 1–1, for an overshoot of 4.1 V the percentage of high time for the overshoot can be as high as 31.97 % over a 10-year period. Percentage of high time is calculated as ((delta T)/T) × 100. This 10-year period assumes the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations where the device is in an idle state, lifetimes are increased.

Figure 1–1. Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone III devices. The steady-state voltage and current values expected from Cyclone III devices are provided in the Table 1–3. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} *(3)*	Supply voltage for internal logic and input buffers	—	1.15	1.2	1.25	V
V_{CCIO} *(3)*	Supply voltage for output buffers, 3.3-V operation	—	3.15	3.3	3.45	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} *(3)*	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} *(3)*	Supply (digital) voltage for PLL	—	1.15	1.2	1.25	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
tRAMP	Power supply ramptime	Standard POR *(4)*	50 µs	—	50 ms	—
		Fast POR *(5)*	50 µs	—	3 ms	—

Notes to Table 1–3:

(1) V_{CCIO} for all I/O banks should be powered up during device operation. All V_{CCA} pins must be powered to 2.5 V (even when PLLs are not used), and must be powered-up and powered-down at the same time.

(2) V_{CCD_PLL} must always be connected to V_{CCINT} through a decoupling capacitor and ferrite bead.

(3) The V_{CC} must rise monotonically.

(4) POR time for Standard POR will range between 50 – 200 ms. All supplies must be up and stable within 50 ms.

(5) POR time for Fast POR will range between 3 – 9 ms. All supplies must be up and stable within 3 ms.

DC Characteristics

This section lists the I/O leakage currents, pin capacitance, on chip termination tolerance and and bus hold specifications for Cyclone III devices.

Supply Current

Standby current is the current the device draws after the device is configured with no inputs/outputs toggling and no activity in the device. Since these currents vary largely with resources used, use the Excel based Early Power Estimator to get supply current estimates for your design. Table 1–4 lists I/O pin leakage current for Cyclone III.

Table 1–4. Cyclone III I/O Pin Leakage Current *Notes (1), (2)* **(Part 1 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input Pin Leakage Current	$V_I = V_{CCIOMAX}$ to 0 V	–10	—	10	µA
I_{OZ}	Tri-stated I/O Pin Leakage Current	$V_O = V_{CCIOMAX}$ to 0 V	–10	—	10	µA

Table 1–4. Cyclone III I/O Pin Leakage Current *Notes (1), (2)* **(Part 2 of 2)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCINT0}	V_{CCINT} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J= 25C	EP3C5	1.7	*(3)*	mA
			EP3C10	1.7		mA
			EP3C16	3.0		mA
			EP3C25	3.5		mA
			EP3C40	4.3		mA
			EP3C55	5.2		mA
			EP3C80	6.5		mA
			EP3C120	8.4		mA
I_{CCA0}	V_{CCA} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	11.3	*(3)*	mA
			EP3C10	11.3		mA
			EP3C16	11.4		mA
			EP3C25	18.4		mA
			EP3C40	18.6		mA
			EP3C55	18.7		mA
			EP3C80	18.9		mA
			EP3C120	19.2		mA
I_{CCD_PLL0}	V_{CCD_PLL} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	4.1	*(3)*	mA
			EP3C10	4.1		mA
			EP3C16	8.2		mA
			EP3C25	8.2		mA
			EP3C40	8.2		mA
			EP3C55	8.2		mA
			EP3C80	8.2		mA
			EP3C120	8.2		mA
I_{CCIO0}	V_{CCIO} supply current (standby)	V_I = ground, no load, no toggling inputs, T_J = 25C	EP3C5	0.6	*(3)*	mA
			EP3C10	0.6		mA
			EP3C16	0.9		mA
			EP3C25	0.9		mA
			EP3C40	1.3		mA
			EP3C55	1.3		mA
			EP3C80	1.3		mA
			EP3C120	1.2		mA

Notes to Table 1–4:

(1) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5 and 1.2 V).

(2) 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be the observed when the diode is on.

(3) Maximum values depend on the actual T_J and design utilization. Refer to the Excel-based PowerPlay Early Power Estimator (available at **www.altera.com/support/devices/estimator/cy3-estimator/cy3-power_estimator.html**) or the Quartus II PowerPlay Power Analyzer feature for maximum values. Refer to the "Power Consumption" on page 1–11" for more information.

Bus Hold

Bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode. Table 1–5 lists bus hold specifications for Cyclone III. Also listed are the input pin capacitances and on-chip termination tolerance specifications.

Table 1–5. Cyclone III Bus Hold Parameter *Note (1)*

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold low, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold high, overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA
Bus-hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–5:
(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

On-Chip Termination (OCT) Specifications

Table 1–6 lists variation of uncalibrated OCT across process, temperature and voltage.

Table 1–6. Uncalibrated On-Chip Series Termination Specifications **Preliminary**

Symbol	V_{CCIO} (V)	Resistance Tolerance				Unit
		Commercial		Industrial		
		Min	Max	Min	Max	
Series Termination without calibration	3.0	–30	+30	(1)	(1)	%
	2.5	–30	+30	(1)	(1)	%
	1.8	–30	+30	(1)	(1)	%
	1.5	–30	+30	(1)	(1)	%
	1.2	–40	+40	(1)	(1)	%

Note to Table 1–6:
(1) Pending silicon characterization

OCT calibration is automatically performed at power up for OCT enabled I/Os.

Table 1–7 lists the OCT calibration accuracy at power up.

Table 1–7. **On-Chip Series Termination Power-up Calibration Specifications** **Preliminary**

Symbol	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Max	Industrial Max	
Series Termination with power-up calibration	3.0	±10%	*(1)*	%
	2.5	±10%	*(1)*	%
	1.8	±10%	*(1)*	%
	1.5	±10%	*(1)*	%
	1.2	±10%	*(1)*	%

Note to Table 1–7:
(1) Pending silicon characterization

Table 1–8 lists the percentage change of the OCT resistance with voltage and temperature. Use Table 1–8 and Equation 1–1 to determine OCT variation after power-up calibration.

Table 1–8. On-Chip Termination Variation After Power-up Calibration

Nominal Voltage	dR/dT (%ΔOhm/°C)	dR/dmV (%ΔOhm/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Note to Table 1–8:
(1) This table is needed to calculate the final OCT resistance with the variation of temperature and voltage.

Equation 1–1. *Notes (1), (2), (3), (4), (5), (6), (7), (8), (9), (10), (11), (12)*

$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dmV$ ----- (1)

$\Delta R_T = (T_2 - T_1) \times dR/dT$ ----- (2)

For $\Delta R_x < 0$; $MF_x = 1/ (|\Delta R_x| /100 + 1)$ ----- (3)

For $\Delta R_x > 0$; $MF_x = \Delta R_x/100 + 1$ ----- (4)

$MF = MF_V \times MF_T$ ----- (5)

$R_{final} = R_{initial} \times MF$ ----- (6)

Notes to Equation 1–1:

(1) ΔR_V is variation of resistance with voltage.
(2) ΔR_T is variation of resistance with temperature.
(3) dR/dT is the percentage change of resistance with temperature.
(4) dR/dmV is the percentage change of resistance with voltage.
(5) V_2 is final voltage.
(6) V_1 is the initial voltage.
(7) T_2 is the final temperature.
(8) T_1 is the initial temperature.
(9) MF is multiplication factor.
(10) R_{final} is final resistance.
(11) $R_{initial}$ is initial resistance.
(12) Subscript x refers to both $_V$ and $_T$.

For example, to calculate the change of 50 Ω I/O impedance from 25° C at 3.0 V to 85° C at 3.15 V,

$\Delta R_V = (3.15 - 3) \times 1000 \times -0.026 = -3.83$
$\Delta R_T = (85 - 25) \times 0.262 = 15.72$

Since ΔR_V is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Since ΔR_T is positive,

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = \underline{55.71}\ \Omega$

Pin Capacitance

Table 1–9 shows the Cyclone III device family pin capacitance.

Table 1–9. Cyclone III Device Pin Capacitance *Note (1)* ***(Part 1 of 2)*** **Preliminary**

Symbol	Parameter	Typical – QFP	Typical – FBGA	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	7	6	pF
C_{IOLR}	Input capacitance on left/right I/O pins	6	5	pF
C_{LVDSLR}	Input capacitance on left/right I/O pins with Dedicated LVDS output	8	7	pF
C_{VREFLR}	Input capacitance on left/right I/O pins with V_{REF}	21	21	pF
C_{VREFTB}	Input capacitance on top/bottom I/O pins with V_{REF}	21 *(2)*	21 *(2)*	pF
C_{CLKTB}	Input capacitance on top/bottom dedicated clock input pins	7	6	pF

Table 1–9. Cyclone III Device Pin Capacitance Note (1) (Part 2 of 2)				Preliminary
Symbol	**Parameter**	**Typical – QFP**	**Typical – FBGA**	**Unit**
C_{CLKLR}	Input capacitance on left/right dedicated clock input pins	6	5	pF

Notes to Table 1–9:
(1) Pending silicon characterization.
(2) C_{VREFTB} for EP3C25 is 30 pF.

Internal Weak Pull-up and Weak Pull-down Resistor

Table 1–10 lists the weak pull-up and pull-down resistor values for Cyclone III devices.

Table 1–10. Cyclone III Internal Weak Pull-Up / Weak Pull-Down Resistor Note (1)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
R_{CONF_PU} (2)	Value of I/O pin pull-up resistor before and during configuration	V_I = 0 V, V_{CCIO} = 3.3 V ± 5% (3), (4)	7	25	41	KΩ
		V_I = 0 V, V_{CCIO} = 3.0 V ± 5% (3), (4)	7	28	47	KΩ
		V_I = 0 V, V_{CCIO} = 2.5 V ± 5% (3), (4)	8	35	61	KΩ
		V_I = 0 V, V_{CCIO} = 1.8 V ± 5% (3), (4)	10	57	108	KΩ
		V_I = 0 V, V_{CCIO} = 1.5 V ± 5% (3), (4)	13	82	163	KΩ
		V_I = 0 V, V_{CCIO} = 1.2 V ± 5% (3), (4)	19	143	351	KΩ
R_{CONF_PD} (2)	Value of I/O pin pull-down resistor before and during configuration	V_I = 0 V, V_{CCIO} = 3.3 V ± 5% (3), (4)	6	19	30	KΩ
		V_I = 0 V, V_{CCIO} = 3.0 V ± 5% (3), (4)	6	22	36	KΩ
		V_I = 0 V, V_{CCIO} = 2.5 V ± 5% (3), (4)	6	25	43	KΩ
		V_I = 0 V, V_{CCIO} = 1.8 V ± 5% (3), (4)	7	35	71	KΩ
		V_I = 0 V, V_{CCIO} = 1.5 V ± 5% (3), (4)	8	50	112	KΩ

Notes to Table 1–10:
(1) All I/O pins have an option to enable weak pull-up except configuration, test and JTAG pin. Weak pull-down feature is only available for JTAG TCK.
(2) R_{CONF} values are based on characterization. $R_{CONF} = V_{CCIO}/I_{RCONF}$. R_{CONF} values may be different if V_I value is not 0 V. V_I refers to the input voltage at the I/O pin.
(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(4) Minimum condition at –40° C and high V_{CC}, typical condition at 25° C and nominal V_{CC} and maximum condition at 125° C and low V_{CC} for R_{CONF} values.

Hot Socketing

Table 1–11 lists the hot-socketing specifications for Cyclone III devices.

Table 1–11. Cyclone III Hot Socketing Specifications		
Symbol	**Parameter**	**Maximum**
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA (1)

Note to Table 1–11:
(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, where C is I/O pin capacitance and *dv/dt* is the slew rate.

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), and output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Cyclone III devices. Table 1–12 to Table 1–17 show the Cyclone III device family I/O standard specifications. Refer to "Single-ended Voltage referenced I/O Standard" in "Glossary" for voltage referenced receiver input waveform and explanation of terms used in Table 1–12.

***Table 1–12. Single-Ended I/O Standard Specifications** Note (1)*

I/O Standard	V_{CCIO}(V)			V_{IL}(V)		V_{IH}(V)		V_{OL}(V)	V_{OH}(V)	I_{OL} (3) (mA)	I_{OH} (3) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL (2)	3.15	3.3	3.45	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS (2)	3.15	3.3	3.45	—	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL (2)	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0-V LVCMOS (2)	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5-V LVTTL and LVCMOS (2)	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.2	2.1	0.1	–0.1
								0.4	2.0	1	–1
								0.7	1.7	2	–2
1.8-V LVTTL and LVCMOS	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5-V LVCMOS	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2-V LVCMOS	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
PCI and PCI-X	2.85	3.0	3.15	—	0.3 * V_{CCIO}	0.5 * V_{CCIO}	V_{CCIO} + 0.3	0.1 * V_{CCIO}	0.9 * V_{CCIO}	1.5	–0.5

Notes to Table 1–12:

(1) AC load CL = 10 pF.

(2) For more detail of interfacing Cyclone III devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems.

(3) Specified I_{OL} and I_{OH} are valid with lowest current strength setting available for respective I/O standards. I_{OL} and I_{OH} values correspond to the selected current strength settings value. For example, current drive characteristics for 3.3-V LVTTL with 8 mA current strength setting are 8 mA (I_{OL}) and –8 mA (I_{OH}) at 0.45 V (V_{OL}) and 2.4 V (V_{OH}), respectively.

Refer to "Glossary" for explanation of terms used in Table 1–13.

Table 1–13. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V) (3)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 * V_{CCIO} (1)	0.5 * V_{CCIO} (1)	0.52 * V_{CCIO} (1)	—	0.5 * V_{CCIO}	—
				0.47 * V_{CCIO} (2)	0.5 * V_{CCIO} (2)	0.53 * V_{CCIO} (2)			

Notes to Table 1–13:

(1) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.

(2) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

(3) V_{TT} of transmitting device must track V_{REF} of the receiving device.

Table 1–14. Single-Ended SSTL and HSTL I/O Standards Signal Specifications

I/O Standard	$V_{IL(DC)}$(V)		$V_{IH(DC)}$(V)		$V_{IL(AC)}$(V)		$V_{IH(AC)}$(V)		V_{OL}(V)	V_{OH}(V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more illustrations of receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook.*

Table 1–15. Differential SSTL I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			$V_{Swing(DC)}$(V)		$V_{X(DC)}$(V)			$V_{Swing(AC)}$(V)		$V_{OX(AC)}$(V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.7	V_{CCIO}	*(1)*	—	*(1)*
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO}	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125

Note to Table 1–15:
(1) Pending silicon characterization.

Table 1–16. Differential HSTL I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			$V_{DIF(DC)}$(V)		$V_{X(AC)}$(V)			$V_{CM(DC)}$(V)			$V_{DIF(AC)}$(V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.48 * V_{CCIO}	—	0.52 * V_{CCIO}	0.3	0.48 * V_{CCIO}

Refer to "Transmitter Output Waveform" in "Glossary" for an explanation of terms used in Table 1–17.

Table 1–17. Differential I/O Standard Specifications

I/O Standard	V_{CCIO}(V)			V_{TH}(mV)			V_{IN}(V)			V_{OD}(mV) *(1)*			V_{OS}(V) *(1)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(2)*	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVPECL (Column I/Os) *(2)*	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVDS (Row I/Os)	2.375	2.5	2.625	–100	V_{CM} =1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
LVDS (Column I/Os)	2.375	2.5	2.625	–100	V_{CM} = 1.25V	100	0	D_{MAX} ≤500 Mbps	1.85	247	—	600	1.125	1.25	1.375
							0.5	500 Mbps ≤D_{MAX} ≤700 Mbps	1.85						
							1	D_{MAX} > 700 Mbps	1.6						
mini-LVDS (Row I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) *(3) (4)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS® (Row I/Os) *(3) (4)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) *(3)*	2.375	2.5	2.625	—	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–17:

(1) R_L range : 90 ≤R_L ≤110 Ω

(2) LVPECL input standard is only supported at clock input. Output standard is not supported.

(3) Mini-LVDS, RSDS and PPDS standards are only supported at output pins of Cyclone III devices.

(4) RSDS and PPDS are registered trademarks of National Semiconductor.

Power Consumption

Altera® offers two ways to estimate power for a design: the Excel-based Early Power Estimator and the Quartus® II **PowerPlay Power Analyzer** feature.

The interactive Excel-based Early Power Estimator is typically used prior to designing the device in order to get a magnitude estimate of the device power. The Quartus II **PowerPlay Power Analyzer** provides better quality estimates based on the specifics of the design after place-and-route is complete. The **PowerPlay Power Analyzer** can apply a combination of user-entered, simulation-derived, and estimated signal activities which, combined with detailed circuit models, can yield very accurate power estimates.

For more information on power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapters in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Cyclone III core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary and Final. Each designation is defined below.

Preliminary	Final
Preliminary characteristics are created using simulation results, process data, and other known parameters.	Final numbers are based on actual silicon characterization and testing. These numbers reflect the actual performance of the device under worst-case silicon process, voltage and junction temperature conditions.

The upper-right hand corner of a table shows the designation as '***Preliminary***' or '***Final***'.

Core Performance Specifications

Clock Tree Specifications

Table 1–18 lists the clock tree specifications for Cyclone III devices.

Table 1–18. Cyclone III Clock Tree Performance **Preliminary**

Device	Performance			Unit
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
EP3C5	500	*(2)*	*(2)*	MHz
EP3C10	500	*(2)*	*(2)*	MHz
EP3C16	500	*(2)*	*(2)*	MHz
EP3C25	500	*(2)*	*(2)*	MHz
EP3C40	500	*(2)*	*(2)*	MHz
EP3C55	500	*(2)*	*(2)*	MHz
EP3C80	500	*(2)*	*(2)*	MHz
EP3C120	*(1)*	437.5	*(2)*	MHz

Notes to Table 1–18:
(1) EP3C120 offered in –7 and –8 speed grades only.
(2) Pending silicon characterization.

PLL Specifications

Table 1–19 describes the Cyclone III PLL specifications when operating in both the commercial junction temperature range (0° C to 85° C) and the industrial junction temperature range (–40° C to 100° C). For more information on PLL Block, refer to "PLL Block" in "Glossary".

Table 1–19. Cyclone III PLL Specifications *Note (5)* ***(Part 1 of 2)*** **Preliminary**

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} *(1)*	Input clock frequency (–6 speed grade)	5	—	472.5	MHz
	Input clock frequency (–7 speed grade)	5	—	472.5	MHz
	Input clock frequency (–8 speed grade)	5	—	472.5	MHz
f_{INPFD}	PFD input frequency (–6 speed grade)	5	—	325	MHz
	PFD input frequency (–7 speed grade)	5	—	325	MHz
	PFD input frequency (–8 speed grade)	5	—	325	MHz

Table 1–19. Cyclone III PLL Specifications Note (5) (Part 2 of 2)					Preliminary
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
f_{VCO}	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER}$	Input clock period jitter	—	200	—	ps
f_{OUT_EXT} (external clock output) (1)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	472.5	MHz
	PLL output frequency (–8 speed grade)	5	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	5	—	472.5	MHz
	PLL output frequency (–7 speed grade)	5	—	450	MHz
	PLL output frequency (–8 speed grade)	5	—	402.5	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	100 (2)	µs
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
$t_{OU\ TJIT\ TE\ R_DEDCLK}$	Dedicated clock output period jitter	—	—	300	ps
$t_{OU\ TJIT\ TE\ R_IO}$	Regular I/O period jitter	—	—	(4)	ps
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±60	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (3)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz

Notes to Table 1–19:
(1) This parameter is limited in Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
(2) For extended temperature devices, the maximum lock time is 500 µs.
(3) With 100 MHz `scanclk` frequency.
(4) Pending silicon characterization.
(5) V_{CCD_PLL} should always be connected to V_{CCINT} through decoupling capacitor and ferrite bead.

Embedded Multiplier Specifications

Table 1–20 describes the Cyclone III embedded multiplier specifications.

Table 1–20. Cyclone III Embedded Multiplier Specifications					Preliminary
Mode	**Resources Used**	**Performance**			**Unit**
	Number of Multipliers	**–6 Speed Grade**	**–7 Speed Grade**	**–8 Speed Grade**	
9 × 9-bit multiplier	1	260	223	180	MHz
18 × 18-bit multiplier	1	260	223	180	MHz

Memory Block Specifications

Table 1–21 describes the Cyclone III M9K Memory block specifications.

Table 1–21. Cyclone III Memory Block Performance Specifications *Note (1)* — **Preliminary**

Memory	Mode	Resources Used		Performance	
		LEs	M9K Memory	–6 Speed Grade	Unit
M9K Block	FIFO 256×36	47	1	260	MHz
	Single-port 256×36	0	1	260	MHz
	Simple dual-port 256×36 CLK	0	1	260	MHz
	True dual port 512×18 single CLK	0	1	260	MHz

Note to Table 1–21:
(1) Values for device speed grade –7 and –8 will be available after characterization.

Configuration and JTAG Specifications

Table 1–22 lists the Cyclone III Configuration Mode Specifications.

Table 1–22. Cyclone III Configuration Mode Specifications — **Preliminary**

Programming Mode	DCLK F_{max}	Unit
Passive Serial (PS)	133	MHz
Fast Passive Parallel (FPP) *(1)*	100	MHz

Note to Table 1–22:
(1) EP3C25 and smaller family members support 133 MHz.

Table 1–23 lists the Cyclone III Active Configuration Mode Specifications.

Table 1–23. Cyclone III Active Configuration Mode Specifications — **Preliminary**

Programming Mode	DCLK Range	Unit
Active Parallel (AP)	20 – 40	MHz
Active Serial (AS)	20 – 40	MHz

Table 1–24 shows the JTAG timing parameters and values for Cyclone III. For more information, refer to "JTAG Waveform" in "Glossary".

Table 1–24. Cyclone III JTAG Timing Parameters (Part 1 of 2) — **Preliminary**

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI *(1)*	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS *(1)*	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(1)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(1)*	—	15	ns

Table 1–24. Cyclone III JTAG Timing Parameters (Part 2 of 2)				Preliminary
Symbol	**Parameter**	**Min**	**Max**	**Unit**
t_{JPXZ}	JTAG port valid output to high impedance *(1)*	—	15	ns
t_{JSSU}	Capture register setup time *(1)*	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Note to Table 1–24:
(1) The specification is shown for 3.3 V, 3.0 V and 2.5 V LVTTL/LVCMOS operation of JTAG pins. For 1.8- V LVTTL/LVCMOS and 1.5- V LVCMOS, the JTAG port clock to output time is 16 ns.

Periphery Performance

High-Speed I/O Specification

Table 1–25 to Table 1–34 show the high-speed I/O timing for Cyclone III devices. Refer to "Glossary" for definitions of high-speed timing specifications.

Table 1–25. Dedicated RSDS Transmitter Timing Specification *Notes (2), (3)*					
Symbol	**Modes**	**–6 Speed Grade**			**Unit**
		Min	**Typ**	**Max**	
f_{HSCLK} (input clock frequency)	×10	10	—	180	MHz
	×8	10	—	180	MHz
	×7	10	—	180	MHz
	×4	10	—	180	MHz
	×2	10	—	180	MHz
	×1	10	—	360	MHz
Device operation in Mbps	×10	100	—	360	Mbps
	×8	80	—	360	Mbps
	×7	70	—	360	Mbps
	×4	40	—	360	Mbps
	×2	20	—	360	Mbps
	×1	10	—	360	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	*(1)*	ns
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–25:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated RSDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–26. Single-Resistor RSDS Transmitter Timing Specification Notes (2), (3)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	85	MHz
	×8	10	—	85	MHz
	×7	10	—	85	MHz
	×4	10	—	85	MHz
	×2	10	—	85	MHz
	×1	10	—	85	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps
t_{FALL}	80 – 20%	—	(1)	—	ps
t_{LOCK}	—	—	—	(1)	ms

Notes to Table 1–26:

(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Single-resistor RSDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–27. Three-Resistor RSDS Transmitter Timing Specification Notes (2), (3) (Part 1 of 2)

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	MHz
	×8	10	—	155.5	MHz
	×7	10	—	155.5	MHz
	×4	10	—	155.5	MHz
	×2	10	—	155.5	MHz
	×1	10	—	155.5	MHz
Device operation in Mbps	×10	100	—	(1)	Mbps
	×8	80	—	(1)	Mbps
	×7	70	—	(1)	Mbps
	×4	40	—	(1)	Mbps
	×2	20	—	(1)	Mbps
	×1	10	—	(1)	Mbps
t_{DUTY}	—	(1)	—	(1)	%
TCCS	—	—	—	(1)	ps
Output jitter (peak to peak)	—	—	—	(1)	ps
t_{RISE}	20 – 80%	—	(1)	—	ps

Table 1–27. Three-Resistor RSDS Transmitter Timing Specification *Notes (2), (3)* **(Part 2 of 2)**

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–27:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor RSDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–28. Dedicated PPDS Transmitter Timing Specification *Notes (2), (3)*

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	*(1)*	MHz
	×8	10	—	*(1)*	MHz
	×7	10	—	*(1)*	MHz
	×4	10	—	*(1)*	MHz
	×2	10	—	*(1)*	MHz
	×1	10	—	*(1)*	MHz
Device operation in Mbps	×10	100	—	*(1)*	Mbps
	×8	80	—	*(1)*	Mbps
	×7	70	—	*(1)*	Mbps
	×4	40	—	*(1)*	Mbps
	×2	20	—	*(1)*	Mbps
	×1	10	—	*(1)*	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	*(1)*	ps
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–28:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated PPDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–29. Three-Resistor PPDS Transmitter Timing Specification *Notes (2), (3)* **(Part 1 of 2)**

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	*(1)*	MHz
	×8	10	—	*(1)*	MHz
	×7	10	—	*(1)*	MHz
	×4	10	—	*(1)*	MHz
	×2	10	—	*(1)*	MHz
	×1	10	—	*(1)*	MHz

Table 1–29. Three-Resistor PPDS Transmitter Timing Specification *Notes (2), (3)* **(Part 2 of 2)**

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
Device operation in Mbps	×10	100	—	*(1)*	Mbps
	×8	80	—	*(1)*	Mbps
	×7	70	—	*(1)*	Mbps
	×4	40	—	*(1)*	Mbps
	×2	20	—	*(1)*	Mbps
	×1	10	—	*(1)*	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	*(1)*	ps
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–29:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor PPDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–30. Dedicated Mini-LVDS Transmitter Timing Specification *Notes (2), (3)*

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	200	MHz
	×8	10	—	200	MHz
	×7	10	—	200	MHz
	×4	10	—	200	MHz
	×2	10	—	200	MHz
	×1	10	—	400	MHz
Device operation in Mbps	×10	100	—	400	Mbps
	×8	80	—	400	Mbps
	×7	70	—	400	Mbps
	×4	40	—	400	Mbps
	×2	20	—	400	Mbps
	×1	10	—	400	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	1.30	ns
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–30:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated mini-LVDS is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–31. Three-Resistor mini-LVDS Transmitter Timing Specification *Notes (2), (3)*

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	155.5	MHz
	×8	10	—	155.5	MHz
	×7	10	—	155.5	MHz
	×4	10	—	155.5	MHz
	×2	10	—	155.5	MHz
	×1	10	—	155.5	MHz
Device operation in Mbps	×10	100	—	*(1)*	Mbps
	×8	80	—	*(1)*	Mbps
	×7	70	—	*(1)*	Mbps
	×4	40	—	*(1)*	Mbps
	×2	20	—	*(1)*	Mbps
	×1	10	—	*(1)*	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	%
TCCS	—	—	—	*(1)*	ps
Output jitter (peak to peak)	—	—	—	*(1)*	ps
t_{RISE}	20 – 80%	—	*(1)*	—	ps
t_{FALL}	80 – 20%	—	*(1)*	—	ps
t_{LOCK}	—	—	—	*(1)*	ms

Notes to Table 1–31:

(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Three-resistor mini-LVDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–32. Dedicated LVDS Transmitter Timing Specification *Notes (2), (5)* **(Part 1 of 2)**

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max *(3)*	Max *(4)*	
f_{HSCLK} (input clock frequency)	×10	10	—	420	*(1)*	MHz
	×8	10	—	420	*(1)*	MHz
	×7	10	—	420	*(1)*	MHz
	×4	10	—	420	*(1)*	MHz
	×2	10	—	420	*(1)*	MHz
	×1	10	—	420	*(1)*	MHz
HSIODR	×10	100	—	840	*(1)*	Mbps
	×8	80	—	840	*(1)*	Mbps
	×7	70	—	840	*(1)*	Mbps
	×4	40	—	840	*(1)*	Mbps
	×2	20	—	840	*(1)*	Mbps
	×1	10	—	420	*(1)*	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	*(1)*	%
TCCS	—	—	—	248		ps
Output jitter (peak to peak)	—	—	—	*(1)*	—	ps

Table 1–32. Dedicated LVDS Transmitter Timing Specification *Notes (2), (5)* **(Part 2 of 2)**

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max *(3)*	Max *(4)*	
t_{RISE}	20 – 80%	*(1)*	*(1)*	*(1)*	*(1)*	ps
t_{FALL}	80 – 20%	*(1)*	*(1)*	*(1)*	*(1)*	ps
t_{LOCK}	—	—	—	*(1)*	—	ms

Notes to Table 1–32:

(1) Pending silicon characterization.

(2) Values for device speed grade –7 and –8 will be available after characterization.

(3) The maximum data rate that complies with duty cycle distortion of 45–55%.

(4) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1625 ps) and a tDUTY of 250 ps, the duty cycle distortion is:
tDUTY/(UI*2) *100% = 250 ps/(1625 *2) * 100% = 7.7%, which gives you a duty cycle distortion of 42.3–57.7%.

(5) Dedicated LVDS transmitter is only supported at output pin of Row I/O (Banks 1, 2, 5, and 6).

Table 1–33. Three-Resistor LVDS Transmitter Timing Specification *Notes (2), (5)* **(Part 1 of 2)**

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max *(3)*	Max *(4)*	
f_{HSCLK} (input clock frequency)	×10	10	—	320	320	MHz
	×8	10	—	320	320	MHz
	×7	10	—	320	320	MHz
	×4	10	—	320	320	MHz
	×2	10	—	320	320	MHz
	×1	10	—	402.5	402.5	MHz
HSIODR	×10	*(1)*	—	*(1)*	*(1)*	Mbps
	×8	*(1)*	—	*(1)*	*(1)*	Mbps
	×7	*(1)*	—	*(1)*	*(1)*	Mbps
	×4	*(1)*	—	*(1)*	*(1)*	Mbps
	×2	*(1)*	—	*(1)*	*(1)*	Mbps
	×1	*(1)*	—	*(1)*	*(1)*	Mbps
t_{DUTY}	—	*(1)*	—	*(1)*	*(1)*	%
TCCS	—	—	—	*(1)*	*(1)*	ps
Output jitter (peak to peak)	—	—	—	*(1)*	*(1)*	ps
t_{RISE}	20 – 80%	*(1)*	*(1)*	*(1)*	*(1)*	ps
t_{FALL}	80 – 20%	*(1)*	*(1)*	*(1)*	*(1)*	ps

Table 1–33. Three-Resistor LVDS Transmitter Timing Specification *Notes (2), (5)* **(Part 2 of 2)**

Symbol	Modes	–6 Speed Grade				Unit
		Min	Typ	Max *(3)*	Max *(4)*	
t_{LOCK}	—	—	—	*(1)*	—	ms

Notes to Table 1–33:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) The maximum data rate that complies with duty cycle distortion of 45–55%.
(4) The maximum data rate when taking duty cycle in absolute ps into consideration that may not comply with 45–55% duty cycle distortion. If the downstream receiver can handle duty cycle distortion beyond the 45–55% range, you may use the higher data rate values from this column. You can calculate the duty cycle distortion as a percentage using the absolute ps value. For example, for a data rate of 640 Mbps (UI = 1625 ps) and a t_{DUTY} of 250 ps, the duty cycle distortion is t_{DUTY}/(UI*2) *100% = 250 ps/(1625 *2) * 100% = 7.7%, which gives you a duty cycle distortion of 42.3–57.7%.
(5) Three-resistor LVDS is only supported at output pin of Column I/O (Banks 3, 4, 7, and 8).

Table 1–34. Dedicated LVDS Receiver Timing Specification *Notes (2), (3)*

Symbol	Modes	–6 Speed Grade			Unit
		Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	10	—	437.5	MHz
	×8	10	—	437.5	MHz
	×7	10	—	437.5	MHz
	×4	10	—	437.5	MHz
	×2	10	—	437.5	MHz
	×1	10	—	437.5	MHz
HSIODR	×10	100	—	875	Mbps
	×8	80	—	875	Mbps
	×7	70	—	875	Mbps
	×4	40	—	875	Mbps
	×2	20	—	875	Mbps
	×1	10	—	437.5	Mbps
SW	—	—	—	400	ps
Input jitter tolerance	—	—	—	*(1)*	ps
t_{LOCK}	—	—	—	*(1)*	ps

Notes to Table 1–34:
(1) Pending silicon characterization.
(2) Values for device speed grade –7 and –8 will be available after characterization.
(3) Dedicated LVDS Receiver is supported at all banks.

External Memory Interface Specifications

Cyclone III devices support external memory interfaces up to 200 MHz. Cyclone III external memory interfaces are auto-calibrating and easy to implement. Table 1–35 to Table 1–38 list the External Memory Interface Specifications for the Cyclone III device family.

Use the following tables for memory interface timing analysis.

Table 1–35. Cyclone III Maximum Clock Rate Support for External Memory Interfaces *Notes (1) (5)*

Memory Standard	I/O Standard	Commercial					
		–6 Speed Grade (MHz)		–7 Speed Grade (MHz)		–8 Speed Grade (MHz)	
		Column I/Os	Row I/Os	Column I/Os	Row I/Os	Column I/Os	Row I/Os
DDR2 SDRAM *(2)*	SSTL-18 class I	200	167	167	150	167	133
	SSTL-18 class II	133	125	125	*(3)*	*(3)*	*(3)*
DDR SDRAM *(2)*	SSTL-2 class I	167	150	150	133	133	125
	SSTL-2 class II	133	125	125	100	100	*(3)*
QDRII SRAM *(4)*	1.8-V HSTL class I	167	150	150	133	133	125
	1.8V HSTL class II	100	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*

Notes to Table 1–35:
(1) These numbers are preliminary until characterization is final.
(2) The values apply for interfaces with both modules and components.
(3) Support will be evaluated after characterization.
(4) QDRII SRAM also supports the 1.5-V HSTL I/O standard. However, Altera recommends using the 1.8-V HSTL I/O standard for maximum performance because of the higher I/O Current Strength.
(5) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–36. FPGA Sampling Window (SW) Requirement – Read Side *Note (1)* **Preliminary**

Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Units
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	
DDR2 SDRAM	620	620	745	745	755	755	840	840	790	790	945	945	ps
DDR SDRAM	595	595	730	730	728	728	843	843	850	850	975	975	ps
QDRII SRAM	695	695	780	780	790	790	885	885	895	895	970	970	ps

Note to Table 1–36:
(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–37. Transmitter Channel-to-Channel Skew (TCCS) – Write Side Note (1)													Preliminary
Memory Standards	–6 Speed Grade				–7 Speed Grade				–8 Speed Grade				Units
	Column I/Os		Row I/Os		Column I/Os		Row I/Os		Column I/Os		Row I/Os		
	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	Lead	Lag	
DDR2 SDRAM	585	585	645	645	595	595	650	650	595	595	660	660	ps
DDR SDRAM	610	610	670	670	620	620	680	680	630	630	685	685	ps
QDRII SRAM	670	670	725	725	675	675	735	735	685	685	740	740	ps

Note to Table 1–37:
(1) Column I/Os refer to Top and Bottom I/Os. Row I/Os refer to Right and Left I/Os.

Table 1–38. DDIO Outputs Half-Period Jitter			
Name	Description	Max	Unit
$t_{OUTFULLJITTER}$	Half-period jitter (PLL driving DDIO outputs)	(1)	ps

Note to Table 1–38:
(1) Pending silicon characterization.

DCD Specifications

Table 1–39 lists the worst case duty cycle distortion for Cyclone III devices. Detailed information on duty cycle distortion will be published after characterization.

Table 1–39. Duty Cycle Distortion on Cyclone III I/O Pins Notes (1) (2)							
Symbol	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	40	60	%

Notes to Table 1–39:
(1) Preliminary DCD specification applies to clock outputs from PLLs, global clock tree and IOE driving dedicated and general purpose I/O pins.
(2) Detailed DCD specification pending silicon characterization.

I/O Timing

Timing Model

The DirectDrive™ technology and MultiTrack™ interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Cyclone III device densities and speed grades. This section describes and specifies the performance of I/Os and internal timing.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

The timing numbers listed in the tables of this section are extracted from the Quartus II software version 7.0 Build 31.

Preliminary, Correlated and Final Timing

Timing models can have either preliminary, correlated, or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 1–40 shows the status of the Cyclone III device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Correlated numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Final timing numbers are based on complete correlation to actual devices and addressing any minor deviations from the correlated timing model. When the timing models are final, all or most of the Cyclone III family devices have been completely characterized and no further changes to the timing model are expected.

Table 1–40. Cyclone III Device Timing Model Status

Device	Preliminary	Correlated	Final
EP3C5	*(1)*	—	—
EP3C10	✓	—	—
EP3C16	✓	—	—
EP3C25	✓	—	—
EP3C40	✓	—	—
EP3C55	✓	—	—
EP3C80	✓	—	—
EP3C120	✓	—	—

Note to Table 1–40:
(1) Timing model for EP3C5 will be available in Quartus II software 7.1.

I/O Timing Measurement Methodology

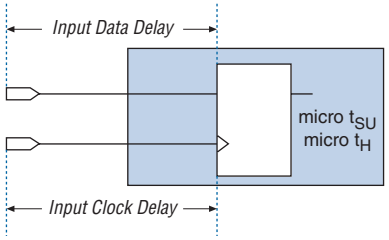
Altera characterizes timing delays at the worst-case process, minimum voltage, and maximum temperature for input register setup time (t_{SU}) and hold time (t_H). The Quartus II software uses the following equations to calculate t_{SU} and t_H timing for Cyclone III devices input signals:

t_{SU} = + data delay from input pin to input register
+ micro setup time of the input register
– clock delay from input pin to input register

t_H = – data delay from input pin to input register
+ micro hold time of the input register
+ clock delay from input pin to input register

Figure 1–2 shows the setup and hold timing diagram for input registers.

Figure 1–2. Input Register Setup and Hold Timing Diagram



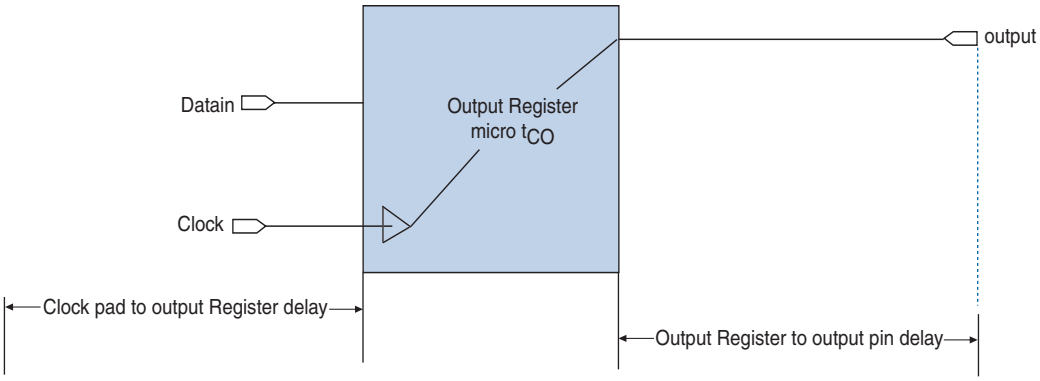
For output timing, different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination for each I/O standard and with 0 pF (except for PCI and PCI-X which use 10 pF) loading and the timing is specified up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standards.

The following measurements are made during device characterization. Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for default loading conditions shown in Table 1–41. Use the following equations to calculate clock pin to output pin timing for Cyclone III devices.

t_{CO} from clock pin to I/O pin =

- + delay from clock pad to I/O output register
- + IOE output register clock-to-output delay
- + delay from output register to output pin

Figure 1–3. Output Register Clock to Output Timing Diagram



Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by the Quartus II software and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 1–41.

2. Record the time to V_{MEAS}.

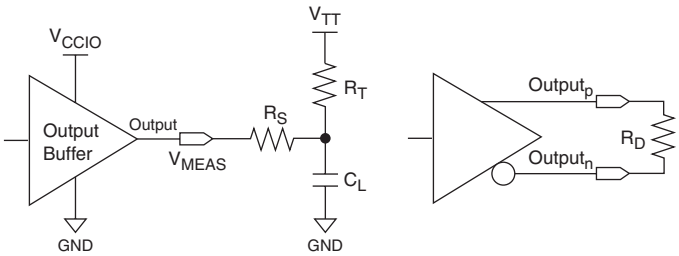
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.

4. Record the time to V_{MEAS}.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-output) of the PCB trace.

The Quartus II software reports the timing with the conditions shown in Table 1–41 using the above equation. Figure 1–4 shows the model of the circuit that is represented by the output timing of the Quartus II software.

***Figure 1–4. Output Delay Timing Reporting Setup Modeled by Quartus II** Notes (1), (2)*



Notes to Figure 1–4:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) V_{CCINT} is 1.10 V unless otherwise specified.

Figure 1–5 and Figure 1–6 show the I/O interface with single and multiple external output resistors.

Figure 1–5. I/O Interface with Single External Output Resistor

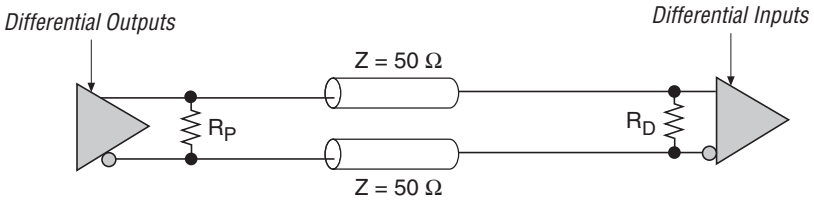


Figure 1–6. I/O Interface with Three External Output Resistor Network

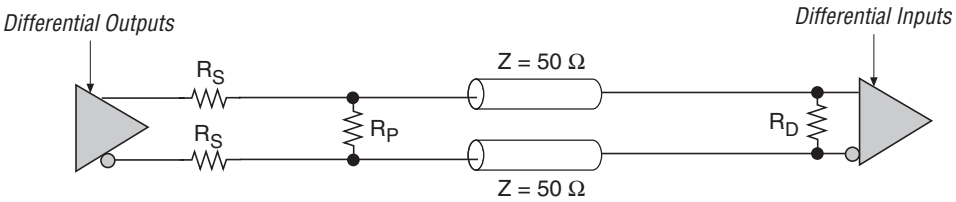


Table 1–41. Output Timing Measurement Methodology for Output Pins Notes (1), (2), (4), (5) **Preliminary**

I/O Standard	Loading and Termination							Measurement Point
	R_S (Ω)	R_T (Ω)	R_D (Ω)	R_P (Ω)	V_{CCIO} (V)	V_{TT} (V)	C_L (pF)	V_{MEAS} (V)
3.3-V LVTTL	—	—	—	—	3.135	—	0	1.5675
3.3-V LVCMOS	—	—	—	—	3.135	—	0	1.5675
3.0-V LVTTL	—	—	—	—	2.85	—	0	1.425
3.0-V LVCMOS	—	—	—	—	2.85	—	0	1.425
2.5-V LVTTL/LVCMOS	—	—	—	—	2.375	—	0	1.1875
1.8-V LVTTL/LVCMOS	—	—	—	—	1.71	—	0	0.855
1.5-V LVCMOS	—	—	—	—	1.425	—	0	0.7125
1.2-V LVCMOS	—	—	—	—	1.15	—	0	0.575
3.0-V PCI	—	—	—	—	2.85	—	10	1.425
3.0-V PCI-X	—	—	—	—	2.85	—	10	1.425
SSTL-2 Class I	25	50	—	—	2.375	1.1875	0	1.1875
SSTL-2 Class II	25	25	—	—	2.375	1.1875	0	1.1875
SSTL-18 Class I	25	50	—	—	1.71	0.855	0	0.855
SSTL-18 Class II	25	25	—	—	1.71	0.855	0	0.855
1.8-V HSTL Class I	50	50	—	—	1.71	0.855	0	0.855
1.8-V HSTL Class II	25	25	—	—	1.71	0.855	0	0.855
1.5-V HSTL Class I	50	50	—	—	1.425	0.7125	0	0.7125
1.5-V HSTL Class II	—	25	—	—	1.425	0.7125	0	0.7125
1.2-V HSTL CLASS I	—	50	—	—	1.15	0.575	0	0.575
1.2-V HSTL CLASS II	—	25 (50 || 50)	—	—	1.15	0.575	0	0.575
LVDS	—	—	100	—	2.375	—	0	1.1875
LVDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
mini-LVDS	—	—	100	—	2.375	—	0	1.1875
mini-LVDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
PPDS	—	—	100	—	2.375	—	0	1.1875
PPDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875
RSDS	—	—	100	—	2.375	—	0	1.1875
RSDS_E_1R	—	—	100	100 *(6)*	2.375	—	0	1.1875
RSDS_E_3R	120 *(6)*	—	100	170 *(6)*	2.375	—	0	1.1875

Notes to Table 1–41:

(1) Input measurement point at internal node is $0.5 \times V_{CCINT}$.

(2) Output measuring point for V_{MEAS} at buffer output is $0.5 \times V_{CCIO}$.

(3) Input stimulus edge rate is 0 to V_{CC} in 0.2 ns (internal signal) from the driver preceding the I/O buffer.

(4) Less than 50-mV ripple on V_{CCIO}. V_{CCINT} = 1.10 V with less than 30-mV ripple.

(5) The interface has to use external termination RT. The termination voltage V_{TT} may either be supplied by an independent power supply or created through a Thevenin equivalent circuit.

(6) Pending silicon characterization.

I/O Default Capacitive Loading

Refer to Table 1–42 for default capacitive loading of different I/O standards.

Table 1–42. Default Loading of Different I/O Standards for Cyclone III **Preliminary**

I/O Standard	Capacitive Load	Unit
3.3-V LVTTL	0	pF
3.3-V LVCMOS	0	pF
3.0-V LVTTL	0	pF
3.0-V LVCMOS	0	pF
2.5-V LVTTL/LVCMOS	0	pF
1.8-V LVTTL/LVCMOS	0	pF
1.5-V LVCMOS	0	pF
1.2-V LVCMOS	0	pF
3.0-V PCI	10	pF
3.0-V PCI-X	10	pF
SSTL-2 Class I	0	pF
SSTL-2 Class II	0	pF
SSTL-18 Class I	0	pF
SSTL-18 Class II	0	pF
1.8-V HSTL Class I	0	pF
1.8-V HSTL Class II	0	pF
1.5-V HSTL Class I	0	pF
1.5-V HSTL Class II	0	pF
1.2-V HSTL CLASS I	0	pF
1.2-V HSTL CLASS II	0	pF
Differential SSTL-2 Class I	0	pF
Differential SSTL-2 Class II	0	pF
Differential SSTL-18 Class I	0	pF
Differential SSTL-18 Class II	0	pF
1.2-V Differential HSTL Class I	0	pF
1.2-V Differential HSTL Class II	0	pF
1.5-V Differential HSTL Class I	0	pF
1.5-V Differential HSTL Class II	0	pF
1.8-V Differential HSTL Class I	0	pF
1.8-V Differential HSTL Class II	0	pF
LVDS	0	pF
LVDS_E_3R	0	pF
mini-LVDS	0	pF
mini-LVDS_E_3R	0	pF
PPDS	0	pF
PPDS_E_3R	0	pF
RSDS	0	pF
RSDS_E_1R	0	pF
RSDS_E_3R	0	pF

Maximum Input and Output Clock Toggle Rate

The maximum clock toggle rate is defined as the maximum frequency achievable for a clock type signal at an I/O pin. The I/O pin can be a regular I/O pin or a dedicated clock I/O pin.

The maximum clock toggle rate is different from the maximum data bit rate. If the maximum clock toggle rate on a regular I/O pin is 300 MHz, the maximum data bit rate for dual data rate (DDR) could be potentially as high as 600 Mbps on the same I/O pin.

Table 1–43 specifies the maximum input clock toggle rates. Table 1–44 specifies the maximum output clock toggle rates at 0 pF load. Table 1–45 specifies the derating factors for the output clock toggle rate for a non 0 pF load.

To calculate the output toggle rate for a non 0 pF load, use this formula:

The toggle rate for a non 0 pF load

= 1000 / (1000/ toggle rate at 0 pF load + derating factor * load value in pF /1000)

For example, the output toggle rate at 0 pF load for SSTL-18 Class II 16 µA I/O standard is 260 MHz on a –6 device clock output pin. The derating factor is 26 ps/pF. For a 10 pF load the toggle rate is calculated as:

1000 / (1000/260 + 26 × 10 /1000) = 243 (MHz)

Table 1–43 through Table 1–45 show the I/O toggle rates for Cyclone III devices.

Table 1–43. Maximum Input Toggle Rate on Cyclone III Devices (Part 1 of 2) **Preliminary**

I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	450	405	360	450	405	360	450	405	360
3.3-V LVCMOS	450	405	360	450	405	360	450	405	360
3.0-V LVTTL	450	405	360	450	405	360	450	405	360
3.0-V LVCMOS	450	405	360	450	405	360	450	405	360
2.5-V LVTTL/LVCMOS	450	405	360	450	405	360	450	405	360
1.8-V LVTTL/LVCMOS	450	405	360	450	405	360	450	405	360
1.5-V LVCMOS	300	270	240	300	270	240	300	270	240
1.2-V LVCMOS	300	270	240	300	270	240	300	270	240
SSTL_2_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_2_CLASS_II	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_I	500	500	500	500	500	500	500	500	500
SSTL_18_CLASS_II	500	500	500	500	500	500	500	500	500
1.8 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.8 V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.5 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.5 V_HSTL_CLASS_II	500	500	500	500	500	500	500	500	500
1.2 V_HSTL_CLASS_I	500	500	500	500	500	500	500	500	500
1.2 V_HSTL_CLASS_II	500	500	500	*(1)*	*(1)*	*(1)*	500	500	500
3.0-V PCI	350	315	280	350	315	280	350	315	280

Table 1–43. Maximum Input Toggle Rate on Cyclone III Devices (Part 2 of 2) **Preliminary**

I/O Standard	Maximum Input Toggle Rate on CIII Devices (MHz)								
	Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.0-V PCI-X	350	315	280	350	315	280	350	315	280
DIFFERENTIAL_SSTL_2_CLASS_I	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
DIFFERENTIAL_SSTL_2_CLASS_II	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_I	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
DIFFERENTIAL_SSTL_18_CLASS_II	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.8 V_DIFFERENTIAL_HSTL_CLASS_I	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.8 V_DIFFERENTIAL_HSTL_CLASS_II	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.5 V_DIFFERENTIAL_HSTL_CLASS_I	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.5 V_DIFFERENTIAL_HSTL_CLASS_II	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.2 V_DIFFERENTIAL_HSTL_CLASS_I	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
1.2 V_DIFFERENTIAL_HSTL_CLASS_II	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	*(2)*	500	500	500
LVPECL	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	403	403	403
LVDS	403	403	403	438	438	438	403	403	403

Notes to Table 1–43:

(1) The 1.2 V_HSTL_CLASS_II is only supported on column I/O pins.

(2) Input differential standard is only supported on GCLK pin.

(3) Input LVPECL is only supported on GCLK pin.

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 1 of 4) **Preliminary**

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	4 mA	120	100	80	120	100	80	120	100	80
	8 mA	200	170	140	200	170	140	200	170	140
3.3-V LVCMOS	2 mA	120	100	80	120	100	80	120	100	80
3.0-V LVTTL	4 mA	185	155	125	100	86	70	185	155	125
	8 mA	220	190	150	170	145	120	220	190	150
	12 mA	300	245	200	240	200	160	300	245	200
	16 mA	311	260	215	250	205	170	311	260	215
3.0-V LVCMOS	4 mA	280	233	190	195	165	130	280	233	190
	8 mA	280	233	190	220	180	150	280	233	190
	12 mA	300	250	205	240	200	165	300	250	205
	16 mA	311	260	210	250	210	170	311	260	210

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 2 of 4) **Preliminary**

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	4 mA	200	166	133	100	83	66	200	166	133
	8 mA	200	166	133	155	130	100	200	166	133
	12 mA	305	255	210	245	205	165	305	255	210
	16 mA	311	280	240	250	225	195	311	280	240
1.8-V LVTTL/LVCMOS	2 mA	210	170	140	85	70	60	210	170	140
	4 mA	255	210	170	130	110	85	255	210	170
	6 mA	285	233	195	160	130	110	285	233	195
	8 mA	250	210	166	170	140	115	250	210	166
	10 mA	266	220	185	215	180	150	266	220	185
	12 mA	311	260	210	250	210	170	311	260	210
	16 mA	311	260	210	250	210	170	311	260	210
1.5-V LVCMOS	2 mA	290	145	120	60	45	36	290	145	120
	4 mA	225	190	155	93	80	66	225	190	155
	6 mA	245	200	166	129	110	86	245	200	166
	8 mA	240	195	166	166	136	115	240	195	166
	10 mA	266	220	185	215	180	150	266	220	185
	12 mA	311	260	210	250	210	170	311	260	210
	16 mA	311	260	210	250	210	170	311	260	210
1.2-V LVCMOS	2 mA	190	145	120	66	50	40	190	145	120
	4 mA	225	190	155	110	90	75	225	190	155
	6 mA	245	200	166	150	125	100	245	200	166
	8 mA	240	197	166	192	160	133	240	197	166
	10 mA	266	220	185	250	210	175	266	220	185
	12 mA	311	260	210	*(2)*	*(2)*	*(2)*	311	260	210
SSTL_2_CLASS_I	8 mA	300	255	210	250	210	175	300	255	210
	12 mA	300	255	210	250	210	175	300	255	210
SSTL_2_CLASS_II	16 mA	300	250	205	250	205	170	300	250	205
SSTL_18_CLASS_I	8 mA	320	270	220	280	233	190	320	270	220
	10 mA	320	260	215	290	233	290	320	260	215
	12 mA	333	270	225	300	250	200	333	270	225
SSTL_18_CLASS_II	12 mA	333	280	233	266	233	190	333	280	233
	16 mA	333	280	233	300	250	210	333	280	233
1.8 V_HSTL_CLASS_I	8 mA	290	245	200	270	230	190	290	245	200
	10 mA	310	260	220	310	260	220	310	260	220
	12 mA	333	280	230	333	280	230	333	280	230
1.8 V_HSTL_CLASS_II	16 mA	333	275	233	300	250	210	333	275	233
1.5 V_HSTL_CLASS_I	8 mA	320	260	210	275	220	180	320	260	210
	10 mA	320	260	220	285	235	195	320	260	220
	12 mA	333	275	233	300	250	210	333	275	233
1.5 V_HSTL_CLASS_II	16 mA	333	270	222	300	240	200	333	270	222

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 3 of 4) **Preliminary**

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.2 V_HSTL_CLASS_I	8 mA	240	190	160	250	205	160	240	190	160
	10 mA	240	195	160	250	205	160	240	195	160
	12 mA	250	210	175	(2)	(2)	(2)	250	210	175
1.2 V_HSTL_CLASS_II	14 mA	250	200	166	(2)	(2)	(2)	250	200	166
3.0-V PCI	—	133	120	106	133	120	105	133	120	106
3.0-V PCI-X	—	133	120	106	133	120	105	133	120	106
DIFFERENTIAL_SSTL_2_CLASS_I	8 mA	(3)	(3)	(3)	(3)	(3)	(3)	400	340	280
	12 mA	(3)	(3)	(3)	(3)	(3)	(3)	400	340	280
DIFFERENTIAL_SSTL_2_CLASS_II	16 mA	(3)	(3)	(3)	(3)	(3)	(3)	350	290	240
DIFFERENTIAL_SSTL_18_CLASS_I	8 mA	(3)	(3)	(3)	(3)	(3)	(3)	260	220	180
	10 mA	(3)	(3)	(3)	(3)	(3)	(3)	270	220	180
	12 mA	(3)	(3)	(3)	(3)	(3)	(3)	280	230	190
DIFFERENTIAL_SSTL_18_CLASS_II	16 mA	(3)	(3)	(3)	(3)	(3)	(3)	260	220	180
1.8 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	(3)	(3)	(3)	(3)	(3)	(3)	260	220	180
	10 mA	(3)	(3)	(3)	(3)	(3)	(3)	300	250	210
	12 mA	(3)	(3)	(3)	(3)	(3)	(3)	320	270	220
1.8 V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	(3)	(3)	(3)	(3)	(3)	(3)	230	190	160
1.5 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	(3)	(3)	(3)	(3)	(3)	(3)	210	170	140
	10 mA	(3)	(3)	(3)	(3)	(3)	(3)	220	180	150
	12 mA	(3)	(3)	(3)	(3)	(3)	(3)	230	190	160
1.5 V_DIFFERENTIAL_HSTL_CLASS_II	16 mA	(3)	(3)	(3)	(3)	(3)	(3)	210	170	140
1.2 V_DIFFERENTIAL_HSTL_CLASS_I	8 mA	(3)	(3)	(3)	(3)	(3)	(3)	210	170	140
	10 mA	(3)	(3)	(3)	(3)	(3)	(3)	220	180	150
	12 mA	(3)	(3)	(3)	(3)	(3)	(3)	230	190	160
1.2 V_DIFFERENTIAL_HSTL_CLASS_II	14 mA	(3)	(3)	(3)	(3)	(3)	(3)	210	170	140
LVDS	—	(6)	(6)	(6)	438	370	305	438	370	305
LVDS_E_3R	—	350	300	245	(5)	(5)	(5)	438	370	305
mini-LVDS	—	(4)	(4)	(4)	200	170	140	200	170	140
mini-LVDS_E_3R	—	200	170	140	(5)	(5)	(5)	200	170	140
PPDS	—	(4)	(4)	(4)	220	187	154	220	187	154
PPDS_E_3R	—	220	187	154	(5)	(5)	(5)	220	187	154
RSDS	—	(4)	(4)	(4)	180	153	126	180	153	126
RSDS_E_1R	—	180	153	126	(5)	(5)	(5)	180	153	126
RSDS_E_3R	—	180	153	126	(5)	(5)	(5)	180	153	126
3.0-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

Table 1–44. Maximum Output Toggle Rate on Cyclone III Devices (Part 4 of 4) **Preliminary**

I/O Standard		Maximum Output Toggle Rate on CIII Devices (MHz)								
		Column I/O Pins			Row I/O Pins			Dedicated Clock Inputs		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
1.8-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
1.2-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

Notes to Table 1–44:

(1) The current version of the Quartus II software does not have the information for the standard.
(2) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I / II (12 mA and 14 mA respectively) are only supported on column I/O pins.
(3) Output differential standard is only supported on `PLLCLKOUT` pin.
(4) Dedicated differential standards are supported at row I/O pins.
(5) Differential standards with external resistor network are supported at column I/O pins.
(6) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 1 of 3) **Preliminary**

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	4 mA	117	123	123	116	122	122
	8 mA	50	52	52	50	52	52
3.3V LVCMOS	2 mA	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V LVTTL	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V LVCMOS	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 2 of 3) **Preliminary**

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
2.5-V LVTTL/LVCMOS	4 mA	36	37	37	35	37	37
	8 mA	30	32	32	30	32	32
	12 mA	27	28	28	(1)	(1)	(1)
	16 mA	26	27	27	(1)	(1)	(1)
1.8-V LVTTL/LVCMOS	2 mA	115	121	121	116	121	121
	4 mA	93	97	97	91	96	96
	6 mA	48	50	50	47	50	50
	8 mA	39	41	41	39	41	41
	10 mA	36	37	37	35	37	37
	12 mA	33	35	35	33	34	34
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
1.5-V LVCMOS	2 mA	164	172	172	164	172	172
	4 mA	92	96	96	91	96	96
	6 mA	44	46	46	43	45	45
	8 mA	37	39	39	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	(1)	(1)	(1)	(1)	(1)	(1)
1.2-V LVCMOS	2 mA	(1)	(1)	(1)	(1)	(1)	(1)
	4 mA	(1)	(1)	(1)	(1)	(1)	(1)
	6 mA	(1)	(1)	(1)	(1)	(1)	(1)
	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(2)	(2)	(2)
SSTL_2_CLASS_I	8 mA	26	27	27	25	27	27
	12 mA	25	26	26	25	26	26
SSTL_2_CLASS_II	16 mA	28	29	29	27	28	28
SSTL_18_CLASS_I	8 mA	24	25	25	23	24	24
	10 mA	23	24	24	24	25	25
	12 mA	24	25	25	(1)	(1)	(1)
SSTL_18_ CLASS_II	16 mA	26	27	27	(1)	(1)	(1)
	18 mA	26	27	27	(1)	(1)	(1)
1.8 V_HSTL_ CLASS_I	8 mA	24	25	25	25	26	26
	10 mA	26	27	27	23	24	24
	12 mA	26	28	28	25	26	26
1.8 V_HSTL_ CLASS_II	12 mA	(1)	(1)	(1)	(1)	(1)	(1)
	16 mA	30	31	31	(1)	(1)	(1)

Table 1–45. Maximum Output Clock Toggle Rate Derating Factors on Cyclone III Devices (Part 3 of 3) **Preliminary**

I/O Standard	Current Strength or OCT Setting	Maximum Output Clock Toggle Rate Derating Factors (ps/pf)					
		Column I/O Pins			Row I/O Pins		
		–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
1.5 V_HSTL_ CLASS_I	8 mA	26	28	28	25	26	26
	10 mA	25	27	27	(1)	(1)	(1)
	12 mA	25	26	26	(1)	(1)	(1)
1.5 V_HSTL_ CLASS_II	16 mA	31	33	33	(1)	(1)	(1)
1.2 V_HSTL_ CLASS_I	8 mA	(1)	(1)	(1)	(1)	(1)	(1)
	10 mA	(1)	(1)	(1)	(1)	(1)	(1)
	12 mA	(1)	(1)	(1)	(2)	(2)	(2)
1.2 V_HSTL_ CLASS_II	14 mA	(1)	(1)	(1)	(2)	(2)	(2)
3.0-V PCI	—	(1)	(1)	(1)	(1)	(1)	(1)
3.0-V PCI-X	—	(1)	(1)	(1)	(1)	(1)	(1)
LVDS	—	(6)	(6)	(6)	39	41	41
LVDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
mini-LVDS	—	(4)	(4)	(4)	(1)	(1)	(1)
mini-LVDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
PPDS	—	(4)	(4)	(4)	(1)	(1)	(1)
PPDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
RSDS	—	(4)	(4)	(4)	(1)	(1)	(1)
RSDS_E_1R	—	(1)	(1)	(1)	(5)	(5)	(5)
RSDS_E_3R	—	(1)	(1)	(1)	(5)	(5)	(5)
3.0-V	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
2.5-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	240	200	160	240	200	160
1.8-V LVTTL/LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	290	240	200	290	240	200
1.2-V LVCMOS	OCT_25_OHMS	(1)	(1)	(1)	(1)	(1)	(1)
	OCT_50_OHMS	(1)	(1)	(1)	(1)	(1)	(1)

Notes to Table 1–45:

(1) Current version of Quartus II software does not have the information for the standard.
(2) The 1.2 V (12 mA) and 1.2 V_HSTL_CLASS_I/II (12 mA and 14 mA, respectively) are only supported on column I/O pins.
(3) Output differential standard is only supported on `PLLCLKOUT` pin.
(4) Dedicated differential standards are supported at row I/O pins.
(5) Differential standards with external resistor network are supported at column I/O pins.
(6) Output dedicated LVDS is only supported on row I/O pins. Input dedicated LVDS is supported at all I/O pins.
(7) Indicate the lowest value of derating factor.

IOE Programmable Delay

Table 1–46 and Table 1–47 show IOE programmable delay for Cyclone III devices.

Table 1–46. Cyclone III IOE Programmable Delay on Column Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad to I/O dataout to core	7	0	1.369	0	2.267	0	2.413	0	2.526	ns
Input Delay from Pin to Input Register	Pad to I/O input register	8	0	1.528	0	2.446	0	2.571	0	2.696	ns
Delay from Output Register to Output Pin	I/O output register to Pad	2	0	0.582	0	1	0	1.098	0	1.199	ns

Notes to Table 1–46:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.
(3) The fast model timing parameter is for commercial devices.

Table 1–47. Cyclone III IOE Programmable Delay on Row Pins Notes (1), (2)

Parameter	Paths Affected	Number of Settings	Fast Corner (3)		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		Unit
			Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	Min Offset	Max Offset	
Input Delay from Pin to Internal Cells	Pad to I/O dataout to core	7	0	1.369	0	2.244	0	2.39	0	2.495	ns
Input Delay from Pin to Input Register	Pad to I/O input register	8	0	1.538	0	2.459	0	2.586	0	2.716	ns
Delay from Output Register to Output Pin	I/O output register to Pad	2	0	0.62	0	1.065	0	1.171	0	1.277	ns

Notes to Table 1–47:
(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.
(2) The minimum and maximum offset timing numbers are in reference to setting "0" as available in the Quartus II software.
(3) The fast model timing parameter is for commercial devices.

Typical Design Performance

User I/O Pin Timing Parameters

Table 1–48 to Table 1–95 show user I/O pin timing for Cyclone III devices. I/O buffer t_{SU}, t_H and t_{CO} are reported for the cases when clock is driven by global clock and a PLL.

The 12 µA programmable current strength for 1.2 V and 1.2-V HSTL Class I I/O standard is not supported at row I/Os. The 1.2-V HSTL Class II standard is only supported at column I/Os. PCI and PCI-X do not support programmable current strength.

For more information about programmable current strength, refer to the *Cyclone III Device I/O Features* chapter of the *Cyclone III Handbook*.

Dedicated LVDS, mini-LVDS, PPDS, and RSDS I/O standards are supported at row I/Os. External resistor networks are required if the differential standards are used as output pins at column banks. LVDS I/O standard is supported at both input and output pins. PPDS, RSDS, and mini-LVDS standards are only supported at output pins.

For more information about the differential I/O interface, refer to *High-Speed Differential Interfaces in Cyclone III Devices* of the *Cyclone III Handbook*.

EP3C5 I/O Timing Parameters

Table 1–48 through Table 1–53 show the maximum I/O timing parameters for EP3C5 devices.

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	2.969	3.178	3.368	ns
			t_H	–2.689	–2.860	–3.014	ns
2.5V	4 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	8 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	12 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
	16 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.912	3.133	3.336	ns
			t_H	–2.632	–2.816	–2.983	ns
1.8V	2 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	4 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	6 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	8 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	12 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
	16 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.847	3.094	3.323	ns
			t_H	–2.569	–2.778	–2.969	ns
1.5V	2 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	4 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	6 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	8 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	10 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	12 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns
	16 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.916	3.186	3.440	ns
			t_H	–2.636	–2.868	–3.084	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	4 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	6 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	8 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	10 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
	12 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.068	3.366	3.646	ns
			t_H	–2.786	–3.044	–3.286	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns
	12 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.057	1.133	1.188	ns
			t_H	–0.777	–0.816	–0.833	ns
		GCLK PLL	t_{SU}	2.901	3.151	3.385	ns
			t_H	–2.621	–2.834	–3.030	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	10 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	16 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	10 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
	12 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.118	1.222	1.303	ns
			t_H	–0.838	–0.903	–0.946	ns
		GCLK PLL	t_{SU}	2.962	3.240	3.500	ns
			t_H	–2.682	–2.921	–3.143	ns

Table 1–48. EP3C5 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
	10 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
	12 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.074	1.182	1.269	ns
			t_H	–0.794	–0.864	–0.913	ns
		GCLK PLL	t_{SU}	2.918	3.200	3.466	ns
			t_H	–2.638	–2.882	–3.110	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
	10 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
	12 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.206	1.341	1.453	ns
			t_H	–0.924	–1.019	–1.093	ns
		GCLK PLL	t_{SU}	3.050	3.359	3.650	ns
			t_H	–2.768	–3.037	–3.290	ns
3.0-V PCI	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	2.965	3.174	3.363	ns
			t_H	–2.685	–2.856	–3.009	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	2.965	3.174	3.363	ns
			t_H	–2.685	–2.856	–3.009	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	12 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	16 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	8 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
	16 mA	GCLK	t_{SU}	1.148	1.186	1.205	ns
			t_H	–0.868	–0.868	–0.850	ns
		GCLK PLL	t_{SU}	2.997	3.266	3.464	ns
			t_H	–2.717	–2.948	–3.109	ns
2.5V	4 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	8 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	12 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns
	16 mA	GCLK	t_{SU}	1.091	1.142	1.176	ns
			t_H	–0.811	–0.825	–0.822	ns
		GCLK PLL	t_{SU}	2.940	3.222	3.435	ns
			t_H	–2.660	–2.905	–3.081	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	4 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	6 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	8 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	10 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	12 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
	16 mA	GCLK	t_{SU}	1.012	1.088	1.147	ns
			t_H	–0.734	–0.772	–0.792	ns
		GCLK PLL	t_{SU}	2.876	3.183	3.421	ns
			t_H	–2.598	–2.867	–3.066	ns
1.5V	2 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	4 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	6 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	10 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	12 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
	16 mA	GCLK	t_{SU}	1.081	1.181	1.265	ns
			t_H	–0.801	–0.863	–0.909	ns
		GCLK PLL	t_{SU}	2.945	3.276	3.539	ns
			t_H	–2.665	–2.958	–3.183	ns
1.2V	2 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	4 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	6 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	8 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns
	10 mA	GCLK	t_{SU}	1.234	1.361	1.472	ns
			t_H	–0.952	–1.039	–1.111	ns
		GCLK PLL	t_{SU}	3.098	3.456	3.746	ns
			t_H	–2.816	–3.134	–3.385	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
	12 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.081	1.161	1.224	ns
			t_H	–0.801	–0.843	–0.868	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.480	ns
			t_H	–2.650	–2.866	–3.124	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	10 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	16 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	10 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
	12 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.128	1.235	1.326	ns
			t_H	–0.848	–0.916	–0.968	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.597	ns
			t_H	–2.712	–2.954	–3.239	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
	10 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
	12 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.083	1.194	1.289	ns
			t_H	–0.803	–0.876	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.560	ns
			t_H	–2.667	–2.914	–3.203	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.214	1.352	1.474	ns
			t_H	–0.932	–1.030	–1.114	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.745	ns
			t_H	–2.796	–3.068	–3.385	ns
	10 mA	GCLK	t_{SU}	1.214	1.352	1.474	ns
			t_H	–0.932	–1.030	–1.114	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.745	ns
			t_H	–2.796	–3.068	–3.385	ns

Table 1–49. EP3C5 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{SU}	1.144	1.182	1.201	ns
			t_H	–0.864	–0.864	–0.846	ns
	—	GCLK PLL	t_{SU}	2.993	3.262	3.460	ns
			t_H	–2.713	–2.944	–3.105	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.144	1.182	1.201	ns
			t_H	–0.864	–0.864	–0.846	ns
	—	GCLK PLL	t_{SU}	2.993	3.262	3.460	ns
			t_H	–2.713	–2.944	–3.105	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.365	5.861	6.384	ns
		GCLK PLL	t_{CO}	3.516	3.838	4.183	ns
	8 mA	GCLK	t_{CO}	5.365	5.861	6.384	ns
		GCLK PLL	t_{CO}	3.516	3.838	4.183	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.324	5.642	5.986	ns
		GCLK PLL	t_{CO}	3.475	3.619	3.785	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.075	5.564	6.082	ns
		GCLK PLL	t_{CO}	3.226	3.541	3.881	ns
	8 mA	GCLK	t_{CO}	4.804	5.280	5.783	ns
		GCLK PLL	t_{CO}	2.955	3.257	3.582	ns
	12 mA	GCLK	t_{CO}	4.707	5.179	5.679	ns
		GCLK PLL	t_{CO}	2.858	3.156	3.478	ns
	16 mA	GCLK	t_{CO}	4.660	5.127	5.621	ns
		GCLK PLL	t_{CO}	2.811	3.104	3.420	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.802	5.277	5.780	ns
		GCLK PLL	t_{CO}	2.953	3.254	3.579	ns
	8 mA	GCLK	t_{CO}	4.661	5.129	5.625	ns
		GCLK PLL	t_{CO}	2.812	3.106	3.424	ns
	12 mA	GCLK	t_{CO}	4.624	5.089	5.582	ns
		GCLK PLL	t_{CO}	2.775	3.066	3.381	ns
	16 mA	GCLK	t_{CO}	4.608	5.074	5.567	ns
		GCLK PLL	t_{CO}	2.759	3.051	3.366	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{CO}	5.133	5.650	6.196	ns
		GCLK PLL	t_{CO}	3.284	3.627	3.995	ns
	8 mA	GCLK	t_{CO}	4.890	5.397	5.932	ns
		GCLK PLL	t_{CO}	3.041	3.374	3.731	ns
	12 mA	GCLK	t_{CO}	4.792	5.291	5.819	ns
		GCLK PLL	t_{CO}	2.943	3.268	3.618	ns
	16 mA	GCLK	t_{CO}	4.753	5.251	5.778	ns
		GCLK PLL	t_{CO}	2.904	3.228	3.577	ns
1.8V	2 mA	GCLK	t_{CO}	6.244	6.903	7.594	ns
		GCLK PLL	t_{CO}	4.395	4.880	5.393	ns
	4 mA	GCLK	t_{CO}	5.717	6.358	7.030	ns
		GCLK PLL	t_{CO}	3.868	4.335	4.829	ns
	6 mA	GCLK	t_{CO}	5.492	6.100	6.738	ns
		GCLK PLL	t_{CO}	3.643	4.077	4.537	ns
	8 mA	GCLK	t_{CO}	5.389	5.983	6.609	ns
		GCLK PLL	t_{CO}	3.540	3.960	4.408	ns
	10 mA	GCLK	t_{CO}	5.337	5.935	6.563	ns
		GCLK PLL	t_{CO}	3.488	3.912	4.362	ns
	12 mA	GCLK	t_{CO}	5.280	5.868	6.488	ns
		GCLK PLL	t_{CO}	3.431	3.845	4.287	ns
	16 mA	GCLK	t_{CO}	5.226	5.809	6.423	ns
		GCLK PLL	t_{CO}	3.377	3.786	4.222	ns
1.5V	2 mA	GCLK	t_{CO}	6.632	7.465	8.333	ns
		GCLK PLL	t_{CO}	4.783	5.442	6.132	ns
	4 mA	GCLK	t_{CO}	6.157	6.904	7.685	ns
		GCLK PLL	t_{CO}	4.308	4.881	5.484	ns
	6 mA	GCLK	t_{CO}	5.987	6.721	7.488	ns
		GCLK PLL	t_{CO}	4.138	4.698	5.287	ns
	8 mA	GCLK	t_{CO}	5.899	6.608	7.350	ns
		GCLK PLL	t_{CO}	4.050	4.585	5.149	ns
	10 mA	GCLK	t_{CO}	5.840	6.548	7.289	ns
		GCLK PLL	t_{CO}	3.991	4.525	5.088	ns
	12 mA	GCLK	t_{CO}	5.807	6.507	7.239	ns
		GCLK PLL	t_{CO}	3.958	4.484	5.038	ns
	16 mA	GCLK	t_{CO}	5.693	6.365	7.069	ns
		GCLK PLL	t_{CO}	3.844	4.342	4.868	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{CO}	7.805	8.993	10.222	ns
		GCLK PLL	t_{CO}	5.956	6.970	8.021	ns
	4 mA	GCLK	t_{CO}	7.360	8.467	9.615	ns
		GCLK PLL	t_{CO}	5.511	6.444	7.414	ns
	6 mA	GCLK	t_{CO}	7.211	8.286	9.401	ns
		GCLK PLL	t_{CO}	5.362	6.263	7.200	ns
	8 mA	GCLK	t_{CO}	7.142	8.206	9.311	ns
		GCLK PLL	t_{CO}	5.293	6.183	7.110	ns
	10 mA	GCLK	t_{CO}	7.006	8.024	9.080	ns
		GCLK PLL	t_{CO}	5.157	6.001	6.879	ns
	12 mA	GCLK	t_{CO}	6.978	7.998	9.058	ns
		GCLK PLL	t_{CO}	5.129	5.975	6.857	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.752	5.244	5.764	ns
		GCLK PLL	t_{CO}	2.900	3.217	3.559	ns
	12 mA	GCLK	t_{CO}	4.730	5.220	5.741	ns
		GCLK PLL	t_{CO}	2.878	3.193	3.536	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.670	5.158	5.675	ns
		GCLK PLL	t_{CO}	2.818	3.131	3.470	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.186	5.757	6.359	ns
		GCLK PLL	t_{CO}	3.334	3.730	4.154	ns
	10 mA	GCLK	t_{CO}	5.161	5.726	6.322	ns
		GCLK PLL	t_{CO}	3.309	3.699	4.117	ns
	12 mA	GCLK	t_{CO}	5.149	5.712	6.305	ns
		GCLK PLL	t_{CO}	3.297	3.685	4.100	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.120	5.683	6.277	ns
		GCLK PLL	t_{CO}	3.268	3.656	4.072	ns
	16 mA	GCLK	t_{CO}	5.107	5.670	6.263	ns
		GCLK PLL	t_{CO}	3.255	3.643	4.058	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.148	5.709	6.301	ns
		GCLK PLL	t_{CO}	3.296	3.682	4.096	ns
	10 mA	GCLK	t_{CO}	5.137	5.702	6.297	ns
		GCLK PLL	t_{CO}	3.285	3.675	4.092	ns
	12 mA	GCLK	t_{CO}	5.128	5.688	6.277	ns
		GCLK PLL	t_{CO}	3.276	3.661	4.072	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.063	5.622	6.211	ns
		GCLK PLL	t_{CO}	3.211	3.595	4.006	ns

Table 1–50. EP3C5 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.662	6.330	7.032	ns
		GCLK PLL	t_{CO}	3.810	4.303	4.827	ns
	10 mA	GCLK	t_{CO}	5.665	6.330	7.027	ns
		GCLK PLL	t_{CO}	3.813	4.303	4.822	ns
	12 mA	GCLK	t_{CO}	5.653	6.322	7.023	ns
		GCLK PLL	t_{CO}	3.801	4.295	4.818	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.591	6.254	6.948	ns
		GCLK PLL	t_{CO}	3.739	4.227	4.743	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.875	7.868	8.899	ns
		GCLK PLL	t_{CO}	5.023	5.841	6.694	ns
	10 mA	GCLK	t_{CO}	6.813	7.779	8.783	ns
		GCLK PLL	t_{CO}	4.961	5.752	6.578	ns
	12 mA	GCLK	t_{CO}	6.815	7.785	8.792	ns
		GCLK PLL	t_{CO}	4.963	5.758	6.587	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.770	7.732	8.732	ns
		GCLK PLL	t_{CO}	4.918	5.705	6.527	ns
3.0-V PCI	—	GCLK	t_{CO}	4.955	5.421	5.916	ns
		GCLK PLL	t_{CO}	3.106	3.398	3.715	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.955	5.421	5.916	ns
		GCLK PLL	t_{CO}	3.106	3.398	3.715	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.305	5.794	6.309	ns
		GCLK PLL	t_{CO}	3.471	3.786	4.122	ns
	8 mA	GCLK	t_{CO}	5.305	5.794	6.309	ns
		GCLK PLL	t_{CO}	3.471	3.786	4.122	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.305	5.620	5.959	ns
		GCLK PLL	t_{CO}	3.471	3.612	3.772	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.019	5.501	6.010	ns
		GCLK PLL	t_{CO}	3.185	3.493	3.823	ns
	8 mA	GCLK	t_{CO}	4.762	5.234	5.733	ns
		GCLK PLL	t_{CO}	2.928	3.226	3.546	ns
	12 mA	GCLK	t_{CO}	4.673	5.139	5.631	ns
		GCLK PLL	t_{CO}	2.839	3.131	3.444	ns
	16 mA	GCLK	t_{CO}	4.627	5.088	5.576	ns
		GCLK PLL	t_{CO}	2.793	3.080	3.389	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.760	5.232	5.731	ns
		GCLK PLL	t_{CO}	2.926	3.224	3.544	ns
	8 mA	GCLK	t_{CO}	4.627	5.089	5.579	ns
		GCLK PLL	t_{CO}	2.793	3.081	3.392	ns
	12 mA	GCLK	t_{CO}	4.592	5.053	5.540	ns
		GCLK PLL	t_{CO}	2.758	3.045	3.353	ns
	16 mA	GCLK	t_{CO}	4.577	5.037	5.523	ns
		GCLK PLL	t_{CO}	2.743	3.029	3.336	ns
2.5V	4 mA	GCLK	t_{CO}	5.117	5.615	6.140	ns
		GCLK PLL	t_{CO}	3.283	3.607	3.953	ns
	8 mA	GCLK	t_{CO}	4.882	5.371	5.886	ns
		GCLK PLL	t_{CO}	3.048	3.363	3.699	ns
	12 mA	GCLK	t_{CO}	4.783	5.266	5.776	ns
		GCLK PLL	t_{CO}	2.949	3.258	3.589	ns
	16 mA	GCLK	t_{CO}	4.742	5.224	5.733	ns
		GCLK PLL	t_{CO}	2.908	3.216	3.546	ns
1.8V	2 mA	GCLK	t_{CO}	6.226	6.866	7.535	ns
		GCLK PLL	t_{CO}	4.377	4.843	5.333	ns
	4 mA	GCLK	t_{CO}	5.713	6.338	6.991	ns
		GCLK PLL	t_{CO}	3.864	4.315	4.789	ns
	6 mA	GCLK	t_{CO}	5.492	6.084	6.704	ns
		GCLK PLL	t_{CO}	3.643	4.061	4.502	ns
	8 mA	GCLK	t_{CO}	5.391	5.970	6.578	ns
		GCLK PLL	t_{CO}	3.542	3.947	4.376	ns
	10 mA	GCLK	t_{CO}	5.340	5.921	6.532	ns
		GCLK PLL	t_{CO}	3.491	3.898	4.330	ns
	12 mA	GCLK	t_{CO}	5.285	5.858	6.459	ns
		GCLK PLL	t_{CO}	3.436	3.835	4.257	ns
	16 mA	GCLK	t_{CO}	5.242	5.811	6.410	ns
		GCLK PLL	t_{CO}	3.393	3.788	4.208	ns
1.5V	2 mA	GCLK	t_{CO}	6.620	7.433	8.280	ns
		GCLK PLL	t_{CO}	4.771	5.410	6.078	ns
	4 mA	GCLK	t_{CO}	6.164	6.889	7.647	ns
		GCLK PLL	t_{CO}	4.315	4.866	5.445	ns
	6 mA	GCLK	t_{CO}	5.997	6.711	7.456	ns
		GCLK PLL	t_{CO}	4.148	4.688	5.254	ns
	8 mA	GCLK	t_{CO}	5.921	6.618	7.346	ns
		GCLK PLL	t_{CO}	4.072	4.595	5.144	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	10 mA	GCLK	t_{CO}	5.861	6.555	7.280	ns
		GCLK PLL	t_{CO}	4.012	4.532	5.078	ns
	12 mA	GCLK	t_{CO}	5.827	6.512	7.229	ns
		GCLK PLL	t_{CO}	3.978	4.489	5.027	ns
	16 mA	GCLK	t_{CO}	5.730	6.404	7.110	ns
		GCLK PLL	t_{CO}	3.881	4.381	4.908	ns
1.2V	2 mA	GCLK	t_{CO}	7.808	8.973	10.176	ns
		GCLK PLL	t_{CO}	5.959	6.950	7.974	ns
	4 mA	GCLK	t_{CO}	7.373	8.459	9.584	ns
		GCLK PLL	t_{CO}	5.524	6.436	7.382	ns
	6 mA	GCLK	t_{CO}	7.245	8.305	9.405	ns
		GCLK PLL	t_{CO}	5.396	6.282	7.203	ns
	8 mA	GCLK	t_{CO}	7.173	8.223	9.310	ns
		GCLK PLL	t_{CO}	5.324	6.200	7.108	ns
	10 mA	GCLK	t_{CO}	7.042	8.060	9.115	ns
		GCLK PLL	t_{CO}	5.193	6.037	6.913	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.721	5.208	5.724	ns
		GCLK PLL	t_{CO}	2.864	3.178	3.515	ns
	12 mA	GCLK	t_{CO}	4.702	5.189	5.703	ns
		GCLK PLL	t_{CO}	2.845	3.159	3.494	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.647	5.132	5.643	ns
		GCLK PLL	t_{CO}	2.790	3.102	3.434	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.170	5.738	6.334	ns
		GCLK PLL	t_{CO}	3.298	3.693	4.110	ns
	10 mA	GCLK	t_{CO}	5.157	5.720	6.313	ns
		GCLK PLL	t_{CO}	3.285	3.675	4.089	ns
	12 mA	GCLK	t_{CO}	5.144	5.705	6.295	ns
		GCLK PLL	t_{CO}	3.272	3.660	4.071	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.114	5.676	6.267	ns
		GCLK PLL	t_{CO}	3.242	3.631	4.043	ns
	16 mA	GCLK	t_{CO}	5.106	5.670	6.262	ns
		GCLK PLL	t_{CO}	3.234	3.625	4.038	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.134	5.692	6.279	ns
		GCLK PLL	t_{CO}	3.262	3.647	4.055	ns
	10 mA	GCLK	t_{CO}	5.129	5.688	6.276	ns
		GCLK PLL	t_{CO}	3.257	3.643	4.052	ns
	12 mA	GCLK	t_{CO}	5.122	5.681	6.269	ns
		GCLK PLL	t_{CO}	3.250	3.636	4.045	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.060	5.615	6.198	ns
		GCLK PLL	t_{CO}	3.188	3.570	3.974	ns

Table 1–51. EP3C5 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.649	6.313	7.008	ns
		GCLK PLL	t_{CO}	3.777	4.268	4.784	ns
	10 mA	GCLK	t_{CO}	5.661	6.325	7.019	ns
		GCLK PLL	t_{CO}	3.789	4.280	4.795	ns
	12 mA	GCLK	t_{CO}	5.649	6.316	7.014	ns
		GCLK PLL	t_{CO}	3.777	4.271	4.790	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.594	6.259	6.953	ns
		GCLK PLL	t_{CO}	3.722	4.214	4.729	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.886	7.885	8.921	ns
		GCLK PLL	t_{CO}	5.014	5.840	6.697	ns
	10 mA	GCLK	t_{CO}	6.825	7.800	8.812	ns
		GCLK PLL	t_{CO}	4.953	5.755	6.588	ns
3.0-V PCI	—	GCLK	t_{CO}	4.919	5.380	5.866	ns
		GCLK PLL	t_{CO}	3.085	3.372	3.679	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.919	5.380	5.866	ns
		GCLK PLL	t_{CO}	3.085	3.372	3.679	ns

Table 1–52. EP3C5 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.953	1.036	1.096	ns
			t_H	–0.675	–0.720	–0.743	ns
	—	GCLK PLL	t_{SU}	2.798	3.057	3.295	ns
			t_H	–2.520	–2.741	–2.942	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.081	5.569	6.089	ns
		GCLK PLL	t_{CO}	3.248	3.562	3.903	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns

Table 1–53. EP3C5 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	1.035	1.120	1.190	ns
			t_H	–0.757	–0.805	–0.836	ns
			t_{CO}	3.879	4.265	4.675	ns
	—	GCLK PLL	t_{SU}	2.819	3.079	3.329	ns
			t_H	–2.541	–2.764	–2.975	ns
			t_{CO}	2.021	2.233	2.462	ns
mini-LVDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
PPDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
RSDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns

EP3C10 I/O Timing Parameters

Table 1–54 through Table 1–59 show the maximum I/O timing parameters for EP3C10 devices.

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	8 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	12 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns
	16 mA	GCLK	t_{SU}	1.123	1.156	1.167	ns
			t_H	–0.843	–0.838	–0.813	ns
		GCLK PLL	t_{SU}	3.025	3.232	3.391	ns
			t_H	–2.745	–2.914	–3.037	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	8 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	12 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
	16 mA	GCLK	t_{SU}	1.066	1.111	1.135	ns
			t_H	–0.786	–0.794	–0.782	ns
		GCLK PLL	t_{SU}	2.968	3.187	3.359	ns
			t_H	–2.688	–2.870	–3.006	ns
1.8V	2 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	4 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	6 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	8 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	10 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
	12 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.001	1.072	1.122	ns
			t_H	–0.723	–0.756	–0.768	ns
		GCLK PLL	t_{SU}	2.903	3.148	3.346	ns
			t_H	–2.625	–2.832	–2.992	ns
1.5V	2 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	4 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	6 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	8 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	10 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	12 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
	16 mA	GCLK	t_{SU}	1.070	1.164	1.239	ns
			t_H	–0.790	–0.846	–0.883	ns
		GCLK PLL	t_{SU}	2.972	3.240	3.463	ns
			t_H	–2.692	–2.922	–3.107	ns
1.2V	2 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	4 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	8 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	10 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
	12 mA	GCLK	t_{SU}	1.222	1.344	1.445	ns
			t_H	–0.940	–1.022	–1.085	ns
		GCLK PLL	t_{SU}	3.124	3.420	3.669	ns
			t_H	–2.842	–3.098	–3.309	ns
SSTL–2 Class I	8 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
	12 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.055	1.129	1.184	ns
			t_H	–0.775	–0.812	–0.829	ns
		GCLK PLL	t_{SU}	2.954	3.143	3.376	ns
			t_H	–2.674	–2.826	–3.021	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	10 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	16 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	10 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
	12 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.116	1.218	1.299	ns
			t_H	–0.836	–0.899	–0.942	ns
		GCLK PLL	t_{SU}	3.015	3.232	3.491	ns
			t_H	–2.735	–2.913	–3.134	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
	10 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
	12 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.072	1.178	1.265	ns
			t_H	–0.792	–0.860	–0.909	ns
		GCLK PLL	t_{SU}	2.971	3.192	3.457	ns
			t_H	–2.691	–2.874	–3.101	ns

Table 1–54. EP3C10 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
	10 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
	12 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.204	1.337	1.449	ns
			t_H	–0.922	–1.015	–1.089	ns
		GCLK PLL	t_{SU}	3.103	3.351	3.641	ns
			t_H	–2.821	–3.029	–3.281	ns
3.0-V PCI	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	3.021	3.228	3.386	ns
			t_H	–2.741	–2.910	–3.032	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.119	1.152	1.162	ns
			t_H	–0.839	–0.834	–0.808	ns
	—	GCLK PLL	t_{SU}	3.021	3.228	3.386	ns
			t_H	–2.741	–2.910	–3.032	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			th	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	12 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	16 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	8 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	12 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns
	16 mA	GCLK	t_{SU}	1.155	1.193	1.213	ns
			t_H	–0.875	–0.875	–0.858	ns
		GCLK PLL	t_{SU}	2.999	3.213	3.411	ns
			t_H	–2.719	–2.895	–3.056	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	8 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	12 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
	16 mA	GCLK	t_{SU}	1.098	1.149	1.184	ns
			t_H	–0.818	–0.832	–0.830	ns
		GCLK PLL	t_{SU}	2.942	3.169	3.382	ns
			t_H	–2.662	–2.852	–3.028	ns
1.8V	2 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	4 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	6 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	8 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	10 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
	12 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.034	1.110	1.170	ns
			t_H	–0.756	–0.794	–0.815	ns
		GCLK PLL	t_{SU}	2.878	3.130	3.368	ns
			t_H	–2.600	–2.814	–3.013	ns
1.5V	2 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	4 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	tsu	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	6 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	8 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	10 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	12 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns
	16 mA	GCLK	t_{SU}	1.103	1.203	1.288	ns
			t_H	–0.823	–0.885	–0.932	ns
		GCLK PLL	t_{SU}	2.947	3.223	3.486	ns
			t_H	–2.667	–2.905	–3.130	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	4 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	6 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	8 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
	10 mA	GCLK	t_{SU}	1.256	1.383	1.495	ns
			t_H	–0.974	–1.061	–1.134	ns
		GCLK PLL	t_{SU}	3.100	3.403	3.693	ns
			t_H	–2.818	–3.081	–3.332	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns
	12 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.082	1.162	1.225	ns
			t_H	–0.802	–0.844	–0.869	ns
		GCLK PLL	t_{SU}	2.930	3.184	3.428	ns
			t_H	–2.650	–2.866	–3.072	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	10 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	16 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	10 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
	12 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.129	1.236	1.327	ns
			t_H	–0.849	–0.917	–0.969	ns
		GCLK PLL	t_{SU}	2.992	3.273	3.545	ns
			t_H	–2.712	–2.954	–3.187	ns

Table 1–55. EP3C10 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
	10 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
	12 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.084	1.195	1.290	ns
			t_H	–0.804	–0.877	–0.933	ns
		GCLK PLL	t_{SU}	2.947	3.232	3.508	ns
			t_H	–2.667	–2.914	–3.151	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.215	1.353	1.475	ns
			t_H	–0.933	–1.031	–1.115	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.693	ns
			t_H	–2.796	–3.068	–3.333	ns
	10 mA	GCLK	t_{SU}	1.215	1.353	1.475	ns
			t_H	–0.933	–1.031	–1.115	ns
		GCLK PLL	t_{SU}	3.078	3.390	3.693	ns
			t_H	–2.796	–3.068	–3.333	ns
3.0-V PCI	—	GCLK	t_{SU}	1.151	1.189	1.209	ns
			t_H	–0.871	–0.871	–0.854	ns
	—	GCLK PLL	t_{SU}	2.995	3.209	3.407	ns
			t_H	–2.715	–2.891	–3.052	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.151	1.189	1.209	ns
			t_H	–0.871	–0.871	–0.854	ns
	—	GCLK PLL	t_{SU}	2.995	3.209	3.407	ns
			t_H	–2.715	–2.891	–3.052	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.371	5.866	6.382	ns
		GCLK PLL	t_{CO}	3.512	3.831	4.181	ns
	8 mA	GCLK	t_{CO}	5.371	5.866	6.382	ns
		GCLK PLL	t_{CO}	3.512	3.831	4.181	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.330	5.647	5.984	ns
		GCLK PLL	t_{CO}	3.471	3.612	3.783	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.081	5.569	6.080	ns
		GCLK PLL	t_{CO}	3.222	3.534	3.879	ns
	8 mA	GCLK	t_{CO}	4.810	5.285	5.781	ns
		GCLK PLL	t_{CO}	2.951	3.250	3.580	ns
	12 mA	GCLK	t_{CO}	4.713	5.184	5.677	ns
		GCLK PLL	t_{CO}	2.854	3.149	3.476	ns
	16 mA	GCLK	t_{CO}	4.666	5.132	5.619	ns
		GCLK PLL	t_{CO}	2.807	3.097	3.418	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.808	5.282	5.778	ns
		GCLK PLL	t_{CO}	2.949	3.247	3.577	ns
	8 mA	GCLK	t_{CO}	4.667	5.134	5.623	ns
		GCLK PLL	t_{CO}	2.808	3.099	3.422	ns
	12 mA	GCLK	t_{CO}	4.630	5.094	5.580	ns
		GCLK PLL	t_{CO}	2.771	3.059	3.379	ns
	16 mA	GCLK	t_{CO}	4.614	5.079	5.565	ns
		GCLK PLL	t_{CO}	2.755	3.044	3.364	ns
2.5V	4 mA	GCLK	t_{CO}	5.139	5.655	6.194	ns
		GCLK PLL	t_{CO}	3.280	3.620	3.993	ns
	8 mA	GCLK	t_{CO}	4.896	5.402	5.930	ns
		GCLK PLL	t_{CO}	3.037	3.367	3.729	ns
	12 mA	GCLK	t_{CO}	4.798	5.296	5.817	ns
		GCLK PLL	t_{CO}	2.939	3.261	3.616	ns
	16 mA	GCLK	t_{CO}	4.759	5.256	5.776	ns
		GCLK PLL	t_{CO}	2.900	3.221	3.575	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.250	6.908	7.592	ns
		GCLK PLL	t_{CO}	4.391	4.873	5.391	ns
	4 mA	GCLK	t_{CO}	5.723	6.363	7.028	ns
		GCLK PLL	t_{CO}	3.864	4.328	4.827	ns
	6 mA	GCLK	t_{CO}	5.498	6.105	6.736	ns
		GCLK PLL	t_{CO}	3.639	4.070	4.535	ns
	8 mA	GCLK	t_{CO}	5.395	5.988	6.607	ns
		GCLK PLL	t_{CO}	3.536	3.953	4.406	ns
	10 mA	GCLK	t_{CO}	5.343	5.940	6.561	ns
		GCLK PLL	t_{CO}	3.484	3.905	4.360	ns
	12 mA	GCLK	t_{CO}	5.286	5.873	6.486	ns
		GCLK PLL	t_{CO}	3.427	3.838	4.285	ns
	16 mA	GCLK	t_{CO}	5.232	5.814	6.421	ns
		GCLK PLL	t_{CO}	3.373	3.779	4.220	ns
1.5V	2 mA	GCLK	t_{CO}	6.638	7.470	8.331	ns
		GCLK PLL	t_{CO}	4.779	5.435	6.130	ns
	4 mA	GCLK	t_{CO}	6.163	6.909	7.683	ns
		GCLK PLL	t_{CO}	4.304	4.874	5.482	ns
	6 mA	GCLK	t_{CO}	5.993	6.726	7.486	ns
		GCLK PLL	t_{CO}	4.134	4.691	5.285	ns
	8 mA	GCLK	t_{CO}	5.905	6.613	7.348	ns
		GCLK PLL	t_{CO}	4.046	4.578	5.147	ns
	10 mA	GCLK	t_{CO}	5.846	6.553	7.287	ns
		GCLK PLL	t_{CO}	3.987	4.518	5.086	ns
	12 mA	GCLK	t_{CO}	5.813	6.512	7.237	ns
		GCLK PLL	t_{CO}	3.954	4.477	5.036	ns
	16 mA	GCLK	t_{CO}	5.699	6.370	7.067	ns
		GCLK PLL	t_{CO}	3.840	4.335	4.866	ns
1.2V	2 mA	GCLK	t_{CO}	7.811	8.998	10.220	ns
		GCLK PLL	t_{CO}	5.952	6.963	8.019	ns
	4 mA	GCLK	t_{CO}	7.366	8.472	9.613	ns
		GCLK PLL	t_{CO}	5.507	6.437	7.412	ns
	6 mA	GCLK	t_{CO}	7.217	8.291	9.399	ns
		GCLK PLL	t_{CO}	5.358	6.256	7.198	ns
	8 mA	GCLK	t_{CO}	7.148	8.211	9.309	ns
		GCLK PLL	t_{CO}	5.289	6.176	7.108	ns
	10 mA	GCLK	t_{CO}	7.012	8.029	9.078	ns
		GCLK PLL	t_{CO}	5.153	5.994	6.877	ns
	12 mA	GCLK	t_{CO}	6.984	8.003	9.056	ns
		GCLK PLL	t_{CO}	5.125	5.968	6.855	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.754	5.240	5.750	ns
		GCLK PLL	t_{CO}	2.901	3.228	3.570	ns
	12 mA	GCLK	t_{CO}	4.732	5.216	5.727	ns
		GCLK PLL	t_{CO}	2.879	3.204	3.547	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.672	5.154	5.661	ns
		GCLK PLL	t_{CO}	2.819	3.142	3.481	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.188	5.753	6.345	ns
		GCLK PLL	t_{CO}	3.335	3.741	4.165	ns
	10 mA	GCLK	t_{CO}	5.163	5.722	6.308	ns
		GCLK PLL	t_{CO}	3.310	3.710	4.128	ns
	12 mA	GCLK	t_{CO}	5.151	5.708	6.291	ns
		GCLK PLL	t_{CO}	3.298	3.696	4.111	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.122	5.679	6.263	ns
		GCLK PLL	t_{CO}	3.269	3.667	4.083	ns
	16 mA	GCLK	t_{CO}	5.109	5.666	6.249	ns
		GCLK PLL	t_{CO}	3.256	3.654	4.069	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.150	5.705	6.287	ns
		GCLK PLL	t_{CO}	3.297	3.693	4.107	ns
	10 mA	GCLK	t_{CO}	5.139	5.698	6.283	ns
		GCLK PLL	t_{CO}	3.286	3.686	4.103	ns
	12 mA	GCLK	t_{CO}	5.130	5.684	6.263	ns
		GCLK PLL	t_{CO}	3.277	3.672	4.083	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.065	5.618	6.197	ns
		GCLK PLL	t_{CO}	3.212	3.606	4.017	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.664	6.326	7.018	ns
		GCLK PLL	t_{CO}	3.811	4.314	4.838	ns
	10 mA	GCLK	t_{CO}	5.667	6.326	7.013	ns
		GCLK PLL	t_{CO}	3.814	4.314	4.833	ns
	12 mA	GCLK	t_{CO}	5.655	6.318	7.009	ns
		GCLK PLL	t_{CO}	3.802	4.306	4.829	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.593	6.250	6.934	ns
		GCLK PLL	t_{CO}	3.740	4.238	4.754	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.877	7.864	8.885	ns
		GCLK PLL	t_{CO}	5.024	5.852	6.705	ns
	10 mA	GCLK	t_{CO}	6.815	7.775	8.769	ns
		GCLK PLL	t_{CO}	4.962	5.763	6.589	ns
	12 mA	GCLK	t_{CO}	6.817	7.781	8.778	ns
		GCLK PLL	t_{CO}	4.964	5.769	6.598	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.772	7.728	8.718	ns
		GCLK PLL	t_{CO}	4.919	5.716	6.538	ns

Table 1–56. EP3C10 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{CO}	4.961	5.426	5.914	ns
		GCLK PLL	t_{CO}	3.102	3.391	3.713	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.961	5.426	5.914	ns
		GCLK PLL	t_{CO}	3.102	3.391	3.713	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.308	5.797	6.311	ns
		GCLK PLL	t_{CO}	3.467	3.783	4.118	ns
	8 mA	GCLK	t_{CO}	5.308	5.797	6.311	ns
		GCLK PLL	t_{CO}	3.467	3.783	4.118	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.308	5.623	5.961	ns
		GCLK PLL	t_{CO}	3.467	3.609	3.768	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.022	5.504	6.012	ns
		GCLK PLL	t_{CO}	3.181	3.490	3.819	ns
	8 mA	GCLK	t_{CO}	4.765	5.237	5.735	ns
		GCLK PLL	t_{CO}	2.924	3.223	3.542	ns
	12 mA	GCLK	t_{CO}	4.676	5.142	5.633	ns
		GCLK PLL	t_{CO}	2.835	3.128	3.440	ns
	16 mA	GCLK	t_{CO}	4.630	5.091	5.578	ns
		GCLK PLL	t_{CO}	2.789	3.077	3.385	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.763	5.235	5.733	ns
		GCLK PLL	t_{CO}	2.922	3.221	3.540	ns
	8 mA	GCLK	t_{CO}	4.630	5.092	5.581	ns
		GCLK PLL	t_{CO}	2.789	3.078	3.388	ns
	12 mA	GCLK	t_{CO}	4.595	5.056	5.542	ns
		GCLK PLL	t_{CO}	2.754	3.042	3.349	ns
	16 mA	GCLK	t_{CO}	4.580	5.040	5.525	ns
		GCLK PLL	t_{CO}	2.739	3.026	3.332	ns
2.5V	4 mA	GCLK	t_{CO}	5.120	5.618	6.142	ns
		GCLK PLL	t_{CO}	3.279	3.604	3.949	ns
	8 mA	GCLK	t_{CO}	4.885	5.374	5.888	ns
		GCLK PLL	t_{CO}	3.044	3.360	3.695	ns
	12 mA	GCLK	t_{CO}	4.786	5.269	5.778	ns
		GCLK PLL	t_{CO}	2.945	3.255	3.585	ns
	16 mA	GCLK	t_{CO}	4.745	5.227	5.735	ns
		GCLK PLL	t_{CO}	2.904	3.213	3.542	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.214	6.854	7.522	ns
		GCLK PLL	t_{CO}	4.373	4.840	5.329	ns
	4 mA	GCLK	t_{CO}	5.701	6.326	6.978	ns
		GCLK PLL	t_{CO}	3.860	4.312	4.785	ns
	6 mA	GCLK	t_{CO}	5.480	6.072	6.691	ns
		GCLK PLL	t_{CO}	3.639	4.058	4.498	ns
	8 mA	GCLK	t_{CO}	5.379	5.958	6.565	ns
		GCLK PLL	t_{CO}	3.538	3.944	4.372	ns
	10 mA	GCLK	t_{CO}	5.328	5.909	6.519	ns
		GCLK PLL	t_{CO}	3.487	3.895	4.326	ns
	12 mA	GCLK	t_{CO}	5.273	5.846	6.446	ns
		GCLK PLL	t_{CO}	3.432	3.832	4.253	ns
	16 mA	GCLK	t_{CO}	5.230	5.799	6.397	ns
		GCLK PLL	t_{CO}	3.389	3.785	4.204	ns
1.5V	2 mA	GCLK	t_{CO}	6.608	7.421	8.267	ns
		GCLK PLL	t_{CO}	4.767	5.407	6.074	ns
	4 mA	GCLK	t_{CO}	6.152	6.877	7.634	ns
		GCLK PLL	t_{CO}	4.311	4.863	5.441	ns
	6 mA	GCLK	t_{CO}	5.985	6.699	7.443	ns
		GCLK PLL	t_{CO}	4.144	4.685	5.250	ns
	8 mA	GCLK	t_{CO}	5.909	6.606	7.333	ns
		GCLK PLL	t_{CO}	4.068	4.592	5.140	ns
	10 mA	GCLK	t_{CO}	5.849	6.543	7.267	ns
		GCLK PLL	t_{CO}	4.008	4.529	5.074	ns
	12 mA	GCLK	t_{CO}	5.815	6.500	7.216	ns
		GCLK PLL	t_{CO}	3.974	4.486	5.023	ns
	16 mA	GCLK	t_{CO}	5.718	6.392	7.097	ns
		GCLK PLL	t_{CO}	3.877	4.378	4.904	ns
1.2V	2 mA	GCLK	t_{CO}	7.796	8.961	10.163	ns
		GCLK PLL	t_{CO}	5.955	6.947	7.970	ns
	4 mA	GCLK	t_{CO}	7.361	8.447	9.571	ns
		GCLK PLL	t_{CO}	5.520	6.433	7.378	ns
	6 mA	GCLK	t_{CO}	7.233	8.293	9.392	ns
		GCLK PLL	t_{CO}	5.392	6.279	7.199	ns
	8 mA	GCLK	t_{CO}	7.161	8.211	9.297	ns
		GCLK PLL	t_{CO}	5.320	6.197	7.104	ns
	10 mA	GCLK	t_{CO}	7.030	8.048	9.102	ns
		GCLK PLL	t_{CO}	5.189	6.034	6.909	ns

Table 1–57. EP3C10 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.720	5.207	5.723	ns
		GCLK PLL	t_{CO}	2.865	3.176	3.513	ns
	12 mA	GCLK	t_{CO}	4.701	5.188	5.702	ns
		GCLK PLL	t_{CO}	2.846	3.157	3.492	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.646	5.131	5.642	ns
		GCLK PLL	t_{CO}	2.791	3.100	3.432	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.169	5.737	6.333	ns
		GCLK PLL	t_{CO}	3.299	3.691	4.108	ns
	10 mA	GCLK	t_{CO}	5.156	5.719	6.312	ns
		GCLK PLL	t_{CO}	3.286	3.673	4.087	ns
	12 mA	GCLK	t_{CO}	5.143	5.704	6.294	ns
		GCLK PLL	t_{CO}	3.273	3.658	4.069	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.113	5.675	6.266	ns
		GCLK PLL	t_{CO}	3.243	3.629	4.041	ns
	16 mA	GCLK	t_{CO}	5.105	5.669	6.261	ns
		GCLK PLL	t_{CO}	3.235	3.623	4.036	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.133	5.691	6.278	ns
		GCLK PLL	t_{CO}	3.263	3.645	4.053	ns
	10 mA	GCLK	t_{CO}	5.128	5.687	6.275	ns
		GCLK PLL	t_{CO}	3.258	3.641	4.050	ns
	12 mA	GCLK	t_{CO}	5.121	5.680	6.268	ns
		GCLK PLL	t_{CO}	3.251	3.634	4.043	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.059	5.614	6.197	ns
		GCLK PLL	t_{CO}	3.189	3.568	3.972	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.648	6.312	7.007	ns
		GCLK PLL	t_{CO}	3.778	4.266	4.782	ns
	10 mA	GCLK	t_{CO}	5.660	6.324	7.018	ns
		GCLK PLL	t_{CO}	3.790	4.278	4.793	ns
	12 mA	GCLK	t_{CO}	5.648	6.315	7.013	ns
		GCLK PLL	t_{CO}	3.778	4.269	4.788	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.593	6.258	6.952	ns
		GCLK PLL	t_{CO}	3.723	4.212	4.727	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.885	7.884	8.920	ns
		GCLK PLL	t_{CO}	5.015	5.838	6.695	ns
	10 mA	GCLK	t_{CO}	6.824	7.799	8.811	ns
		GCLK PLL	t_{CO}	4.954	5.753	6.586	ns
3.0-V PCI	—	GCLK	t_{CO}	4.922	5.383	5.868	ns
		GCLK PLL	t_{CO}	3.081	3.369	3.675	ns
3.0-V PCI-X	—	GCLK	t_{CO}	4.922	5.383	5.868	ns
		GCLK PLL	t_{CO}	3.081	3.369	3.675	ns

Table 1–58. EP3C10 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.953	1.036	1.096	ns
			t_H	–0.675	–0.720	–0.743	ns
	—	GCLK PLL	t_{SU}	2.798	3.057	3.295	ns
			t_H	–2.520	–2.741	–2.942	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.081	5.569	6.089	ns
		GCLK PLL	t_{CO}	3.248	3.562	3.903	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.700	5.190	5.711	ns
		GCLK PLL	t_{CO}	2.867	3.183	3.525	ns

Table 1–59. EP3C10 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	1.035	1.120	1.190	ns
			t_H	–0.757	–0.805	–0.836	ns
			t_{CO}	3.879	4.265	4.675	ns
	—	GCLK PLL	t_{SU}	2.819	3.079	3.329	ns
			t_H	–2.541	–2.764	–2.975	ns
			t_{CO}	2.021	2.233	2.462	ns
mini-LVDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
PPDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns
RSDS	—	GCLK	t_{CO}	3.879	4.265	4.675	ns
		GCLK PLL	t_{CO}	2.021	2.233	2.462	ns

EP3C16 I/O Timing Parameters

Table 1–60 through Table 1–71 show the maximum I/O timing parameters for EP3C16 devices.

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	12 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	16 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	8 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	12 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
	16 mA	GCLK	t_{SU}	1.100	1.126	1.135	ns
			t_H	–0.820	–0.808	–0.781	ns
		GCLK PLL	t_{SU}	2.753	2.937	3.106	ns
			t_H	–2.473	–2.619	–2.752	ns
2.5V	4 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	8 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	12 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns
	16 mA	GCLK	t_{SU}	1.043	1.081	1.103	ns
			t_H	–0.763	–0.764	–0.750	ns
		GCLK PLL	t_{SU}	2.696	2.892	3.074	ns
			t_H	–2.416	–2.575	–2.721	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	4 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	6 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	8 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	10 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	12 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
	16 mA	GCLK	t_{SU}	0.978	1.042	1.090	ns
			t_H	–0.700	–0.726	–0.736	ns
		GCLK PLL	t_{SU}	2.630	2.852	3.061	ns
			t_H	–2.352	–2.536	–2.707	ns
1.5V	2 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	4 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	6 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	10 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	12 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
	16 mA	GCLK	t_{SU}	1.047	1.134	1.207	ns
			t_H	–0.767	–0.816	–0.851	ns
		GCLK PLL	t_{SU}	2.699	2.944	3.178	ns
			t_H	–2.419	–2.626	–2.822	ns
1.2V	2 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	4 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	6 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	8 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	10 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns
	12 mA	GCLK	t_{SU}	1.199	1.314	1.413	ns
			t_H	–0.917	–0.992	–1.053	ns
		GCLK PLL	t_{SU}	2.851	3.124	3.384	ns
			t_H	–2.569	–2.802	–3.024	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
	12 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.032	1.100	1.152	ns
			t_H	–0.752	–0.783	–0.797	ns
		GCLK PLL	t_{SU}	2.685	2.909	3.123	ns
			t_H	–2.405	–2.592	–2.768	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	10 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	16 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	10 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
	12 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.093	1.189	1.267	ns
			t_H	–0.813	–0.870	–0.910	ns
		GCLK PLL	t_{SU}	2.745	2.998	3.238	ns
			t_H	–2.465	–2.679	–2.881	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
	10 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
	12 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.049	1.149	1.233	ns
			t_H	–0.769	–0.831	–0.877	ns
		GCLK PLL	t_{SU}	2.701	2.958	3.204	ns
			t_H	–2.421	–2.640	–2.848	ns

Table 1–60. EP3C16 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
	10 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
	12 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
1.2–V HSTL Class II	14 mA	GCLK	t_{SU}	1.181	1.308	1.417	ns
			t_H	–0.899	–0.986	–1.057	ns
		GCLK PLL	t_{SU}	2.833	3.117	3.388	ns
			t_H	–2.551	–2.795	–3.028	ns
3.0-V PCI	—	GCLK	t_{SU}	1.096	1.122	1.130	ns
			t_H	–0.816	–0.804	–0.776	ns
	—	GCLK PLL	t_{SU}	2.749	2.933	3.101	ns
			t_H	–2.469	–2.615	–2.747	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.096	1.122	1.130	ns
			t_H	–0.816	–0.804	–0.776	ns
	—	GCLK PLL	t_{SU}	2.749	2.933	3.101	ns
			t_H	–2.469	–2.615	–2.747	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	12 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	16 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	8 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	12 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns
	16 mA	GCLK	t_{SU}	1.141	1.173	1.187	ns
			t_H	–0.861	–0.855	–0.832	ns
		GCLK PLL	t_{SU}	2.796	2.986	3.164	ns
			t_H	–2.516	–2.668	–2.809	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	8 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	12 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
	16 mA	GCLK	t_{SU}	1.084	1.129	1.158	ns
			t_H	–0.804	–0.812	–0.804	ns
		GCLK PLL	t_{SU}	2.739	2.942	3.135	ns
			t_H	–2.459	–2.625	–2.781	ns
1.8V	2 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	4 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	6 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	8 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	10 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
	12 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	1.020	1.090	1.144	ns
			t_H	–0.742	–0.774	–0.789	ns
		GCLK PLL	t_{SU}	2.675	2.903	3.121	ns
			t_H	–2.397	–2.587	–2.766	ns
1.5V	2 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	4 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	6 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	8 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	10 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	12 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
	16 mA	GCLK	t_{SU}	1.089	1.183	1.262	ns
			t_H	–0.809	–0.865	–0.906	ns
		GCLK PLL	t_{SU}	2.744	2.996	3.239	ns
			t_H	–2.464	–2.678	–2.883	ns
1.2V	2 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	4 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	8 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
	10 mA	GCLK	t_{SU}	1.242	1.363	1.469	ns
			t_H	–0.960	–1.041	–1.108	ns
		GCLK PLL	t_{SU}	2.897	3.176	3.446	ns
			t_H	–2.615	–2.854	–3.085	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
	12 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.074	1.148	1.209	ns
			t_H	–0.794	–0.830	–0.853	ns
		GCLK PLL	t_{SU}	2.729	2.952	3.174	ns
			t_H	–2.449	–2.634	–2.818	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	10 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	16 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	10 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
	12 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.136	1.237	1.326	ns
			t_H	–0.856	–0.918	–0.968	ns
		GCLK PLL	t_{SU}	2.791	3.041	3.291	ns
			t_H	–2.511	–2.722	–2.933	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
	10 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
	12 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.091	1.196	1.289	ns
			t_H	–0.811	–0.878	–0.932	ns
		GCLK PLL	t_{SU}	2.746	3.000	3.254	ns
			t_H	–2.466	–2.682	–2.897	ns

Table 1–61. EP3C16 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.222	1.354	1.474	ns
			t_H	–0.940	–1.032	–1.114	ns
		GCLK PLL	t_{SU}	2.877	3.158	3.439	ns
			t_H	–2.595	–2.836	–3.079	ns
1.2-V HSTL Class I	10 mA	GCLK	t_{SU}	1.222	1.354	1.474	ns
			t_H	–0.940	–1.032	–1.114	ns
		GCLK PLL	t_{SU}	2.877	3.158	3.439	ns
			t_H	–2.595	–2.836	–3.079	ns
3.0-V PCI	—	GCLK	t_{SU}	1.137	1.169	1.183	ns
			t_H	–0.857	–0.851	–0.828	ns
	—	GCLK PLL	t_{SU}	2.792	2.982	3.160	ns
			t_H	–2.512	–2.664	–2.805	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.137	1.169	1.183	ns
			t_H	–0.857	–0.851	–0.828	ns
	—	GCLK PLL	t_{SU}	2.792	2.982	3.160	ns
			t_H	–2.512	–2.664	–2.805	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.480	5.983	6.509	ns
		GCLK PLL	t_{CO}	3.827	4.173	4.537	ns
	8 mA	GCLK	t_{CO}	5.480	5.983	6.509	ns
		GCLK PLL	t_{CO}	3.827	4.173	4.537	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.439	5.764	6.111	ns
		GCLK PLL	t_{CO}	3.786	3.954	4.139	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.190	5.686	6.207	ns
		GCLK PLL	t_{CO}	3.537	3.876	4.235	ns
	8 mA	GCLK	t_{CO}	4.919	5.402	5.908	ns
		GCLK PLL	t_{CO}	3.266	3.592	3.936	ns
	12 mA	GCLK	t_{CO}	4.822	5.301	5.804	ns
		GCLK PLL	t_{CO}	3.169	3.491	3.832	ns
	16 mA	GCLK	t_{CO}	4.775	5.249	5.746	ns
		GCLK PLL	t_{CO}	3.122	3.439	3.774	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.917	5.399	5.905	ns
		GCLK PLL	t_{CO}	3.264	3.589	3.933	ns
	8 mA	GCLK	t_{CO}	4.776	5.251	5.750	ns
		GCLK PLL	t_{CO}	3.123	3.441	3.778	ns
	12 mA	GCLK	t_{CO}	4.739	5.211	5.707	ns
		GCLK PLL	t_{CO}	3.086	3.401	3.735	ns
	16 mA	GCLK	t_{CO}	4.723	5.196	5.692	ns
		GCLK PLL	t_{CO}	3.070	3.386	3.720	ns
2.5V	4 mA	GCLK	t_{CO}	5.248	5.772	6.321	ns
		GCLK PLL	t_{CO}	3.595	3.962	4.349	ns
	8 mA	GCLK	t_{CO}	5.005	5.519	6.057	ns
		GCLK PLL	t_{CO}	3.352	3.709	4.085	ns
	12 mA	GCLK	t_{CO}	4.907	5.413	5.944	ns
		GCLK PLL	t_{CO}	3.254	3.603	3.972	ns
	16 mA	GCLK	t_{CO}	4.868	5.373	5.903	ns
		GCLK PLL	t_{CO}	3.215	3.563	3.931	ns
1.8V	2 mA	GCLK	t_{CO}	6.359	7.025	7.719	ns
		GCLK PLL	t_{CO}	4.707	5.215	5.747	ns
	4 mA	GCLK	t_{CO}	5.832	6.480	7.155	ns
		GCLK PLL	t_{CO}	4.180	4.670	5.183	ns
	6 mA	GCLK	t_{CO}	5.607	6.222	6.863	ns
		GCLK PLL	t_{CO}	3.955	4.412	4.891	ns
	8 mA	GCLK	t_{CO}	5.504	6.105	6.734	ns
		GCLK PLL	t_{CO}	3.852	4.295	4.762	ns
	10 mA	GCLK	t_{CO}	5.452	6.057	6.688	ns
		GCLK PLL	t_{CO}	3.800	4.247	4.716	ns
	12 mA	GCLK	t_{CO}	5.395	5.990	6.613	ns
		GCLK PLL	t_{CO}	3.743	4.180	4.641	ns
	16 mA	GCLK	t_{CO}	5.341	5.931	6.548	ns
		GCLK PLL	t_{CO}	3.689	4.121	4.576	ns
1.5V	2 mA	GCLK	t_{CO}	6.747	7.587	8.458	ns
		GCLK PLL	t_{CO}	5.095	5.777	6.486	ns
	4 mA	GCLK	t_{CO}	6.272	7.026	7.810	ns
		GCLK PLL	t_{CO}	4.620	5.216	5.838	ns
	6 mA	GCLK	t_{CO}	6.102	6.843	7.613	ns
		GCLK PLL	t_{CO}	4.450	5.033	5.641	ns
	8 mA	GCLK	t_{CO}	6.014	6.730	7.475	ns
		GCLK PLL	t_{CO}	4.362	4.920	5.503	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	10 mA	GCLK	t_{CO}	5.955	6.670	7.414	ns
		GCLK PLL	t_{CO}	4.303	4.860	5.442	ns
	12 mA	GCLK	t_{CO}	5.922	6.629	7.364	ns
		GCLK PLL	t_{CO}	4.270	4.819	5.392	ns
	16 mA	GCLK	t_{CO}	5.808	6.487	7.194	ns
		GCLK PLL	t_{CO}	4.156	4.677	5.222	ns
1.2V	2 mA	GCLK	t_{CO}	7.920	9.115	10.347	ns
		GCLK PLL	t_{CO}	6.268	7.305	8.375	ns
	4 mA	GCLK	t_{CO}	7.475	8.589	9.740	ns
		GCLK PLL	t_{CO}	5.823	6.779	7.768	ns
	6 mA	GCLK	t_{CO}	7.326	8.408	9.526	ns
		GCLK PLL	t_{CO}	5.674	6.598	7.554	ns
	8 mA	GCLK	t_{CO}	7.257	8.328	9.436	ns
		GCLK PLL	t_{CO}	5.605	6.518	7.464	ns
	10 mA	GCLK	t_{CO}	7.121	8.146	9.205	ns
		GCLK PLL	t_{CO}	5.469	6.336	7.233	ns
	12 mA	GCLK	t_{CO}	7.093	8.120	9.183	ns
		GCLK PLL	t_{CO}	5.441	6.310	7.211	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.863	5.361	5.885	ns
		GCLK PLL	t_{CO}	3.210	3.552	3.913	ns
	12 mA	GCLK	t_{CO}	4.841	5.337	5.862	ns
		GCLK PLL	t_{CO}	3.188	3.528	3.890	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.781	5.275	5.796	ns
		GCLK PLL	t_{CO}	3.128	3.466	3.824	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.297	5.874	6.480	ns
		GCLK PLL	t_{CO}	3.645	4.065	4.508	ns
	10 mA	GCLK	t_{CO}	5.272	5.843	6.443	ns
		GCLK PLL	t_{CO}	3.620	4.034	4.471	ns
	12 mA	GCLK	t_{CO}	5.260	5.829	6.426	ns
		GCLK PLL	t_{CO}	3.608	4.020	4.454	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.231	5.800	6.398	ns
		GCLK PLL	t_{CO}	3.579	3.991	4.426	ns
	16 mA	GCLK	t_{CO}	5.218	5.787	6.384	ns
		GCLK PLL	t_{CO}	3.566	3.978	4.412	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.259	5.826	6.422	ns
		GCLK PLL	t_{CO}	3.607	4.017	4.450	ns
	10 mA	GCLK	t_{CO}	5.248	5.819	6.418	ns
		GCLK PLL	t_{CO}	3.596	4.010	4.446	ns
	12 mA	GCLK	t_{CO}	5.239	5.805	6.398	ns
		GCLK PLL	t_{CO}	3.587	3.996	4.426	ns

Table 1–62. EP3C16 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.174	5.739	6.332	ns
		GCLK PLL	t_{CO}	3.522	3.930	4.360	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.773	6.447	7.153	ns
		GCLK PLL	t_{CO}	4.121	4.638	5.181	ns
	10 mA	GCLK	t_{CO}	5.776	6.447	7.148	ns
		GCLK PLL	t_{CO}	4.124	4.638	5.176	ns
	12 mA	GCLK	t_{CO}	5.764	6.439	7.144	ns
		GCLK PLL	t_{CO}	4.112	4.630	5.172	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.702	6.371	7.069	ns
		GCLK PLL	t_{CO}	4.050	4.562	5.097	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.986	7.985	9.020	ns
		GCLK PLL	t_{CO}	5.334	6.176	7.048	ns
	10 mA	GCLK	t_{CO}	6.924	7.896	8.904	ns
		GCLK PLL	t_{CO}	5.272	6.087	6.932	ns
	12 mA	GCLK	t_{CO}	6.926	7.902	8.913	ns
		GCLK PLL	t_{CO}	5.274	6.093	6.941	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.881	7.849	8.853	ns
		GCLK PLL	t_{CO}	5.229	6.040	6.881	ns
3.0-V PCI	—	GCLK	t_{CO}	5.070	5.543	6.041	ns
		GCLK PLL	t_{CO}	3.417	3.733	4.069	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.070	5.543	6.041	ns
		GCLK PLL	t_{CO}	3.417	3.733	4.069	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.412	5.907	6.427	ns
		GCLK PLL	t_{CO}	3.757	4.094	4.450	ns
	8 mA	GCLK	t_{CO}	5.412	5.907	6.427	ns
		GCLK PLL	t_{CO}	3.757	4.094	4.450	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.412	5.733	6.077	ns
		GCLK PLL	t_{CO}	3.757	3.920	4.100	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.126	5.614	6.128	ns
		GCLK PLL	t_{CO}	3.471	3.801	4.151	ns
	8 mA	GCLK	t_{CO}	4.869	5.347	5.851	ns
		GCLK PLL	t_{CO}	3.214	3.534	3.874	ns
	12 mA	GCLK	t_{CO}	4.780	5.252	5.749	ns
		GCLK PLL	t_{CO}	3.125	3.439	3.772	ns
	16 mA	GCLK	t_{CO}	4.734	5.201	5.694	ns
		GCLK PLL	t_{CO}	3.079	3.388	3.717	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.867	5.345	5.849	ns
		GCLK PLL	t_{CO}	3.212	3.532	3.872	ns
	8 mA	GCLK	t_{CO}	4.734	5.202	5.697	ns
		GCLK PLL	t_{CO}	3.079	3.389	3.720	ns
	12 mA	GCLK	t_{CO}	4.699	5.166	5.658	ns
		GCLK PLL	t_{CO}	3.044	3.353	3.681	ns
	16 mA	GCLK	t_{CO}	4.684	5.150	5.641	ns
		GCLK PLL	t_{CO}	3.029	3.337	3.664	ns
2.5V	4 mA	GCLK	t_{CO}	5.224	5.728	6.258	ns
		GCLK PLL	t_{CO}	3.569	3.915	4.281	ns
	8 mA	GCLK	t_{CO}	4.989	5.484	6.004	ns
		GCLK PLL	t_{CO}	3.334	3.671	4.027	ns
	12 mA	GCLK	t_{CO}	4.890	5.379	5.894	ns
		GCLK PLL	t_{CO}	3.235	3.566	3.917	ns
	16 mA	GCLK	t_{CO}	4.849	5.337	5.851	ns
		GCLK PLL	t_{CO}	3.194	3.524	3.874	ns
1.8V	2 mA	GCLK	t_{CO}	6.318	6.964	7.638	ns
		GCLK PLL	t_{CO}	4.663	5.151	5.661	ns
	4 mA	GCLK	t_{CO}	5.805	6.436	7.094	ns
		GCLK PLL	t_{CO}	4.150	4.623	5.117	ns
	6 mA	GCLK	t_{CO}	5.584	6.182	6.807	ns
		GCLK PLL	t_{CO}	3.929	4.369	4.830	ns
	8 mA	GCLK	t_{CO}	5.483	6.068	6.681	ns
		GCLK PLL	t_{CO}	3.828	4.255	4.704	ns
	10 mA	GCLK	t_{CO}	5.432	6.019	6.635	ns
		GCLK PLL	t_{CO}	3.777	4.206	4.658	ns
	12 mA	GCLK	t_{CO}	5.377	5.956	6.562	ns
		GCLK PLL	t_{CO}	3.722	4.143	4.585	ns
	16 mA	GCLK	t_{CO}	5.334	5.909	6.513	ns
		GCLK PLL	t_{CO}	3.679	4.096	4.536	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{CO}	6.712	7.531	8.383	ns
		GCLK PLL	t_{CO}	5.057	5.718	6.406	ns
	4 mA	GCLK	t_{CO}	6.256	6.987	7.750	ns
		GCLK PLL	t_{CO}	4.601	5.174	5.773	ns
	6 mA	GCLK	t_{CO}	6.089	6.809	7.559	ns
		GCLK PLL	t_{CO}	4.434	4.996	5.582	ns
	8 mA	GCLK	t_{CO}	6.013	6.716	7.449	ns
		GCLK PLL	t_{CO}	4.358	4.903	5.472	ns
	10 mA	GCLK	t_{CO}	5.953	6.653	7.383	ns
		GCLK PLL	t_{CO}	4.298	4.840	5.406	ns
	12 mA	GCLK	t_{CO}	5.919	6.610	7.332	ns
		GCLK PLL	t_{CO}	4.264	4.797	5.355	ns
	16 mA	GCLK	t_{CO}	5.822	6.502	7.213	ns
		GCLK PLL	t_{CO}	4.167	4.689	5.236	ns
1.2V	2 mA	GCLK	t_{CO}	7.900	9.071	10.279	ns
		GCLK PLL	t_{CO}	6.245	7.258	8.302	ns
	4 mA	GCLK	t_{CO}	7.465	8.557	9.687	ns
		GCLK PLL	t_{CO}	5.810	6.744	7.710	ns
	6 mA	GCLK	t_{CO}	7.337	8.403	9.508	ns
		GCLK PLL	t_{CO}	5.682	6.590	7.531	ns
	8 mA	GCLK	t_{CO}	7.265	8.321	9.413	ns
		GCLK PLL	t_{CO}	5.610	6.508	7.436	ns
	10 mA	GCLK	t_{CO}	7.134	8.158	9.218	ns
		GCLK PLL	t_{CO}	5.479	6.345	7.241	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.818	5.311	5.829	ns
		GCLK PLL	t_{CO}	3.163	3.507	3.864	ns
	12 mA	GCLK	t_{CO}	4.799	5.292	5.808	ns
		GCLK PLL	t_{CO}	3.144	3.488	3.843	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.744	5.235	5.748	ns
		GCLK PLL	t_{CO}	3.089	3.431	3.783	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.252	5.826	6.424	ns
		GCLK PLL	t_{CO}	3.597	4.022	4.459	ns
	10 mA	GCLK	t_{CO}	5.239	5.808	6.403	ns
		GCLK PLL	t_{CO}	3.584	4.004	4.438	ns
	12 mA	GCLK	t_{CO}	5.226	5.793	6.385	ns
		GCLK PLL	t_{CO}	3.571	3.989	4.420	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.196	5.764	6.357	ns
		GCLK PLL	t_{CO}	3.541	3.960	4.392	ns
	16 mA	GCLK	t_{CO}	5.188	5.758	6.352	ns
		GCLK PLL	t_{CO}	3.533	3.954	4.387	ns

Table 1–63. EP3C16 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.216	5.780	6.369	ns
		GCLK PLL	t_{CO}	3.561	3.976	4.404	ns
	10 mA	GCLK	t_{CO}	5.211	5.776	6.366	ns
		GCLK PLL	t_{CO}	3.556	3.972	4.401	ns
	12 mA	GCLK	t_{CO}	5.204	5.769	6.359	ns
		GCLK PLL	t_{CO}	3.549	3.965	4.394	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.142	5.703	6.288	ns
		GCLK PLL	t_{CO}	3.487	3.899	4.323	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.731	6.401	7.098	ns
		GCLK PLL	t_{CO}	4.076	4.597	5.133	ns
	10 mA	GCLK	t_{CO}	5.743	6.413	7.109	ns
		GCLK PLL	t_{CO}	4.088	4.609	5.144	ns
	12 mA	GCLK	t_{CO}	5.731	6.404	7.104	ns
		GCLK PLL	t_{CO}	4.076	4.600	5.139	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.676	6.347	7.043	ns
		GCLK PLL	t_{CO}	4.021	4.543	5.078	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	6.968	7.973	9.011	ns
		GCLK PLL	t_{CO}	5.313	6.169	7.046	ns
	10 mA	GCLK	t_{CO}	6.907	7.888	8.902	ns
		GCLK PLL	t_{CO}	5.252	6.084	6.937	ns
3.0-V PCI	—	GCLK	t_{CO}	5.026	5.493	5.984	ns
		GCLK PLL	t_{CO}	3.371	3.680	4.007	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.026	5.493	5.984	ns
		GCLK PLL	t_{CO}	3.371	3.680	4.007	ns

Table 1–64. EP3C16 Column Pin Differential I/O Timing Parameters (Part 1 of 2)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.928	1.003	1.060	ns
			t_H	–0.650	–0.687	–0.707	ns
		GCLK PLL	t_{SU}	2.581	2.813	3.032	ns
			t_H	–2.303	–2.497	–2.679	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.191	5.686	6.207	ns
		GCLK PLL	t_{CO}	3.538	3.876	4.235	ns

Table 1–64. EP3C16 Column Pin Differential I/O Timing Parameters (Part 2 of 2)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
RSDS_E_1R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.810	5.307	5.829	ns
		GCLK PLL	t_{CO}	3.157	3.497	3.857	ns

Table 1–65. EP3C16 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.959	1.038	1.105	ns
			t_H	–0.681	–0.723	–0.751	ns
			t_{CO}	3.983	4.375	4.789	ns
	—	GCLK PLL	t_{SU}	2.612	2.848	3.077	ns
			t_H	–2.334	–2.533	–2.723	ns
			t_{CO}	2.330	2.565	2.817	ns
mini-LVDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns
PPDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns
RSDS	—	GCLK	t_{CO}	3.983	4.375	4.789	ns
		GCLK PLL	t_{CO}	2.330	2.565	2.817	ns

EP3C25 I/O Timing Parameters

Table 1–66 through Table 1–71 show the maximum I/O timing parameters for EP3C25 devices.

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	12 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	16 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	8 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	12 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns
	16 mA	GCLK	t_{SU}	1.049	1.070	1.072	ns
			t_H	–0.769	–0.752	–0.718	ns
		GCLK PLL	t_{SU}	2.793	2.983	3.155	ns
			t_H	–2.513	–2.665	–2.801	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	8 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	12 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
	16 mA	GCLK	t_{SU}	0.992	1.025	1.040	ns
			t_H	–0.712	–0.708	–0.687	ns
		GCLK PLL	t_{SU}	2.736	2.938	3.123	ns
			t_H	–2.456	–2.621	–2.770	ns
1.8V	2 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	4 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	6 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	8 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	10 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
	12 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.927	0.986	1.027	ns
			t_H	–0.649	–0.670	–0.673	ns
		GCLK PLL	t_{SU}	2.671	2.899	3.110	ns
			t_H	–2.393	–2.583	–2.756	ns
1.5V	2 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	4 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	6 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	8 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	10 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
	12 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	16 mA	GCLK	t_{SU}	0.996	1.078	1.144	ns
			t_H	–0.716	–0.760	–0.788	ns
		GCLK PLL	t_{SU}	2.740	2.991	3.227	ns
			t_H	–2.460	–2.673	–2.871	ns
1.2V	2 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	4 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	6 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	8 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	10 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
	12 mA	GCLK	t_{SU}	1.148	1.258	1.350	ns
			t_H	–0.866	–0.936	–0.990	ns
		GCLK PLL	t_{SU}	2.892	3.171	3.433	ns
			t_H	–2.610	–2.849	–3.073	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns
	12 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.981	1.043	1.089	ns
			t_H	–0.701	–0.726	–0.734	ns
		GCLK PLL	t_{SU}	2.722	2.953	3.171	ns
			t_H	–2.442	–2.636	–2.816	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	10 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	16 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	10 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
	12 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.042	1.132	1.204	ns
			t_H	–0.762	–0.813	–0.847	ns
		GCLK PLL	t_{SU}	2.783	3.042	3.286	ns
			t_H	–2.503	–2.723	–2.929	ns

Table 1–66. EP3C25 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
	10 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
	12 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.998	1.092	1.170	ns
			t_H	–0.718	–0.774	–0.814	ns
		GCLK PLL	t_{SU}	2.739	3.002	3.252	ns
			t_H	–2.459	–2.684	–2.896	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
	10 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
	12 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.130	1.251	1.354	ns
			t_H	–0.848	–0.929	–0.994	ns
		GCLK PLL	t_{SU}	2.871	3.161	3.436	ns
			t_H	–2.589	–2.839	–3.076	ns
3.0-V PCI	—	GCLK	t_{SU}	1.045	1.066	1.067	ns
			t_H	–0.765	–0.748	–0.713	ns
	—	GCLK PLL	t_{SU}	2.789	2.979	3.150	ns
			t_H	–2.509	–2.661	–2.796	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.045	1.066	1.067	ns
			t_H	–0.765	–0.748	–0.713	ns
	—	GCLK PLL	t_{SU}	2.789	2.979	3.150	ns
			t_H	–2.509	–2.661	–2.796	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	12 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	16 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	8 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	12 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns
	16 mA	GCLK	t_{SU}	1.082	1.112	1.121	ns
			t_H	–0.802	–0.794	–0.766	ns
		GCLK PLL	t_{SU}	2.823	3.020	3.205	ns
			t_H	–2.543	–2.702	–2.850	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	8 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	12 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
	16 mA	GCLK	t_{SU}	1.025	1.068	1.092	ns
			t_H	–0.745	–0.751	–0.738	ns
		GCLK PLL	t_{SU}	2.766	2.976	3.176	ns
			t_H	–2.486	–2.659	–2.822	ns
1.8V	2 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	4 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	6 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	8 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	10 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
	12 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.961	1.029	1.078	ns
			t_H	–0.683	–0.713	–0.723	ns
		GCLK PLL	t_{SU}	2.702	2.937	3.162	ns
			t_H	–2.424	–2.621	–2.807	ns
1.5V	2 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	4 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	6 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	8 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	10 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	12 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
	16 mA	GCLK	t_{SU}	1.030	1.122	1.196	ns
			t_H	–0.750	–0.804	–0.840	ns
		GCLK PLL	t_{SU}	2.771	3.030	3.280	ns
			t_H	–2.491	–2.712	–2.924	ns
1.2V	2 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	4 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	8 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
	10 mA	GCLK	t_{SU}	1.183	1.302	1.403	ns
			t_H	–0.901	–0.980	–1.042	ns
		GCLK PLL	t_{SU}	2.924	3.210	3.487	ns
			t_H	–2.642	–2.888	–3.126	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
	12 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	1.016	1.086	1.140	ns
			t_H	–0.736	–0.768	–0.784	ns
		GCLK PLL	t_{SU}	2.756	2.995	3.229	ns
			t_H	–2.476	–2.677	–2.873	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	10 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	16 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	10 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
	12 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	1.078	1.175	1.257	ns
			t_H	–0.798	–0.856	–0.899	ns
		GCLK PLL	t_{SU}	2.818	3.084	3.346	ns
			t_H	–2.538	–2.765	–2.988	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
	10 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
	12 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	1.033	1.134	1.220	ns
			t_H	–0.753	–0.816	–0.863	ns
		GCLK PLL	t_{SU}	2.773	3.043	3.309	ns
			t_H	–2.493	–2.725	–2.952	ns

Table 1–67. EP3C25 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.164	1.292	1.405	ns
			t_H	–0.882	–0.970	–1.045	ns
		GCLK PLL	t_{SU}	2.904	3.201	3.494	ns
			t_H	–2.622	–2.879	–3.134	ns
	10 mA	GCLK	t_{SU}	1.164	1.292	1.405	ns
			t_H	–0.882	–0.970	–1.045	ns
		GCLK PLL	t_{SU}	2.904	3.201	3.494	ns
			t_H	–2.622	–2.879	–3.134	ns
3.0-V PCI	—	GCLK	t_{SU}	1.078	1.108	1.117	ns
			t_H	–0.798	–0.790	–0.762	ns
	—	GCLK PLL	t_{SU}	2.819	3.016	3.201	ns
			t_H	–2.539	–2.698	–2.846	ns
3.0-V PCI-X	—	GCLK	t_{SU}	1.078	1.108	1.117	ns
			t_H	–0.798	–0.790	–0.762	ns
	—	GCLK PLL	t_{SU}	2.819	3.016	3.201	ns
			t_H	–2.539	–2.698	–2.846	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.531	6.039	6.571	ns
		GCLK PLL	t_{CO}	3.787	4.126	4.488	ns
	8 mA	GCLK	t_{CO}	5.531	6.039	6.571	ns
		GCLK PLL	t_{CO}	3.787	4.126	4.488	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.490	5.820	6.173	ns
		GCLK PLL	t_{CO}	3.746	3.907	4.090	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.241	5.742	6.269	ns
		GCLK PLL	t_{CO}	3.497	3.829	4.186	ns
	8 mA	GCLK	t_{CO}	4.970	5.458	5.970	ns
		GCLK PLL	t_{CO}	3.226	3.545	3.887	ns
	12 mA	GCLK	t_{CO}	4.873	5.357	5.866	ns
		GCLK PLL	t_{CO}	3.129	3.444	3.783	ns
	16 mA	GCLK	t_{CO}	4.826	5.305	5.808	ns
		GCLK PLL	t_{CO}	3.082	3.392	3.725	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.968	5.455	5.967	ns
		GCLK PLL	t_{CO}	3.224	3.542	3.884	ns
	8 mA	GCLK	t_{CO}	4.827	5.307	5.812	ns
		GCLK PLL	t_{CO}	3.083	3.394	3.729	ns
	12 mA	GCLK	t_{CO}	4.790	5.267	5.769	ns
		GCLK PLL	t_{CO}	3.046	3.354	3.686	ns
	16 mA	GCLK	t_{CO}	4.774	5.252	5.754	ns
		GCLK PLL	t_{CO}	3.030	3.339	3.671	ns
2.5V	4 mA	GCLK	t_{CO}	5.299	5.828	6.383	ns
		GCLK PLL	t_{CO}	3.555	3.915	4.300	ns
	8 mA	GCLK	t_{CO}	5.056	5.575	6.119	ns
		GCLK PLL	t_{CO}	3.312	3.662	4.036	ns
	12 mA	GCLK	t_{CO}	4.958	5.469	6.006	ns
		GCLK PLL	t_{CO}	3.214	3.556	3.923	ns
	16 mA	GCLK	t_{CO}	4.919	5.429	5.965	ns
		GCLK PLL	t_{CO}	3.175	3.516	3.882	ns
1.8V	2 mA	GCLK	t_{CO}	6.410	7.081	7.781	ns
		GCLK PLL	t_{CO}	4.666	5.168	5.698	ns
	4 mA	GCLK	t_{CO}	5.883	6.536	7.217	ns
		GCLK PLL	t_{CO}	4.139	4.623	5.134	ns
	6 mA	GCLK	t_{CO}	5.658	6.278	6.925	ns
		GCLK PLL	t_{CO}	3.914	4.365	4.842	ns
	8 mA	GCLK	t_{CO}	5.555	6.161	6.796	ns
		GCLK PLL	t_{CO}	3.811	4.248	4.713	ns
	10 mA	GCLK	t_{CO}	5.503	6.113	6.750	ns
		GCLK PLL	t_{CO}	3.759	4.200	4.667	ns
	12 mA	GCLK	t_{CO}	5.446	6.046	6.675	ns
		GCLK PLL	t_{CO}	3.702	4.133	4.592	ns
	16 mA	GCLK	t_{CO}	5.392	5.987	6.610	ns
		GCLK PLL	t_{CO}	3.648	4.074	4.527	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{CO}	6.798	7.643	8.520	ns
		GCLK PLL	t_{CO}	5.054	5.730	6.437	ns
	4 mA	GCLK	t_{CO}	6.323	7.082	7.872	ns
		GCLK PLL	t_{CO}	4.579	5.169	5.789	ns
	6 mA	GCLK	t_{CO}	6.153	6.899	7.675	ns
		GCLK PLL	t_{CO}	4.409	4.986	5.592	ns
	8 mA	GCLK	t_{CO}	6.065	6.786	7.537	ns
		GCLK PLL	t_{CO}	4.321	4.873	5.454	ns
	10 mA	GCLK	t_{CO}	6.006	6.726	7.476	ns
		GCLK PLL	t_{CO}	4.262	4.813	5.393	ns
	12 mA	GCLK	t_{CO}	5.973	6.685	7.426	ns
		GCLK PLL	t_{CO}	4.229	4.772	5.343	ns
	16 mA	GCLK	t_{CO}	5.859	6.543	7.256	ns
		GCLK PLL	t_{CO}	4.115	4.630	5.173	ns
1.2V	2 mA	GCLK	t_{CO}	7.971	9.171	10.409	ns
		GCLK PLL	t_{CO}	6.227	7.258	8.326	ns
	4 mA	GCLK	t_{CO}	7.526	8.645	9.802	ns
		GCLK PLL	t_{CO}	5.782	6.732	7.719	ns
	6 mA	GCLK	t_{CO}	7.377	8.464	9.588	ns
		GCLK PLL	t_{CO}	5.633	6.551	7.505	ns
	8 mA	GCLK	t_{CO}	7.308	8.384	9.498	ns
		GCLK PLL	t_{CO}	5.564	6.471	7.415	ns
	10 mA	GCLK	t_{CO}	7.172	8.202	9.267	ns
		GCLK PLL	t_{CO}	5.428	6.289	7.184	ns
	12 mA	GCLK	t_{CO}	7.144	8.176	9.245	ns
		GCLK PLL	t_{CO}	5.400	6.263	7.162	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.914	5.418	5.947	ns
		GCLK PLL	t_{CO}	3.173	3.508	3.864	ns
	12 mA	GCLK	t_{CO}	4.892	5.394	5.924	ns
		GCLK PLL	t_{CO}	3.151	3.484	3.841	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.832	5.332	5.858	ns
		GCLK PLL	t_{CO}	3.091	3.422	3.775	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.348	5.931	6.542	ns
		GCLK PLL	t_{CO}	3.607	4.021	4.459	ns
	10 mA	GCLK	t_{CO}	5.323	5.900	6.505	ns
		GCLK PLL	t_{CO}	3.582	3.990	4.422	ns
	12 mA	GCLK	t_{CO}	5.311	5.886	6.488	ns
		GCLK PLL	t_{CO}	3.570	3.976	4.405	ns

Table 1–68. EP3C25 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.282	5.857	6.460	ns
		GCLK PLL	t_{CO}	3.541	3.947	4.377	ns
	16 mA	GCLK	t_{CO}	5.269	5.844	6.446	ns
		GCLK PLL	t_{CO}	3.528	3.934	4.363	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.310	5.883	6.484	ns
		GCLK PLL	t_{CO}	3.569	3.973	4.401	ns
	10 mA	GCLK	t_{CO}	5.299	5.876	6.480	ns
		GCLK PLL	t_{CO}	3.558	3.966	4.397	ns
	12 mA	GCLK	t_{CO}	5.290	5.862	6.460	ns
		GCLK PLL	t_{CO}	3.549	3.952	4.377	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.225	5.796	6.394	ns
		GCLK PLL	t_{CO}	3.484	3.886	4.311	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.824	6.504	7.215	ns
		GCLK PLL	t_{CO}	4.083	4.594	5.132	ns
	10 mA	GCLK	t_{CO}	5.827	6.504	7.210	ns
		GCLK PLL	t_{CO}	4.086	4.594	5.127	ns
	12 mA	GCLK	t_{CO}	5.815	6.496	7.206	ns
		GCLK PLL	t_{CO}	4.074	4.586	5.123	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.753	6.428	7.131	ns
		GCLK PLL	t_{CO}	4.012	4.518	5.048	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.037	8.042	9.082	ns
		GCLK PLL	t_{CO}	5.296	6.132	6.999	ns
	10 mA	GCLK	t_{CO}	6.975	7.953	8.966	ns
		GCLK PLL	t_{CO}	5.234	6.043	6.883	ns
	12 mA	GCLK	t_{CO}	6.977	7.959	8.975	ns
		GCLK PLL	t_{CO}	5.236	6.049	6.892	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	6.932	7.906	8.915	ns
		GCLK PLL	t_{CO}	5.191	5.996	6.832	ns
3.0-V PCI	—	GCLK	t_{CO}	5.121	5.599	6.103	ns
		GCLK PLL	t_{CO}	3.377	3.686	4.020	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.121	5.599	6.103	ns
		GCLK PLL	t_{CO}	3.377	3.686	4.020	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.471	5.968	6.493	ns
		GCLK PLL	t_{CO}	3.730	4.060	4.409	ns
	8 mA	GCLK	t_{CO}	5.471	5.968	6.493	ns
		GCLK PLL	t_{CO}	3.730	4.060	4.409	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.471	5.794	6.143	ns
		GCLK PLL	t_{CO}	3.730	3.886	4.059	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.185	5.675	6.194	ns
		GCLK PLL	t_{CO}	3.444	3.767	4.110	ns
	8 mA	GCLK	t_{CO}	4.928	5.408	5.917	ns
		GCLK PLL	t_{CO}	3.187	3.500	3.833	ns
	12 mA	GCLK	t_{CO}	4.839	5.313	5.815	ns
		GCLK PLL	t_{CO}	3.098	3.405	3.731	ns
	16 mA	GCLK	t_{CO}	4.793	5.262	5.760	ns
		GCLK PLL	t_{CO}	3.052	3.354	3.676	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	4.926	5.406	5.915	ns
		GCLK PLL	t_{CO}	3.185	3.498	3.831	ns
	8 mA	GCLK	t_{CO}	4.793	5.263	5.763	ns
		GCLK PLL	t_{CO}	3.052	3.355	3.679	ns
	12 mA	GCLK	t_{CO}	4.758	5.227	5.724	ns
		GCLK PLL	t_{CO}	3.017	3.319	3.640	ns
	16 mA	GCLK	t_{CO}	4.743	5.211	5.707	ns
		GCLK PLL	t_{CO}	3.002	3.303	3.623	ns
2.5V	4 mA	GCLK	t_{CO}	5.283	5.789	6.324	ns
		GCLK PLL	t_{CO}	3.542	3.881	4.240	ns
	8 mA	GCLK	t_{CO}	5.048	5.545	6.070	ns
		GCLK PLL	t_{CO}	3.307	3.637	3.986	ns
	12 mA	GCLK	t_{CO}	4.949	5.440	5.960	ns
		GCLK PLL	t_{CO}	3.208	3.532	3.876	ns
	16 mA	GCLK	t_{CO}	4.908	5.398	5.917	ns
		GCLK PLL	t_{CO}	3.167	3.490	3.833	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.377	7.025	7.704	ns
		GCLK PLL	t_{CO}	4.636	5.117	5.620	ns
	4 mA	GCLK	t_{CO}	5.864	6.497	7.160	ns
		GCLK PLL	t_{CO}	4.123	4.589	5.076	ns
	6 mA	GCLK	t_{CO}	5.643	6.243	6.873	ns
		GCLK PLL	t_{CO}	3.902	4.335	4.789	ns
	8 mA	GCLK	t_{CO}	5.542	6.129	6.747	ns
		GCLK PLL	t_{CO}	3.801	4.221	4.663	ns
	10 mA	GCLK	t_{CO}	5.491	6.080	6.701	ns
		GCLK PLL	t_{CO}	3.750	4.172	4.617	ns
	12 mA	GCLK	t_{CO}	5.436	6.017	6.628	ns
		GCLK PLL	t_{CO}	3.695	4.109	4.544	ns
	16 mA	GCLK	t_{CO}	5.393	5.970	6.579	ns
		GCLK PLL	t_{CO}	3.652	4.062	4.495	ns
1.5V	2 mA	GCLK	t_{CO}	6.771	7.592	8.449	ns
		GCLK PLL	t_{CO}	5.030	5.684	6.365	ns
	4 mA	GCLK	t_{CO}	6.315	7.048	7.816	ns
		GCLK PLL	t_{CO}	4.574	5.140	5.732	ns
	6 mA	GCLK	t_{CO}	6.148	6.870	7.625	ns
		GCLK PLL	t_{CO}	4.407	4.962	5.541	ns
	8 mA	GCLK	t_{CO}	6.072	6.777	7.515	ns
		GCLK PLL	t_{CO}	4.331	4.869	5.431	ns
	10 mA	GCLK	t_{CO}	6.012	6.714	7.449	ns
		GCLK PLL	t_{CO}	4.271	4.806	5.365	ns
	12 mA	GCLK	t_{CO}	5.978	6.671	7.398	ns
		GCLK PLL	t_{CO}	4.237	4.763	5.314	ns
	16 mA	GCLK	t_{CO}	5.881	6.563	7.279	ns
		GCLK PLL	t_{CO}	4.140	4.655	5.195	ns
1.2V	2 mA	GCLK	t_{CO}	7.959	9.132	10.345	ns
		GCLK PLL	t_{CO}	6.218	7.224	8.261	ns
	4 mA	GCLK	t_{CO}	7.524	8.618	9.753	ns
		GCLK PLL	t_{CO}	5.783	6.710	7.669	ns
	6 mA	GCLK	t_{CO}	7.396	8.464	9.574	ns
		GCLK PLL	t_{CO}	5.655	6.556	7.490	ns
	8 mA	GCLK	t_{CO}	7.324	8.382	9.479	ns
		GCLK PLL	t_{CO}	5.583	6.474	7.395	ns
	10 mA	GCLK	t_{CO}	7.193	8.219	9.284	ns
		GCLK PLL	t_{CO}	5.452	6.311	7.200	ns

Table 1–69. EP3C25 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	4.876	5.373	5.898	ns
		GCLK PLL	t_{CO}	3.136	3.464	3.809	ns
	12 mA	GCLK	t_{CO}	4.857	5.354	5.877	ns
		GCLK PLL	t_{CO}	3.117	3.445	3.788	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.802	5.297	5.817	ns
		GCLK PLL	t_{CO}	3.062	3.388	3.728	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.310	5.888	6.493	ns
		GCLK PLL	t_{CO}	3.570	3.979	4.404	ns
	10 mA	GCLK	t_{CO}	5.297	5.870	6.472	ns
		GCLK PLL	t_{CO}	3.557	3.961	4.383	ns
	12 mA	GCLK	t_{CO}	5.284	5.855	6.454	ns
		GCLK PLL	t_{CO}	3.544	3.946	4.365	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.254	5.826	6.426	ns
		GCLK PLL	t_{CO}	3.514	3.917	4.337	ns
	16 mA	GCLK	t_{CO}	5.246	5.820	6.421	ns
		GCLK PLL	t_{CO}	3.506	3.911	4.332	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.274	5.842	6.438	ns
		GCLK PLL	t_{CO}	3.534	3.933	4.349	ns
	10 mA	GCLK	t_{CO}	5.269	5.838	6.435	ns
		GCLK PLL	t_{CO}	3.529	3.929	4.346	ns
	12 mA	GCLK	t_{CO}	5.262	5.831	6.428	ns
		GCLK PLL	t_{CO}	3.522	3.922	4.339	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.200	5.765	6.357	ns
		GCLK PLL	t_{CO}	3.460	3.856	4.268	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.789	6.463	7.167	ns
		GCLK PLL	t_{CO}	4.049	4.554	5.078	ns
	10 mA	GCLK	t_{CO}	5.801	6.475	7.178	ns
		GCLK PLL	t_{CO}	4.061	4.566	5.089	ns
	12 mA	GCLK	t_{CO}	5.789	6.466	7.173	ns
		GCLK PLL	t_{CO}	4.049	4.557	5.084	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.734	6.409	7.112	ns
		GCLK PLL	t_{CO}	3.994	4.500	5.023	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.026	8.035	9.080	ns
		GCLK PLL	t_{CO}	5.286	6.126	6.991	ns
	10 mA	GCLK	t_{CO}	6.965	7.950	8.971	ns
		GCLK PLL	t_{CO}	5.225	6.041	6.882	ns
3.0-V PCI	—	GCLK	t_{CO}	5.085	5.554	6.050	ns
		GCLK PLL	t_{CO}	3.344	3.646	3.966	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.085	5.554	6.050	ns
		GCLK PLL	t_{CO}	3.344	3.646	3.966	ns

Table 1–70. EP3C25 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.876	0.946	0.996	ns
			t_H	–0.598	–0.630	–0.643	ns
	—	GCLK PLL	t_{SU}	2.618	2.857	3.080	ns
			t_H	–2.340	–2.541	–2.727	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.242	5.743	6.271	ns
		GCLK PLL	t_{CO}	3.500	3.832	4.187	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.861	5.364	5.893	ns
		GCLK PLL	t_{CO}	3.119	3.453	3.809	ns

Table 1–71. EP3C25 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.906	0.982	1.042	ns
			t_H	–0.628	–0.667	–0.688	ns
			t_{CO}	4.038	4.433	4.853	ns
	—	GCLK PLL	t_{SU}	2.648	2.893	3.127	ns
			t_H	–2.370	–2.578	–2.773	ns
			t_{CO}	2.295	2.522	2.769	ns
mini-LVDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns
PPDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns
RSDS	—	GCLK	t_{CO}	4.038	4.433	4.853	ns
		GCLK PLL	t_{CO}	2.295	2.522	2.769	ns

EP3C40 I/O Timing Parameters

Table 1–72 through Table 1–77 show the maximum I/O timing parameters for EP3C40 devices.

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	12 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	16 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	8 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
	16 mA	GCLK	t_{SU}	0.920	0.929	0.918	ns
			t_H	–0.640	–0.611	–0.564	ns
		GCLK PLL	t_{SU}	2.800	2.997	3.176	ns
			t_H	–2.520	–2.679	–2.822	ns
2.5V	4 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	8 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	12 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
	16 mA	GCLK	t_{SU}	0.863	0.884	0.886	ns
			t_H	–0.583	–0.567	–0.533	ns
		GCLK PLL	t_{SU}	2.743	2.952	3.144	ns
			t_H	–2.463	–2.635	–2.791	ns
1.8V	2 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	4 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	6 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	8 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	12 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
	16 mA	GCLK	t_{SU}	0.799	0.845	0.873	ns
			t_H	–0.521	–0.529	–0.519	ns
		GCLK PLL	t_{SU}	2.678	2.913	3.131	ns
			t_H	–2.400	–2.597	–2.777	ns
1.5V	2 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	4 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	6 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	8 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	10 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	12 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns
	16 mA	GCLK	t_{SU}	0.868	0.937	0.990	ns
			t_H	–0.588	–0.619	–0.634	ns
		GCLK PLL	t_{SU}	2.747	3.005	3.248	ns
			t_H	–2.467	–2.687	–2.892	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	4 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	6 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	8 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	10 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
	12 mA	GCLK	t_{SU}	1.020	1.117	1.196	ns
			t_H	–0.738	–0.795	–0.836	ns
		GCLK PLL	t_{SU}	2.899	3.185	3.454	ns
			t_H	–2.617	–2.863	–3.094	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns
	12 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.852	0.902	0.935	ns
			t_H	–0.572	–0.585	–0.580	ns
		GCLK PLL	t_{SU}	2.733	2.969	3.193	ns
			t_H	–2.453	–2.652	–2.838	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	10 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	16 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	10 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
	12 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.913	0.991	1.050	ns
			t_H	–0.633	–0.672	–0.693	ns
		GCLK PLL	t_{SU}	2.794	3.058	3.308	ns
			t_H	–2.514	–2.739	–2.951	ns

Table 1–72. EP3C40 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
	10 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
	12 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.869	0.951	1.016	ns
			t_H	–0.589	–0.633	–0.660	ns
		GCLK PLL	t_{SU}	2.750	3.018	3.274	ns
			t_H	–2.470	–2.700	–2.918	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
	10 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
	12 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	1.001	1.110	1.200	ns
			t_H	–0.719	–0.788	–0.840	ns
		GCLK PLL	t_{SU}	2.882	3.177	3.458	ns
			t_H	–2.600	–2.855	–3.098	ns
3.0-V PCI	—	GCLK	t_{SU}	0.916	0.925	0.913	ns
			t_H	–0.636	–0.607	–0.559	ns
		GCLK PLL	t_{SU}	2.796	2.993	3.171	ns
			t_H	–2.516	–2.675	–2.817	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.916	0.925	0.913	ns
			t_H	–0.636	–0.607	–0.559	ns
		GCLK PLL	t_{SU}	2.796	2.993	3.171	ns
			t_H	–2.516	–2.675	–2.817	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	12 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	16 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	8 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
	16 mA	GCLK	t_{SU}	0.953	0.966	0.962	ns
			t_H	–0.673	–0.648	–0.607	ns
		GCLK PLL	t_{SU}	2.843	3.046	3.214	ns
			t_H	–2.563	–2.728	–2.859	ns
2.5V	4 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	8 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	12 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
	16 mA	GCLK	t_{SU}	0.896	0.922	0.933	ns
			t_H	–0.616	–0.605	–0.579	ns
		GCLK PLL	t_{SU}	2.786	3.002	3.185	ns
			t_H	–2.506	–2.685	–2.831	ns
1.8V	2 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	4 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	6 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	8 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	12 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
	16 mA	GCLK	t_{SU}	0.832	0.883	0.919	ns
			t_H	–0.554	–0.567	–0.564	ns
		GCLK PLL	t_{SU}	2.722	2.963	3.171	ns
			t_H	–2.444	–2.647	–2.816	ns
1.5V	2 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	4 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	6 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	8 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	10 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	12 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns
	16 mA	GCLK	t_{SU}	0.901	0.976	1.037	ns
			t_H	–0.621	–0.658	–0.681	ns
		GCLK PLL	t_{SU}	2.791	3.056	3.289	ns
			t_H	–2.511	–2.738	–2.933	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	4 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	6 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	8 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
	10 mA	GCLK	t_{SU}	1.054	1.156	1.244	ns
			t_H	–0.772	–0.834	–0.883	ns
		GCLK PLL	t_{SU}	2.944	3.236	3.496	ns
			t_H	–2.662	–2.914	–3.135	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns
	12 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.882	0.940	0.976	ns
			t_H	–0.602	–0.622	–0.620	ns
		GCLK PLL	t_{SU}	2.776	3.020	3.247	ns
			t_H	–2.496	–2.702	–2.891	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	10 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	16 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
	10 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class I	12 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.944	1.029	1.093	ns
			t_H	–0.664	–0.710	–0.735	ns
		GCLK PLL	t_{SU}	2.838	3.109	3.364	ns
			t_H	–2.558	–2.790	–3.006	ns

Table 1–73. EP3C40 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
	10 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
	12 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.899	0.988	1.056	ns
			t_H	–0.619	–0.670	–0.699	ns
		GCLK PLL	t_{SU}	2.793	3.068	3.327	ns
			t_H	–2.513	–2.750	–2.970	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	1.030	1.146	1.241	ns
			t_H	–0.748	–0.824	–0.881	ns
		GCLK PLL	t_{SU}	2.924	3.226	3.512	ns
			t_H	–2.642	–2.904	–3.152	ns
	10 mA	GCLK	t_{SU}	1.030	1.146	1.241	ns
			t_H	–0.748	–0.824	–0.881	ns
		GCLK PLL	t_{SU}	2.924	3.226	3.512	ns
			t_H	–2.642	–2.904	–3.152	ns
3.0-V PCI	—	GCLK	t_{SU}	0.949	0.962	0.958	ns
			t_H	–0.669	–0.644	–0.603	ns
	—	GCLK PLL	t_{SU}	2.839	3.042	3.210	ns
			t_H	–2.559	–2.724	–2.855	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.949	0.962	0.958	ns
			t_H	–0.669	–0.644	–0.603	ns
	—	GCLK PLL	t_{SU}	2.839	3.042	3.210	ns
			t_H	–2.559	–2.724	–2.855	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.660	6.180	6.725	ns
		GCLK PLL	t_{CO}	3.780	4.112	4.467	ns
	8 mA	GCLK	t_{CO}	5.660	6.180	6.725	ns
		GCLK PLL	t_{CO}	3.780	4.112	4.467	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.619	5.961	6.327	ns
		GCLK PLL	t_{CO}	3.739	3.893	4.069	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.370	5.883	6.423	ns
		GCLK PLL	t_{CO}	3.490	3.815	4.165	ns
	8 mA	GCLK	t_{CO}	5.099	5.599	6.124	ns
		GCLK PLL	t_{CO}	3.219	3.531	3.866	ns
	12 mA	GCLK	t_{CO}	5.002	5.498	6.020	ns
		GCLK PLL	t_{CO}	3.122	3.430	3.762	ns
	16 mA	GCLK	t_{CO}	4.955	5.446	5.962	ns
		GCLK PLL	t_{CO}	3.075	3.378	3.704	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.097	5.596	6.121	ns
		GCLK PLL	t_{CO}	3.217	3.528	3.863	ns
	8 mA	GCLK	t_{CO}	4.956	5.448	5.966	ns
		GCLK PLL	t_{CO}	3.076	3.380	3.708	ns
	12 mA	GCLK	t_{CO}	4.919	5.408	5.923	ns
		GCLK PLL	t_{CO}	3.039	3.340	3.665	ns
	16 mA	GCLK	t_{CO}	4.903	5.393	5.908	ns
		GCLK PLL	t_{CO}	3.023	3.325	3.650	ns
2.5V	4 mA	GCLK	t_{CO}	5.428	5.969	6.537	ns
		GCLK PLL	t_{CO}	3.548	3.901	4.279	ns
	8 mA	GCLK	t_{CO}	5.185	5.716	6.273	ns
		GCLK PLL	t_{CO}	3.305	3.648	4.015	ns
	12 mA	GCLK	t_{CO}	5.087	5.610	6.160	ns
		GCLK PLL	t_{CO}	3.207	3.542	3.902	ns
	16 mA	GCLK	t_{CO}	5.048	5.570	6.119	ns
		GCLK PLL	t_{CO}	3.168	3.502	3.861	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.538	7.222	7.935	ns
		GCLK PLL	t_{CO}	4.659	5.154	5.677	ns
	4 mA	GCLK	t_{CO}	6.011	6.677	7.371	ns
		GCLK PLL	t_{CO}	4.132	4.609	5.113	ns
	6 mA	GCLK	t_{CO}	5.786	6.419	7.079	ns
		GCLK PLL	t_{CO}	3.907	4.351	4.821	ns
	8 mA	GCLK	t_{CO}	5.683	6.302	6.950	ns
		GCLK PLL	t_{CO}	3.804	4.234	4.692	ns
	10 mA	GCLK	t_{CO}	5.631	6.254	6.904	ns
		GCLK PLL	t_{CO}	3.752	4.186	4.646	ns
	12 mA	GCLK	t_{CO}	5.574	6.187	6.829	ns
		GCLK PLL	t_{CO}	3.695	4.119	4.571	ns
	16 mA	GCLK	t_{CO}	5.520	6.128	6.764	ns
		GCLK PLL	t_{CO}	3.641	4.060	4.506	ns
1.5V	2 mA	GCLK	t_{CO}	6.926	7.784	8.674	ns
		GCLK PLL	t_{CO}	5.047	5.716	6.416	ns
	4 mA	GCLK	t_{CO}	6.451	7.223	8.026	ns
		GCLK PLL	t_{CO}	4.572	5.155	5.768	ns
	6 mA	GCLK	t_{CO}	6.281	7.040	7.829	ns
		GCLK PLL	t_{CO}	4.402	4.972	5.571	ns
	8 mA	GCLK	t_{CO}	6.193	6.927	7.691	ns
		GCLK PLL	t_{CO}	4.314	4.859	5.433	ns
	10 mA	GCLK	t_{CO}	6.134	6.867	7.630	ns
		GCLK PLL	t_{CO}	4.255	4.799	5.372	ns
	12 mA	GCLK	t_{CO}	6.101	6.826	7.580	ns
		GCLK PLL	t_{CO}	4.222	4.758	5.322	ns
	16 mA	GCLK	t_{CO}	5.987	6.684	7.410	ns
		GCLK PLL	t_{CO}	4.108	4.616	5.152	ns
1.2V	2 mA	GCLK	t_{CO}	8.099	9.312	10.563	ns
		GCLK PLL	t_{CO}	6.220	7.244	8.305	ns
	4 mA	GCLK	t_{CO}	7.654	8.786	9.956	ns
		GCLK PLL	t_{CO}	5.775	6.718	7.698	ns
	6 mA	GCLK	t_{CO}	7.505	8.605	9.742	ns
		GCLK PLL	t_{CO}	5.626	6.537	7.484	ns
	8 mA	GCLK	t_{CO}	7.436	8.525	9.652	ns
		GCLK PLL	t_{CO}	5.557	6.457	7.394	ns
	10 mA	GCLK	t_{CO}	7.300	8.343	9.421	ns
		GCLK PLL	t_{CO}	5.421	6.275	7.163	ns
	12 mA	GCLK	t_{CO}	7.272	8.317	9.399	ns
		GCLK PLL	t_{CO}	5.393	6.249	7.141	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.043	5.559	6.101	ns
		GCLK PLL	t_{CO}	3.162	3.492	3.843	ns
	12 mA	GCLK	t_{CO}	5.021	5.535	6.078	ns
		GCLK PLL	t_{CO}	3.140	3.468	3.820	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.961	5.473	6.012	ns
		GCLK PLL	t_{CO}	3.080	3.406	3.754	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.477	6.072	6.696	ns
		GCLK PLL	t_{CO}	3.596	4.005	4.438	ns
	10 mA	GCLK	t_{CO}	5.452	6.041	6.659	ns
		GCLK PLL	t_{CO}	3.571	3.974	4.401	ns
	12 mA	GCLK	t_{CO}	5.440	6.027	6.642	ns
		GCLK PLL	t_{CO}	3.559	3.960	4.384	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.411	5.998	6.614	ns
		GCLK PLL	t_{CO}	3.530	3.931	4.356	ns
	16 mA	GCLK	t_{CO}	5.398	5.985	6.600	ns
		GCLK PLL	t_{CO}	3.517	3.918	4.342	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.439	6.024	6.638	ns
		GCLK PLL	t_{CO}	3.558	3.957	4.380	ns
	10 mA	GCLK	t_{CO}	5.428	6.017	6.634	ns
		GCLK PLL	t_{CO}	3.547	3.950	4.376	ns
	12 mA	GCLK	t_{CO}	5.419	6.003	6.614	ns
		GCLK PLL	t_{CO}	3.538	3.936	4.356	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.354	5.937	6.548	ns
		GCLK PLL	t_{CO}	3.473	3.870	4.290	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.953	6.645	7.369	ns
		GCLK PLL	t_{CO}	4.072	4.578	5.111	ns
	10 mA	GCLK	t_{CO}	5.956	6.645	7.364	ns
		GCLK PLL	t_{CO}	4.075	4.578	5.106	ns
	12 mA	GCLK	t_{CO}	5.944	6.637	7.360	ns
		GCLK PLL	t_{CO}	4.063	4.570	5.102	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.882	6.569	7.285	ns
		GCLK PLL	t_{CO}	4.001	4.502	5.027	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.166	8.183	9.236	ns
		GCLK PLL	t_{CO}	5.285	6.116	6.978	ns
	10 mA	GCLK	t_{CO}	7.104	8.094	9.120	ns
		GCLK PLL	t_{CO}	5.223	6.027	6.862	ns
	12 mA	GCLK	t_{CO}	7.106	8.100	9.129	ns
		GCLK PLL	t_{CO}	5.225	6.033	6.871	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.061	8.047	9.069	ns
		GCLK PLL	t_{CO}	5.180	5.980	6.811	ns

Table 1–74. EP3C40 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V PCI	—	GCLK	t_{CO}	5.250	5.740	6.257	ns
		GCLK PLL	t_{CO}	3.370	3.672	3.999	ns
3.0-V PCI–X	—	GCLK	t_{CO}	5.250	5.740	6.257	ns
		GCLK PLL	t_{CO}	3.370	3.672	3.999	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.600	6.114	6.652	ns
		GCLK PLL	t_{CO}	3.710	4.034	4.400	ns
	8 mA	GCLK	t_{CO}	5.600	6.114	6.652	ns
		GCLK PLL	t_{CO}	3.710	4.034	4.400	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.600	5.940	6.302	ns
		GCLK PLL	t_{CO}	3.710	3.860	4.050	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.314	5.821	6.353	ns
		GCLK PLL	t_{CO}	3.424	3.741	4.101	ns
	8 mA	GCLK	t_{CO}	5.057	5.554	6.076	ns
		GCLK PLL	t_{CO}	3.167	3.474	3.824	ns
	12 mA	GCLK	t_{CO}	4.968	5.459	5.974	ns
		GCLK PLL	t_{CO}	3.078	3.379	3.722	ns
	16 mA	GCLK	t_{CO}	4.922	5.408	5.919	ns
		GCLK PLL	t_{CO}	3.032	3.328	3.667	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.055	5.552	6.074	ns
		GCLK PLL	t_{CO}	3.165	3.472	3.822	ns
	8 mA	GCLK	t_{CO}	4.922	5.409	5.922	ns
		GCLK PLL	t_{CO}	3.032	3.329	3.670	ns
	12 mA	GCLK	t_{CO}	4.887	5.373	5.883	ns
		GCLK PLL	t_{CO}	2.997	3.293	3.631	ns
	16 mA	GCLK	t_{CO}	4.872	5.357	5.866	ns
		GCLK PLL	t_{CO}	2.982	3.277	3.614	ns
2.5V	4 mA	GCLK	t_{CO}	5.412	5.935	6.483	ns
		GCLK PLL	t_{CO}	3.522	3.855	4.231	ns
	8 mA	GCLK	t_{CO}	5.177	5.691	6.229	ns
		GCLK PLL	t_{CO}	3.287	3.611	3.977	ns
	12 mA	GCLK	t_{CO}	5.078	5.586	6.119	ns
		GCLK PLL	t_{CO}	3.188	3.506	3.867	ns
	16 mA	GCLK	t_{CO}	5.037	5.544	6.076	ns
		GCLK PLL	t_{CO}	3.147	3.464	3.824	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{CO}	6.506	7.171	7.863	ns
		GCLK PLL	t_{CO}	4.616	5.091	5.611	ns
	4 mA	GCLK	t_{CO}	5.993	6.643	7.319	ns
		GCLK PLL	t_{CO}	4.103	4.563	5.067	ns
	6 mA	GCLK	t_{CO}	5.772	6.389	7.032	ns
		GCLK PLL	t_{CO}	3.882	4.309	4.780	ns
	8 mA	GCLK	t_{CO}	5.671	6.275	6.906	ns
		GCLK PLL	t_{CO}	3.781	4.195	4.654	ns
	10 mA	GCLK	t_{CO}	5.620	6.226	6.860	ns
		GCLK PLL	t_{CO}	3.730	4.146	4.608	ns
	12 mA	GCLK	t_{CO}	5.565	6.163	6.787	ns
		GCLK PLL	t_{CO}	3.675	4.083	4.535	ns
	16 mA	GCLK	t_{CO}	5.522	6.116	6.738	ns
		GCLK PLL	t_{CO}	3.632	4.036	4.486	ns
1.5V	2 mA	GCLK	t_{CO}	6.900	7.738	8.608	ns
		GCLK PLL	t_{CO}	5.010	5.658	6.356	ns
	4 mA	GCLK	t_{CO}	6.444	7.194	7.975	ns
		GCLK PLL	t_{CO}	4.554	5.114	5.723	ns
	6 mA	GCLK	t_{CO}	6.277	7.016	7.784	ns
		GCLK PLL	t_{CO}	4.387	4.936	5.532	ns
	8 mA	GCLK	t_{CO}	6.201	6.923	7.674	ns
		GCLK PLL	t_{CO}	4.311	4.843	5.422	ns
	10 mA	GCLK	t_{CO}	6.141	6.860	7.608	ns
		GCLK PLL	t_{CO}	4.251	4.780	5.356	ns
	12 mA	GCLK	t_{CO}	6.107	6.817	7.557	ns
		GCLK PLL	t_{CO}	4.217	4.737	5.305	ns
	16 mA	GCLK	t_{CO}	6.010	6.709	7.438	ns
		GCLK PLL	t_{CO}	4.120	4.629	5.186	ns
1.2V	2 mA	GCLK	t_{CO}	8.088	9.278	10.504	ns
		GCLK PLL	t_{CO}	6.198	7.198	8.252	ns
	4 mA	GCLK	t_{CO}	7.653	8.764	9.912	ns
		GCLK PLL	t_{CO}	5.763	6.684	7.660	ns
	6 mA	GCLK	t_{CO}	7.525	8.610	9.733	ns
		GCLK PLL	t_{CO}	5.635	6.530	7.481	ns
	8 mA	GCLK	t_{CO}	7.453	8.528	9.638	ns
		GCLK PLL	t_{CO}	5.563	6.448	7.386	ns
	10 mA	GCLK	t_{CO}	7.322	8.365	9.443	ns
		GCLK PLL	t_{CO}	5.432	6.285	7.191	ns

Table 1–75. EP3C40 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.010	5.519	6.062	ns
		GCLK PLL	t_{CO}	3.116	3.439	3.791	ns
	12 mA	GCLK	t_{CO}	4.991	5.500	6.041	ns
		GCLK PLL	t_{CO}	3.097	3.420	3.770	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	4.936	5.443	5.981	ns
		GCLK PLL	t_{CO}	3.042	3.363	3.710	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.444	6.034	6.657	ns
		GCLK PLL	t_{CO}	3.550	3.954	4.386	ns
	10 mA	GCLK	t_{CO}	5.431	6.016	6.636	ns
		GCLK PLL	t_{CO}	3.537	3.936	4.365	ns
	12 mA	GCLK	t_{CO}	5.418	6.001	6.618	ns
		GCLK PLL	t_{CO}	3.524	3.921	4.347	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.388	5.972	6.590	ns
		GCLK PLL	t_{CO}	3.494	3.892	4.319	ns
	16 mA	GCLK	t_{CO}	5.380	5.966	6.585	ns
		GCLK PLL	t_{CO}	3.486	3.886	4.314	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.408	5.988	6.602	ns
		GCLK PLL	t_{CO}	3.514	3.908	4.331	ns
	10 mA	GCLK	t_{CO}	5.403	5.984	6.599	ns
		GCLK PLL	t_{CO}	3.509	3.904	4.328	ns
	12 mA	GCLK	t_{CO}	5.396	5.977	6.592	ns
		GCLK PLL	t_{CO}	3.502	3.897	4.321	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.334	5.911	6.521	ns
		GCLK PLL	t_{CO}	3.440	3.831	4.250	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	5.923	6.609	7.331	ns
		GCLK PLL	t_{CO}	4.029	4.529	5.060	ns
	10 mA	GCLK	t_{CO}	5.935	6.621	7.342	ns
		GCLK PLL	t_{CO}	4.041	4.541	5.071	ns
	12 mA	GCLK	t_{CO}	5.923	6.612	7.337	ns
		GCLK PLL	t_{CO}	4.029	4.532	5.066	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.868	6.555	7.276	ns
		GCLK PLL	t_{CO}	3.974	4.475	5.005	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.160	8.181	9.244	ns
		GCLK PLL	t_{CO}	5.266	6.101	6.973	ns
	10 mA	GCLK	t_{CO}	7.099	8.096	9.135	ns
		GCLK PLL	t_{CO}	5.205	6.016	6.864	ns
3.0-V PCI	—	GCLK	t_{CO}	5.214	5.700	6.209	ns
		GCLK PLL	t_{CO}	3.324	3.620	3.957	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.214	5.700	6.209	ns
		GCLK PLL	t_{CO}	3.324	3.620	3.957	ns

Table 1–76. EP3C40 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.748	0.806	0.844	ns
			t_H	-0.470	-0.490	-0.491	ns
	—	GCLK PLL	t_{SU}	2.628	2.872	3.101	ns
			t_H	-2.350	-2.556	-2.748	ns
LVDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.370	5.883	6.423	ns
		GCLK PLL	t_{CO}	3.490	3.817	4.166	ns
RSDS_E_1R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns
RSDS_E_3R	—	GCLK	t_{CO}	4.989	5.504	6.045	ns
		GCLK PLL	t_{CO}	3.109	3.438	3.788	ns

Table 1–77. EP3C40 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	-6	-7	-8	Units
LVDS	—	GCLK	t_{SU}	0.772	0.836	0.879	ns
			t_H	-0.494	-0.521	-0.525	ns
			t_{CO}	4.170	4.579	5.015	ns
	—	GCLK PLL	t_{SU}	2.652	2.902	3.136	ns
			t_H	-2.374	-2.587	-2.782	ns
			t_{CO}	2.290	2.513	2.758	ns
mini-LVDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns
PPDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns
RSDS	—	GCLK	t_{CO}	4.170	4.579	5.015	ns
		GCLK PLL	t_{CO}	2.290	2.513	2.758	ns

EP3C55 I/O Timing Parameters

Table 1–78 through Table 1–83 show the maximum I/O timing parameters for EP3C55 devices.

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	tsu	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	12 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	16 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	8 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	12 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
	16 mA	GCLK	t_{SU}	0.816	0.816	0.797	ns
			t_H	–0.536	–0.498	–0.443	ns
		GCLK PLL	t_{SU}	2.750	2.946	3.114	ns
			t_H	–2.470	–2.628	–2.760	ns
2.5V	4 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	8 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	12 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns
	16 mA	GCLK	t_{SU}	0.759	0.771	0.765	ns
			t_H	–0.479	–0.454	–0.412	ns
		GCLK PLL	t_{SU}	2.693	2.901	3.082	ns
			t_H	–2.413	–2.584	–2.729	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	4 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	6 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	8 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	10 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	12 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns
	16 mA	GCLK	t_{SU}	0.694	0.732	0.752	ns
			t_H	–0.416	–0.416	–0.398	ns
		GCLK PLL	t_{SU}	2.628	2.863	3.069	ns
			t_H	–2.350	–2.547	–2.715	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	2 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	4 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	6 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	8 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	10 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	12 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns
	16 mA	GCLK	t_{SU}	0.763	0.824	0.869	ns
			t_H	–0.483	–0.506	–0.513	ns
		GCLK PLL	t_{SU}	2.697	2.955	3.186	ns
			t_H	–2.417	–2.637	–2.830	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	4 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	6 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	8 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	10 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
	12 mA	GCLK	t_{SU}	0.915	1.004	1.075	ns
			t_H	–0.633	–0.682	–0.715	ns
		GCLK PLL	t_{SU}	2.849	3.135	3.392	ns
			t_H	–2.567	–2.813	–3.032	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns
	12 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.747	0.789	0.812	ns
			t_H	–0.467	–0.472	–0.457	ns
		GCLK PLL	t_{SU}	2.683	2.917	3.137	ns
			t_H	–2.403	–2.600	–2.782	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	10 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	16 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	10 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
	12 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.808	0.878	0.930	ns
			t_H	–0.528	–0.559	–0.573	ns
		GCLK PLL	t_{SU}	2.744	3.009	3.248	ns
			t_H	–2.464	–2.690	–2.891	ns

Table 1–78. EP3C55 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
	10 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
	12 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.764	0.838	0.896	ns
			t_H	–0.484	–0.520	–0.540	ns
		GCLK PLL	t_{SU}	2.700	2.969	3.214	ns
			t_H	–2.420	–2.651	–2.858	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
	10 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
	12 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.896	0.997	1.080	ns
			t_H	–0.614	–0.675	–0.720	ns
		GCLK PLL	t_{SU}	2.832	3.128	3.398	ns
			t_H	–2.550	–2.806	–3.038	ns
3.0-V PCI	—	GCLK	t_{SU}	0.812	0.812	0.792	ns
			t_H	–0.532	–0.494	–0.438	ns
	—	GCLK PLL	t_{SU}	2.746	2.942	3.109	ns
			t_H	–2.466	–2.624	–2.755	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.812	0.812	0.792	ns
			t_H	–0.532	–0.494	–0.438	ns
	—	GCLK PLL	t_{SU}	2.746	2.942	3.109	ns
			t_H	–2.466	–2.624	–2.755	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	12 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	16 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	8 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	12 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
	16 mA	GCLK	t_{SU}	0.840	0.849	0.832	ns
			t_H	–0.560	–0.531	–0.477	ns
		GCLK PLL	t_{SU}	2.794	2.993	3.161	ns
			t_H	–2.514	–2.675	–2.806	ns
2.5V	4 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	8 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	12 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns
	16 mA	GCLK	t_{SU}	0.783	0.805	0.803	ns
			t_H	–0.503	–0.488	–0.449	ns
		GCLK PLL	t_{SU}	2.737	2.949	3.132	ns
			t_H	–2.457	–2.632	–2.778	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	2 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	4 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	6 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	8 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	10 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	12 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
	16 mA	GCLK	t_{SU}	0.719	0.766	0.789	ns
			t_H	–0.441	–0.450	–0.434	ns
		GCLK PLL	t_{SU}	2.673	2.910	3.118	ns
			t_H	–2.395	–2.594	–2.763	ns
1.5V	2 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	4 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	6 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	8 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	10 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	12 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
	16 mA	GCLK	t_{SU}	0.788	0.859	0.907	ns
			t_H	–0.508	–0.541	–0.551	ns
		GCLK PLL	t_{SU}	2.742	3.003	3.236	ns
			t_H	–2.462	–2.685	–2.880	ns
1.2V	2 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	4 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	6 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	8 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns
	10 mA	GCLK	t_{SU}	0.941	1.039	1.114	ns
			t_H	–0.659	–0.717	–0.753	ns
		GCLK PLL	t_{SU}	2.895	3.183	3.443	ns
			t_H	–2.613	–2.861	–3.082	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
	12 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.773	0.824	0.851	ns
			t_H	–0.493	–0.506	–0.495	ns
		GCLK PLL	t_{SU}	2.722	2.960	3.177	ns
			t_H	–2.442	–2.642	–2.821	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	10 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	16 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
	10 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns

Table 1–79. EP3C55 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8-V HSTL Class I	12 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.835	0.913	0.968	ns
			t_H	–0.555	–0.594	–0.610	ns
		GCLK PLL	t_{SU}	2.784	3.049	3.294	ns
			t_H	–2.504	–2.730	–2.936	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
	10 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
	12 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.790	0.872	0.931	ns
			t_H	–0.510	–0.554	–0.574	ns
		GCLK PLL	t_{SU}	2.739	3.008	3.257	ns
			t_H	–2.459	–2.690	–2.900	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.921	1.030	1.116	ns
			t_H	–0.639	–0.708	–0.756	ns
		GCLK PLL	t_{SU}	2.870	3.166	3.442	ns
			t_H	–2.588	–2.844	–3.082	ns
	10 mA	GCLK	t_{SU}	0.921	1.030	1.116	ns
			t_H	–0.639	–0.708	–0.756	ns
		GCLK PLL	t_{SU}	2.870	3.166	3.442	ns
			t_H	–2.588	–2.844	–3.082	ns
3.0-V PCI	—	GCLK	t_{SU}	0.836	0.845	0.828	ns
			t_H	–0.556	–0.527	–0.473	ns
	—	GCLK PLL	t_{SU}	2.790	2.989	3.157	ns
			t_H	–2.510	–2.671	–2.802	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.836	0.845	0.828	ns
			t_H	–0.556	–0.527	–0.473	ns
	—	GCLK PLL	t_{SU}	2.790	2.989	3.157	ns
			t_H	–2.510	–2.671	–2.802	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.764	6.293	6.845	ns
		GCLK PLL	t_{CO}	3.830	4.163	4.528	ns
	8 mA	GCLK	t_{CO}	5.764	6.293	6.845	ns
		GCLK PLL	t_{CO}	3.830	4.163	4.528	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.723	6.074	6.447	ns
		GCLK PLL	t_{CO}	3.789	3.944	4.130	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.474	5.996	6.543	ns
		GCLK PLL	t_{CO}	3.540	3.866	4.226	ns
	8 mA	GCLK	t_{CO}	5.203	5.712	6.244	ns
		GCLK PLL	t_{CO}	3.269	3.582	3.927	ns
	12 mA	GCLK	t_{CO}	5.106	5.611	6.140	ns
		GCLK PLL	t_{CO}	3.172	3.481	3.823	ns
	16 mA	GCLK	t_{CO}	5.059	5.559	6.082	ns
		GCLK PLL	t_{CO}	3.125	3.429	3.765	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.201	5.709	6.241	ns
		GCLK PLL	t_{CO}	3.267	3.579	3.924	ns
	8 mA	GCLK	t_{CO}	5.060	5.561	6.086	ns
		GCLK PLL	t_{CO}	3.126	3.431	3.769	ns
	12 mA	GCLK	t_{CO}	5.023	5.521	6.043	ns
		GCLK PLL	t_{CO}	3.089	3.391	3.726	ns
	16 mA	GCLK	t_{CO}	5.007	5.506	6.028	ns
		GCLK PLL	t_{CO}	3.073	3.376	3.711	ns
2.5V	4 mA	GCLK	t_{CO}	5.532	6.082	6.657	ns
		GCLK PLL	t_{CO}	3.598	3.952	4.340	ns
	8 mA	GCLK	t_{CO}	5.289	5.829	6.393	ns
		GCLK PLL	t_{CO}	3.355	3.699	4.076	ns
	12 mA	GCLK	t_{CO}	5.191	5.723	6.280	ns
		GCLK PLL	t_{CO}	3.257	3.593	3.963	ns
	16 mA	GCLK	t_{CO}	5.152	5.683	6.239	ns
		GCLK PLL	t_{CO}	3.218	3.553	3.922	ns
1.8V	2 mA	GCLK	t_{CO}	6.643	7.335	8.056	ns
		GCLK PLL	t_{CO}	4.709	5.204	5.738	ns
	4 mA	GCLK	t_{CO}	6.116	6.790	7.492	ns
		GCLK PLL	t_{CO}	4.182	4.659	5.174	ns
	6 mA	GCLK	t_{CO}	5.891	6.532	7.200	ns
		GCLK PLL	t_{CO}	3.957	4.401	4.882	ns
	8 mA	GCLK	t_{CO}	5.788	6.415	7.071	ns
		GCLK PLL	t_{CO}	3.854	4.284	4.753	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{CO}	5.736	6.367	7.025	ns
		GCLK PLL	t_{CO}	3.802	4.236	4.707	ns
	12 mA	GCLK	t_{CO}	5.679	6.300	6.950	ns
		GCLK PLL	t_{CO}	3.745	4.169	4.632	ns
	16 mA	GCLK	t_{CO}	5.625	6.241	6.885	ns
		GCLK PLL	t_{CO}	3.691	4.110	4.567	ns
1.5V	2 mA	GCLK	t_{CO}	7.031	7.897	8.795	ns
		GCLK PLL	t_{CO}	5.097	5.766	6.477	ns
	4 mA	GCLK	t_{CO}	6.556	7.336	8.147	ns
		GCLK PLL	t_{CO}	4.622	5.205	5.829	ns
	6 mA	GCLK	t_{CO}	6.386	7.153	7.950	ns
		GCLK PLL	t_{CO}	4.452	5.022	5.632	ns
	8 mA	GCLK	t_{CO}	6.298	7.040	7.812	ns
		GCLK PLL	t_{CO}	4.364	4.909	5.494	ns
	10 mA	GCLK	t_{CO}	6.239	6.980	7.751	ns
		GCLK PLL	t_{CO}	4.305	4.849	5.433	ns
	12 mA	GCLK	t_{CO}	6.206	6.939	7.701	ns
		GCLK PLL	t_{CO}	4.272	4.808	5.383	ns
	16 mA	GCLK	t_{CO}	6.092	6.797	7.531	ns
		GCLK PLL	t_{CO}	4.158	4.666	5.213	ns
1.2V	2 mA	GCLK	t_{CO}	8.204	9.425	10.684	ns
		GCLK PLL	t_{CO}	6.270	7.294	8.366	ns
	4 mA	GCLK	t_{CO}	7.759	8.899	10.077	ns
		GCLK PLL	t_{CO}	5.825	6.768	7.759	ns
	6 mA	GCLK	t_{CO}	7.610	8.718	9.863	ns
		GCLK PLL	t_{CO}	5.676	6.587	7.545	ns
	8 mA	GCLK	t_{CO}	7.541	8.638	9.773	ns
		GCLK PLL	t_{CO}	5.607	6.507	7.455	ns
	10 mA	GCLK	t_{CO}	7.405	8.456	9.542	ns
		GCLK PLL	t_{CO}	5.471	6.325	7.224	ns
	12 mA	GCLK	t_{CO}	7.377	8.430	9.520	ns
		GCLK PLL	t_{CO}	5.443	6.299	7.202	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.148	5.672	6.224	ns
		GCLK PLL	t_{CO}	3.212	3.544	3.899	ns
	12 mA	GCLK	t_{CO}	5.126	5.648	6.201	ns
		GCLK PLL	t_{CO}	3.190	3.520	3.876	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.066	5.586	6.135	ns
		GCLK PLL	t_{CO}	3.130	3.458	3.810	ns

Table 1–80. EP3C55 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.582	6.185	6.816	ns
		GCLK PLL	t_{CO}	3.646	4.054	4.498	ns
	10 mA	GCLK	t_{CO}	5.557	6.154	6.779	ns
		GCLK PLL	t_{CO}	3.621	4.023	4.461	ns
	12 mA	GCLK	t_{CO}	5.545	6.140	6.762	ns
		GCLK PLL	t_{CO}	3.609	4.009	4.444	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.516	6.111	6.734	ns
		GCLK PLL	t_{CO}	3.580	3.980	4.416	ns
	16 mA	GCLK	t_{CO}	5.503	6.098	6.720	ns
		GCLK PLL	t_{CO}	3.567	3.967	4.402	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.544	6.137	6.758	ns
		GCLK PLL	t_{CO}	3.608	4.006	4.440	ns
	10 mA	GCLK	t_{CO}	5.533	6.130	6.754	ns
		GCLK PLL	t_{CO}	3.597	3.999	4.436	ns
	12 mA	GCLK	t_{CO}	5.524	6.116	6.734	ns
		GCLK PLL	t_{CO}	3.588	3.985	4.416	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.459	6.050	6.668	ns
		GCLK PLL	t_{CO}	3.523	3.919	4.350	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.058	6.758	7.489	ns
		GCLK PLL	t_{CO}	4.122	4.627	5.171	ns
	10 mA	GCLK	t_{CO}	6.061	6.758	7.484	ns
		GCLK PLL	t_{CO}	4.125	4.627	5.166	ns
	12 mA	GCLK	t_{CO}	6.049	6.750	7.480	ns
		GCLK PLL	t_{CO}	4.113	4.619	5.162	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.987	6.682	7.405	ns
		GCLK PLL	t_{CO}	4.051	4.551	5.087	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.271	8.296	9.356	ns
		GCLK PLL	t_{CO}	5.335	6.165	7.038	ns
	10 mA	GCLK	t_{CO}	7.209	8.207	9.240	ns
		GCLK PLL	t_{CO}	5.273	6.076	6.922	ns
	12 mA	GCLK	t_{CO}	7.211	8.213	9.249	ns
		GCLK PLL	t_{CO}	5.275	6.082	6.931	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.166	8.160	9.189	ns
		GCLK PLL	t_{CO}	5.230	6.029	6.871	ns
3.0-V PCI	—	GCLK	t_{CO}	5.354	5.853	6.377	ns
		GCLK PLL	t_{CO}	3.420	3.723	4.060	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.354	5.853	6.377	ns
		GCLK PLL	t_{CO}	3.420	3.723	4.060	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.713	6.231	6.782	ns
		GCLK PLL	t_{CO}	3.759	4.087	4.453	ns
	8 mA	GCLK	t_{CO}	5.713	6.231	6.782	ns
		GCLK PLL	t_{CO}	3.759	4.087	4.453	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.713	6.057	6.432	ns
		GCLK PLL	t_{CO}	3.759	3.913	4.103	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.427	5.938	6.483	ns
		GCLK PLL	t_{CO}	3.473	3.794	4.154	ns
	8 mA	GCLK	t_{CO}	5.170	5.671	6.206	ns
		GCLK PLL	t_{CO}	3.216	3.527	3.877	ns
	12 mA	GCLK	t_{CO}	5.081	5.576	6.104	ns
		GCLK PLL	t_{CO}	3.127	3.432	3.775	ns
	16 mA	GCLK	t_{CO}	5.035	5.525	6.049	ns
		GCLK PLL	t_{CO}	3.081	3.381	3.720	ns
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.168	5.669	6.204	ns
		GCLK PLL	t_{CO}	3.214	3.525	3.875	ns
	8 mA	GCLK	t_{CO}	5.035	5.526	6.052	ns
		GCLK PLL	t_{CO}	3.081	3.382	3.723	ns
	12 mA	GCLK	t_{CO}	5.000	5.490	6.013	ns
		GCLK PLL	t_{CO}	3.046	3.346	3.684	ns
	16 mA	GCLK	t_{CO}	4.985	5.474	5.996	ns
		GCLK PLL	t_{CO}	3.031	3.330	3.667	ns
2.5V	4 mA	GCLK	t_{CO}	5.525	6.052	6.613	ns
		GCLK PLL	t_{CO}	3.571	3.908	4.284	ns
	8 mA	GCLK	t_{CO}	5.290	5.808	6.359	ns
		GCLK PLL	t_{CO}	3.336	3.664	4.030	ns
	12 mA	GCLK	t_{CO}	5.191	5.703	6.249	ns
		GCLK PLL	t_{CO}	3.237	3.559	3.920	ns
	16 mA	GCLK	t_{CO}	5.150	5.661	6.206	ns
		GCLK PLL	t_{CO}	3.196	3.517	3.877	ns
1.8V	2 mA	GCLK	t_{CO}	6.619	7.288	7.993	ns
		GCLK PLL	t_{CO}	4.665	5.144	5.664	ns
	4 mA	GCLK	t_{CO}	6.106	6.760	7.449	ns
		GCLK PLL	t_{CO}	4.152	4.616	5.120	ns
	6 mA	GCLK	t_{CO}	5.885	6.506	7.162	ns
		GCLK PLL	t_{CO}	3.931	4.362	4.833	ns
	8 mA	GCLK	t_{CO}	5.784	6.392	7.036	ns
		GCLK PLL	t_{CO}	3.830	4.248	4.707	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{CO}	5.733	6.343	6.990	ns
		GCLK PLL	t_{CO}	3.779	4.199	4.661	ns
	12 mA	GCLK	t_{CO}	5.678	6.280	6.917	ns
		GCLK PLL	t_{CO}	3.724	4.136	4.588	ns
	16 mA	GCLK	t_{CO}	5.635	6.233	6.868	ns
		GCLK PLL	t_{CO}	3.681	4.089	4.539	ns
1.5V	2 mA	GCLK	t_{CO}	7.013	7.855	8.738	ns
		GCLK PLL	t_{CO}	5.059	5.711	6.409	ns
	4 mA	GCLK	t_{CO}	6.557	7.311	8.105	ns
		GCLK PLL	t_{CO}	4.603	5.167	5.776	ns
	6 mA	GCLK	t_{CO}	6.390	7.133	7.914	ns
		GCLK PLL	t_{CO}	4.436	4.989	5.585	ns
	8 mA	GCLK	t_{CO}	6.314	7.040	7.804	ns
		GCLK PLL	t_{CO}	4.360	4.896	5.475	ns
	10mA	GCLK	t_{CO}	6.254	6.977	7.738	ns
		GCLK PLL	t_{CO}	4.300	4.833	5.409	ns
	12 mA	GCLK	t_{CO}	6.220	6.934	7.687	ns
		GCLK PLL	t_{CO}	4.266	4.790	5.358	ns
	16 mA	GCLK	t_{CO}	6.123	6.826	7.568	ns
		GCLK PLL	t_{CO}	4.169	4.682	5.239	ns
1.2V	2 mA	GCLK	t_{CO}	8.201	9.395	10.634	ns
		GCLK PLL	t_{CO}	6.247	7.251	8.305	ns
	4 mA	GCLK	t_{CO}	7.766	8.881	10.042	ns
		GCLK PLL	t_{CO}	5.812	6.737	7.713	ns
	6 mA	GCLK	t_{CO}	7.638	8.727	9.863	ns
		GCLK PLL	t_{CO}	5.684	6.583	7.534	ns
	8 mA	GCLK	t_{CO}	7.566	8.645	9.768	ns
		GCLK PLL	t_{CO}	5.612	6.501	7.439	ns
	10 mA	GCLK	t_{CO}	7.435	8.482	9.573	ns
		GCLK PLL	t_{CO}	5.481	6.338	7.244	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.119	5.635	6.187	ns
		GCLK PLL	t_{CO}	3.170	3.499	3.861	ns
	12 mA	GCLK	t_{CO}	5.100	5.616	6.166	ns
		GCLK PLL	t_{CO}	3.151	3.480	3.840	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.045	5.559	6.106	ns
		GCLK PLL	t_{CO}	3.096	3.423	3.780	ns

Table 1–81. EP3C55 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 3)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.553	6.150	6.782	ns
		GCLK PLL	t_{CO}	3.604	4.014	4.456	ns
	10 mA	GCLK	t_{CO}	5.540	6.132	6.761	ns
		GCLK PLL	t_{CO}	3.591	3.996	4.435	ns
	12 mA	GCLK	t_{CO}	5.527	6.117	6.743	ns
		GCLK PLL	t_{CO}	3.578	3.981	4.417	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.497	6.088	6.715	ns
		GCLK PLL	t_{CO}	3.548	3.952	4.389	ns
	16 mA	GCLK	t_{CO}	5.489	6.082	6.710	ns
		GCLK PLL	t_{CO}	3.540	3.946	4.384	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.517	6.104	6.727	ns
		GCLK PLL	t_{CO}	3.568	3.968	4.401	ns
	10 mA	GCLK	t_{CO}	5.512	6.100	6.724	ns
		GCLK PLL	t_{CO}	3.563	3.964	4.398	ns
	12 mA	GCLK	t_{CO}	5.505	6.093	6.717	ns
		GCLK PLL	t_{CO}	3.556	3.957	4.391	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.443	6.027	6.646	ns
		GCLK PLL	t_{CO}	3.494	3.891	4.320	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.032	6.725	7.456	ns
		GCLK PLL	t_{CO}	4.083	4.589	5.130	ns
	10 mA	GCLK	t_{CO}	6.044	6.737	7.467	ns
		GCLK PLL	t_{CO}	4.095	4.601	5.141	ns
	12 mA	GCLK	t_{CO}	6.032	6.728	7.462	ns
		GCLK PLL	t_{CO}	4.083	4.592	5.136	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	5.977	6.671	7.401	ns
		GCLK PLL	t_{CO}	4.028	4.535	5.075	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.269	8.297	9.369	ns
		GCLK PLL	t_{CO}	5.320	6.161	7.043	ns
	10 mA	GCLK	t_{CO}	7.208	8.212	9.260	ns
		GCLK PLL	t_{CO}	5.259	6.076	6.934	ns
3.0-V PCI	—	GCLK	t_{CO}	5.327	5.817	6.339	ns
		GCLK PLL	t_{CO}	3.373	3.673	4.010	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.327	5.817	6.339	ns
		GCLK PLL	t_{CO}	3.373	3.673	4.010	ns

Table 1–82. EP3C55 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.644	0.695	0.720	ns
			t_H	–0.366	–0.379	–0.367	ns
	—	GCLK PLL	t_{SU}	2.579	2.821	3.042	ns
			t_H	–2.301	–2.505	–2.689	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.474	5.994	6.547	ns
		GCLK PLL	t_{CO}	3.539	3.868	4.225	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.093	5.615	6.169	ns
		GCLK PLL	t_{CO}	3.158	3.489	3.847	ns

Table 1–83. EP3C55 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.670	0.725	0.758	ns
			t_H	–0.392	–0.410	–0.404	ns
			t_{CO}	4.278	4.693	5.139	ns
	—	GCLK PLL	t_{SU}	2.607	2.852	3.081	ns
			t_H	–2.329	–2.537	–2.727	ns
			t_{CO}	2.336	2.562	2.813	ns
mini-LVDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns
PPDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns
RSDS	—	GCLK	t_{CO}	4.278	4.693	5.139	ns
		GCLK PLL	t_{CO}	2.336	2.562	2.813	ns

EP3C80 I/O Timing Parameters

Table 1–84 through Table 1–89 show the maximum I/O timing parameters for EP3C80 devices.

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	12 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	16 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	8 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
	16 mA	GCLK	t_{SU}	0.721	0.713	0.679	ns
			t_H	–0.441	–0.395	–0.325	ns
		GCLK PLL	t_{SU}	2.774	2.968	3.138	ns
			t_H	–2.494	–2.650	–2.784	ns
2.5V	4 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	8 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	12 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
	16 mA	GCLK	t_{SU}	0.664	0.668	0.647	ns
			t_H	–0.384	–0.351	–0.294	ns
		GCLK PLL	t_{SU}	2.717	2.923	3.106	ns
			t_H	–2.437	–2.606	–2.753	ns
1.8V	2 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	4 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	6 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	8 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	12 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
	16 mA	GCLK	t_{SU}	0.599	0.629	0.634	ns
			t_H	–0.321	–0.313	–0.280	ns
		GCLK PLL	t_{SU}	2.652	2.885	3.093	ns
			t_H	–2.374	–2.569	–2.739	ns
1.5V	2 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	4 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	6 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	8 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	10 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	12 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns
	16 mA	GCLK	t_{SU}	0.668	0.721	0.751	ns
			t_H	–0.388	–0.403	–0.395	ns
		GCLK PLL	t_{SU}	2.721	2.977	3.210	ns
			t_H	–2.441	–2.659	–2.854	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	4 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	6 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	8 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	10 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
	12 mA	GCLK	t_{SU}	0.820	0.901	0.957	ns
			t_H	–0.538	–0.579	–0.597	ns
		GCLK PLL	t_{SU}	2.873	3.157	3.416	ns
			t_H	–2.591	–2.835	–3.056	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns
	12 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.654	0.686	0.694	ns
			t_H	–0.374	–0.369	–0.339	ns
		GCLK PLL	t_{SU}	2.705	2.940	3.154	ns
			t_H	–2.425	–2.623	–2.799	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	10 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	16 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	10 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
	12 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.715	0.775	0.809	ns
			t_H	–0.435	–0.456	–0.452	ns
		GCLK PLL	t_{SU}	2.766	3.029	3.269	ns
			t_H	–2.486	–2.710	–2.912	ns

Table 1–84. EP3C80 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
	10 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
	12 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.671	0.735	0.775	ns
			t_H	–0.391	–0.417	–0.419	ns
		GCLK PLL	t_{SU}	2.722	2.989	3.235	ns
			t_H	–2.442	–2.671	–2.879	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
	10 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
	12 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.803	0.894	0.959	ns
			t_H	–0.521	–0.572	–0.599	ns
		GCLK PLL	t_{SU}	2.854	3.148	3.419	ns
			t_H	–2.572	–2.826	–3.059	ns
3.0-V PCI	—	GCLK	t_{SU}	0.717	0.709	0.674	ns
			t_H	–0.437	–0.391	–0.320	ns
	—	GCLK PLL	t_{SU}	2.770	2.964	3.133	ns
			t_H	–2.490	–2.646	–2.779	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.717	0.709	0.674	ns
			t_H	–0.437	–0.391	–0.320	ns
	—	GCLK PLL	t_{SU}	2.770	2.964	3.133	ns
			t_H	–2.490	–2.646	–2.779	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	12 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	16 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	8 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	12 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
	16 mA	GCLK	t_{SU}	0.733	0.731	0.700	ns
			t_H	–0.453	–0.413	–0.345	ns
		GCLK PLL	t_{SU}	2.804	3.006	3.164	ns
			t_H	–2.524	–2.688	–2.809	ns
2.5V	4 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	8 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	12 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
	16 mA	GCLK	t_{SU}	0.676	0.687	0.671	ns
			t_H	–0.396	–0.370	–0.317	ns
		GCLK PLL	t_{SU}	2.747	2.962	3.135	ns
			t_H	–2.467	–2.645	–2.781	ns
1.8V	2 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	4 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	6 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	8 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.8V	10 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	12 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
	16 mA	GCLK	t_{SU}	0.612	0.648	0.657	ns
			t_H	–0.334	–0.332	–0.302	ns
		GCLK PLL	t_{SU}	2.683	2.923	3.121	ns
			t_H	–2.405	–2.607	–2.766	ns
1.5V	2 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.–472	–2.698	–2.883	ns
	4 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	6 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	8 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	10 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	12 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns
	16 mA	GCLK	t_{SU}	0.681	0.741	0.775	ns
			t_H	–0.401	–0.423	–0.419	ns
		GCLK PLL	t_{SU}	2.752	3.016	3.239	ns
			t_H	–2.472	–2.698	–2.883	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.2V	2 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	4 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	6 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	8 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
	10 mA	GCLK	t_{SU}	0.834	0.921	0.982	ns
			t_H	–0.552	–0.599	–0.621	ns
		GCLK PLL	t_{SU}	2.905	3.196	3.446	ns
			t_H	–2.623	–2.874	–3.085	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
	12 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.666	0.706	0.719	ns
			t_H	–0.386	–0.388	–0.363	ns
		GCLK PLL	t_{SU}	2.730	2.982	3.199	ns
			t_H	–2.450	–2.664	–2.843	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	10 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
SSTL-18 Class I	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	16 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	10 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
	12 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.728	0.795	0.836	ns
			t_H	–0.448	–0.476	–0.478	ns
		GCLK PLL	t_{SU}	2.792	3.071	3.316	ns
			t_H	–2.512	–2.752	–2.958	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
	10 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
	12 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns

Table 1–85. EP3C80 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 6)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.683	0.754	0.799	ns
			t_H	–0.403	–0.436	–0.442	ns
		GCLK PLL	t_{SU}	2.747	3.030	3.279	ns
			t_H	–2.467	–2.712	–2.922	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.814	0.912	0.984	ns
			t_H	–0.532	–0.590	–0.624	ns
		GCLK PLL	t_{SU}	2.878	3.188	3.464	ns
			t_H	–2.596	–2.866	–3.104	ns
	10 mA	GCLK	t_{SU}	0.814	0.912	0.984	ns
			t_H	–0.532	–0.590	–0.624	ns
		GCLK PLL	t_{SU}	2.878	3.188	3.464	ns
			t_H	–2.596	–2.866	–3.104	ns
3.0-V PCI	—	GCLK	t_{SU}	0.729	0.727	0.696	ns
			t_H	–0.449	–0.409	–0.341	ns
	—	GCLK PLL	t_{SU}	2.800	3.002	3.160	ns
			t_H	–2.520	–2.684	–2.805	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.729	0.727	0.696	ns
			t_H	–0.449	–0.409	–0.341	ns
	—	GCLK PLL	t_{SU}	2.800	3.002	3.160	ns
			t_H	–2.520	–2.684	–2.805	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.858	6.396	6.964	ns
		GCLK PLL	t_{CO}	3.805	4.141	4.505	ns
	8 mA	GCLK	t_{CO}	5.858	6.396	6.964	ns
		GCLK PLL	t_{CO}	3.805	4.141	4.505	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.817	6.177	6.566	ns
		GCLK PLL	t_{CO}	3.764	3.922	4.107	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.568	6.099	6.662	ns
		GCLK PLL	t_{CO}	3.515	3.844	4.203	ns
	8 mA	GCLK	t_{CO}	5.297	5.815	6.363	ns
		GCLK PLL	t_{CO}	3.244	3.560	3.904	ns
	12 mA	GCLK	t_{CO}	5.200	5.714	6.259	ns
		GCLK PLL	t_{CO}	3.147	3.459	3.800	ns
	16 mA	GCLK	t_{CO}	5.153	5.662	6.201	ns
		GCLK PLL	t_{CO}	3.100	3.407	3.742	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.295	5.812	6.360	ns
		GCLK PLL	t_{CO}	3.242	3.557	3.901	ns
	8 mA	GCLK	t_{CO}	5.154	5.664	6.205	ns
		GCLK PLL	t_{CO}	3.101	3.409	3.746	ns
	12 mA	GCLK	t_{CO}	5.117	5.624	6.162	ns
		GCLK PLL	t_{CO}	3.064	3.369	3.703	ns
	16 mA	GCLK	t_{CO}	5.101	5.609	6.147	ns
		GCLK PLL	t_{CO}	3.048	3.354	3.688	ns
2.5V	4 mA	GCLK	t_{CO}	5.626	6.185	6.776	ns
		GCLK PLL	t_{CO}	3.573	3.930	4.317	ns
	8 mA	GCLK	t_{CO}	5.383	5.932	6.512	ns
		GCLK PLL	t_{CO}	3.330	3.677	4.053	ns
	12 mA	GCLK	t_{CO}	5.285	5.826	6.399	ns
		GCLK PLL	t_{CO}	3.232	3.571	3.940	ns
	16 mA	GCLK	t_{CO}	5.246	5.786	6.358	ns
		GCLK PLL	t_{CO}	3.193	3.531	3.899	ns
1.8V	2 mA	GCLK	t_{CO}	6.737	7.438	8.174	ns
		GCLK PLL	t_{CO}	4.684	5.181	5.715	ns
	4 mA	GCLK	t_{CO}	6.210	6.893	7.610	ns
		GCLK PLL	t_{CO}	4.157	4.636	5.151	ns
	6 mA	GCLK	t_{CO}	5.985	6.635	7.318	ns
		GCLK PLL	t_{CO}	3.932	4.378	4.859	ns
	8 mA	GCLK	t_{CO}	5.882	6.518	7.189	ns
		GCLK PLL	t_{CO}	3.829	4.261	4.730	ns
	10 mA	GCLK	t_{CO}	5.830	6.470	7.143	ns
		GCLK PLL	t_{CO}	3.777	4.213	4.684	ns
	12 mA	GCLK	t_{CO}	5.773	6.403	7.068	ns
		GCLK PLL	t_{CO}	3.720	4.146	4.609	ns
	16 mA	GCLK	t_{CO}	5.719	6.344	7.003	ns
		GCLK PLL	t_{CO}	3.666	4.087	4.544	ns
1.5V	2 mA	GCLK	t_{CO}	7.125	8.000	8.913	ns
		GCLK PLL	t_{CO}	5.072	5.743	6.454	ns
	4 mA	GCLK	t_{CO}	6.650	7.439	8.265	ns
		GCLK PLL	t_{CO}	4.597	5.182	5.806	ns
	6 mA	GCLK	t_{CO}	6.480	7.256	8.068	ns
		GCLK PLL	t_{CO}	4.427	4.999	5.609	ns
	8 mA	GCLK	t_{CO}	6.392	7.143	7.930	ns
		GCLK PLL	t_{CO}	4.339	4.886	5.471	ns
	10 mA	GCLK	t_{CO}	6.333	7.083	7.869	ns
		GCLK PLL	t_{CO}	4.280	4.826	5.410	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	6.300	7.042	7.819	ns
		GCLK PLL	t_{CO}	4.247	4.785	5.360	ns
	16 mA	GCLK	t_{CO}	6.186	6.900	7.649	ns
		GCLK PLL	t_{CO}	4.133	4.643	5.190	ns
1.2V	2 mA	GCLK	t_{CO}	8.298	9.528	10.802	ns
		GCLK PLL	t_{CO}	6.245	7.271	8.343	ns
	4 mA	GCLK	t_{CO}	7.853	9.002	10.195	ns
		GCLK PLL	t_{CO}	5.800	6.745	7.736	ns
	6 mA	GCLK	t_{CO}	7.704	8.821	9.981	ns
		GCLK PLL	t_{CO}	5.651	6.564	7.522	ns
	8 mA	GCLK	t_{CO}	7.635	8.741	9.891	ns
		GCLK PLL	t_{CO}	5.582	6.484	7.432	ns
	10 mA	GCLK	t_{CO}	7.499	8.559	9.660	ns
		GCLK PLL	t_{CO}	5.446	6.302	7.201	ns
	12 mA	GCLK	t_{CO}	7.471	8.533	9.638	ns
		GCLK PLL	t_{CO}	5.418	6.276	7.179	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.240	5.774	6.341	ns
		GCLK PLL	t_{CO}	3.190	3.521	3.882	ns
	12 mA	GCLK	t_{CO}	5.218	5.750	6.318	ns
		GCLK PLL	t_{CO}	3.168	3.497	3.859	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.158	5.688	6.252	ns
		GCLK PLL	t_{CO}	3.108	3.435	3.793	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.674	6.287	6.937	ns
		GCLK PLL	t_{CO}	3.624	4.034	4.477	ns
	10 mA	GCLK	t_{CO}	5.649	6.256	6.900	ns
		GCLK PLL	t_{CO}	3.599	4.003	4.440	ns
	12 mA	GCLK	t_{CO}	5.637	6.242	6.883	ns
		GCLK PLL	t_{CO}	3.587	3.989	4.423	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.608	6.213	6.855	ns
		GCLK PLL	t_{CO}	3.558	3.960	4.395	ns
	16 mA	GCLK	t_{CO}	5.595	6.200	6.841	ns
		GCLK PLL	t_{CO}	3.545	3.947	4.381	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.636	6.239	6.879	ns
		GCLK PLL	t_{CO}	3.586	3.986	4.419	ns
	10 mA	GCLK	t_{CO}	5.625	6.232	6.875	ns
		GCLK PLL	t_{CO}	3.575	3.979	4.415	ns
	12 mA	GCLK	t_{CO}	5.616	6.218	6.855	ns
		GCLK PLL	t_{CO}	3.566	3.965	4.395	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.551	6.152	6.789	ns
		GCLK PLL	t_{CO}	3.501	3.899	4.329	ns

Table 1–86. EP3C80 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.150	6.860	7.610	ns
		GCLK PLL	t_{CO}	4.100	4.607	5.150	ns
	10 mA	GCLK	t_{CO}	6.153	6.860	7.605	ns
		GCLK PLL	t_{CO}	4.103	4.607	5.145	ns
	12 mA	GCLK	t_{CO}	6.141	6.852	7.601	ns
		GCLK PLL	t_{CO}	4.091	4.599	5.141	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.079	6.784	7.526	ns
		GCLK PLL	t_{CO}	4.029	4.531	5.066	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.363	8.398	9.477	ns
		GCLK PLL	t_{CO}	5.313	6.145	7.017	ns
	10 mA	GCLK	t_{CO}	7.301	8.309	9.361	ns
		GCLK PLL	t_{CO}	5.251	6.056	6.901	ns
	12 mA	GCLK	t_{CO}	7.303	8.315	9.370	ns
		GCLK PLL	t_{CO}	5.253	6.062	6.910	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	7.258	8.262	9.310	ns
		GCLK PLL	t_{CO}	5.208	6.009	6.850	ns
3.0-V PCI	—	GCLK	t_{CO}	5.448	5.956	6.496	ns
		GCLK PLL	t_{CO}	3.395	3.701	4.037	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.448	5.956	6.496	ns
		GCLK PLL	t_{CO}	3.395	3.701	4.037	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	5.820	6.349	6.914	ns
		GCLK PLL	t_{CO}	3.749	4.074	4.450	ns
	8 mA	GCLK	t_{CO}	5.820	6.349	6.914	ns
		GCLK PLL	t_{CO}	3.749	4.074	4.450	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	5.820	6.175	6.564	ns
		GCLK PLL	t_{CO}	3.749	3.900	4.100	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	5.534	6.056	6.615	ns
		GCLK PLL	t_{CO}	3.463	3.781	4.151	ns
	8 mA	GCLK	t_{CO}	5.277	5.789	6.338	ns
		GCLK PLL	t_{CO}	3.206	3.514	3.874	ns
	12 mA	GCLK	t_{CO}	5.188	5.694	6.236	ns
		GCLK PLL	t_{CO}	3.117	3.419	3.772	ns
	16 mA	GCLK	t_{CO}	5.142	5.643	6.181	ns
		GCLK PLL	t_{CO}	3.071	3.368	3.717	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.275	5.787	6.336	ns
		GCLK PLL	t_{CO}	3.204	3.512	3.872	ns
	8 mA	GCLK	t_{CO}	5.142	5.644	6.184	ns
		GCLK PLL	t_{CO}	3.071	3.369	3.720	ns
	12 mA	GCLK	t_{CO}	5.107	5.608	6.145	ns
		GCLK PLL	t_{CO}	3.036	3.333	3.681	ns
	16 mA	GCLK	t_{CO}	5.092	5.592	6.128	ns
		GCLK PLL	t_{CO}	3.021	3.317	3.664	ns
2.5V	4 mA	GCLK	t_{CO}	5.632	6.170	6.745	ns
		GCLK PLL	t_{CO}	3.561	3.895	4.281	ns
	8 mA	GCLK	t_{CO}	5.397	5.926	6.491	ns
		GCLK PLL	t_{CO}	3.326	3.651	4.027	ns
	12 mA	GCLK	t_{CO}	5.298	5.821	6.381	ns
		GCLK PLL	t_{CO}	3.227	3.546	3.917	ns
	16 mA	GCLK	t_{CO}	5.257	5.779	6.338	ns
		GCLK PLL	t_{CO}	3.186	3.504	3.874	ns
1.8V	2 mA	GCLK	t_{CO}	6.726	7.406	8.125	ns
		GCLK PLL	t_{CO}	4.655	5.131	5.661	ns
	4 mA	GCLK	t_{CO}	6.213	6.878	7.581	ns
		GCLK PLL	t_{CO}	4.142	4.603	5.117	ns
	6 mA	GCLK	t_{CO}	5.992	6.624	7.294	ns
		GCLK PLL	t_{CO}	3.921	4.349	4.830	ns
	8 mA	GCLK	t_{CO}	5.891	6.510	7.168	ns
		GCLK PLL	t_{CO}	3.820	4.235	4.704	ns
	10 mA	GCLK	t_{CO}	5.840	6.461	7.122	ns
		GCLK PLL	t_{CO}	3.769	4.186	4.658	ns
	12 mA	GCLK	t_{CO}	5.785	6.398	7.049	ns
		GCLK PLL	t_{CO}	3.714	4.123	4.585	ns
	16 mA	GCLK	t_{CO}	5.742	6.351	7.000	ns
		GCLK PLL	t_{CO}	3.671	4.076	4.536	ns
1.5V	2 mA	GCLK	t_{CO}	7.120	7.973	8.870	ns
		GCLK PLL	t_{CO}	5.049	5.698	6.406	ns
	4 mA	GCLK	t_{CO}	6.664	7.429	8.237	ns
		GCLK PLL	t_{CO}	4.593	5.154	5.773	ns
	6 mA	GCLK	t_{CO}	6.497	7.251	8.046	ns
		GCLK PLL	t_{CO}	4.426	4.976	5.582	ns
	8 mA	GCLK	t_{CO}	6.421	7.158	7.936	ns
		GCLK PLL	t_{CO}	4.350	4.883	5.472	ns
	10 mA	GCLK	t_{CO}	6.361	7.095	7.870	ns
		GCLK PLL	t_{CO}	4.290	4.820	5.406	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	6.327	7.052	7.819	ns
		GCLK PLL	t_{CO}	4.256	4.777	5.355	ns
	16 mA	GCLK	t_{CO}	6.230	6.944	7.700	ns
		GCLK PLL	t_{CO}	4.159	4.669	5.236	ns
1.2V	2 mA	GCLK	t_{CO}	8.308	9.513	10.766	ns
		GCLK PLL	t_{CO}	6.237	7.238	8.302	ns
	4 mA	GCLK	t_{CO}	7.873	8.999	10.174	ns
		GCLK PLL	t_{CO}	5.802	6.724	7.710	ns
	6 mA	GCLK	t_{CO}	7.745	8.845	9.995	ns
		GCLK PLL	t_{CO}	5.674	6.570	7.531	ns
	8 mA	GCLK	t_{CO}	7.673	8.763	9.900	ns
		GCLK PLL	t_{CO}	5.602	6.488	7.436	ns
	10 mA	GCLK	t_{CO}	7.542	8.600	9.705	ns
		GCLK PLL	t_{CO}	5.471	6.325	7.241	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.226	5.753	6.319	ns
		GCLK PLL	t_{CO}	3.162	3.477	3.839	ns
	12 mA	GCLK	t_{CO}	5.207	5.734	6.298	ns
		GCLK PLL	t_{CO}	3.143	3.458	3.818	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.152	5.677	6.238	ns
		GCLK PLL	t_{CO}	3.088	3.401	3.758	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	5.660	6.268	6.914	ns
		GCLK PLL	t_{CO}	3.596	3.992	4.434	ns
	10 mA	GCLK	t_{CO}	5.647	6.250	6.893	ns
		GCLK PLL	t_{CO}	3.583	3.974	4.413	ns
	12 mA	GCLK	t_{CO}	5.634	6.235	6.875	ns
		GCLK PLL	t_{CO}	3.570	3.959	4.395	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	5.604	6.206	6.847	ns
		GCLK PLL	t_{CO}	3.540	3.930	4.367	ns
	16 mA	GCLK	t_{CO}	5.596	6.200	6.842	ns
		GCLK PLL	t_{CO}	3.532	3.924	4.362	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	5.624	6.222	6.859	ns
		GCLK PLL	t_{CO}	3.560	3.946	4.379	ns
	10 mA	GCLK	t_{CO}	5.619	6.218	6.856	ns
		GCLK PLL	t_{CO}	3.555	3.942	4.376	ns
	12 mA	GCLK	t_{CO}	5.612	6.211	6.849	ns
		GCLK PLL	t_{CO}	3.548	3.935	4.369	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	5.550	6.145	6.778	ns
		GCLK PLL	t_{CO}	3.486	3.869	4.298	ns

Table 1–87. EP3C80 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.139	6.843	7.588	ns
		GCLK PLL	t_{CO}	4.075	4.567	5.108	ns
	10 mA	GCLK	t_{CO}	6.151	6.855	7.599	ns
		GCLK PLL	t_{CO}	4.087	4.579	5.119	ns
	12 mA	GCLK	t_{CO}	6.139	6.846	7.594	ns
		GCLK PLL	t_{CO}	4.075	4.570	5.114	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.084	6.789	7.533	ns
		GCLK PLL	t_{CO}	4.020	4.513	5.053	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	7.376	8.415	9.501	ns
		GCLK PLL	t_{CO}	5.312	6.139	7.021	ns
	10 mA	GCLK	t_{CO}	7.315	8.330	9.392	ns
		GCLK PLL	t_{CO}	5.251	6.054	6.912	ns
3.0-V PCI	—	GCLK	t_{CO}	5.434	5.935	6.471	ns
		GCLK PLL	t_{CO}	3.363	3.660	4.007	ns
3.0-V PCI-X	—	GCLK	t_{CO}	5.434	5.935	6.471	ns
		GCLK PLL	t_{CO}	3.363	3.660	4.007	ns

Table 1–88. EP3C80 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.548	0.588	0.601	ns
			t_H	–0.270	–0.272	–0.248	ns
	—	GCLK PLL	t_{SU}	2.599	2.842	3.061	ns
			t_H	–2.321	–2.526	–2.708	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
		GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
		GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
PPDS_E_3R	—	GCLK	t_{CO}	5.570	6.101	6.666	ns
	—	GCLK PLL	t_{CO}	3.519	3.847	4.206	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
	—	GCLK PLL	t_{CO}	3.138	3.468	3.828	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.189	5.722	6.288	ns
	—	GCLK PLL	t_{CO}	3.138	3.468	3.828	ns

Table 1–89. EP3C80 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–6	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.572	0.616	0.638	ns
			t_H	–0.294	–0.301	–0.284	ns
			t_{CO}	4.385	4.811	5.271	ns
	—	GCLK PLL	t_{SU}	2.628	2.874	3.102	ns
			t_H	–2.350	–2.559	–2.748	ns
			t_{CO}	2.321	2.546	2.799	ns
mini-LVDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns
PPDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns
RSDS	—	GCLK	t_{CO}	4.385	4.811	5.271	ns
		GCLK PLL	t_{CO}	2.321	2.546	2.799	ns

EP3C120 I/O Timing Parameters

Table 1–90 through Table 1–95 show the maximum I/O timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	8 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVTTL	8 mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	12mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	16mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
3.0-V LVCMOS	4mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	8mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	12mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
	16mA	GCLK	t_{SU}	0.501	0.449	ns
			t_H	–0.183	–0.095	ns
		GCLK PLL	t_{SU}	3.089	3.258	ns
			t_H	–2.771	–2.904	ns
2.5V	4mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
	8mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
	12mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
2.5V	16 mA	GCLK	t_{SU}	0.456	0.417	ns
			t_H	–0.139	–0.064	ns
		GCLK PLL	t_{SU}	3.044	3.226	ns
			t_H	–2.727	–2.873	ns
1.8V	2 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	4 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	6 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	8 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	10 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	12 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
	16 mA	GCLK	t_{SU}	0.417	0.404	ns
			t_H	–0.101	–0.050	ns
		GCLK PLL	t_{SU}	3.005	3.217	ns
			t_H	–2.689	–2.863	ns
1.5V	2 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	4 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	6 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	8 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	10 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	12 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
	16 mA	GCLK	t_{SU}	0.509	0.521	ns
			t_H	–0.191	–0.165	ns
		GCLK PLL	t_{SU}	3.097	3.334	ns
			t_H	–2.779	–2.978	ns
1.2V	2 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	4 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	6 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	8 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
	10 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2V	12 mA	GCLK	t_{SU}	0.689	0.727	ns
			t_H	–0.367	–0.367	ns
		GCLK PLL	t_{SU}	3.277	3.540	ns
			t_H	–2.955	–3.180	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
	12 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.478	0.463	ns
			t_H	–0.161	–0.108	ns
		GCLK PLL	t_{SU}	3.059	3.278	ns
			t_H	–2.742	–2.923	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	10 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	16 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.8-V HSTL Class I	8 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	10 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
	12 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.564	0.578	ns
			t_H	–0.245	–0.221	ns
		GCLK PLL	t_{SU}	3.161	3.403	ns
			t_H	–2.842	–3.046	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
	10 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
	12 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.524	0.544	ns
			t_H	–0.206	–0.188	ns
		GCLK PLL	t_{SU}	3.121	3.369	ns
			t_H	–2.803	–3.013	ns

Table 1–90. EP3C120 Column I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
	10 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
	12 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{SU}	0.683	0.728	ns
			t_H	–0.361	–0.368	ns
		GCLK PLL	t_{SU}	3.280	3.553	ns
			t_H	–2.958	–3.193	ns
3.0-V PCI	—	GCLK	t_{SU}	0.497	0.444	ns
			t_H	–0.179	–0.090	ns
	—	GCLK PLL	t_{SU}	3.085	3.253	ns
			t_H	–2.767	–2.899	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.497	0.444	ns
			t_H	–0.179	–0.090	ns
	—	GCLK PLL	t_{SU}	3.085	3.253	ns
			t_H	–2.767	–2.899	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 1 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 2 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVCMOS	2 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
3.0-V LVTTL	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	12 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	16 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
3.0-V LVCMOS	4 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	8 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	12 mA	GCLK	t_{SU}	0.640	0.608	ns
			t_H	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns
	16 mA	GCLK	t_{SU}	0.640	0.608	ns
			th	–0.322	–0.253	ns
		GCLK PLL	t_{SU}	3.233	3.429	ns
			t_H	–2.915	–3.074	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 3 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
2.5V	4 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	8 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	12 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
	16 mA	GCLK	t_{SU}	0.596	0.579	ns
			t_H	–0.279	–0.225	ns
		GCLK PLL	t_{SU}	3.189	3.400	ns
			t_H	–2.872	–3.046	ns
1.8V	2 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	4 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	6 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	8 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	10 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
	12 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 4 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.8V	16 mA	GCLK	t_{SU}	0.557	0.565	ns
			t_H	–0.241	–0.210	ns
		GCLK PLL	t_{SU}	3.150	3.386	ns
			t_H	–2.834	–3.031	ns
1.5V	2 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	4 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	6 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	8 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	10 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	12 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
	16 mA	GCLK	t_{SU}	0.650	0.683	ns
			t_H	–0.332	–0.327	ns
		GCLK PLL	t_{SU}	3.243	3.504	ns
			t_H	–2.925	–3.148	ns
1.2V	2 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	4 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 5 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2V	6 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	8 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			t_H	–3.101	–3.350	ns
	10 mA	GCLK	t_{SU}	0.830	0.890	ns
			t_H	–0.508	–0.529	ns
		GCLK PLL	t_{SU}	3.423	3.711	ns
			th	–3.101	–3.350	ns
SSTL-2 Class I	8 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
	12 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
SSTL-2 Class II	16 mA	GCLK	t_{SU}	0.615	0.627	ns
			t_H	–0.297	–0.271	ns
		GCLK PLL	t_{SU}	3.208	3.448	ns
			t_H	–2.890	–3.092	ns
SSTL-18 Class I	8 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	10 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 6 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
SSTL-18 Class II	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	16 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.8–V HSTL Class I	8 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	10 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
	12 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{SU}	0.704	0.744	ns
			t_H	–0.385	–0.386	ns
		GCLK PLL	t_{SU}	3.297	3.565	ns
			t_H	–2.978	–3.207	ns
1.5-V HSTL Class I	8 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
	10 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
	12 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{SU}	0.663	0.707	ns
			t_H	–0.345	–0.350	ns
		GCLK PLL	t_{SU}	3.256	3.528	ns
			t_H	–2.938	–3.171	ns

Table 1–91. EP3C120 Row I/O Pin Input Timing Parameters for Single-Ended I/O Standards (Part 7 of 7)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.2-V HSTL Class I	8 mA	GCLK	t_{SU}	0.821	0.892	ns
			t_H	–0.499	–0.532	ns
		GCLK PLL	t_{SU}	3.414	3.713	ns
			t_H	–3.092	–3.353	ns
	10 mA	GCLK	t_{SU}	0.821	0.892	ns
			t_H	–0.499	–0.532	ns
		GCLK PLL	t_{SU}	3.414	3.713	ns
			t_H	–3.092	–3.353	ns
3.0-V PCI	—	GCLK	t_{SU}	0.636	0.604	ns
			t_H	–0.318	–0.249	ns
	—	GCLK PLL	t_{SU}	3.229	3.425	ns
			t_H	–2.911	–3.070	ns
3.0-V PCI-X	—	GCLK	t_{SU}	0.636	0.604	ns
			t_H	–0.318	–0.249	ns
	—	GCLK PLL	t_{SU}	3.229	3.425	ns
			t_H	–2.911	–3.070	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.607	7.194	ns
		GCLK PLL	t_{CO}	4.020	4.385	ns
	8 mA	GCLK	t_{CO}	6.607	7.194	ns
		GCLK PLL	t_{CO}	4.020	4.385	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	6.388	6.796	ns
		GCLK PLL	t_{CO}	3.801	3.987	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	6.310	6.892	ns
		GCLK PLL	t_{CO}	3.723	4.083	ns
	8 mA	GCLK	t_{CO}	6.026	6.593	ns
		GCLK PLL	t_{CO}	3.439	3.784	ns
	12 mA	GCLK	t_{CO}	5.925	6.489	ns
		GCLK PLL	t_{CO}	3.338	3.680	ns
	16 mA	GCLK	t_{CO}	5.873	6.431	ns
		GCLK PLL	t_{CO}	3.286	3.622	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	6.023	6.590	ns
		GCLK PLL	t_{CO}	3.436	3.781	ns
	8 mA	GCLK	t_{CO}	5.875	6.435	ns
		GCLK PLL	t_{CO}	3.288	3.626	ns
	12 mA	GCLK	t_{CO}	5.835	6.392	ns
		GCLK PLL	t_{CO}	3.248	3.583	ns
	16 mA	GCLK	t_{CO}	5.820	6.377	ns
		GCLK PLL	t_{CO}	3.233	3.568	ns
2.5V	4 mA	GCLK	t_{CO}	6.396	7.006	ns
		GCLK PLL	t_{CO}	3.809	4.197	ns
	8 mA	GCLK	t_{CO}	6.143	6.742	ns
		GCLK PLL	t_{CO}	3.556	3.933	ns
	12 mA	GCLK	t_{CO}	6.037	6.629	ns
		GCLK PLL	t_{CO}	3.450	3.820	ns
	16 mA	GCLK	t_{CO}	5.997	6.588	ns
		GCLK PLL	t_{CO}	3.410	3.779	ns
1.8V	2 mA	GCLK	t_{CO}	7.649	8.404	ns
		GCLK PLL	t_{CO}	5.062	5.592	ns
	4 mA	GCLK	t_{CO}	7.104	7.840	ns
		GCLK PLL	t_{CO}	4.517	5.028	ns
	6 mA	GCLK	t_{CO}	6.846	7.548	ns
		GCLK PLL	t_{CO}	4.259	4.736	ns
	8 mA	GCLK	t_{CO}	6.729	7.419	ns
		GCLK PLL	t_{CO}	4.142	4.607	ns
	10 mA	GCLK	t_{CO}	6.681	7.373	ns
		GCLK PLL	t_{CO}	4.094	4.561	ns
	12 mA	GCLK	t_{CO}	6.614	7.298	ns
		GCLK PLL	t_{CO}	4.027	4.486	ns
	16 mA	GCLK	t_{CO}	6.555	7.233	ns
		GCLK PLL	t_{CO}	3.968	4.421	ns
1.5V	2 mA	GCLK	t_{CO}	8.211	9.143	ns
		GCLK PLL	t_{CO}	5.624	6.331	ns
	4 mA	GCLK	t_{CO}	7.650	8.495	ns
		GCLK PLL	t_{CO}	5.063	5.683	ns
	6 mA	GCLK	t_{CO}	7.467	8.298	ns
		GCLK PLL	t_{CO}	4.880	5.486	ns
	8 mA	GCLK	t_{CO}	7.354	8.160	ns
		GCLK PLL	t_{CO}	4.767	5.348	ns
	10 mA	GCLK	t_{CO}	7.294	8.099	ns
		GCLK PLL	t_{CO}	4.707	5.287	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	7.253	8.049	ns
		GCLK PLL	t_{CO}	4.666	5.237	ns
	16 mA	GCLK	t_{CO}	7.111	7.879	ns
		GCLK PLL	t_{CO}	4.524	5.067	ns
1.2V	2 mA	GCLK	t_{CO}	9.739	11.032	ns
		GCLK PLL	t_{CO}	7.152	8.220	ns
	4 mA	GCLK	t_{CO}	9.213	10.425	ns
		GCLK PLL	t_{CO}	6.626	7.613	ns
	6 mA	GCLK	t_{CO}	9.032	10.211	ns
		GCLK PLL	t_{CO}	6.445	7.399	ns
	8 mA	GCLK	t_{CO}	8.952	10.121	ns
		GCLK PLL	t_{CO}	6.365	7.309	ns
	10 mA	GCLK	t_{CO}	8.770	9.890	ns
		GCLK PLL	t_{CO}	6.183	7.078	ns
	12 mA	GCLK	t_{CO}	8.744	9.868	ns
		GCLK PLL	t_{CO}	6.157	7.056	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.983	6.573	ns
		GCLK PLL	t_{CO}	3.402	3.758	ns
	12 mA	GCLK	t_{CO}	5.959	6.550	ns
		GCLK PLL	t_{CO}	3.378	3.735	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.897	6.484	ns
		GCLK PLL	t_{CO}	3.316	3.669	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.499	7.168	ns
		GCLK PLL	t_{CO}	3.903	4.345	ns
	10 mA	GCLK	t_{CO}	6.468	7.131	ns
		GCLK PLL	t_{CO}	3.872	4.308	ns
	12 mA	GCLK	t_{CO}	6.454	7.114	ns
		GCLK PLL	t_{CO}	3.858	4.291	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.425	7.086	ns
		GCLK PLL	t_{CO}	3.829	4.263	ns
	16 mA	GCLK	t_{CO}	6.412	7.072	ns
		GCLK PLL	t_{CO}	3.816	4.249	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.451	7.110	ns
		GCLK PLL	t_{CO}	3.855	4.287	ns
	10 mA	GCLK	t_{CO}	6.444	7.106	ns
		GCLK PLL	t_{CO}	3.848	4.283	ns
	12 mA	GCLK	t_{CO}	6.430	7.086	ns
		GCLK PLL	t_{CO}	3.834	4.263	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.364	7.020	ns
		GCLK PLL	t_{CO}	3.768	4.197	ns

Table 1–92. EP3C120 Column I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	7.072	7.841	ns
		GCLK PLL	t_{CO}	4.476	5.018	ns
	10 mA	GCLK	t_{CO}	7.072	7.836	ns
		GCLK PLL	t_{CO}	4.476	5.013	ns
	12 mA	GCLK	t_{CO}	7.064	7.832	ns
		GCLK PLL	t_{CO}	4.468	5.009	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.996	7.757	ns
		GCLK PLL	t_{CO}	4.400	4.934	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.610	9.708	ns
		GCLK PLL	t_{CO}	6.014	6.885	ns
	10 mA	GCLK	t_{CO}	8.521	9.592	ns
		GCLK PLL	t_{CO}	5.925	6.769	ns
	12 mA	GCLK	t_{CO}	8.527	9.601	ns
		GCLK PLL	t_{CO}	5.931	6.778	ns
1.2-V HSTL Class II	14 mA	GCLK	t_{CO}	8.474	9.541	ns
		GCLK PLL	t_{CO}	5.878	6.718	ns
3.0-V PCI	—	GCLK	t_{CO}	6.167	6.726	ns
		GCLK PLL	t_{CO}	3.580	3.917	ns
3.0-V PCI-X	—	GCLK	t_{CO}	6.167	6.726	ns
		GCLK PLL	t_{CO}	3.580	3.917	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 1 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.3-V LVTTL	4 mA	GCLK	t_{CO}	6.440	7.006	ns
		GCLK PLL	t_{CO}	3.847	4.185	ns
	8 mA	GCLK	t_{CO}	6.440	7.006	ns
		GCLK PLL	t_{CO}	3.847	4.185	ns
3.3-V LVCMOS	2 mA	GCLK	t_{CO}	6.266	6.656	ns
		GCLK PLL	t_{CO}	3.673	3.835	ns
3.0-V LVTTL	4 mA	GCLK	t_{CO}	6.147	6.707	ns
		GCLK PLL	t_{CO}	3.554	3.886	ns
	8 mA	GCLK	t_{CO}	5.880	6.430	ns
		GCLK PLL	t_{CO}	3.287	3.609	ns
	12 mA	GCLK	t_{CO}	5.785	6.328	ns
		GCLK PLL	t_{CO}	3.192	3.507	ns
	16 mA	GCLK	t_{CO}	5.734	6.273	ns
		GCLK PLL	t_{CO}	3.141	3.452	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 2 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
3.0-V LVCMOS	4 mA	GCLK	t_{CO}	5.878	6.428	ns
		GCLK PLL	t_{CO}	3.285	3.607	ns
	8 mA	GCLK	t_{CO}	5.735	6.276	ns
		GCLK PLL	t_{CO}	3.142	3.455	ns
	12 mA	GCLK	t_{CO}	5.699	6.237	ns
		GCLK PLL	t_{CO}	3.106	3.416	ns
	16 mA	GCLK	t_{CO}	5.683	6.220	ns
		GCLK PLL	t_{CO}	3.090	3.399	ns
2.5V	4 mA	GCLK	t_{CO}	6.261	6.837	ns
		GCLK PLL	t_{CO}	3.668	4.016	ns
	8 mA	GCLK	t_{CO}	6.017	6.583	ns
		GCLK PLL	t_{CO}	3.424	3.762	ns
	12 mA	GCLK	t_{CO}	5.912	6.473	ns
		GCLK PLL	t_{CO}	3.319	3.652	ns
	16 mA	GCLK	t_{CO}	5.870	6.430	ns
		GCLK PLL	t_{CO}	3.277	3.609	ns
1.8V	2 mA	GCLK	t_{CO}	7.497	8.217	ns
		GCLK PLL	t_{CO}	4.904	5.396	ns
	4 mA	GCLK	t_{CO}	6.969	7.673	ns
		GCLK PLL	t_{CO}	4.376	4.852	ns
	6 mA	GCLK	t_{CO}	6.715	7.386	ns
		GCLK PLL	t_{CO}	4.122	4.565	ns
	8 mA	GCLK	t_{CO}	6.601	7.260	ns
		GCLK PLL	t_{CO}	4.008	4.439	ns
	10 mA	GCLK	t_{CO}	6.552	7.214	ns
		GCLK PLL	t_{CO}	3.959	4.393	ns
	12 mA	GCLK	t_{CO}	6.489	7.141	ns
		GCLK PLL	t_{CO}	3.896	4.320	ns
	16 mA	GCLK	t_{CO}	6.442	7.092	ns
		GCLK PLL	t_{CO}	3.849	4.271	ns
1.5V	2 mA	GCLK	t_{CO}	8.064	8.962	ns
		GCLK PLL	t_{CO}	5.471	6.141	ns
	4 mA	GCLK	t_{CO}	7.520	8.329	ns
		GCLK PLL	t_{CO}	4.927	5.508	ns
	6 mA	GCLK	t_{CO}	7.342	8.138	ns
		GCLK PLL	t_{CO}	4.749	5.317	ns
	8 mA	GCLK	t_{CO}	7.249	8.028	ns
		GCLK PLL	t_{CO}	4.656	5.207	ns
	10 mA	GCLK	t_{CO}	7.186	7.962	ns
		GCLK PLL	t_{CO}	4.593	5.141	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 3 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5V	12 mA	GCLK	t_{CO}	7.143	7.911	ns
		GCLK PLL	t_{CO}	4.550	5.090	ns
	16 mA	GCLK	t_{CO}	7.035	7.792	ns
		GCLK PLL	t_{CO}	4.442	4.971	ns
1.2V	2 mA	GCLK	t_{CO}	9.604	10.858	ns
		GCLK PLL	t_{CO}	7.011	8.037	ns
	4 mA	GCLK	t_{CO}	9.090	10.266	ns
		GCLK PLL	t_{CO}	6.497	7.445	ns
	6 mA	GCLK	t_{CO}	8.936	10.087	ns
		GCLK PLL	t_{CO}	6.343	7.266	ns
	8 mA	GCLK	t_{CO}	8.854	9.992	ns
		GCLK PLL	t_{CO}	6.261	7.171	ns
	10 mA	GCLK	t_{CO}	8.691	9.797	ns
		GCLK PLL	t_{CO}	6.098	6.976	ns
SSTL-2 Class I	8 mA	GCLK	t_{CO}	5.844	6.411	ns
		GCLK PLL	t_{CO}	3.251	3.590	ns
	12 mA	GCLK	t_{CO}	5.825	6.390	ns
		GCLK PLL	t_{CO}	3.232	3.569	ns
SSTL-2 Class II	16 mA	GCLK	t_{CO}	5.768	6.330	ns
		GCLK PLL	t_{CO}	3.175	3.509	ns
SSTL-18 Class I	8 mA	GCLK	t_{CO}	6.359	7.006	ns
		GCLK PLL	t_{CO}	3.766	4.185	ns
	10 mA	GCLK	t_{CO}	6.341	6.985	ns
		GCLK PLL	t_{CO}	3.748	4.164	ns
	12 mA	GCLK	t_{CO}	6.326	6.967	ns
		GCLK PLL	t_{CO}	3.733	4.146	ns
SSTL-18 Class II	12 mA	GCLK	t_{CO}	6.297	6.939	ns
		GCLK PLL	t_{CO}	3.704	4.118	ns
	16 mA	GCLK	t_{CO}	6.291	6.934	ns
		GCLK PLL	t_{CO}	3.698	4.113	ns
1.8-V HSTL Class I	8 mA	GCLK	t_{CO}	6.313	6.951	ns
		GCLK PLL	t_{CO}	3.720	4.130	ns
	10 mA	GCLK	t_{CO}	6.309	6.948	ns
		GCLK PLL	t_{CO}	3.716	4.127	ns
	12 mA	GCLK	t_{CO}	6.302	6.941	ns
		GCLK PLL	t_{CO}	3.709	4.120	ns
1.8-V HSTL Class II	16 mA	GCLK	t_{CO}	6.236	6.870	ns
		GCLK PLL	t_{CO}	3.643	4.049	ns

Table 1–93. EP3C120 Row I/O Pin Output Timing Parameters for Single-Ended I/O Standards (Part 4 of 4)

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
1.5-V HSTL Class I	8 mA	GCLK	t_{CO}	6.934	7.680	ns
		GCLK PLL	t_{CO}	4.341	4.859	ns
	10 mA	GCLK	t_{CO}	6.946	7.691	ns
		GCLK PLL	t_{CO}	4.353	4.870	ns
	12 mA	GCLK	t_{CO}	6.937	7.686	ns
		GCLK PLL	t_{CO}	4.344	4.865	ns
1.5-V HSTL Class II	16 mA	GCLK	t_{CO}	6.880	7.625	ns
		GCLK PLL	t_{CO}	4.287	4.804	ns
1.2-V HSTL Class I	8 mA	GCLK	t_{CO}	8.506	9.593	ns
		GCLK PLL	t_{CO}	5.913	6.772	ns
	10 mA	GCLK	t_{CO}	8.421	9.484	ns
		GCLK PLL	t_{CO}	5.828	6.663	ns
3.0-V PCI	—	GCLK	t_{CO}	6.026	6.563	ns
		GCLK PLL	t_{CO}	3.433	3.742	ns
3.0-V PCI-X	—	GCLK	t_{CO}	6.026	6.563	ns
		GCLK PLL	t_{CO}	3.433	3.742	ns

Table 1–94. EP3C120 Column Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.379	0.372	ns
			t_H	–0.063	–0.019	ns
	—	GCLK PLL	t_{SU}	2.965	3.187	ns
			t_H	–2.649	–2.834	ns
LVDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
mini-LVDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
PPDS_E_3R	—	GCLK	t_{CO}	6.310	6.895	ns
		GCLK PLL	t_{CO}	3.726	4.083	ns
RSDS_E_1R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns
RSDS_E_3R	—	GCLK	t_{CO}	5.931	6.517	ns
		GCLK PLL	t_{CO}	3.347	3.705	ns

Table 1–95. EP3C120 Row Pin Differential I/O Timing Parameters

IO Standard	Current Strength	Clock	Parameter	–7	–8	Units
LVDS	—	GCLK	t_{SU}	0.519	0.538	ns
			t_H	–0.204	–0.184	ns
			t_{CO}	4.902	5.363	ns
	—	GCLK PLL	t_{SU}	3.105	3.351	ns
			t_H	–2.790	–2.997	ns
			t_{CO}	2.313	2.547	ns
mini-LVDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns
PPDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns
RSDS	—	GCLK	t_{CO}	4.902	5.363	ns
		GCLK PLL	t_{CO}	2.313	2.547	ns

Dedicated Clock Pin Timing Parameters

Table 1–96 to Table 1–111 show clock pin timing for Cyclone III devices.

EP3C5 Clock Timing Parameters

Table 1–96 through Table 1–97 show the maximum clock timing parameters for EP3C5 devices.

Table 1–96. EP3C5 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.543	2.287	2.519	2.790	ns
tcout	—	1.573	2.340	2.580	2.845	ns
tpllcin	—	0.964	1.349	1.462	1.617	ns
tpllcout	—	0.994	1.402	1.523	1.686	ns

Table 1–97. EP3C5 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.540	2.274	2.502	2.769	ns
tcout	—	1.570	2.327	2.563	2.824	ns
tpllcin	—	0.961	1.336	1.445	1.596	ns
tpllcout	—	0.991	1.389	1.506	1.665	ns

EP3C10 Clock Timing Parameters

Table 1–98 through Table 1–99 show the maximum clock timing parameters for EP3C10 devices.

Table 1–98. EP3C10 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.542	2.286	2.518	2.789	ns
tcout	—	1.572	2.339	2.579	2.845	ns
tpllcin	—	0.963	1.348	1.461	1.617	ns
tpllcout	—	0.993	1.401	1.522	1.686	ns

Table 1–99. EP3C10 Row Pin Global Clock Timing Parameters (Part 1 of 2)

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.536	2.274	2.499	2.762	ns
tcout	—	1.566	2.327	2.560	2.819	ns

Table 1–99. EP3C10 Row Pin Global Clock Timing Parameters (Part 2 of 2)

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tpllcin	—	0.957	1.336	1.442	1.591	ns
tpllcout	—	0.987	1.389	1.503	1.660	ns

EP3C16 Clock Timing Parameters

Table 1–100 through Table 1–101 show the maximum clock timing parameters for EP3C16 devices.

Table 1–100. EP3C16 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.620	2.389	2.627	2.896	ns
tcout	—	1.650	2.442	2.688	2.956	ns
tpllcin	—	0.919	1.239	1.335	1.467	ns
tpllcout	—	0.949	1.292	1.396	1.536	ns

Table 1–101. EP3C16 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.605	2.364	2.598	2.858	ns
tcout	—	1.635	2.417	2.659	2.920	ns
tpllcin	—	0.904	1.214	1.306	1.431	ns
tpllcout	—	0.934	1.267	1.367	1.500	ns

EP3C25 Clock Timing Parameters

Table 1–102 through Table 1–103 show the maximum clock timing parameters for EP3C25 devices.

Table 1–102. EP3C25 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.652	2.438	2.682	2.959	ns
tcout	—	1.682	2.491	2.743	3.017	ns
tpllcin	—	0.938	1.271	1.370	1.505	ns
tpllcout	—	0.968	1.324	1.431	1.574	ns

Table 1–103. EP3C25 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.640	2.419	2.660	2.929	ns
tcout	—	1.670	2.472	2.721	2.991	ns
tpllcin	—	0.926	1.252	1.348	1.479	ns
tpllcout	—	0.956	1.305	1.409	1.548	ns

EP3C40 Clock Timing Parameters

Table 1–104 through Table 1–105 show the maximum clock timing parameters for EP3C40 device.

Table 1–104. EP3C40 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.734	2.568	2.824	3.106	ns
tcout	—	1.764	2.621	2.885	3.172	ns
tpllcin	—	0.972	1.318	1.418	1.558	ns
tpllcout	—	1.002	1.371	1.479	1.627	ns

Table 1–105. EP3C40 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.721	2.543	2.804	3.078	ns
tcout	—	1.751	2.596	2.865	3.142	ns
tpllcin	—	0.959	1.293	1.398	1.528	ns
tpllcout	—	0.989	1.346	1.459	1.597	ns

EP3C55 Clock Timing Parameters

Table 1–106 through Table 1–107 show the maximum clock timing parameters for EP3C55 devices.

Table 1–106. EP3C55 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.801	2.672	2.935	3.229	ns
tcout	—	1.831	2.725	2.996	3.296	ns
tpllcin	—	1.014	1.378	1.481	1.629	ns
tpllcout	—	1.044	1.431	1.542	1.698	ns

Table 1–107. EP3C55 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.805	2.666	2.926	3.207	ns
tcout	—	1.835	2.719	2.987	3.276	ns
tpllcin	—	1.018	1.372	1.472	1.609	ns
tpllcout	—	1.048	1.425	1.533	1.678	ns

EP3C80 Clock Timing Parameters

Table 1–108 through Table 1–109 show the maximum clock timing parameters for EP3C80 devices.

Table 1–108. EP3C80 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.868	2.765	3.039	3.345	ns
tcout	—	1.898	2.818	3.100	3.412	ns
tpllcin	—	1.052	1.423	1.526	1.685	ns
tpllcout	—	1.082	1.476	1.587	1.754	ns

Table 1–109. EP3C80 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–6	–7	–8	Units
	Industrial	Commercial				
tcin	—	1.881	2.776	3.038	3.346	ns
tcout	—	1.911	2.829	3.099	3.415	ns
tpllcin	—	1.065	1.434	1.525	1.688	ns
tpllcout	—	1.095	1.487	1.586	1.757	ns

EP3C120 Clock Timing Parameters

Table 1–110 through Table 1–111 show the maximum clock timing parameters for EP3C120 devices. EP3C120 devices are offered in –7 and –8 speed grades only.

Table 1–110. EP3C120 Column Pin Global Clock Timing Parameters

Parameter	Fast Model		–7	-8	Units
	Industrial	Commercial			
tcin	—	1.990	3.249	3.580	ns
tcout	—	2.020	3.310	3.644	ns
tpllcin	—	0.951	1.345	1.480	ns
tpllcout	—	0.981	1.406	1.549	ns

Table 1–111. EP3C120 Row Pin Global Clock Timing Parameters

Parameter	Fast Model		–7	–8	Units
	Industrial	Commercial			
tcin	—	1.921	3.130	3.433	ns
tcout	—	1.951	3.191	3.490	ns
tpllcin	—	0.882	1.226	1.326	ns
tpllcout	—	0.912	1.287	1.395	ns

Glossary

Table 1–112 shows the glossary for this chapter.

Table 1–112. Glossary (Part 1 of 4)

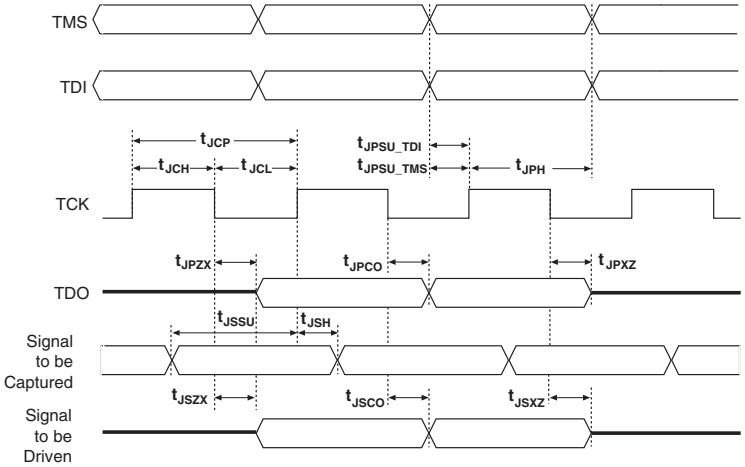
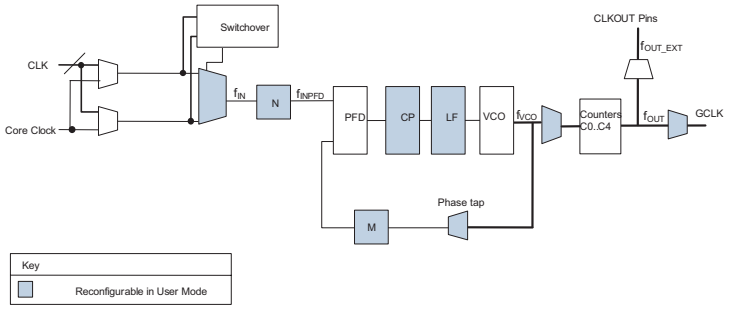
Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	HIGH-SPEED I/O Block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through PLL.
H	HSIODR	HIGH-SPEED I/O Block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following block diagram highlights the PLL Specification parameters. 

Table 1–112. Glossary (Part 2 of 4)

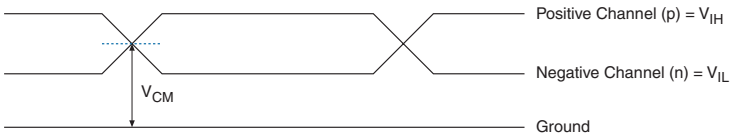
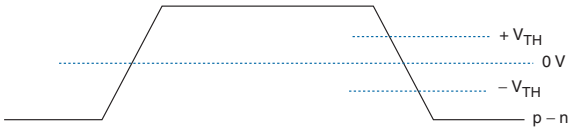
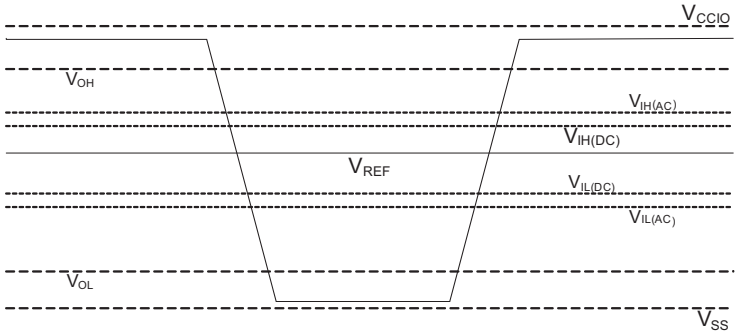
Letter	Term	Definitions
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to Cyclone III device).
	Receiver Input Waveform	Receiver Input Waveform for LVDS and LVPECL Differential Standard. **Single-Ended Waveform**  **Differential Input Waveform** 
	RSKM (Receiver input skew margin)	HIGH-SPEED I/O Block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
S	Single-ended Voltage referenced I/O Standard	 The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. Once the receiver input has crossed the AC value, the receiver will change to the new logic state. The new logic state will then be maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*.
	SW (Sampling Window)	HIGH-SPEED I/O Block: The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window.

Table 1–112. Glossary (Part 3 of 4)

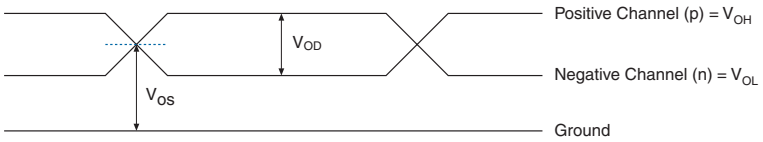
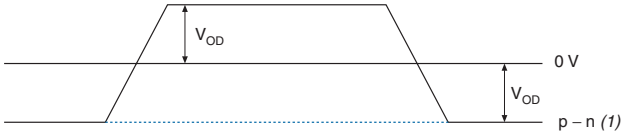
Letter	Term	Definitions
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (Channel-to-channel-skew)	HIGH-SPEED I/O Block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	tcin	Delay from clock pad to I/O input register.
	t_{CO}	Delay from clock pad to I/O output.
	tcout	Delay from clock pad to I/O output register.
	t_{DUTY}	HIGH-SPEED I/O Block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal High-to-low transition time (80-20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	HIGH-SPEED I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
	$t_{INJITTER}$	Period jitter on PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on general purpose I/O driven by a PLL.
	tpllcin	Delay from PLL inclk pad to I/O input register.
	tpllcout	Delay from PLL inclk pad to I/O output register.
	Transmitter Output Waveform	Transmitter Output Waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standard **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	t_{RISE}	Signal Low-to-high transition time (20-80%).
	t_{SU}	Input register setup time.
U	—	—

Table 1–112. Glossary (Part 4 of 4)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC Common Mode Input Voltage.
	$V_{DIF(AC)}$	AC differential Input Voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential Input Voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input Common Mode Voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage Input High: The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage Input Low: The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output Common Mode Voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential Voltage Swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage Output High: The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.
	V_{OL}	Voltage Output Low: The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential Output cross point voltage: The voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for SSTL, HSTL I/O Standards.
	$V_{REF\ (AC)}$	AC input reference voltage for SSTL, HSTL I/O Standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise, The peak-to-peak AC noise on V_{REF} should not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for SSTL, HSTL I/O Standards.
	$V_{SWING\ (AC)}$	AC differential Input Voltage: AC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
	$V_{SWING\ (DC)}$	DC differential Input Voltage: DC Input differential voltage required for switching. Refer to Input Waveforms for the SSTL Differential I/O Standard.
V	V_{TH}	Differential input threshold.
	V_{TT}	Termination voltage for SSTL, HSTL I/O Standards.
	$V_{X\ (AC)}$	AC differential Input cross point Voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Referenced Documents

This chapter references the following documents:

- *AN 447: Interfacing Cyclone III Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*
- *High-Speed Differential Interfaces* chapter in volume 1 of the *Cyclone III Device Handbook*

Document Revision History

Table 1–113 shows the revision history for this document.

Table 1–113. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.3	• Updated Table 1–1 with V_{ESDHBM} and V_{ESDCDM} information. • Updated R_{CONF_PD} information in Table 1–10. • Added *Note (3)* to Table 1–12. • Updated t_{DLOCK} information in Table 1–19. • Updated Table 1–43 and Table 1–44. • Added "Referenced Documents" section.	—
June 2007 v1.2	Updated Cyclone III graphic in cover page.	Revised Cover
May 2007 v1.1	• Corrected current unit in Table 1–1, Table 1–12, and Table 1–14. • Added *Note (3)* to Table 1–3. • Updated Table 1–4 with I_{CCINT0}, I_{CCA0}, I_{CCD_PLL0}, and I_{CCIO0} information. • Updated Table 1–9 and added *Note (2)*. • Updated Table 1–19. • Updated Table 1–22 and added *Note (1)*. • Changed I/O standard from 1.5-V LVTTL/LVCMOS and 1.2-V LVTTL/LVCMOS to 1.5-V LVCMOS and 1.2-V LVCMOS in Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. • Updated Table 1–43 with changes to LVPEC and LVDS and added Note 5. • Updated Table 1–46, Table 1–47, Tables 1–54 through 1–95, and Tables 1–98 through 1–111. • Removed speed grade –6 from Tables 1–90 through 1–95, and from Tables 1–110 through 1–111. • Added new Tables 1–48 through 1–53, Table 1–96, and Table 1–97. • Added a waveform (Receiver Input Waveform) in glossary under letter "R" (Table 1–112).	• Updated Timing Model information and other parts of the document as well.
March 2007 v1.0	Initial Release.	N/A