RTAX-S RadTolerant FPGAs

Designed for Space

- SEU-Hardened Registers Eliminate the Need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET_{TH} > 37 MeV-cm^2/mg
  - SEU Rate < 10^{-10} Errors/Bit-Day in Worst-Case Geosynchronous Orbit
- Expected SRAM Upset Rate of <10^{-10} Errors/Bit-Day with Use of Error Detection and Correction (EDAC) IP (included) with Integrated SRAM Scrubber Featuring
  - Single-Bit Correction, Double-Bit Detection
  - Variable-Rate Background Refreshing
- Total Ionizing Dose Up to 300 krad (Si, Functional)
- Single-Event Latch-Up Immunity (SEL) to LET_{TH} > 104 MeV-cm^2/mg
- JTAG Boundary Scan Testing in Compliance with IEEE Standard 1149.1
- TM1019 Test Data Available

Leading-Edge Performance

- High-Performance Embedded FIFOs
- 350+ MHz System Performance
- 500+ MHz Internal Performance
- 700 Mb/s LVDS Capable I/Os

Specifications

- Up to 2 Million Equivalent System Gates and 250 k Equivalent ASIC Gates
- Up to 10,752 SEU-Hardened Flip-Flops
- Up to 684 I/Os
- Up to 288 kbits Embedded SRAM
- Manufactured on Advanced 0.15 µm CMOS Antifuse Process Technology, 7 Layers of Metal
- Electro Static Discharge ESD (HBM MIL-STD-883, TM3015) – 2000 V

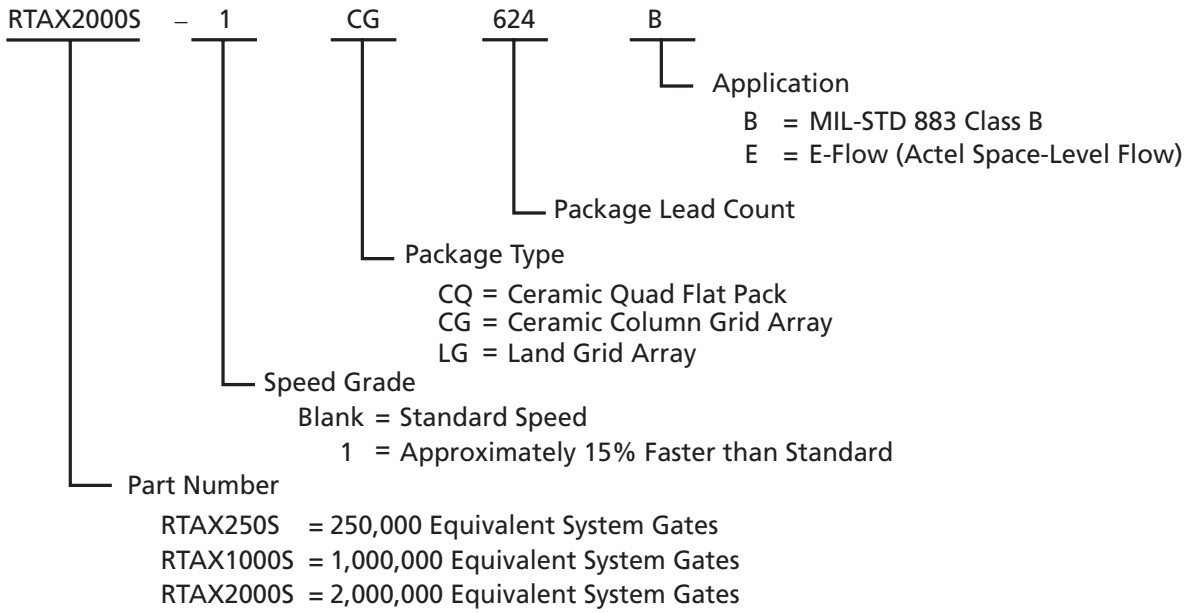
Features

- Single-Chip, Nonvolatile Solution
- 1.5V Core Voltage for Low Power
- Flexible, Multi-Standard I/Os:
  - 1.5V, 1.8V, 2.5V, 3.3V Mixed Voltage Operation
  - Bank-Selectable I/Os – 8 Banks per Chip
  - Single-Ended I/O Standards: LVTTL, LVCMOS, 3.3V PCI
  - Differential I/O Standards: LVPECL and LVDS
  - Voltage-Referenced I/O Standards: GTL+, HSTL Class 1, SSTL2 Class 1 and 2, SSTL3 Class 1 and 2
  - Hot-Swap Compliant with Cold-Sparing Support (Except PCI)
- Embedded Memory:
  - Variable-Aspect 4,608-Bit RAM Blocks
  - x1, x2, x4, x9, x18, x36 Organizations Available
  - Independent, Width-Configurable Read and Write Ports
  - Programmable Embedded FIFO Control Logic
  - ROM Emulation Capability
- Deterministic, User-Controllable Timing
- Low-Cost Prototyping Solution
- Unique In-System Diagnostic and Debug Capability with Actel's Silicon Explorer II or using CLAM (Configurable Logic Analyzer Module)

Table 1 • **RTAX-S Family Product Profile**

Device	RTAX250S	RTAX1000S	RTAX2000S
Capacity			
Equivalent System Gates	250,000	1,000,000	2,000,000
ASIC Gates	30,000	125,000	250,000
Modules			
Register (R-cells)	1,408	6,048	10,752
Combinatorial (C-cells)	2,816	12,096	21,504
Flip-Flops (Maximum)	2,816	12,096	21,504
Embedded RAM/FIFO (without EDAC)			
Core RAM Blocks	12	36	64
Core RAM Bits (K=1,024)	54K	162K	288K
Clocks (Segmentable)			
Hardwired	4	4	4
Routed	4	4	4
I/Os			
I/O Banks	8	8	8
User I/Os (Maximum)	248	516	684
I/O Registers	744	1,548	2,052
Package			
CCGA/LGA	–	624	624, 1152
CQFP	208, 352	352	256, 352

Ordering Information



Temperature Grade Offerings

Package	RTAX250S	RTAX1000S	RTAX2000S
CQ208	E, B	–	–
CQ256	–	–	E, B
CQ352	E, B	E, B	E, B
CG624/LG624	–	E, B	E, B
CG1152/LG1152	–	–	E, B

Note: *E = E-Flow (Actel Space-Level Flow)*
B = MIL-STD-883 Class B

Speed Grade and Temperature Grade Matrix

	Std	–1
E	✓	✓
B	✓	✓

Contact your local Actel representative for device availability.

Device Resources

User I/Os (Including Clock Buffers)			
Device	**RTAX250S**	**RTAX1000S**	**RTAX2000S**
CQ208	115	–	–
CQ256	–	–	138
CQ352	198	198	198
CG624/LG624	–	402	418
CG1152/LG1152	–	402	684

Note: *CQFP = Ceramic Quad Flat Pack and CCGA = Ceramic Column Grid Array, LGA = Land Grid Array*

Actel MIL-STD-883 Class B Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Condition B for CQ352, LG624 Condition D for CQ208 Condition TBD for LG1152 Y_1 Orientation Only	100%
4.	Particle Impact Noise Detection	2020, Condition A	100%
5.	Seal a. Fine b. Gross	1014	 100% 100%
6.	Visual Inspection	2009	100%
7.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
8.	Dynamic Burn-In	1015, Condition D, 160 hours at 125°C or 80 hours at 150°C	100%
9.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
10.	Percent Defective Allowable	5%	All Lots
11.	Final Electrical Test a. Static Tests (1)25°C (Subgroup 1, Table I) (2)–55°C and +125°C (Subgroups 2, 3, Table I) b. Functional Tests (1)25°C (Subgroup 7, Table I) (2)–55°C and +125°C (Subgroups 8A and 8B, Table I) c. Switching Tests at 25°C (Subgroup 9, Table I)	In accordance with applicable Actel device specification, which includes a, b, and c: 5005 5005 5005 5005 5005	 100% 100% 100%
12.	External Visual	2009	100%

Note: *For CCGA devices, all Assembly/Screening/TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*

Actel Extended Flow[1]

Step	Screen	Method	Requirement
1.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
2.	Internal Visual	2010, Condition A	100%
3.	Serialization		100%
4.	Temperature Cycling	1010, Condition C	100%
5.	Constant Acceleration	2001, Condition B for CQ352, LG624 Condition D for CQ208 Condition TBD for LG1152 Y_1 Orientation Only	100%
6.	Particle Impact Noise Detection	2020, Condition A	100%
7.	Radiographic	2012 (one view only)	100%
8.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
9.	Dynamic Burn-In	1015, Condition D, 240 hours at 125°C or 120 hours at 150°C minimum	100%
10.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
11.	Static Burn-In	1015, Condition C, 72 hours at 150°C or 144 hours at 125°C minimum	100%
12.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
13.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters at 25°C	All Lots
14.	Final Electrical Test a. Static Tests (1)25°C (Subgroup 1, Table1) (2)–55°C and +125°C (Subgroups 2, 3, Table 1) b. Functional Tests (1)25°C (Subgroup 7, Table 15) (2)–55°C and +125°C (Subgroups 8A and B, Table 1) c. Switching Tests at 25°C (Subgroup 9, Table 1)	In accordance with Actel applicable device specification which includes a, b, and c: 5005 5005 5005 5005 5005	100% 100% 100% 100%
15.	Seal a. Fine b. Gross	1014	100%
16.	External Visual	2009	100%

Notes:

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Actel is offering this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.*
2. *Method 5004 requires 100 percent nondestructive bond pull to Method 2003. Actel substitutes a destructive bond pull to Method 2011 Condition D on a sample basis only.*
3. *Wafer lot acceptance comply to commercial standards only (requirement per Method 5007 is not performed).*
4. *For CCGA devices, all Assembly/Screening/TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.*

Table of Contents

General Description

Device Architecture 1-1
Programmable Interconnect Element 1-1
Embedded Memory 1-5
I/O Logic 1-5
Routing 1-5
Global Resources 1-7
Design Environment 1-7
Programming 1-7
Low-Cost Prototyping Solution 1-7
In-System Diagnostic and Debug Capabilities 1-7
Summary 1-8
Related Documents 1-9

Detailed Specifications

Operating Conditions 2-2
Calculating Power Dissipation 2-3
I/O Specifications 2-9
Module Specifications 2-41
Routing Specifications 2-50
Global Resources 2-54
Embedded Memory 2-59
Other Architectural Features 2-77
Programming 2-79

Package Pin Assignments

208-Pin CQFP 3-1
256-Pin CQFP 3-4
352-Pin CQFP 3-8
624-Pin CCGA/LGA 3-21
1152-Pin CCGA/LGA 3-34

Datasheet Information

List of Changes 4-1
Datasheet Categories 4-3
International Traffic in Arms Regulations (ITAR) 4-3

General Description

RTAX-S offers high performance at densities of up to two million equivalent system gates for space-based applications. Based upon Actel's commercial Axcelerator family, RTAX-S has several system-level features such as embedded SRAM (with built-in FIFO control logic), segmentable clocks, chip-wide highway routing, and carry logic.

Featuring SEU-hardened flip-flops that offer the benefits of user-implemented Triple Module Redundancy (TMR) without the associated overhead, the RTAX-S family is Actel's second generation product offering for space applications. The RTAX-S devices are manufactured using a 0.15 µm technology at a UMC facility in Taiwan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

Device Architecture

Actel's RTAX-S architecture, derived from the highly-successful SX-A sea-of-modules architecture, has been designed for high performance and total logic module utilization (Figure 1-1). Unlike traditional FPGAs, the entire floor of the RTAX-S device is covered with a grid of logic modules, with virtually no chip area lost to interconnect elements or routing.

Programmable Interconnect Element

The RTAX-S family uses a patented metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal (Figure 1-2 on page 1-2). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on traditional FPGAs) and enables the efficient sea-of-modules architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low-impedance connection, leading to the fastest signal propagation in the industry. In addition, the extremely small size of these interconnect elements gives the RTAX-S family abundant routing resources.

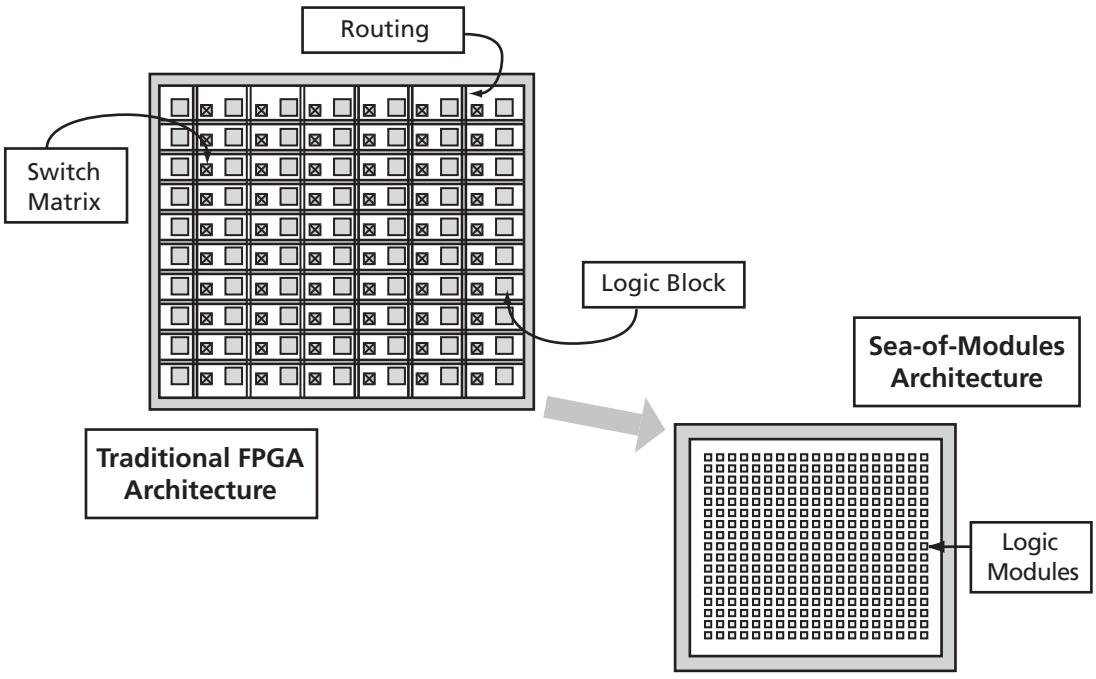


Figure 1-1 • **Sea-of-Modules Comparison**

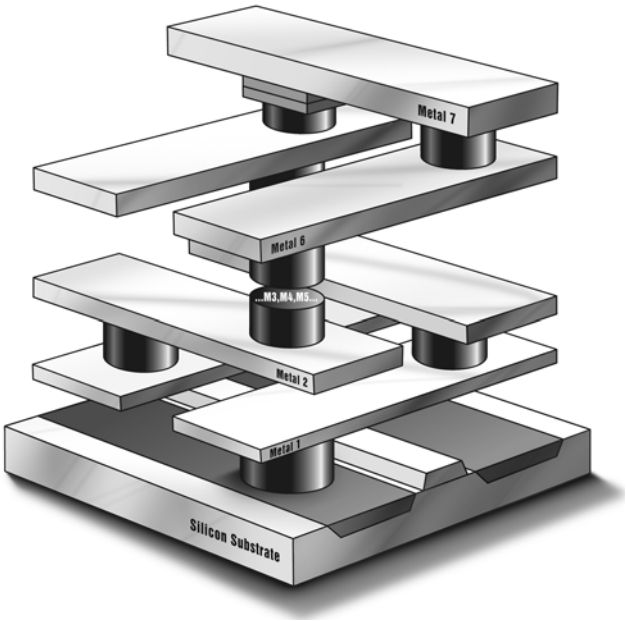


Figure 1-2 • **RTAX-S Family Interconnect Elements**

The very nature of Actel's nonvolatile antifuse technology provides excellent protection against design pirating and cloning (FuseLock technology). Cloning is impossible (even if the security fuse is left unprogrammed) as no bitstream or programming file is ever downloaded or stored in the device. Reverse engineering is virtually impossible due to the difficulty of trying to distinguish between programmed and unprogrammed antifuses and also due to the programming methodology of antifuse devices (see "Security" on page 2-78).

Actel's RTAX-S family provides two types of logic modules: the register cell (R-cell) and the combinatorial cell (C-cell). The RTAX-S C-cell can implement more than 4,000 combinatorial functions of up to five inputs (Figure 1-3 on page 1-3). The C-cell contains carry logic for even more efficient implementation of arithmetic functions. With its small size, the C-cell structure is extremely synthesis-friendly, simplifying the overall design as well as reducing design time.

While each SEU-hardened R-cell appears as a single D-Type flip-flop to the user, each is implemented in silicon using triple redundancy to achieve a LET threshold of greater than 60 MeV-mg/cm^2. Each TMR R-cell consist of three master-slave latch pairs, each with asynchronous self-correcting feedback paths. The output of each latch on the master or slave side votes with the outputs of the other two latches on that side. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents that change from feeding back and permanently latching. Care was also taken in the layout to ensure that a single ion strike could not affect more than one latch (see "R-Cell" on page 2-45 for more details).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Figure 1-3 on page 1-3). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility (e.g., easy mapping of dual-data-rate functions into the FPGA) while conserving valuable clock resources. The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic.

Two C-cells, a single R-cell, and two Transmit (TX) and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Figure 1-4 on page 1-3). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization.

The logic modules within the SuperCluster are arranged so that two combinatorial modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance (Figure 1-5 on page 1-3).

The RTAX-S architecture is fully fracturable, meaning that if one or more of the logic modules in a SuperCluster are used by a particular signal path, the other logic modules are still available for use by other paths.

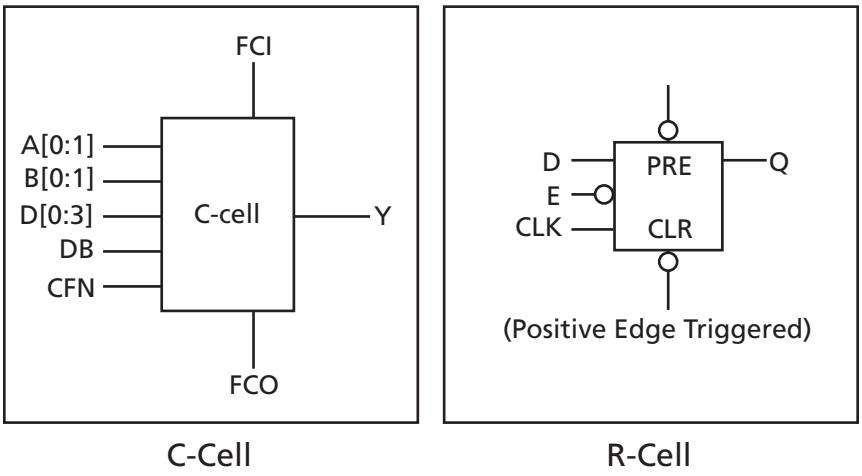


Figure 1-3 • **RTAX-S C-Cell and R-Cell**

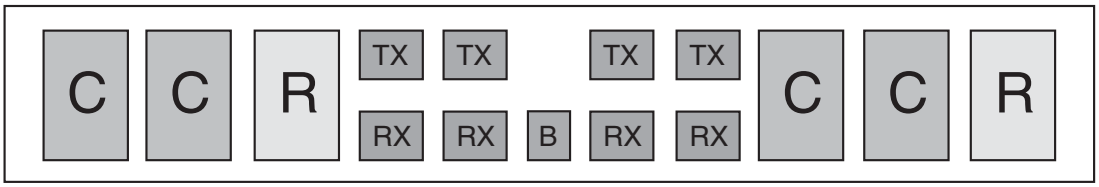


Figure 1-4 • **RTAX-S SuperCluster**

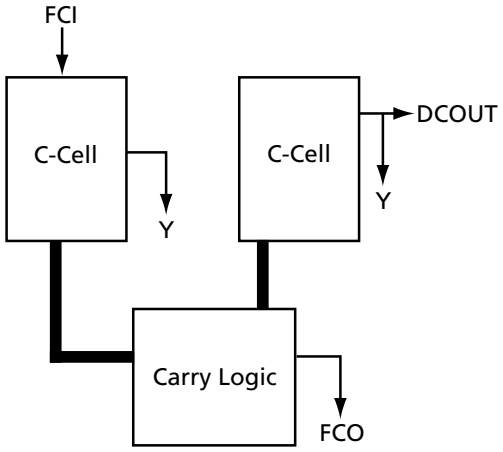


Figure 1-5 • **RTAX-S Two-Bit Carry Logic**

At the chip level, SuperClusters are organized into core tiles, which are arrayed to build up the full chip. For example, the RTAX1000S is composed of a 3x3 array of nine core tiles. Surrounding the array of core tiles are blocks of I/O Clusters and the I/O bank ring (Table 1-1).

Each core tile consists of an array of 336 SuperClusters and four SRAM blocks (176 SuperClusters and three SRAM blocks for the RTAX250S). The SRAM blocks are arranged in a column on the west side of the tile (Figure 1-6).

Table 1-1 • **Number of Core Tiles per Device**

Device	Number of Core Tiles
RTAX250S	4 smaller tiles
RTAX1000S	9 regular tiles
RTAX2000S	16 regular tiles

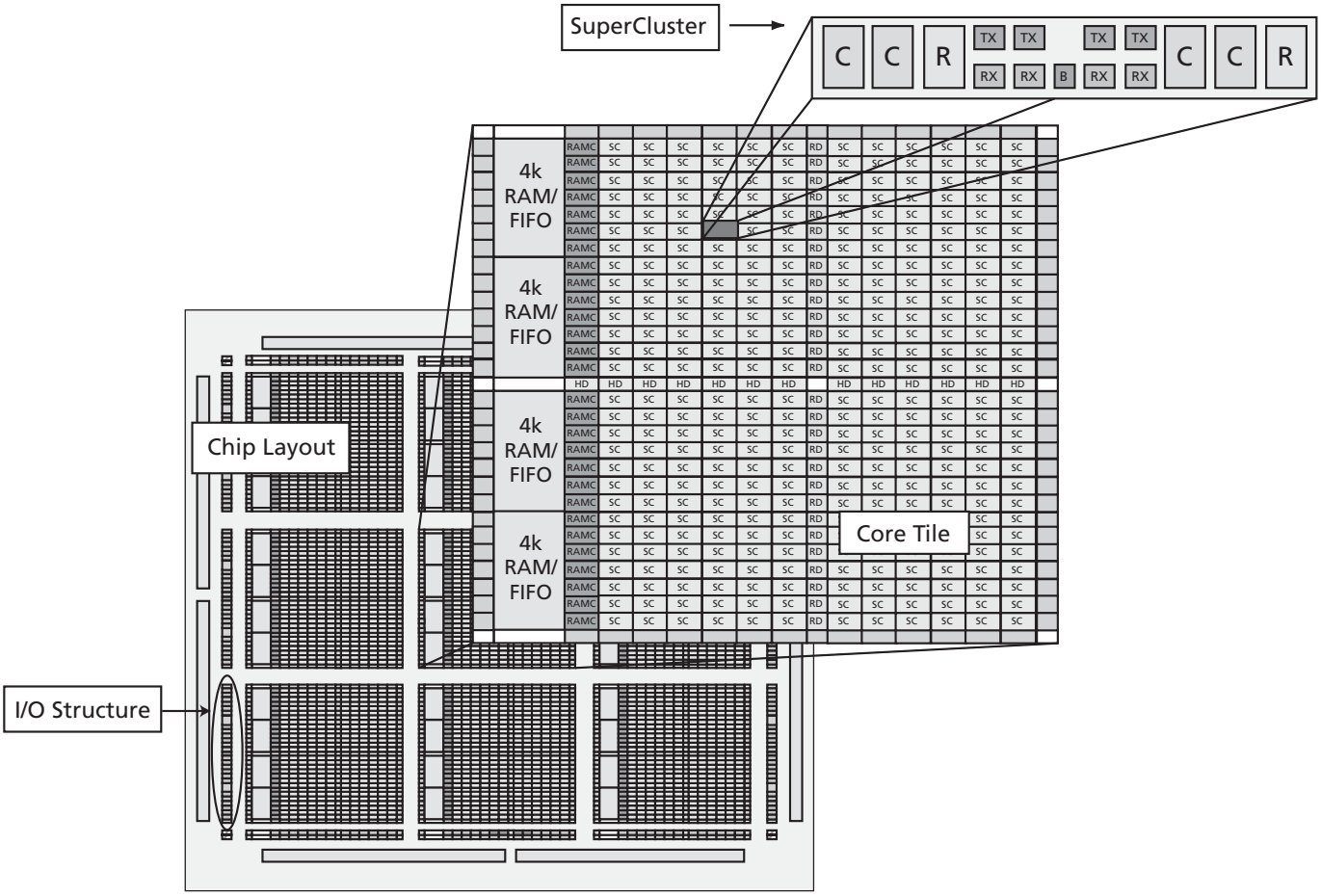


Figure 1-6 • **RTAX-S Device Architecture (RTAX1000S shown)**

Embedded Memory

As mentioned earlier, each core tile has either three (in a smaller tile) or four (in the regular tile) embedded SRAM blocks along the west side, and each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2 or 4kx1 bits. The individual blocks have separate read and write ports that can be configured with different bit widths on each port. For example, data can be written in by eight and read out by one.

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using core logic modules. The FIFO width and depth are programmable. The FIFO also features programmable ALMOST-EMPTY (AEMPTY) and ALMOST-FULL (AFULL) flags in addition to the normal EMPTY and FULL flags. In addition to the flag logic, the embedded FIFO control unit also contains the counters necessary for the generation of the read and write address pointers as well as control circuitry to prevent metastability and erroneous operation. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

The FIFO control unit was not implemented with SEU-hardened registers. Designs requiring high SEU tolerance should implement the FIFO control unit from hardened core logic.

SRAM structures are inherently susceptible to upsets caused by high-energy particles encountered in space. High-energy particles can cause an SRAM cell to change state, resulting in the loss or corruption of a valuable data bit. Actel has enhanced the SEU tolerance of the embedded SRAM within RTAX-S by employing the use of two upset-mitigation techniques:

- Actel has developed Error Detection and Correction (EDAC) IP for use with RTAX-S. EDAC can be accomplished by the use of ACTgen-generated Error Correcting Codes (ECC) IP, which employs the use of shortened Hamming Codes
- A background memory-refresher, or scrubber circuitry, which has been embedded into the EDAC IP. The embedded scrubber circuitry periodically refreshes memory in the background to ensure that no data corruption occurs while the memory is not in use.

The use of EDAC IP combined with the embedded memory scrubber circuitry, gives the RTAX-S an SEU radiation performance level of better than 10^{-10} errors/bit-day. See the application note *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs*.

I/O Logic

The RTAX-S family of FPGAs features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os: 1.5V, 1.8V, 2.5V, and 3.3V. In all, RTAX-S FPGAs support at least 14 different I/O standards (single-ended, differential, voltage-referenced). The I/Os are organized into banks, with eight banks per device (two per side). The configuration of these banks determines the I/O standards supported (see "User I/Os" on page 2-11 for more information). All I/O standards are available in each bank.

Each I/O module has an input register (InReg), an output register (OutReg), and an enable register (EnReg) (Figure 1-7 on page 1-6). An I/O Cluster includes two I/O modules, four RX modules, two TX modules, and a buffer (B) module.

Routing

The RTAX-S hierarchical routing structure ties the logic modules, the embedded memory blocks, and the I/O modules together (Figure 1-8 on page 1-6). At the lowest level, in and between SuperClusters, there are three local routing structures: FastConnect, DirectConnect, and CarryConnect routing. DirectConnects provide the highest performance routing inside the SuperClusters by connecting a C-cell to the adjacent R-cell. DirectConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

FastConnects provide high-performance, horizontal routing inside the SuperCluster and vertical routing to the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering a maximum routing delay of 0.4 ns.

CarryConnects are used for routing carry logic between adjacent SuperClusters. They connect the carry-logic FCO output of one C-cell pair to the carry-logic FCI input of the C-cell pair of the SuperCluster below. CarryConnects do not require an antifuse to make the connection and achieve a signal propagation time of less than 0.1 ns.

The next level contains the core tile routing. Over the SuperClusters within a core tile, both vertical and horizontal tracks run across rows or columns, respectively. At the chip level, vertical and horizontal tracks extend across the full length of the device, both north-to-south and east-to-west. These tracks are composed of highway routing that extend the entire length of the device (segmented at core tile boundaries) as well as segmented routing of varying lengths.

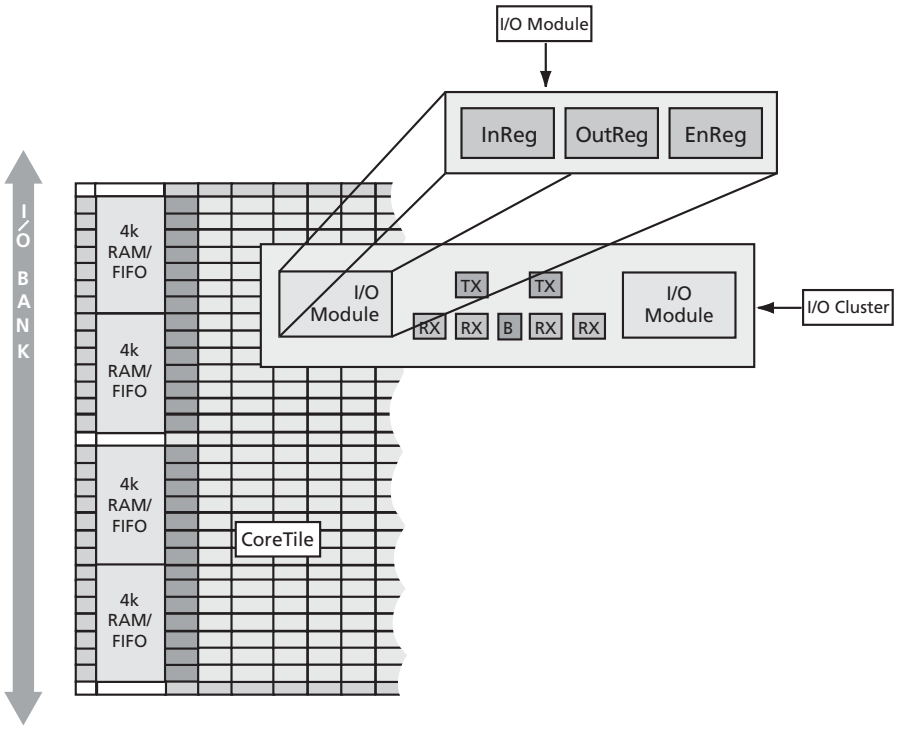


Figure 1-7 • **I/O Cluster Arrangement**

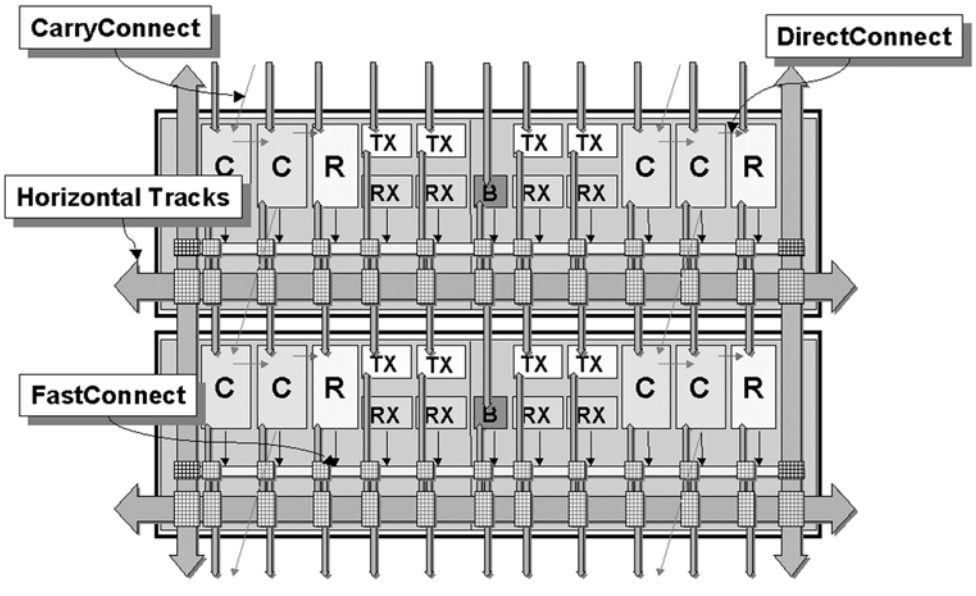


Figure 1-8 • **RTAX-S Routing Structures**

Global Resources

Each family member has three types of global signals available to the designer: HCLK, CLK, and GCLR/GPSET. There are four hardwired clocks (HCLK) per device that can directly drive the clock input of each R-cell. Each of the four routed clocks (CLK) can drive the clock, clear, preset, or enable pin of an R-cell or any input of a C-cell (Figure 1-3 on page 1-3).

Global clear (GCLR) and global preset (GPSET) drive the clear and preset inputs of each R-cell as well as each I/O Register on a chip-wide basis at power-up.

Design Environment

The RTAX-S family of FPGAs is fully supported by both Actel's Libero™ Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the Libero IDE Flow diagram located on Actel's website). Libero IDE includes Synplify® AE from Synplicity®, ViewDraw® AE from Mentor Graphics®, Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD®, and Designer software from Actel.

Actel's Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- Timer – a world-class integrated static timing analyzer and constraints editor which support timing-driven place-and-route
- NetlistViewer – a design netlist schematic viewer
- ChipPlanner – a graphical floorplanner viewer and editor
- SmartPower – allows the designer to quickly estimate the power consumption of a design
- PinEditor – a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor – displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel's back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Actel's integrated verification and logic analysis tool. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors, such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Programming

Programming support is provided through Actel's Silicon Sculptor II, a single-site programmer driven via a PC-based GUI. Factory programming is available for high-volume production needs.

Low-Cost Prototyping Solution

Since the enhanced radiation characteristics of radiation-tolerant devices are not required during the prototyping phase of the design, Actel has developed a prototyping solution for RTAX-S that utilizes commercial Axcelerator devices. The prototyping solution consists of two parts:

- A well-documented design flow that allows the customer to target an RTAX-S design to the equivalent commercial Axcelerator device
- A set of Actel Extender circuit boards that map the commercial device package to the appropriate RTAX-S package footprint

This methodology provides the user with a cost-effective solution while maintaining the short time-to-market associated with Actel FPGAs. Please see the application note *Prototyping RTAX-S Using Axcelerator Devices* for more details.

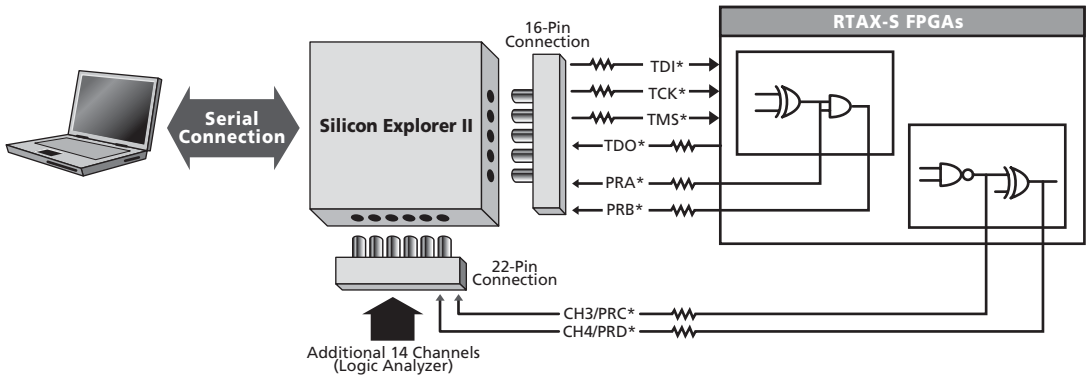
In-System Diagnostic and Debug Capabilities

The RTAX-S family of FPGAs includes internal probe circuitry, allowing the designer to dynamically observe and analyze any signal inside the FPGA without disturbing normal device operation. Up to four individual signals can be brought out to dedicated probe pins (PRA/B/C/D) on the device. The probe circuitry is accessed and controlled via Silicon Explorer II (Figure 1-9 on page 1-8), Actel's integrated verification and logic analysis tool that attaches to the serial port of a PC and communicates with the FPGA via the JTAG port (See "Silicon Explorer II Probe Interface" on page 2-79).

In addition, Actel offers a Configurable Logic Analyzer Module (CLAM), which allows a real-time verification and debug capability to be embedded into IP programmed into Actel FPGAs. CLAM allows signals from the inside of the IP core to be routed to the exterior of the chip for verification purposes.

Summary

Actel's RTAX-S family of FPGAs extends the successful RTSX-S family of radiation-tolerant FPGAs, adding embedded RAM, FIFOs, and high-speed I/Os. With the support of a suite of robust software tools, design engineers can incorporate high gate counts and fixed pins into an RTAX-S design yet still achieve high performance and efficient device utilization in an SEU-hardened device.



Note: **Refer to the "Pin Descriptions" on page 2-9 for more information.*

Figure 1-9 • **Probe Setup**

Related Documents

Application Notes

Simultaneous Switching Noise and Signal Integrity
http://www.actel.com/documents/SSN_AN.pdf
Differences Between RTAX-S and Axcelerator
http://www.actel.com/documents/RTAXS_AX_Features_AN.pdf
Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs
http://www.actel.com/documents/EDAC_AN.pdf
Prototyping RTAX-S Using Axcelerator Devices
http://www.actel.com/documents/PrototypingRTAXS_AN.pdf
Implementing DDR Transmit in Axcelerator
http://www.actel.com/documents/AX_DDR_AN.pdf
Implementation of Security in Actel Antifuse FPGAs
http://www.actel.com/documents/Antifuse_Security_AN.pdf
Actel CQFP to FBGA Adapter Socket Instructions
http://www.actel.com/documents/CCGA_FBGA_AN.pdf
Actel CCGA to FBGA Adapter Socket Instructions
http://www.actel.com/documents/CQ352-FPGA_Adapter_AN.pdf
IEEE Standard 1149.1 (JTAG) in the Axcelerator Family
http://www.actel.com/documents/AX_JTAG_AN.pdf

User's Guides and Manuals

Antifuse Macro Library Guide
http://www.actel.com/documents/libguide_UG.pdf
ACTgen Macros User's Guide
http://www.actel.com/documents/genguide_UG.pdf
Silicon Sculptor II User's Guide
http://www.actel.com/techdocs/manuals/default.asp
Silicon Explorer II User's Guide
http://www.actel.com/documents/Silexpl_UG.pdf

White Papers

Design Security in Nonvolatile Flash and Antifuse FPGAs
http://www.actel.com/documents/DesignSecurity_WP.pdf
Understanding Actel Antifuse Device Security
http://www.actel.com/documents/AntifuseSecurity_WP.pdf

Miscellaneous

Libero IDE flow diagram
http://www.actel.com/products/tools/libero/flow.html

Detailed Specifications

Table 2-1 • **I/O Features Comparison**

I/O Assignment	Clamp Diode	Hot Insertion	5V Tolerance	Input Buffer	Output Buffer
LVTTL	No	Yes	No	Enabled/Disabled	
3.3V PCI	Yes	No	Yes[1]	Enabled/Disabled	
LVCMOS2.5V	No	Yes	No	Enabled/Disabled	
LVCMOS1.8V	No	Yes	No	Enabled/Disabled	
LVCMOS1.5V (JESD8-11)	No	Yes	No	Enabled/Disabled	
Voltage-Referenced Input Buffer	No	Yes	No	Enabled/Disabled	
Differential, LVDS/LVPECL, Input	No	Yes	No	Enabled	Disabled[2]
Differential, LVDS/LVPECL, Output	No	Yes	No	Disabled	Enabled[3]

Notes:

1. *Can be implemented with an external resistor.*
2. *The OE input of the output buffer is automatically deasserted by Designer.*
3. *The OE input of the output buffer is automatically asserted by Designer.*

5V Tolerance

3.3V PCI is the only I/O standard that directly allows 5V tolerance. This standard provides an internal clamp diode between the input pad, and the V_{CCI} pad so that the voltage at the input pin is clamped as shown in EQ 2-1:

$$V_{input} = V_{CCI} + V_{diode} = 3.3V + 0.8V = 4.1V$$

EQ 2-1

An external series resistor (~100Ω) is required between the input pin and the 5V signal source to limit the current (Figure 2-1).

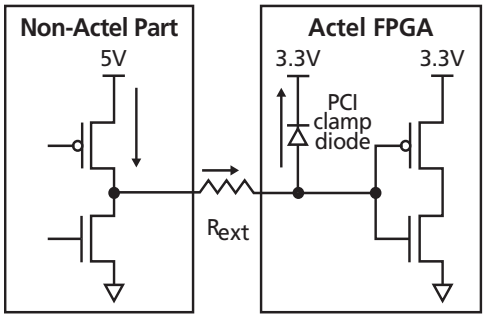


Figure 2-1 • **Use of an External Resistor for 5V Tolerance**

Operating Conditions

Absolute Maximum Conditions

Stresses beyond those listed in Table 2-2 may cause permanent damage to the device. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the recommended operating conditions in Table 2-3.

Table 2-2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CCA}	AC Core Supply Voltage[1]	–0.3 to 1.8	V
V_{CCA}	DC Core Supply Voltage	–0.3 to 1.7	V
V_{CCI}	DC I/O Supply Voltage	–0.3 to 3.75	V
V_{REF}	DC I/O Reference Voltage	–0.3 to 3.75	V
V_I	Input Voltage	–0.5 to 3.75	V
V_O	Output Voltage	–0.5 to 3.75	V
T_{STG}	Storage Temperature	–60 to +150	°C
V_{CCDA}[2]	Supply Voltage for Differential I/Os	–0.3 to 3.75	V

Notes:

1. *The AC transient V_{CCA} limit is for radiation-induced transients less than 10 µs duration and not intended for repetitive use. Core voltage spikes from a single event transient will not negatively affect the reliability of the device if, for this non-repetitive event, the transient does not exceed 1.8 V at any time and the total time that the transient exceeds 1.575 V does not exceed 10 µs in duration.*
2. *Should be the maximum of all VI.*

Table 2-3 • **Recommended Operating Conditions**

Parameter Range	Military	Units
Ambient Temperature (T_A)[1]	–55 to +125	°C
1.5V Core Supply Voltage	1.425 to 1.575	V
1.5V I/O Supply Voltage	1.425 to 1.575	V
1.8V I/O Supply Voltage	1.71 to 1.89	V
2.5V I/O Supply Voltage	2.375 to 2.625	V
3.3V I/O Supply Voltage	3.0 to 3.6	V
2.5V V_{CCDA} I/O Supply Voltage (no differential I/O used)	2.375 to 2.625	V
3.3V V_{CCDA} I/O Supply Voltage (differential or voltage-referenced I/O used)[2]	3.0 to 3.6	V
3.3V V_{PUMP} Supply Voltage	3.0 to 3.6	V

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial grades; case temperature (T_C) is used for military grades.*
2. *Please see "VCCDA Supply Voltage" on page 2-9 more detail.*

Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period or 11 ns (whichever is smaller). Current during the transition must not exceed 95 mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period or 11 ns (whichever is smaller). Current during the transition must not exceed 95 mA.

Note: The above specification does not apply to the PCI standard. The RTAX-S PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

Power-Up/Down Sequence

All RTAX-S I/Os are tristated during power-up until normal device operating conditions are reached, when I/Os enter user mode. V_{CCA}, V_{CCI}, and V_{CCDA} can be powered up or powered down in any sequence.

Calculating Power Dissipation

Table 2-4 • **Standby Current**

Device	Temperature (T_A)	I_{CCA} (mA)	I_{CCI} (mA)	I_{CCDA} (mA)	I_{IH}/I_{IL}
RTAX2000S	25°C	50	10	7	1uA
	125°C	500	35	10	5uA
RTAX1000S	25°C	30	10	7	1uA
	125°C	450	35	10	5uA
RTAX250S	25°C	20	5	5	1uA
	125°C	250	20	10	5uA

Notes:

1. *For calculating the leakage values, use a pull-down/pull-up resistor value of 60 Ω.*
2. *Above values are maximum.*
3. *Values in the I_{CCDA} column refer to the current consumed by all the I/Os.*

Table 2-5 • **Default C_{load}/V_{CCI}**

	C_{LOAD} (pF)	V_{CCI} (V)	P_{LOAD} (uW/MHz)	P_{10} (uW/MHz)	$P_{I/O}$ (uW/MHZ)*
Single-Ended without V_{REF}					
LVCMOS – 15 (JESD8-11)	35	1.5	78.75	49.0	127.8
LVCMOS – 18	35	1.8	113.4	72.8	186.2
LVCMOS – 25	35	2.5	218.75	147.5	366.2
LVTTL 8mA Low Slew	35	3.3	381.15	118.2	499.4
LVTTL 12mA Low Slew	35	3.3	381.15	138.1	519.2
LVTTL 16mA Low Slew	35	3.3	381.15	150.3	531.5
LVTTL 24mA Low Slew	35	3.3	381.15	168.7	549.8
LVTTL 8mA High Slew	35	3.3	381.15	129.8	511.0
LVTTL 12mA High Slew	35	3.3	381.15	165.4	546.5
LVTTL 16mA High Slew	35	3.3	381.15	224.6	605.7
LVTTL 24mA High Slew	35	3.3	381.15	267.0	648.1
PCI	10	3.3	108.9	218.0	326.9
PCI-X	10	3.3	108.9	162.4	271.3
Single-Ended with V_{REF}					
SSTL2-I	30	2.5	–	171.2	171.2
SSTL2-II	30	2.5	–	147.8	147.8
SSTL3-I	30	3.3	–	327.2	327.2
SSTL3-II	30	3.3	–	288.4	288.4
HSTL-I	20	1.5	–	40.9	40.9
GTLP – 33	10	3.3	–	TBD	TBD
Differential					
LVPECL – 33	N/A	3.3	–	260.1	260.1
LVDS – 25	N/A	2.5	–	145.3	145.3

Notes:

1. *$*P_{I/O} = P_{10} + C_{LOAD} * V_{CCI}^2$*
2. *Above values are maximum values.*

Table 2-6 • **Different Components Contributing to the Total Power Consumption in RTAX-S Devices**

Symbol	Power Component	Device-Specific Value (in µW/MHz)		
		RTAX250S	RTAX1000S	RTAX2000S
P1	Core tile HCLK power component	85.8	227.5	378.0
P2	R-cell power component	0.6	0.6	0.6
P3	HCLK signal power dissipation	7.7	23.2	31.0
P4	Core tile RCLK power component	1.8	227.5	378.0
P5	R-cell power component	0.9	0.9	0.9
P6	RCLK signal power dissipation	8.6	25.7	34.3
P7	Power dissipation due to the switching activity on the R-cell	1.6	1.6	1.6
P8	Power dissipation due to the switching activity on the C-cell	1.4	1.4	1.4
P9	Power component associated with the input voltage	10.0	10.0	10.0
P10	Power component associated with the output voltage	See table Per pin contribution		
P11	Power component associated with the read operation in the RAM block	25.0	25.0	25.0
P12	Power component associated with the write operation in the RAM block	30.0	30.0	30.0

$P_{total} = P_{dc} + P_{ac}$

P_{dc} = TBD

P_{ac} = $P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory}$

P_{HCLK}= (P1 + P2 * s + P3 * sqrt[s]) * Fs

s = number of R-cells clocked by this clock

Fs = clock frequency

P_{CLK} = (P4 + P5 * s + P6 * sqrt[s]) * Fs

s = number of R-cells clocked by this clock

Fs = clock frequency

$P_{R\text{-}cells}$ = P7 * ms * Fs

ms = number of R-cells switching at each Fs cycle

Fs = clock frequency

$P_{C\text{-}cells}$ = P8 * mc * Fs

mc = number of C-cells switching at each Fs cycle

Fs = clock frequency

P_{inputs} = P9 * pi * F_{pi}

pi = number of inputs

F_{pi} = average input frequency

$P_{outputs}$ = (P10 + C_{load} * V_{CCI}^2) * po * F_{po}

C_{load} = output load (technology dependent)

V_{CCI} = output voltage (technology dependent)

po = number of outputs

F_{po} = average output frequency

$P_{memory} = P11 * N_{block} * F_{RCLK} + P12 * N_{block} * F_{WCLK}$

N_{block} = number of RAM/FIFO blocks (1 block = 4k)
F_{RCLK} = read-clock frequency of the memory
F_{WCLK} = write-clock frequency of the memory

Power Estimation Example

This example employs an RTAX1000S shift-register design with 1,080 R-cells, one C-cell, one reset input, and one output. This design also uses a single clock (HCLK) at 100 MHz.

ms = 1,080 (in a shift register 100% of R-cells are toggling at each clock cycle)

Fs = 100 MHz
s = 1,080
=> $P_{HCLK} = (P1 + P2 * s + P3 * sqrt[s]) * Fs = 163.8$ mW
and Fs = 100 MHz
=> $P_{R\text{-}cells} = P7 * ms * Fs = 172.8$ mW
mc = 1 (1 C-cell in this design)
and Fs = 100 MHz
=> $P_{C\text{-}cells} = P8 * mc * Fs = 0.14$ mW
F_{pi} ~ 0 MHz
and pi= 1 (1 reset input => this is why F_{pi}=0)
=> $P_{inputs} = P9 * pi * F_{pi} = 0$ mW
F_{po} = 50 MHz
C_{load} = 35 pF
V_{CCI}= 3.3 V
and po = 1
=> $P_{outputs} = (P10 + C_{load} * V_{CCI}^2) * po * F_{po} = 23.6$ mW
No RAM/FIFO in this shift-register
=> $P_{memory} = 0$ mW
P_{ac} = $P_{HCLK} + P_{CLK} + P_{R\text{-}cells} + P_{C\text{-}cells} + P_{inputs} + P_{outputs} + P_{memory} = 360.4$ mW
P_{dc} = TBD
P_{total} = $P_{dc} + P_{ac} = 360.4$ mW + P_{dc}

Thermal Characteristics

Introduction

The temperature variable in Actel's Designer software refers to the junction temperature, not the ambient, case or board temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient, case, or board temperature. EQ 2-2, EQ 2-3, and EQ 2-4 give the relationship between thermal resistance, temperature gradient and power.

$$\theta_{ja} = \frac{T_j - T_a}{P} \quad \text{EQ 2-2}$$

$$\theta_{jc} = \frac{T_j - T_c}{P} \quad \text{EQ 2-3}$$

$$\theta_{jb} = \frac{T_j - T_b}{P} \quad \text{EQ 2-4}$$

Where:

θ_{ja} = Junction-to-air thermal resistance of the package. θ_{ja} numbers are located under Table 2-7.

θ_{jc} = Junction-to-case thermal resistance of the package. θ_{jc} numbers are located under Table 2-7.

θ_{jb} = Junction-to-board thermal resistance of the package. θ_{jb} for a 624-pin CCGA is located in the notes for Table 2-7.

T_j = Junction Temperature

T_a = Ambient Temperature

T_b = Board Temperature

T_c = Case Temperature

P = Power

Package Thermal Characteristics

The device thermal characteristics θ_{jc} and θ_{ja} are given in Table 2-7. The thermal characteristics for θ_{ja} are shown with two different air flow rates. Note that the absolute maximum junction temperature is 125°C.

Table 2-7 • **Package Thermal Characteristics**

Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 1.0m/s	θ_{ja} 2.5m/s	Units
Ceramic Quad Flat Pack (CQFP)[1]	208	2.0	22.0	19.8	18.0	°C/W
Ceramic Quad Flat Pack (CQFP)[1]	352	2.0	17.9	16.1	14.7	°C/W
Ceramic Column Grid Array (CCGA)[2,3]	624	6.5	8.9	8.5	8.0	°C/W
Land Grid Array (LGA)	624	2.0	8.9	8.5	8.0	°C/W
Ceramic Column Grid Array (CCGA)[2,3]	1152	6.5				°C/W
Land Grid Array (LGA)	1152	2.0				°C/W

Notes:

1. *θ_{jc} for CQFP packages refers to the thermal resistance between the junction and the bottom of the package.*
2. *θ_{jc} for CCGA packages refers to the thermal resistance between the junction and the top of the package.*
3. *Thermal resistance from junction to board (θ_{jb}) for the 624-pin CCGA is 3.4 °C/W.*

Maximum Allowed Power Dissipation

Shown below are example calculations to estimate the maximum allowed power dissipation for a given device based upon two different thermal environments while maintaining the device junction temperature at or below worst-case military operating conditions (125°C).

Example 1:

This example assumes that there is still air in the environment. The heat flow is shown by the arrows in Figure 2-2 on page 2-7. The maximum ambient air temperature is assumed to be 50°C; the device package used is the 624-pin CCGA.

$$\text{Max. Allowed Power} = \frac{\text{Max Junction Temp} - \text{Max. Ambient Temp}}{\theta_{ja}} = \frac{125°C - 50°C}{8.9°C/W} = 8.43W$$

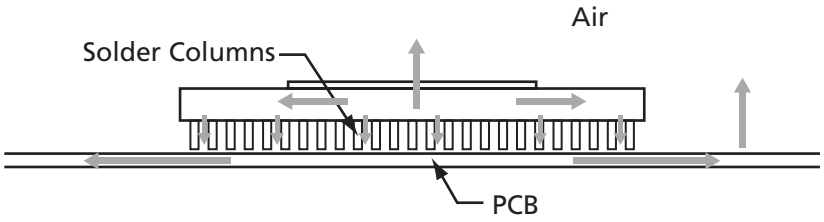


Figure 2-2 • **Hear Flow when Air is Present**

Example 2:

This example assumes that the primary heat conduction path will be through the bottom of the package (neglecting the heat conducted through the package pins) to the board for a package mounted with thermal paste. The heat flow is shown by the arrows in Figure 2-3. The maximum board temperature is assumed to be 70°C. The device package used is the 352-pin CQFP. The thermal resistance (θ_{cb}) of the thermal paste is assumed to be 0.58 °C/W.

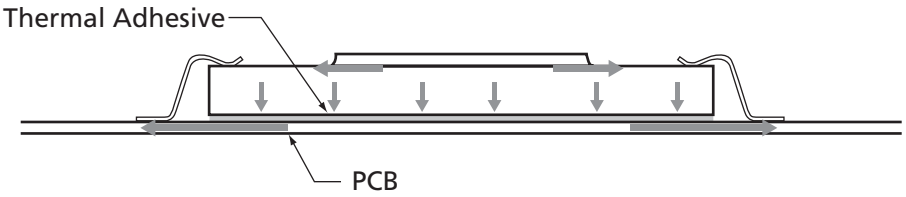


Figure 2-3 • **Heat Flow in a Vacuum**

$$\text{Max. Allowed Power} = \frac{T_j - T_b}{\theta_{jb}} = \frac{T_j - T_b}{\theta_{jc} + \theta_{cb}} = \frac{125°C - 70°C}{2.0°C/W + 0.58°C/W} = 21.32W$$

Timing Derating

RTAX-S devices are manufactured in a CMOS process, therefore, device performance is dependent upon temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing. The derating factors shown in Table 2-8 should be applied to all timing data contained within this datasheet.

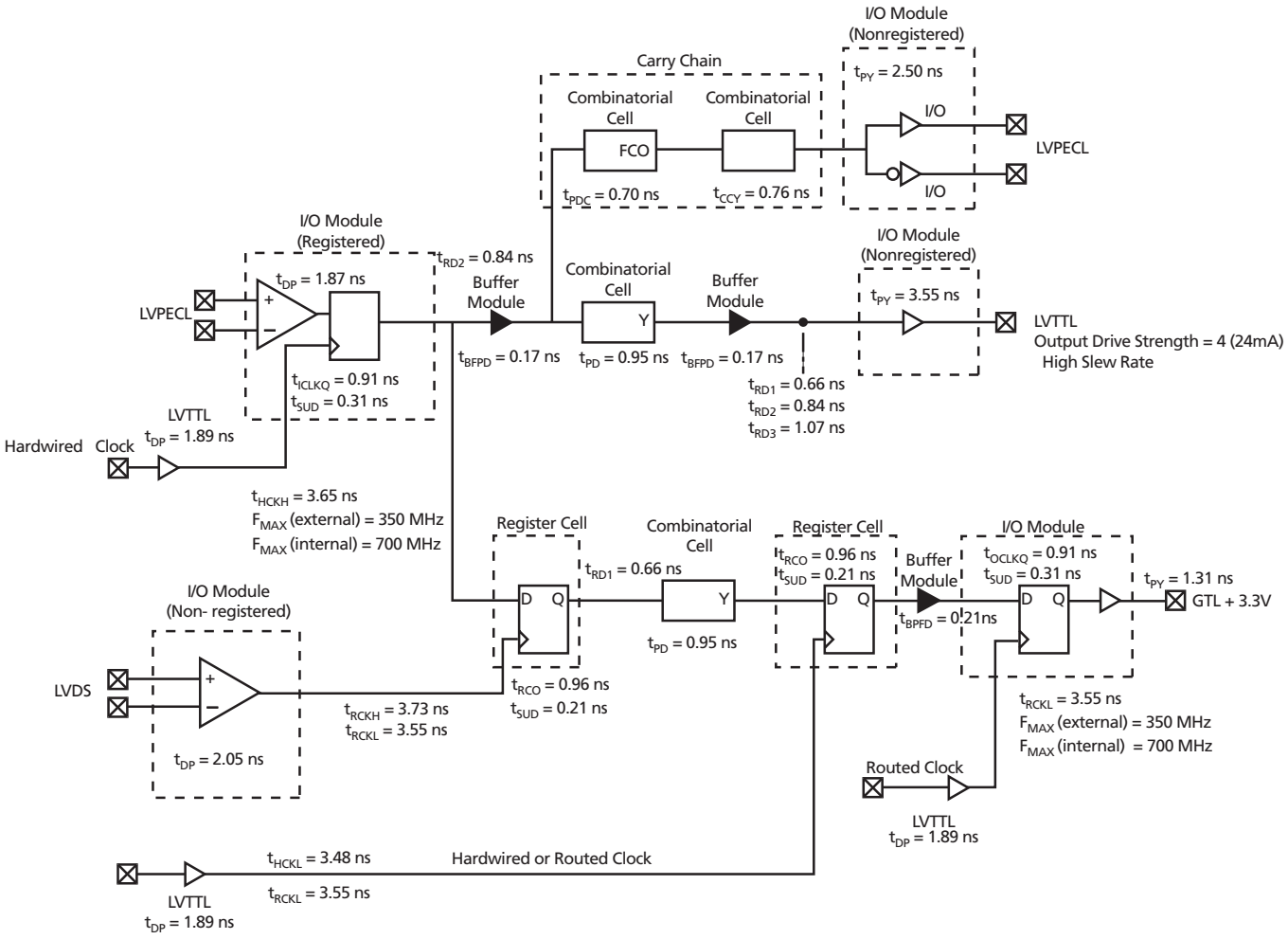
Table 2-8 • **Temperature and Voltage Timing Derating Factors (Normalized to Worst-Case Military = 125°C, V_{CCA} = 1.4V)**

	Junction Temperature						
V_{CCA}	**–55°C**	**–40°C**	**–0°C**	**25°C**	**70°C**	**85°C**	**125°C**
1.4V	0.73	0.75	0.80	0.84	0.89	0.92	1.00
1.425V	0.72	0.74	0.79	0.82	0.87	0.90	0.98
1.5V	0.69	0.70	0.75	0.78	0.83	0.86	0.93
1.525V	0.66	0.68	0.72	0.75	0.80	0.83	0.90
1.6V	0.65	0.67	0.71	0.74	0.79	0.81	0.88

Notes:

1. *The user can set the junction temperature in Designer software to be any integer value in the range of –55°C to 125°C.*
2. *The user can set the core voltage in Designer software to be any value between 1.4V to 1.6V.*

Timing Model



Note: *Timing data is for the RTAX2000S, –1 speed.*

Figure 2-4 • **Timing Model**

Hardwired Clock

External Setup

= $(t_{DP} + t_{RD2} + t_{SUD}) - t_{HCKH}$

= (1.87 + 0.84 + 0.21) – 3.65

= –0.73

Clock-to-Out (Pad-to-Pad)

= $t_{HCKH} + t_{RCO} + t_{RD1} + t_{PY}$

= 3.65 + 0.96 + 0.66 + 3.55

= 8.82 ns

Routed Clock

External Setup

= $(t_{DP} + t_{RD2} + t_{SUD}) - t_{RCKH}$

= (1.87 + 0.84 + 0.21) – 3.73

= –0.81 ns

Clock-to-Out (Pad-to-Pad)

= $t_{RCKH} + t_{RCO} + t_{RD1} + t_{PY}$

= 3.73 + 0.96 + 0.66 + 3.55

= 8.90 ns

I/O Specifications

Pin Descriptions

Supply Pins

GND **Ground**

Low supply voltage.

V_{CCA} **Supply Voltage**

Supply voltage for array (1.5V).

V_{CCIBx} **Supply Voltage**

Supply voltage for I/Os. Bx is the I/O Bank ID – 0 to 7. See "User I/Os" on page 2-11 for more information.

V_{CCDA} **Supply Voltage**

Supply voltage for the I/O differential amplifier and JTAG and probe interfaces. V_{CCDA} is either 3.3V or 2.5V and must use 3.3V when voltage-referenced and/or differential is used. Additionally, V_{CCDA} must be greater than or equal to any V_{CCI} voltages (i.e. $V_{CCDA} \geq V_{CCI}$Bx).

V_{PUMP} **Supply Voltage (External Pump)**

In low-power mode, V_{PUMP} will be used to access an external charge pump (if the user desires to bypass the internal charge pump to further reduce power). The device starts using the external charge pump when the voltage level on V_{PUMP} reaches 3.3V.[1] In normal device operation, when using the internal charge pump, V_{PUMP} should be tied to GND.

User-Defined Supply Pins

V_{REF} **Supply Voltage**

Reference voltage for I/O banks. V_{REF} pins are configured by the user from regular I/O pins; V_{REF} are not in fixed locations. There can be one or more V_{REF} pins in an I/O bank.

Global Pins

HCLKA/B/C/D **Dedicated (Hardwired) Clocks A, B, C, and D**

These pins are the clock input for sequential modules. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. When the HCLK pins are unused, it is recommended that they are tied to the ground.

CLKE/F/G/H **Global Clocks E, F, G, and H**

These pins are clock inputs for clock distribution networks. Input levels are compatible with all supported I/O standards (there is a P/N pin pair for support of differential I/O standards). The clock input is buffered prior to clocking the R-cells. When the CLK pins are unused, Actel recommends that they are tied to a known state.

1. *When V_{PUMP} = 3.3V, it shuts off the internal charge pump.*

JTAG/Probe Pins

PRA/B/C/D[2] Probes A, B, C, and D

The probe pins are used to output data from any user-defined design node within the device (controlled with Silicon Explorer II). These independent diagnostic pins can be used to allow real-time diagnostic output of any signal path within the device. The pins' probe capabilities can be permanently disabled to protect programmed design confidentiality.

TCK[2] Test Clock

Test clock input for JTAG boundary-scan testing and diagnostic probe (Silicon Explorer II).

TDI[2] Test Data Input

Serial input for JTAG boundary-scan testing and diagnostic probe. TDI is equipped with an internal pull-up resistor with approximately 10 kΩ resistance.

TDO[2] Test Data Output

Serial output for JTAG boundary-scan testing.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 boundary-scan pins (TCK, TDI, TDO, TRST). TMS is equipped with an internal pull-up resistor with approximately 10 kΩ resistance.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with a programmable pull-up resistor with approximately 10 kΩ resistance (i.e. with or without the pull-up resistor). Actel recommends that this pin be hardwired to ground for flight.

Special Functions

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

2. *Actel recommends that you use a series termination resistor on every probe connector (TDI, TCK, TDO, PRA, PRB, PRC, and PRD). The series termination is used to prevent data transmission corruption (i.e., due to reflection from the FPGA to the probe connector) during probing and reading back the checksum. With an internal setup we have seen 70-ohm termination resistor improved the signal transmission. Since the series termination depends on the setup, Actel recommends users to calculate the termination resistor for their own setup. Below is a guideline on how to calculate the resistor value.*
   The resistor value should be chosen so that the sum of it and the probe signal's driver impedance equals the effective trace impedance.
   Z0 = Rs + Zd
   Z0= trace impedance (silicon explorer's breakout cable's resistance + PCB trace impedance), Rs= series termination, Zd= probe signal's driver impedance.
   The termination resistor should be placed as close as possible to the driver.
   Among the probe signals, TDI, TCK, and TMS are driven by Silicon Explorer. A54SX16 is used in Silicon Explorer and hence the driver impedances needs to be calculated from SX08/SX16/SX32 IBIS Model (Mixed Voltage Operation). PRA, PRB, PRC, PRD, and TDO are driven by the FPGA and driver impedance can also be calculated from the IBIS Model.
   Silicon explorer's breakout cable's resistance is usually close to 1 ohm.

User I/Os[3]

Introduction

The RTAX-S family features a flexible I/O structure, supporting a range of mixed voltages (1.5V, 1.8V, 2.5V, and 3.3V) with its bank-selectable I/Os. Table 2-9 contains the I/O standards supported by the RTAX-S family.

Each I/O provides programmable slew rates, drive strengths, and weak pull-up and weak pull-down circuits.

All I/O standards are 3.3V tolerant, and I/O standards, except 3.3V PCI, are capable of hot insertion and cold sparing. 3.3V PCI is also 5V tolerant with the aid of an external resistor (see "5V Tolerance" on page 2-1).

Each I/O includes three registers: an input (InReg), an output (OutReg), and an enable register (EnReg).

I/Os are organized into banks, and there are eight banks per device – two per side (Figure 2-7 on page 2-18). Each I/O bank has a common V_{CCI}, the supply voltage for its I/Os.

For voltage-referenced I/Os, each bank also has a common reference-voltage bus, V_{REF}. While V_{REF} must have a common voltage for an entire I/O bank, its location is user-selectable. In other words, any user I/O in the bank can be selected to be a V_{REF}.

The location of the V_{REF} pin should be selected according to the following rules:

- Any pin that is assigned as a V_{REF} can control a maximum of eight user I/O pad locations in each direction (16 total maximum) within the same I/O bank
- I/O package locations listed as no-connects are counted as part of the 16 maximum. In many cases, this leads to fewer than eight user I/O package pins in each direction being controlled by a V_{REF} pin
- Dedicated I/O pins (GND, V_{CCI}...) are not counted as part of the 16
- The user I/O pad immediately adjacent on either side of the V_{REF} pin may only be used as an input. The exception is when there is a V_{CCI}/GND pair separating the Vref pin and the user I/O pad location

The differential amplifier supply voltage V_{CCDA} should be connected to 3.3V. When neither voltage-referenced nor differential I/Os are used, V_{CCDA} may be connected to 2.5V when V_{CCI} <= 2.5V in a given I/O bank; however, it is still recommended to connect V_{CCDA} to 3.3V.

The user can gain access to the various I/O standards in three ways:

- Instantiate specific library macros that represent the desired specific standard
- Use generic I/O macros and then use Actel Designer's PinEditor to specify the desired I/O standards. (Please note that this is not applicable to differential standards.)
- A combination of the first two methods

Please refer to the *I/O Features in AX-S Family Devices* application note and the *Antifuse Macro Library Guide* for more details.

Table 2-9 • **I/O Standards Supported by the RTAX-S Family**

I/O Standard	Input/Output Supply Voltage (V_{CCI})	Input Reference Voltage (V_{REF})	Board Termination Voltage (V_{TT})
LVTTL	3.3	N/A	N/A
LVCMOS 2.5V	2.5	N/A	N/A
LVCMOS 1.8V	1.8	N/A	N/A
LVCMOS 1.5V (JDEC8-11)	1.5	N/A	N/A
3.3V PCI	3.3	N/A	N/A
GTL+ 3.3V	3.3	1.0	1.2
GTL+ 2.5V*	2.5	1.0	1.2
HSTL Class 1	1.5	0.75	0.75
SSTL3 Class 1 and II	3.3	1.5	1.5
SSTL2 Class1 and II	2.5	1.25	1.25
LVDS	2.5	N/A	N/A
LVPECL	3.3	N/A	N/A

Note: ** 2.5V GTL+ is not supported across the full military temperature range.*

3. *Do not use an external resistor to pull the I/O above VCCI for a higher logic "1" voltage level. The desired higher logic "1" voltage level will be degraded due to a small I/O current, which exists when the I/O is pulled up above VCCI.*

Simultaneous Switching Outputs (SSO)

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. This simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or more commonly, ground bounce.

SSN becomes more of an issue in high pin count packages and when using high performance devices such as the RTAX-S family. Based upon our testing, Actel recommends that users not exceed eight simultaneous switching outputs (SSO) per each V_{CCI}/GND pair. To ease this potential burden on designers, Actel has designed all RTAX-S packaging with the goal to not exceed this limit except for a small number of local violations within some I/O banks.

Please refer to the *Simultaneous Switching Noise and Signal Integrity* application note for more information.

I/O Banks and Compatibility

Since each I/O bank has its own user-assigned input reference voltage (V_{REF}) and an input/output supply voltage (V_{CCI}), only I/Os with compatible standards can be assigned to the same bank.

Table 2-10 shows the compatible I/O standards for a common V_{REF} (for voltage-referenced standards). Similarly, Table 2-11 shows compatible standards for a common V_{CCI}.

Table 2-10 • **Compatible I/O Standards for Different V_{REF} Values**

V_{REF}	Compatible Standards
1.5V	SSTL 3 (Class I and II)
1.25V	SSTL 2 (Class I and II)
1.0V	GTL+ (2.5V and 3.3V Outputs)
0.75V	HSTL (Class I)

Table 2-11 • **Compatible I/O Standards for Different V_{CCI} Values**

V_{CCI}[1]	Compatible Standards	V_{REF}
3.3V	LVTTL, PCI, LVPECL, GTL+ 3.3V	1.0
3.3V	SSTL 3 (Class I and II), LVTTL, PCI, LVPECL	1.5
2.5V	LVCMOS 2.5V, GTL+ 2.5V, LVDS[2]	1.0
2.5V	LVCMOS 2.5V, SSTL 2 (Classes I and II), LVDS[2]	1.25
1.8V	LVCMOS 1.8V	N/A
1.5V	LVCMOS 1.5V, HSTL Class I	0.75

Notes:

1. *V_{CCI} is used for both inputs and outputs.*
2. *V_{CCI} tolerance is* ±5%.

Table 2-12 on page 2-13 summarizes the different combinations of voltages and I/O standards that can be used together in the same I/O bank. Note that two I/O standards are compatible if:

- Their V_{CCI} values are identical
- Their V_{REF} standards are identical (if applicable)

For example, if LVTTL 3.3V (V_{REF}= 1.0V) is used, then the other available (i.e. compatible) I/O standards in the same bank are LVTTL 3.3V PCI, GTL+, and LVPECL.

Also note that when multiple I/O standards are used within a bank, the voltage tolerance will be limited to the minimum tolerance of all I/O standards used in the bank. For instance, when using LVCMOS2.5 (+/-8% V_{CCI} tolerance) and LVDS (+/-5% V_{CCI} tolerance) within an I/O bank, the maximum voltage tolerance of the bank will be +/-5% V_{CCI}.

Table 2-12 • **Legal I/O Usage Matrix**

I/O Standard	LVTTL 3.3V	LVCMOS 2.5V	LVCMOS1.8V	LVCMOS1.5V (JESD8-11)	3.3V PCI	GTL + (3.3V)	GTL + (2.5V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS (2.5V ±5%)	LVPECL (3.3V)
LVTTL 3.3V (V_{REF}=1.0V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVTTL 3.3V(V_{REF}=1.5V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVCMOS 2.5V (V_{REF}=1.0V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVCMOS 2.5V (V_{REF}=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVCMOS1.8V	–	–	✓	–	–	–	–	–	–	–	–	–
LVCMOS1.5V (V_{REF}=1.75V) (JESD8-11)	–	–	–	✓	–	–	–	✓	–	–	–	–
3.3V PCI (V_{REF}=1.0V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
3.3V PCI (V_{REF}=1.5V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓
GTL+ (3.3V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
GTL+ (2.5V)	–	✓	–	–	–	–	✓	–	–	–	–	–
HSTL Class I	–	–	–	✓	–	–	–	✓	–	–	–	–
SSTL2 Class I & II	–	✓	–	–	–	–	–	–	✓	–	✓	–
SSTL3 Class I & II	✓	–	–	–	✓	–	–	–	–	✓	–	✓
LVDS (V_{REF}=1.0V)	–	✓	–	–	–	–	✓	–	–	–	✓	–
LVDS (V_{REF}=1.25V)	–	✓	–	–	–	–	–	–	✓	–	✓	–
LVPECL (V_{REF}=1.0V)	✓	–	–	–	✓	✓	–	–	–	–	–	✓
LVPECL (V_{REF}=1.5V)	✓	–	–	–	✓	–	–	–	–	✓	–	✓

Notes:

1. *Note that GTL+2.5V is not supported across the full military temperature range.*
2. *A "✓" indicates whether standards can be used within a bank at the same time.*
   Examples:
   a) LVTTL can be used with 3.3V PCI and GTL+ (3.3V), when V_{REF} = 1.0V (GTL+ requirement).
   b) LVTTL can be used with 3.3V PCI and SSTL3 Class I and II, when V_{REF} = 1.5V (SSTL3 requirement).
   c) LVDS V_{CCI} = 2.5V ±5%.

I/O Clusters

Each I/O cluster incorporates two I/O modules, four RX modules and two TX modules, and a buffer module. In turn, each I/O module contains one Input Register (InReg), one Output Register (OutReg), and one Enable Register (EnReg) (Figure 2-5).

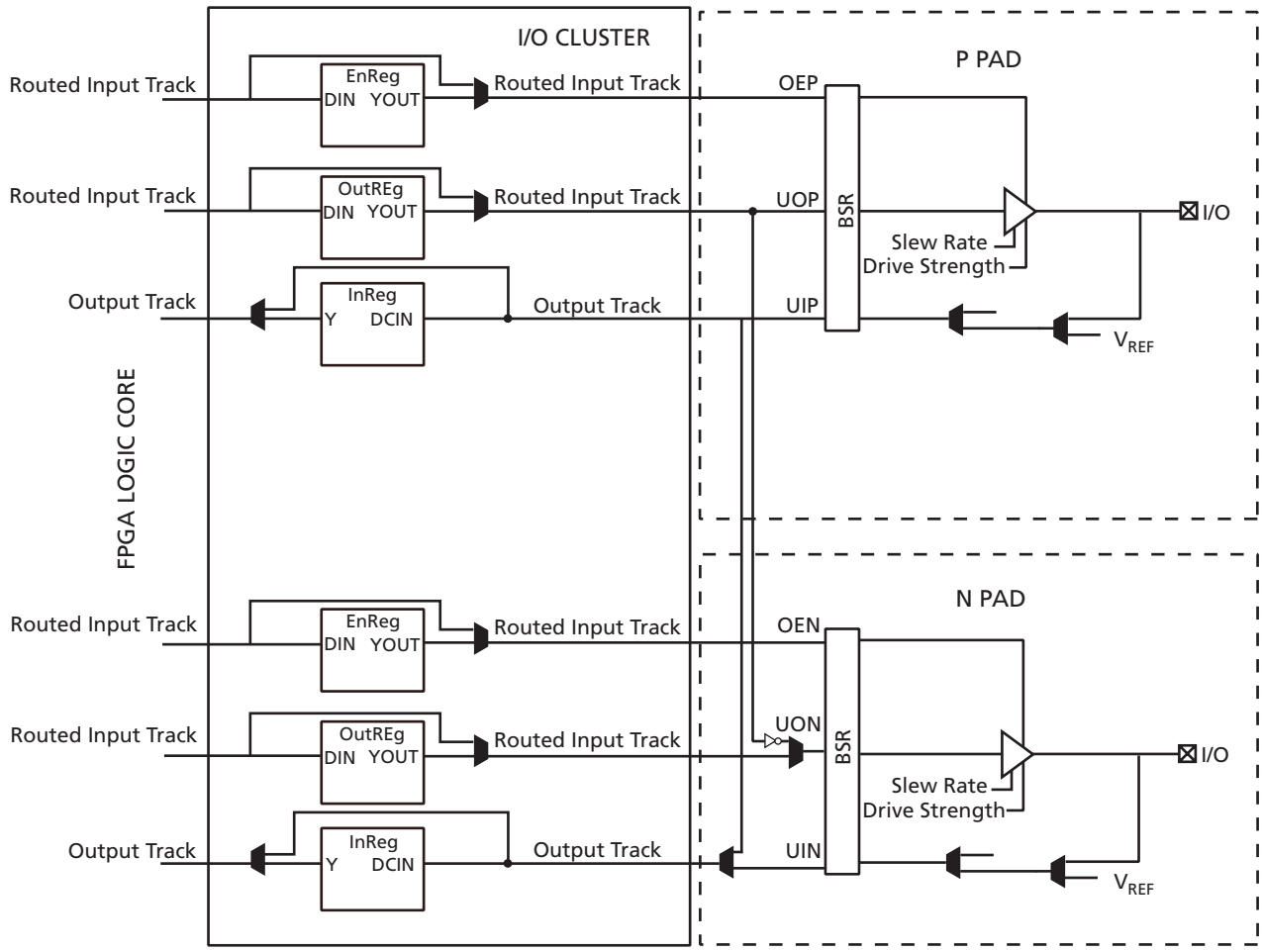


Figure 2-5 • **I/O Cluster Interface**

Using an I/O Register

To access the I/O registers, registers must be instantiated in the netlist and then connected to the I/Os. Usage of each I/O register (register combining) is individually controlled and can be selected/deselected using the PinEditor tool in Actel's Designer software. I/O register combining can also be controlled at the device level, affecting all I/Os. Please note, the I/O register option is deselected by default in any given design.[4]

In addition, Designer software provides a global option to enable/disable the usage of registers in the I/Os. This option is design specific. The setting for each individual I/O overrides this global option. Furthermore, the Global Set Fuse option in the Designer software, when checked, causes all I/O registers to output logic HIGH at device power-up.

Using the Weak Pull-Up and Pull-Down Circuits

Each RTAX-S I/O comes with a weak pull-up/down circuit (on the order of 10 kΩ). I/O macros are provided for combinations of pull up/down for LVTTL, LVCMOS (2.5V, 1.8V, and 1.5V) standards. These macros can be instantiated if a keeper circuit for any input buffer is required.

4. *Please note that register combining for multi fanout nets is not supported.*

Customizing the I/O

RTAX-S I/O slew-rates and drive strength can be customized:

- The slew-rate value for the LVTTL output buffer can be programmed and can be set to either slow or fast.
- The drive strength value for LVTTL output buffers can be programmed as well. There are four different drive strength values – 8mA, 12mA, 16mA, or 24mA – that can be specified in Designer.[5]

Using the Differential I/O Standards

Differential I/O macros should be instantiated in the netlist. The settings for these I/O standards cannot be changed inside Designer. Please note that there are no tristated or bidirectional I/O buffers for differential standards.

Using the Voltage-Referenced I/O Standards

Using these I/O standards is similar to that of single-ended I/O standards. Their settings can be changed in Designer.

Using DDR (Double Data Rate)

In Double Data Rate mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidth and signal integrity requirements, making it very efficient for implementing very high-speed systems.

To implement a DDR, users need to:

1. Instantiate an input buffer (with the required I/O standard).
2. Instantiate the DDR_REG macro (Figure 2-6).
3. Connect the output from the Input buffer to the input of the DDR macro.

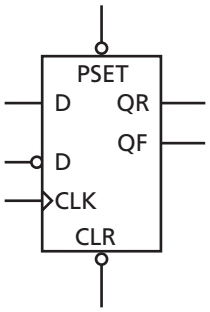


Figure 2-6 • **DDR Register**

Macros for Specific I/O Standards

There are different macro types for any I/O standard or feature that determine the required V_{CCI} and V_{REF} voltages for an I/O. The generic buffer macros require the LVTTL standard with slow slew rate and 24mA-drive strength. LVTTL can support high slew rate but this should only be used for critical signals.

Most of the macro symbols represent variations of the six generic symbol types:

- CLKBUF: Clock Buffer
- HCLKBUF: Hardwired Clock Buffer
- INBUF: Input Buffer
- OUTBUF: Output Buffer
- TRIBUF: Tristate Buffer
- BIBUF: Bidirectional Buffer

Other macros include the following:

- Differential I/O standard macros: The LVDS and LVPECL macros either have a pair of differential inputs (e.g. INBUF_LVDS) or a pair of differential outputs (e.g. OUTBUF_LVPECL).
- Pull-up and pull-down variations of the INBUF, BIBUF, and TRIBUF macros. These are available only with TTL and LVCMOS thresholds. They can be used to model the behavior of the pull-up and pull-down resistors available in the architecture. Whenever an input pin is left unconnected, the output pin will either go high or low rather than unknown. This allows users to leave inputs unconnected without having the negative effect on simulation of propagating unknowns.
- DDR_REG macro. It can be connected to any I/O standard input buffers (i.e. INBUF) to implement a double data rate register. Designer software will map it to the I/O module in the same way it maps the other registers to the I/O module.

Table 2-13, Table 2-14, and Table 2-15 on page 2-17 list all the available macro names differentiated by I/O standard, type, slew rate, and drive strength.

5. *These values are minimum drive strengths.*

Table 2-13 • **Macros for Single-Ended I/O Standards**

Standard	V_{CCI}	Macro Names
LVTTL	3.3V	CLKBUF, HCLKBUF INBUF, OUTBUF, OUTBUF_S_8, OUTBUF_S_12, OUTBUF_S_16, OUTBUF_S_24, OUTBUF_H_8, OUTBUF_H_12, OUTBUF_H_16, OUTBUF_H_24, TRIBUF, TRIBUF_S_8, TRIBUF_S_12, TRIBUF_S_16, TRIBUF_S_24, TRIBUF_H_8, TRIBUF_H_12, TRIBUF_H_16, TRIBUF_H_24, BIBUF, BIBUF_S_8, BIBUF_S_12, BIBUF_S_16, BIBUF_S_24, BIBUF_H_8, BIBUF_H_12, BIBUF_H_16, BIBUF_H_24,
3.3V PCI	3.3V	CLKBUF_PCI, HCLKBUF_PCI, INBUF_PCI, OUTBUF_PCI, TRIBUF_PCI, BIBUF_PCI
LVCMOS25	2.5V	CLKBUF_LVCMOS25, HCLKBUF_LVCMOS25, INBUF_LVCMOS25, OUTBUF_LVCMOS25, TRIBUF_LVCMOS25, BIBUF_LVCMOS25
LVCMOS18	1.8V	CLKBUF_LVCMOS18, HCLKBUF_LVCMOS18, INBUF_LVCMOS18, OUTBUF_LVCMOS18, TRIBUF_LVCMOS18, BIBUF_LVCMOS18
LVCMOS15 (JESD8-11)	1.5V	CLKBUF_LVCMOS15, HCLKBUF_LVCMOS15, INBUF_LVCMOS15, OUTBUF_LVCMOS15, TRIBUF_LVCMOS15, BIBUF_LVCMOS15

Table 2-14 • **I/O Macros for Differential I/O Standards**

Standard	V_{CCI}	Macro Names
LVPECL	3.3V	CLKBUF_LVPECL, HCLKBUF_LVPECL, INBUF_LVPECL, OUTBUF_LVPECL
LVDS	2.5V	CLKBUF_LVDS, HCLKBUF_LVDS, INBUF_LVDS, OUTBUF_LVDS

Table 2-15 • **I/O Macros for Voltage-Referenced I/O Standards**

Standard	V_{CCI}	V_{REF}	Macro Names
GTL+	3.3 V	1.0 V	CLKBUF_GTP33, HCLKBUF_GTP33, INBUF_GTP33, OUTBUF_GTP33, TRIBUF_GTP33, BIBUF_GTP33
GTL+	2.5 V	1.0 V	CLKBUF_GTP25, HCLKBUF_GTP25, INBUF_GTP25, OUTBUF_GTP25, TRIBUF_GTP25, BIBUF_GTP25
SSTL2 Class I	2.5 V	1.25 V	CLKBUF_SSTL2_I, HCLKBUF_SSTL2_I, TRIBUF_SSTL2_I, BIBUF_SSTL2_I , INBUF_SSTL2_I, OUTBUF_SSTL2_I
SSTL2 Class II	2.5 V	1.25 V	CLKBUF_SSTL2_II, HCLKBUF_SSTL2_II, TRIBUF_SSTL2_II, BIBUF_SSTL2_II, INBUF_SSTL2_II, OUTBUF_SSTL2_II
SSTL3 Class I	3.3 V	1.5 V	CLKBUF_SSTL3_I, HCLKBUF_SSTL3_I, TRIBUF_SSTL3_I, BIBUF_SSTL3_I, INBUF_SSTL3_I, OUTBUF_SSTL3_I
SSTL3 Class II	3.3 V	1.5 V	CLKBUF_SSTL3_II, HCLKBUF_SSTL3_II, TRIBUF_SSTL3_II, BIBUF_SSTL3_II , INBUF_SSTL3_II, OUTBUF_SSTL3_II
HSTL Class I	1.5 V	0.75 V	CLKBUF_HSTL_I, BIBUF_HSTL_I , HCLKBUF_HSTL_I, INBUF_HSTL_I, OUTBUF_HSTL_I, TRIBUF_HSTL_I

User I/O Naming Conventions

Due to the complex and flexible nature of the RTAX-S family's user I/Os, a naming scheme is used to show the details of the I/O. The naming scheme explains to which bank an I/O belongs, as well as the pairing and pin polarity for differential I/Os (Figure 2-7).

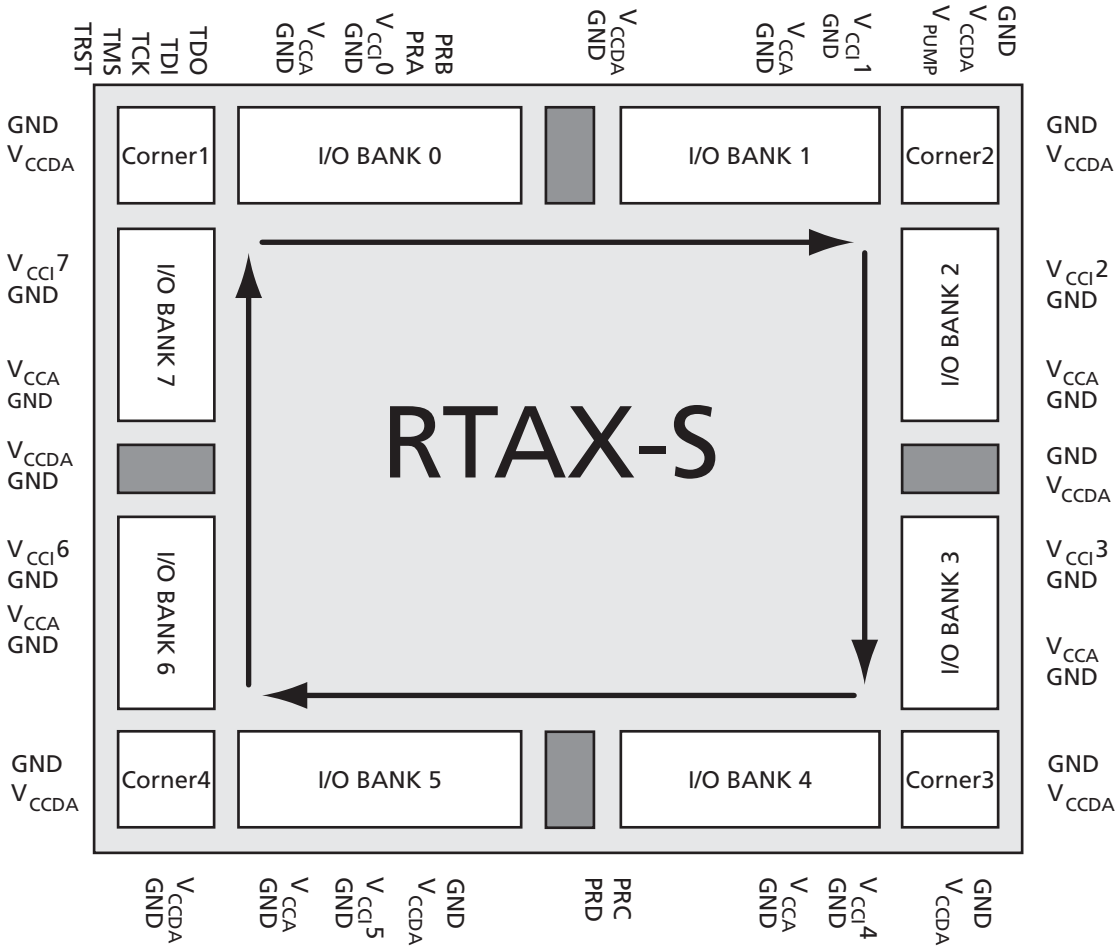
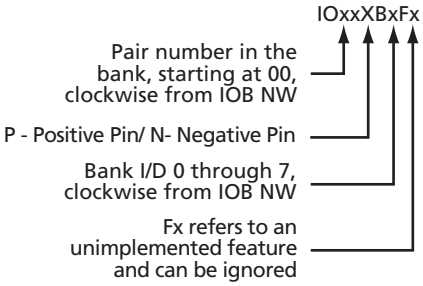


Figure 2-7 • **I/O Bank and Dedicated Pin Layout**



Examples:

IO12PB1F1 Is the positive pin of the thirteenth pair of the first I/O bank (IOB NE). IO12PB1 combined with IO12NB1 form a differential pair.

For those I/Os that can be employed either as a user I/O or as a special function, the following nomenclature is used:

IOxxXBxFx/special_function_name

IOxxPB1Fx/CLKx This pin can be configured as a clock input or as a user I/O

Figure 2-8 • **General Naming Schemes**

I/O Standard Electrical Specifications

Table 2-16 • **Input Capacitance**

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN}=0, f=1.0 MHz		10	pF
C_{INCLK}	Input Capacitance on Clock Pin	V_{IN}=0, f=1.0 MHz		10	pF

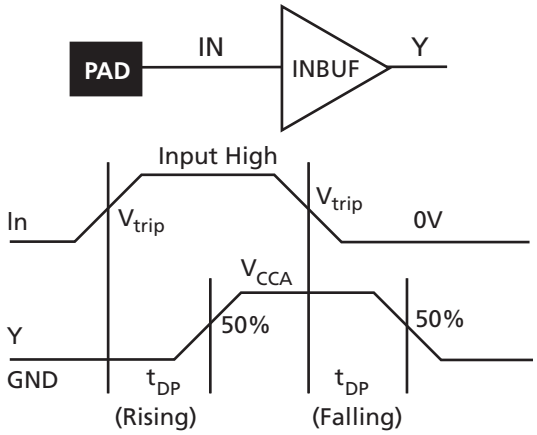


Figure 2-9 • **Input Buffer Delays**

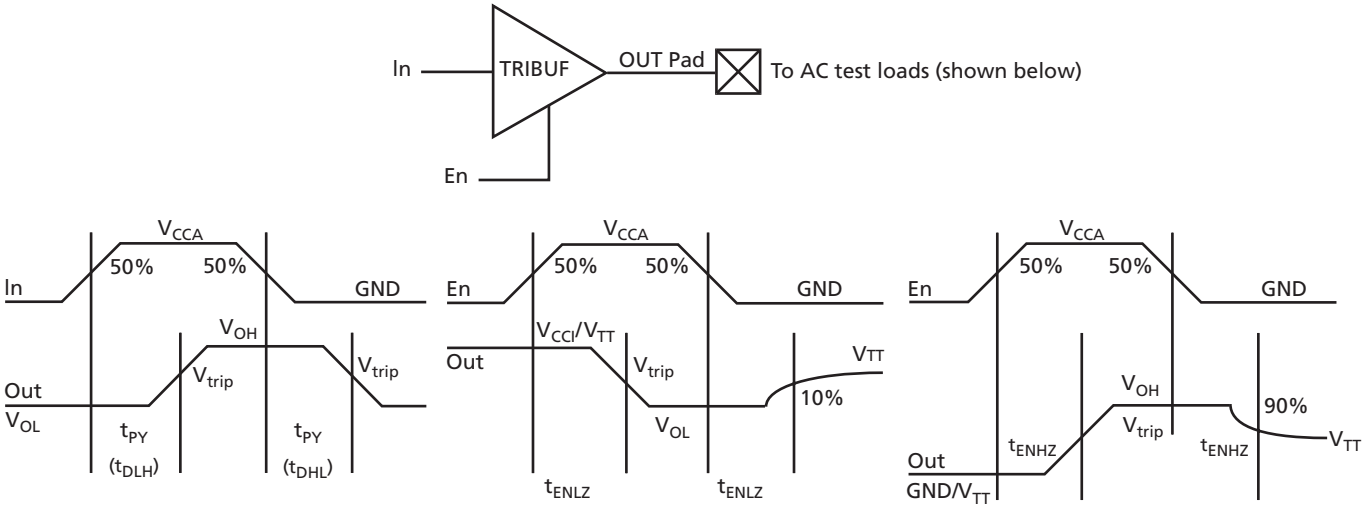


Figure 2-10 • **Output Buffer Delays**

I/O Module Timing Characteristics

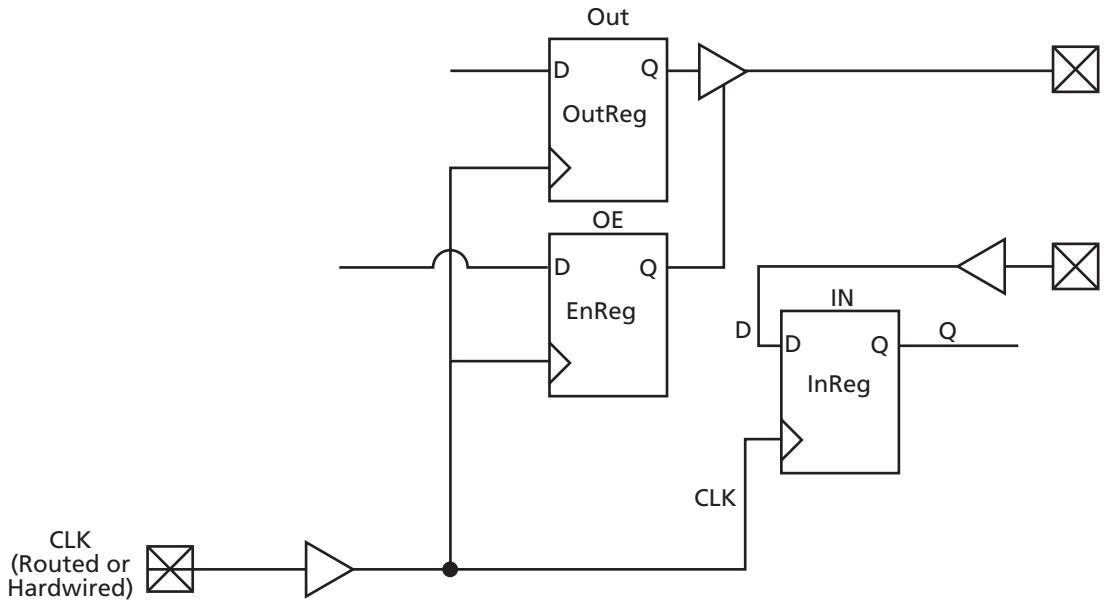


Figure 2-11 • **Timing Model**

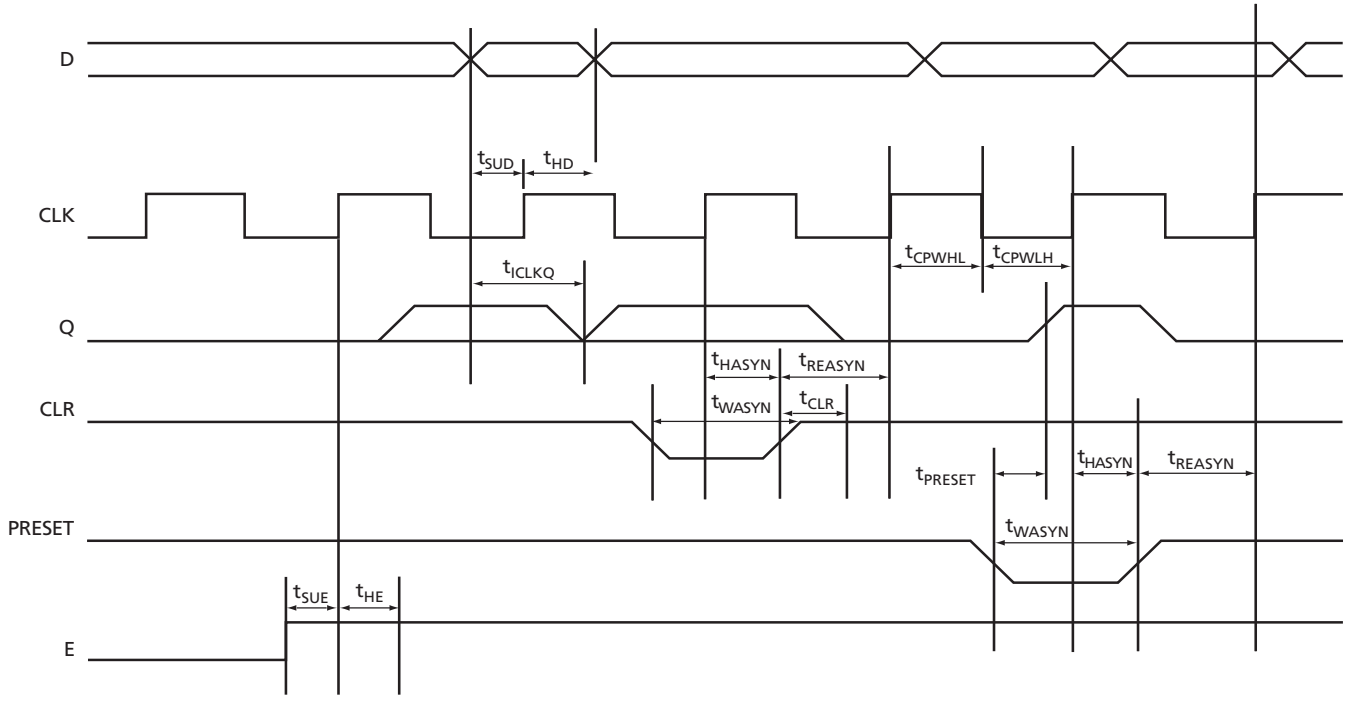


Figure 2-12 • **Input Register Timing Characteristics**

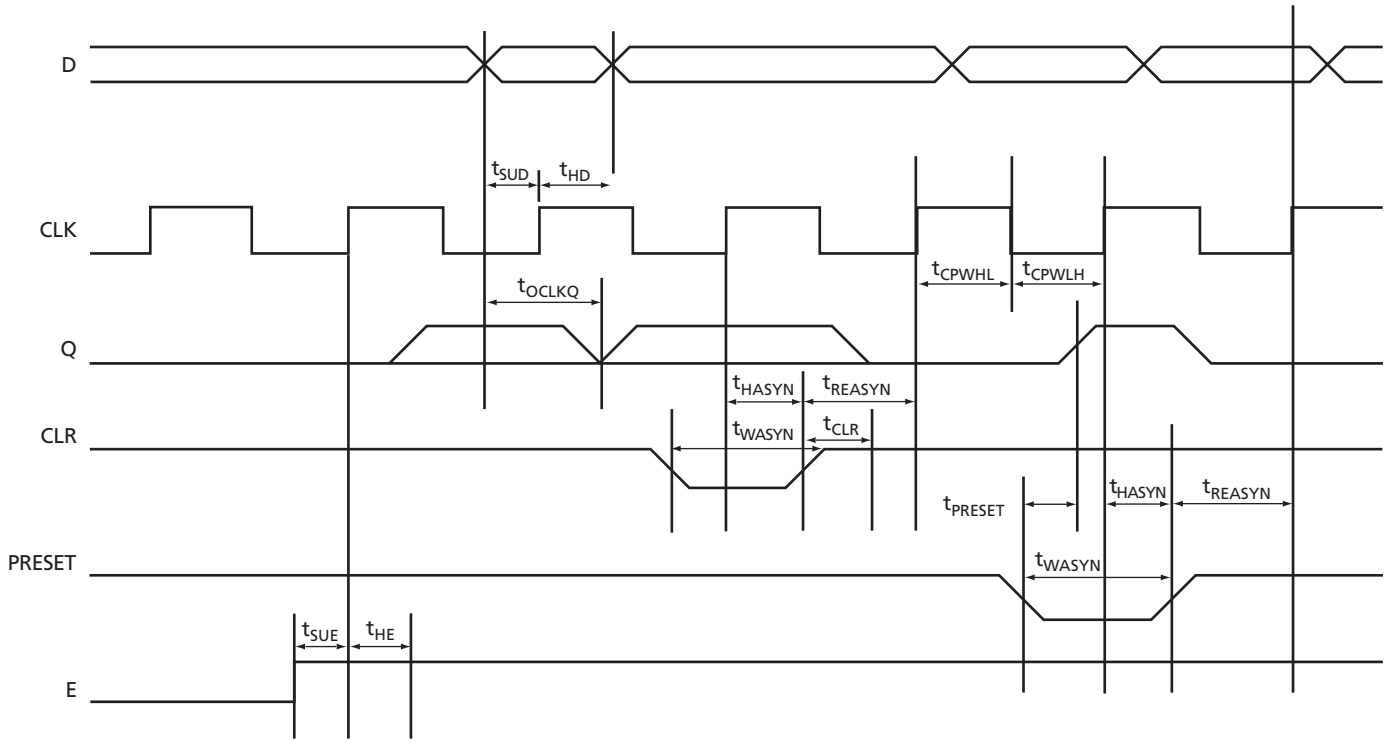


Figure 2-13 • **Output Register Timing Characteristics**

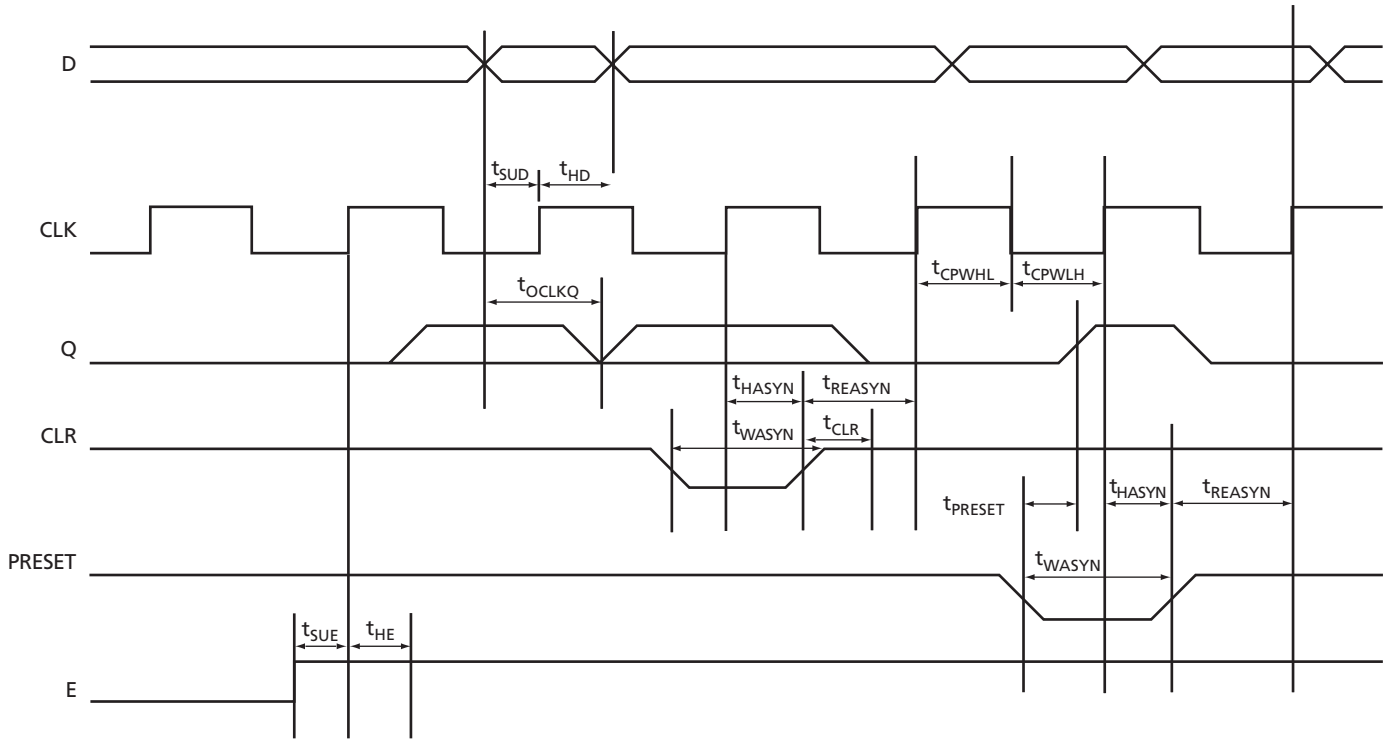


Figure 2-14 • **Output Enable Register Timing Characteristics**

3.3V LVTTL

Low-Voltage Transistor-Transistor Logic is a general purpose standard (EIA/JESD) for 3.3V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-17 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	0.8	2.0	3.6	0.4	2.4	24	–24

AC Loadings

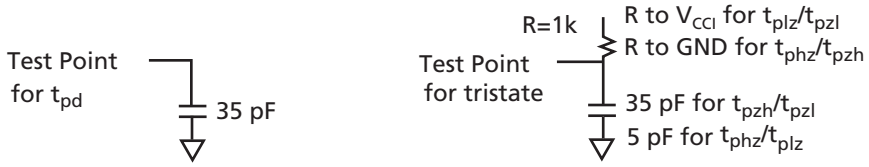


Figure 2-15 • **AC Test Loads**

Table 2-18 • **AC Waveforms, Measuring Points, and Capacitive Load**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	3.0	1.40	N/A	35

** Measuring Point = V_{trip}*

Timing Characteristics

Table 2-19 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	**Max.**	**Min.**	**Max.**	
LVTTL I/O Module Drive Strength = 4 (24mA) /Low Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		11.46		13.46	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-19 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 3 (16mA) / Low Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		12.09		14.21	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 2 (12mA) / Low Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		13.30		15.63	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-19 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 1 (8mA) / Low Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		15.87		18.65	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 4 (24mA) / High Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		3.55		4.17	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-19 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 3 (16mA) / High Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		3.71		4.35	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns
LVTTL I/O Module Drive Strength = 2 (12mA) / High Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		3.91		4.59	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Table 2-19 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C (Continued)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVTTL I/O Module Drive Strength = 1 (8mA) / High Slew Rate						
t_{DP}	Input buffer		1.89		2.22	ns
t_{PY}	Output buffer		4.83		5.67	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

2.5V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 2.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-20 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	0.7	1.7	3.6	0.4	2.0	12	-12

AC Loadings

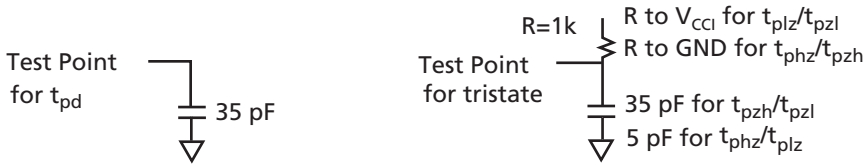


Figure 2-16 • **AC Test Loads**

Table 2-21 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	2.5	1.25	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-22 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 2.3V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS25 I/O Module Timing						
t_{DP}	Input buffer		2.18		2.56	ns
t_{PY}	Output buffer		3.55		4.17	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

1.8V LVCMOS

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.8V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-23 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	$0.2V_{CCI}$	$0.7V_{CCI}$	2.1	0.2	V_{CCI}-0.2	8mA	-8mA

AC Loadings

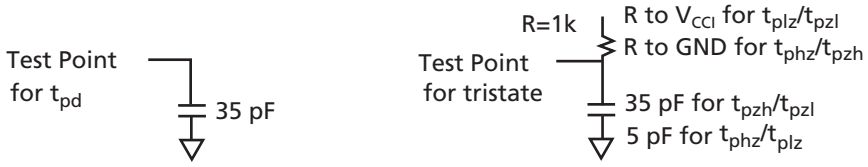


Figure 2-17 • **AC Test Loads**

Table 2-24 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	1.8	$0.5V_{CCI}$	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-25 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 1.7V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	**Max.**	**Min.**	**Max.**	
LVCMOS18 I/O Module Timing						
t_{DP}	Input buffer		3.61		4.24	ns
t_{PY}	Output buffer		4.97		5.83	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

1.5V LVCMOS (JESD8-11)

Low-Voltage Complementary Metal-Oxide Semiconductor for 1.5V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5V applications. It uses a 3.3V tolerant CMOS input buffer and a push-pull output buffer.

Table 2-26 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.5	$0.35V_{CCI}$	$0.65V_{CCI}$	1.95	0.4	V_{CCI}-0.4	8mA	-8mA

AC Loadings

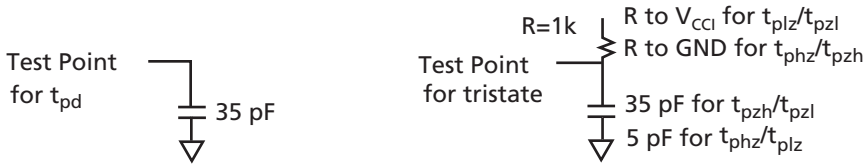


Figure 2-18 • **AC Test Loads**

Table 2-27 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
0	1.5	$0.5V_{CCI}$	N/A	35

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-28 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 1.4V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVCMOS15 (JESD8-11) I/O Module Timing						
t_{DP}	Input buffer		3.98		4.67	ns
t_{PY}	Output buffer		6.58		7.73	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

3.3V PCI

Peripheral Component Interface for 3.3V standard specifies support for 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. The input and output buffers are 5V tolerant with the aid of external components. The RTAX-S 3.3V PCI buffer is compliant with the PCI Local Bus Specification Rev. 2.1.

Table 2-29 • **DC Input and Output Levels**

	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
PCI	-0.5	$0.3V_{CCI}$	$0.5V_{CCI}$	V_{CCI}+0.5	(per PCI specification)			

AC Loadings

Per PCI Specification except for tristate. Actel loading for tristate is in the figure below.

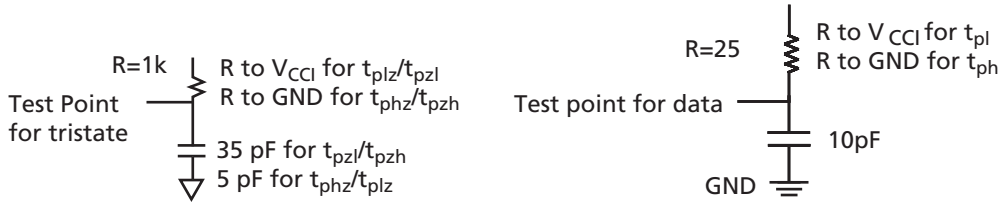


Figure 2-19 • **AC Test Loads**

Table 2-30 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**V_{REF} (typ) (V)**	**C_{load} (pF)**
(Per PCI Spec)			N/A	10

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-31 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	**Description**	**'–1' Speed**		**'Std.' Speed**		**Units**
		Min.	**Max.**	**Min.**	**Max.**	
3.3V PCI I/O Module Timing						
t_{DP}	Input buffer		1.77		2.07	ns
t_{PY}	Output buffer		2.29		2.69	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Voltage-Referenced I/O Standards

GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It requires a differential amplifier input buffer and an open drain output buffer. The V_{CCI} pin should be connected to 2.5V or 3.3V. Note that 2.5V GTL+ is not supported across the full military temperature range.

Table 2-32 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
N/A	V_{REF}-0.1	V_{REF}+0.1	N/A	0.6	NA	NA	NA

AC Loadings

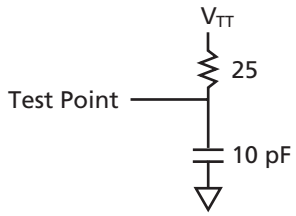


Figure 2-20 • **AC Test Loads**

Table 2-33 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.2	V_{REF}+0.2	V_{REF}	1.0	10

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-34 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3 V GTL+ I/O Module Timing						
t_{DP}	Input buffer		2.06		2.41	ns
t_{PY}	Output buffer		1.31		1.54	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

HSTL Class I

High-Speed Transceiver Logic is a general-purpose high-speed 1.5V bus standard (EIA/JESD8-6). The RTAX-S devices support Class I. This requires a differential amplifier input buffer and a push-pull output buffer.

Table 2-35 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	V_{REF}-0.1	V_{REF}+0.1	3.6	0.4	V_{CC}-0.4	8	-8

AC Loadings

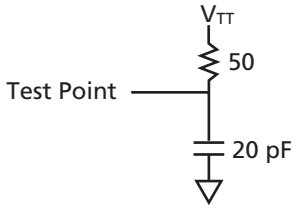


Figure 2-21 • **AC Test Loads**

Table 2-36 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.5	V_{REF}+0.5	V_{REF}	0.75	20

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-37 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 1.4V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
1.5V HSTL Class I I/O Module Timing						
t_{DP}	Input buffer		2.16		2.54	ns
t_{PY}	Output buffer		5.40		6.34	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

SSTL2

Stub Series Terminated Logic for 2.5V is a general-purpose 2.5V memory bus standard (JESD8-9). The RTAX-S devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-38 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.57	V_{REF}+0.57	7.6	-7.6

AC Loadings

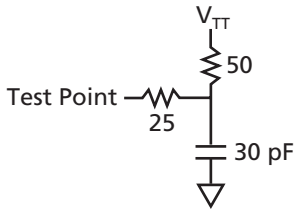


Figure 2-22 • **AC Test Loads**

Table 2-39 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-40 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 2.3V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
2.5V SSTL2 Class I I/O Module Timing						
t_{DP}	Input buffer		2.19		2.57	ns
t_{PY}	Output buffer		2.66		3.12	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Class II

Table 2-41 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.8	V_{REF}+0.8	15.2	-15.2

AC Loadings

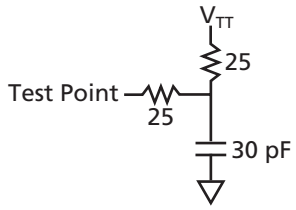


Figure 2-23 • **AC Test Loads**

Table 2-42 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-0.75	V_{REF}+0.75	V_{REF}	1.25	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-43 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 2.3V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
2.5V SSTL2 Class II I/O Module Timing						
t_{DP}	Input buffer		2.27		2.66	ns
t_{PY}	Output buffer		2.66		3.12	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

SSTL3

Stub Series Terminated Logic for 3.3V is a general-purpose 3.3V memory bus standard (JESD8-8). The RTAX-S devices support both classes of this standard. This requires a differential amplifier input buffer and a push-pull output buffer.

Class I

Table 2-44 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.6	V_{REF}+0.6	8	-8

AC Loadings

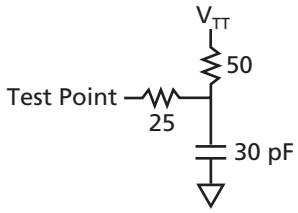


Figure 2-24 • **AC Test Loads**

Table 2-45 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-1.0	V_{REF}+1.0	V_{REF}	1.50	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-46 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3V SSTL3 Class I I/O Module Timing						
t_{DP}	Input buffer		2.14		2.51	ns
t_{PY}	Output buffer		2.59		3.04	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Class II

Table 2-47 • **DC Input and Output Levels**

V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
Min,V	**Max,V**	**Min,V**	**Max,V**	**Max,V**	**Min,V**	**mA**	**mA**
-0.3	V_{REF}-0.2	V_{REF}+0.2	3.6	V_{REF}-0.8	V_{REF}+0.8	16	-16

AC Loadings

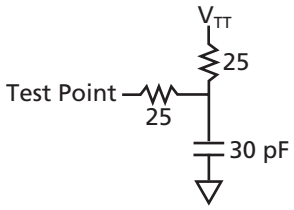


Figure 2-25 • **AC Test Loads**

Table 2-48 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ) (V)	C_{load} (pF)
V_{REF}-1.0	V_{REF}+1.0	V_{REF}	1.50	30

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-49 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
3.3V SSTL3 Class II I/O Module Timing						
t_{DP}	Input buffer		2.21		2.60	ns
t_{PY}	Output buffer		2.59		3.04	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Differential Standards

Physical Implementation

Implementing differential I/O standards requires the configuration of a pair of external I/O pads, resulting in a single internal signal. To facilitate construction of the differential pair, a single I/O cluster contains the resources for a pair of I/Os. Configuration of the I/O Cluster as a differential pair is handled by Actel's Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), and Enable Register (EnReg). However, there is no support for bidirectional I/Os or tristates with these standards.

LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit is carried through two signal lines, so two pins are needed. It also requires an external resistor termination. The voltage swing between these two signal lines is approximately 350mV.

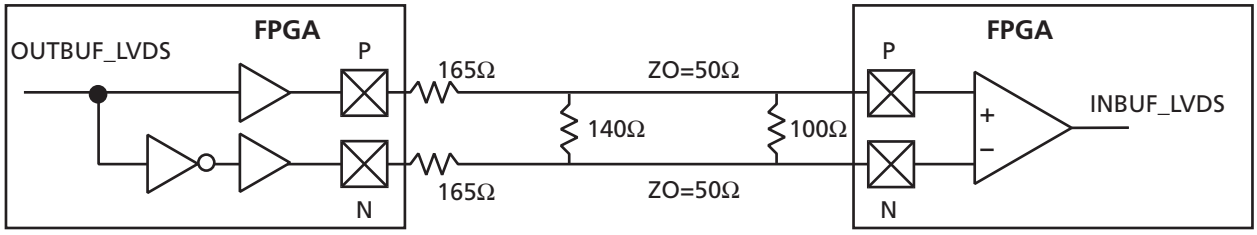


Figure 2-26 • **LVDS Circuit**

The LVDS circuit consists of a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The common-mode range is from 0.2V to 2.2V for a differential input with 400mV swing.

To implement the driver for the LVDS circuit, drivers from two adjacent I/O cells are used to generate the differential signals (Note that the driver is not a current-mode driver). This driver provides a nominal constant current of 3.5mA. When this current flows through a 100Ω termination resistor on the receiver side, a voltage swing of 350mV is developed across the resistor. The direction of the current flow is controlled by the data fed to the driver.

An external-resistor network (three resistors) is needed to reduce the voltage swing to about 350mV. Therefore, four external resistors are required, three for the driver and one for the receiver.

Table 2-50 • **DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}[1]	Supply voltage	2.375	2.5	2.625	V
V_{OH}	Output high voltage	1.25	1.425	1.6	V
V_{OL}	Output low voltage	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}[2]	Input common mode voltage	0.2	1.25	2.2	V

Notes:

1. *+/- 5%*
2. *Differential input voltage =+/-350mV.*

AC Loadings

For AC test loads, see the above LVDS circuit.

Table 2-51 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{load} (pF)
1.2-0.125	1.2+0.125	1.2	N/A

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-52 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 2.3V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVDS I/O Module Timing						
t_{DP}	Input buffer		2.05		2.40	ns
t_{PY}	Output buffer		2.59		3.04	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit is carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination. The voltage swing between these two signal lines is approximately 850 mV.

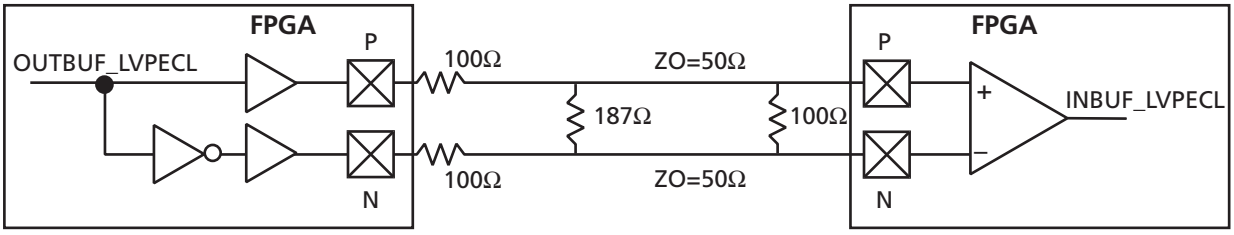


Figure 2-27 • **LVPECL Circuit**

The LVPECL circuit is similar to the LVDS scheme. It requires four external resistors, three for the driver and one for the receiver. The values for the three driver resistors are different from that of LVDS, since the output voltage levels are different. Please note that the V_{OH} levels are 200 mV below the standard LVPECL levels.

Table 2-53 • **DC Input and Output Levels**

DC Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	3.0	–	3.3	–	3.6	–	V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	–	0.3	–	0.3	–	V

AC Loadings

For AC test loads, See the above LVPECL circuit.

Table 2-54 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{load} (pF)
1.6-0.3	1.6+0.3	1.6	N/A

Note: **Measuring Point = V_{trip}*

Timing Characteristics

Table 2-55 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
LVPECL I/O Module Timing						
t_{DP}	Input buffer		1.87		2.20	ns
t_{PY}	Output buffer		2.50		2.93	ns
t_{ICLKQ}	Clock-to-Q for the I/O input register		0.91		1.07	ns
t_{OCLKQ}	Clock-to-Q for the IO output register and the I/O enable register		0.91		1.07	ns
t_{SUD}	Data input setup	0.31		0.37		ns
t_{SUE}	Enable input setup	0.35		0.41		ns
t_{HD}	Data input hold	0.00		0.00		ns
t_{HE}	Enable input hold	0.00		0.00		ns
t_{CPWHL}	Clock pulse width High to Low	0.39		0.39		ns
t_{CPWLH}	Clock pulse width Low to High	0.37		0.37		ns
t_{WASYN}	Asynchronous pulse width	0.37		0.37		ns
t_{REASYN}	Asynchronous recovery time	0.17		0.21		ns
t_{HASYN}	Asynchronous removal time	0.00		0.00		ns
t_{CLR}	Asynchronous Clear-to-Q		0.31		0.37	ns
t_{PRESET}	Asynchronous Preset-to-Q		0.31		0.37	ns

Module Specifications

C-Cell

Introduction

The C-cell is one of the two logic module types in the RTAX-S architecture. It is the combinatorial logic resource in the RTAX-S device. The RTAX-S architecture implements a new Combinatorial Cell that is an extension of the C-cell implemented in the SX-A family. The main enhancement of the new C-cell is the addition of carry-chain logic.

The C-cell can be used in a carry-chain mode to construct arithmetic functions. If carry-chain logic is not required, it can be disabled.

The C-cell features the following (Figure 2-28):

- Eight-input MUX (data: D0-D3, select: A0, A1, B0, B1). User signals can be routed to any one of these inputs. Any of the C-cell inputs (D0-D3, A0, A1, B0, B1) can be tied to one of the four routed clocks (CLKE/F/G/H).
- Inverter (DB input) can be used to drive a complement signal of any of the inputs to the C-cell.
- A carry input and a carry output. The carry input signal of the C-cell is the carry output from the C-cell directly to the north.
- Carry connect for carry-chain logic with a signal propagation time of less than 0.1 ns.
- A hardwired connection (direct connect) to the adjacent R-cell (Register Cell) for all C-cells on the east side of a SuperCluster with a signal propagation time of less than 0.1 ns.

This layout of the C-cell (and the C-cell Cluster) enables the implementation of over 4,000 functions of up to five bits. For example, two C-cells can be used together to implement a four-input XOR function in a single cell delay.

The carry-chain configuration is handled automatically for the user with Actel's extensive macro library (please see Actel's *Antifuse Macro Library Guide* for a complete listing of available RTAX-S macros).

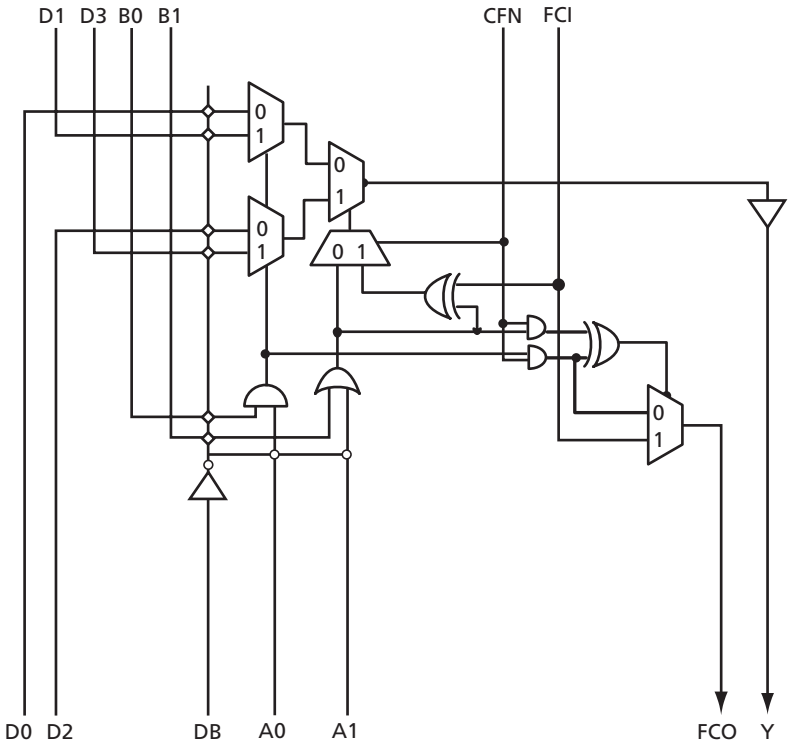


Figure 2-28 • **C-Cell**

Timing Model and Waveforms

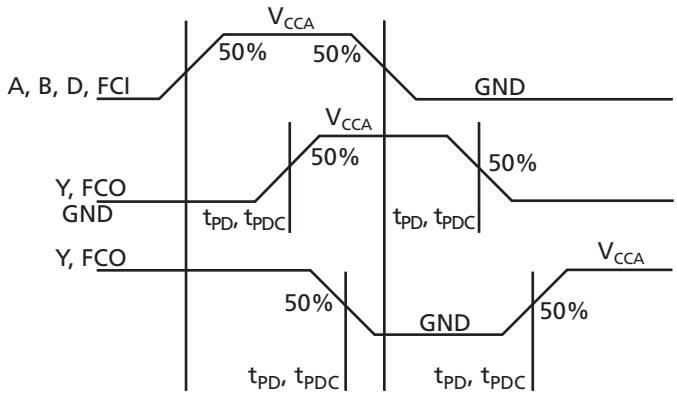


Figure 2-29 • **C-Cell Timing Model and Waveforms**

Timing Characteristics

Table 2-56 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
C-Cell Propagation Delays						
t_{PD}	Any input to output		0.95		1.11	ns
t_{PDC}	Any input to carry chain output (FCO)		0.70		0.82	ns
t_{PDB}	Any input thorough DB when 1 input is used		1.49		1.75	ns
t_{CCY}	Input carry chain (FCI) to Y		0.76		0.90	ns
t_{CC}	Input carry chain (FCI) to carry chain output (FCO)		0.10		0.12	ns

Carry-Chain Logic

The RTAX-S dedicated carry-chain logic offers a very compact solution for implementing arithmetic functions without sacrificing performance.

To implement the carry-chain logic, two C-cells in a Cluster are connected together so the FCO (i.e. carry out) for the two bits is generated in a Carry Look-ahead scheme to achieve minimum propagation delay from the FCI (i.e. carry in) into the two-bit Cluster. The two-bit carry logic is shown in Figure 2-30.

The FCI of one C-cell pair is driven by the FCO of the C-cell pair immediately above it. Similarly, the FCO of one C-cell pair, drives the FCI input of the C-cell pair immediately below it (Figure 1-5 on page 1-3 and Figure 2-31 on page 2-44).

The carry-chain logic is selected via the CFN input. When carry logic is not required, this signal is deasserted to save power. Again, this configuration is handled automatically for the user through Actel's macro library.

The signal propagation delay between two C-cells in the carry-chain sequence is 0.1 ns.

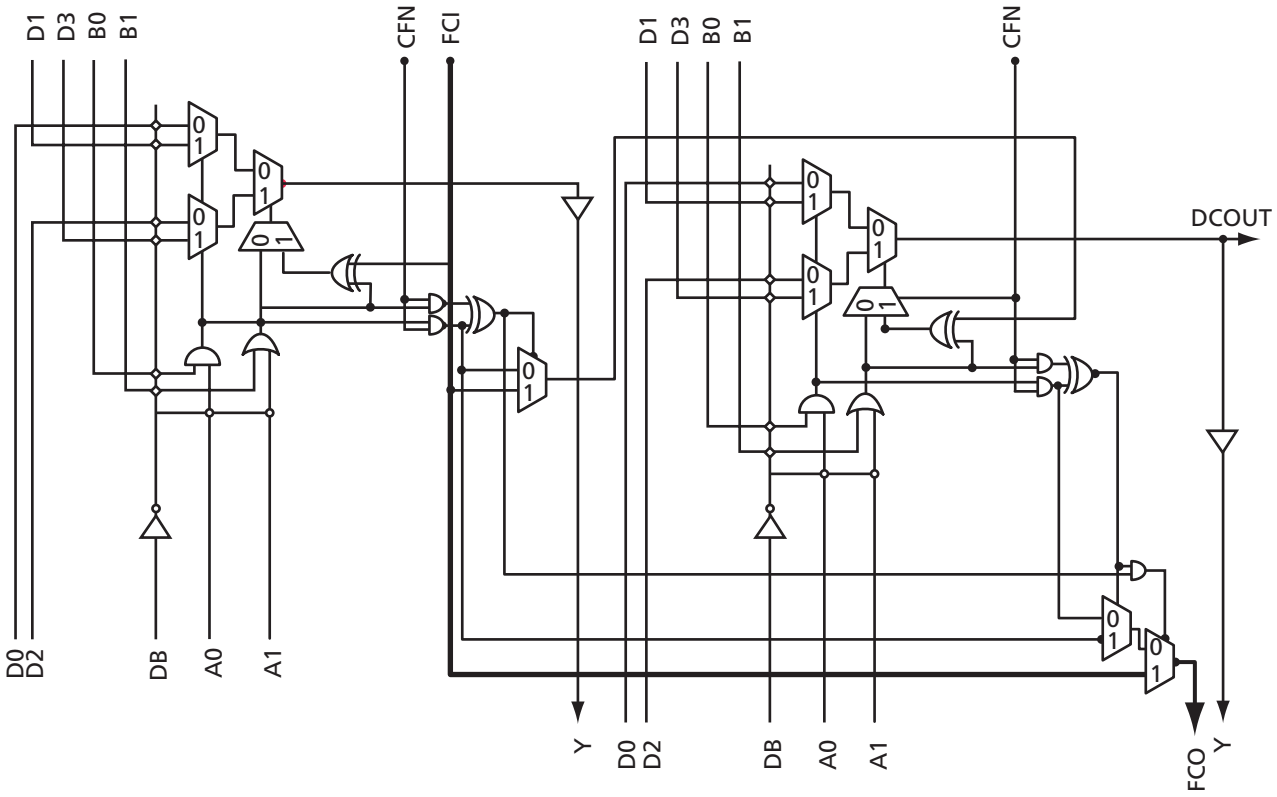
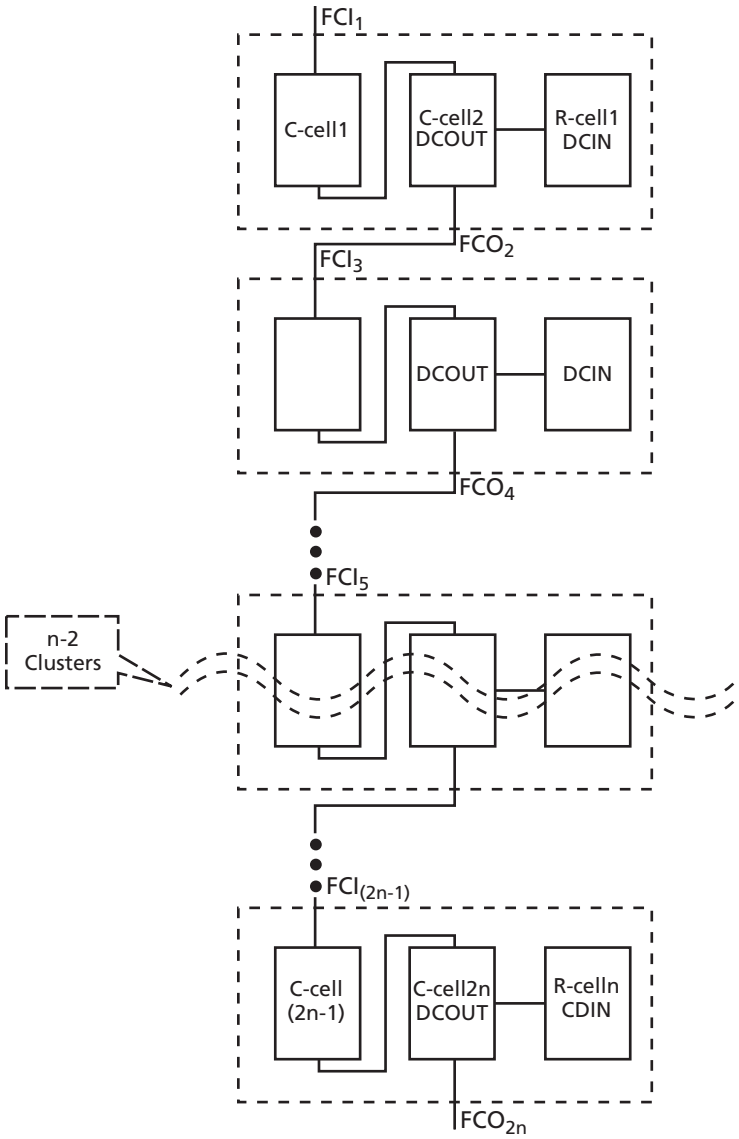


Figure 2-30 • **RTAX-S Two-Bit Carry Logic**



Note: *The carry-chain sequence can end on either C-cell.*

Figure 2-31 • **Carry-Chain Sequencing of C-cells**

Timing Characteristics

Refer to the C-cell Timing Characteristics in Table 2-56 on page 2-42 for more information on carry-chain timing.

R-Cell

Introduction

The R-cell, the sequential logic resource of the RTAX-S devices, is the second logic module type in the RTAX-S family architecture. The RTAX-S R-cell is an enhanced version of the SX-A R-cell. It includes additional clock inputs for all eight global resources of the RTAX-S architecture as well as global presets and clears (Figure 2-32).

The main features of the R-cell include the following:

- Direct connection to the adjacent logic module through the hardwired connection DCIN. DCIN is driven by the DCOUT of an adjacent C-cell via the Direct-Connect routing resource, providing a connection with less than 0.1 ns of routing delay.
- The R-cell can be used as a standalone flip-flop. It can be driven by any C-cell or I/O modules through the regular routing structure (using DIN as a routable data input). This gives the option of using the R-cell as a 2:1 MUXed flip-flop as well.
- Provision of data enable-input (S0).
- Independent active low asynchronous clear (CLR).
- Independent active low asynchronous preset (PSET). If both CLR and PSET are low, CLR has higher priority.
- Clock can be driven by any of the following (CKP selects clock polarity):
  - One of the four high performance hardwired fast clocks (HCLKs)
  - One of the four routed clocks (CLKs)
  - User signals
- Global power-on clear (GCLR) and preset (GPSET), which drive each flip-flop on a chip-wide basis.
  - When the Global Set Fuse option in the Designer software is unchecked (by default), GCLR = 0 and GPSET =1 at device power-up. When the option is checked, GCLR = 1 and GPSET= 0. Both pins are pulled HIGH when the device is in user mode.
- S0, S1, PSET, and CLR can be driven by routed clocks CLKE/F/G/H or user signals.
- DIN and S1 can be driven by user signals.

As with the C-cell, the configuration of the R-cell to perform various functions is handled automatically for the user through Actel's extensive macro library (please see Actel's *Macro Library Guide* for a complete listing of available RTAX-S macros).

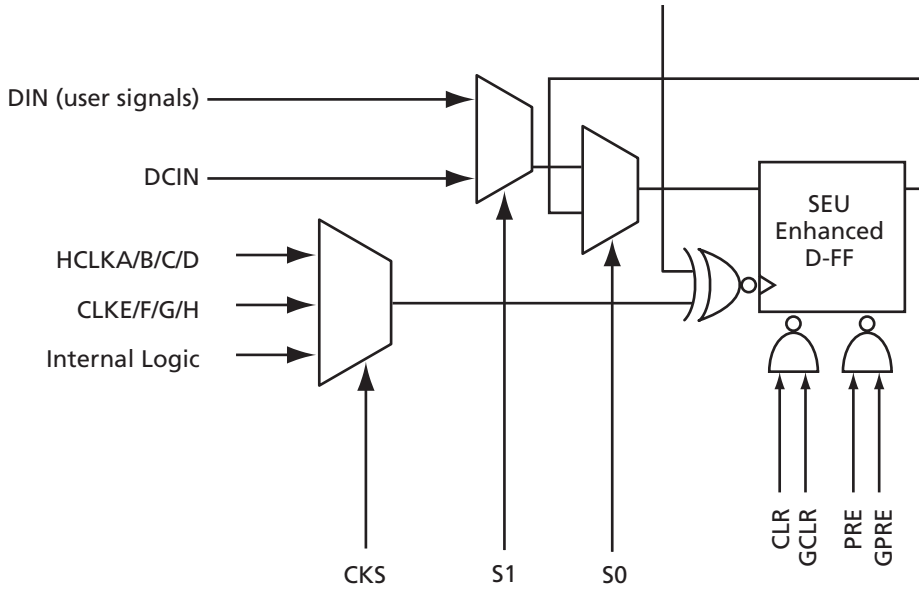


Figure 2-32 • **R-cell**

SEU Hardened D Flip-Flop (DFF)

In order to meet the stringent SEU requirements of a LET_{TH} greater than 37 MeV-cm^2/mg, the internal design of the R-cell was modified without changing the functionality of the cell. Figure 2-33 illustrates a simplified representation of how the D flip-flop in the SuperCluster is implemented in the RTAX-S architecture. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output to the input stage. The potential problem in a space environment is that either of the latches can change state when hit by a particle with enough energy.

To achieve the SEU requirements, the D flip-flop in the RTAX-S R-cell is enhanced (Figure 2-34). Both the master and slave "latches" are actually implemented with three latches. The asynchronous self-correcting feedback paths of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch. Figure 2-35 on page 2-47 is a simplified schematic of the test circuitry that has been added to test the functionality of all the components of the flip-flop. The inputs to each of the three latches are independently controllable, so the voting circuitry in the asynchronous self-correcting feedback paths can be tested exhaustively. This testing is performed on an unprogrammed array during wafer sort, final test, and post-burn-in test. This test circuitry cannot be used to test the flip-flops once the device has been programmed.

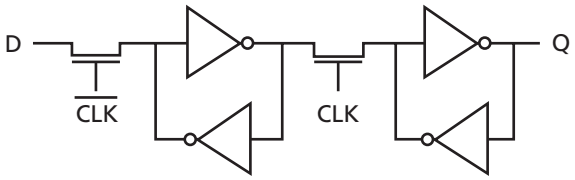


Figure 2-33 • **RTAX-S R-cell Implementation of D Flip-Flop**

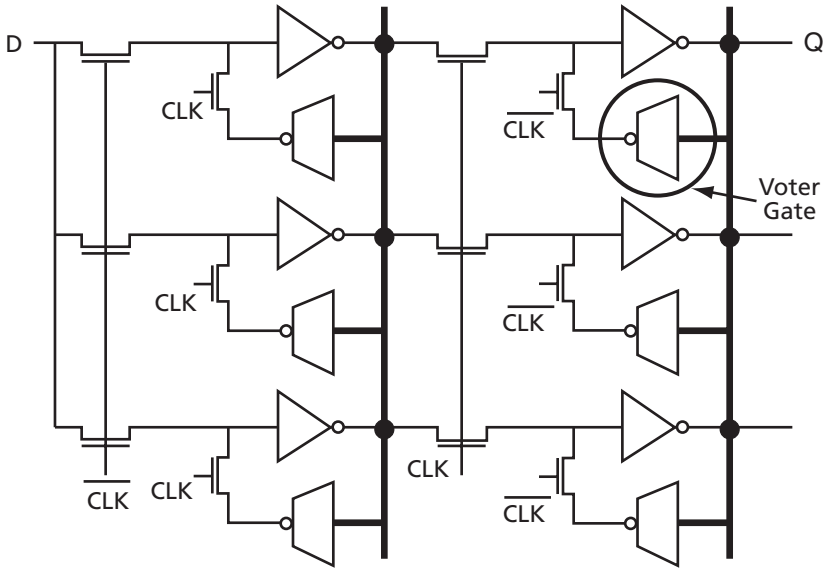


Figure 2-34 • **RTAX-S R-cell Implementation of D Flip-Flop Using Voter Gate Logic**

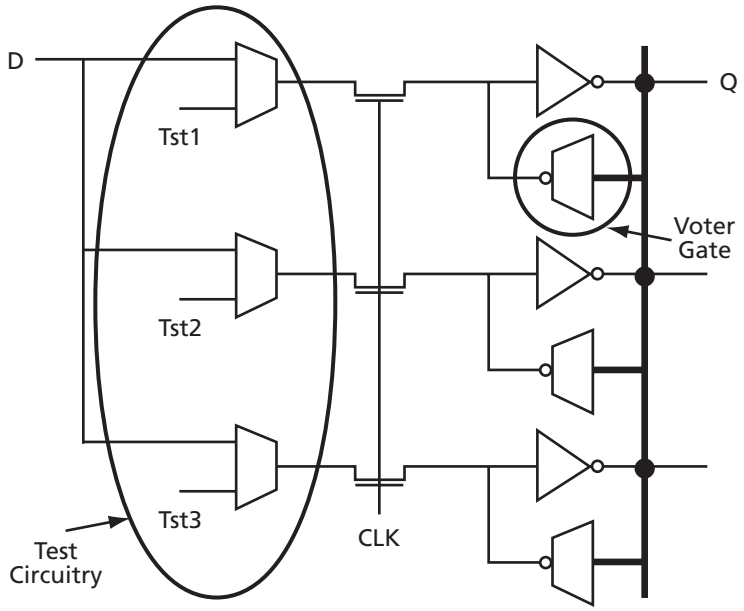


Figure 2-35 • **RTAX-S R-Cell Implementation – Test Circuitry**

Timing Models and Waveforms

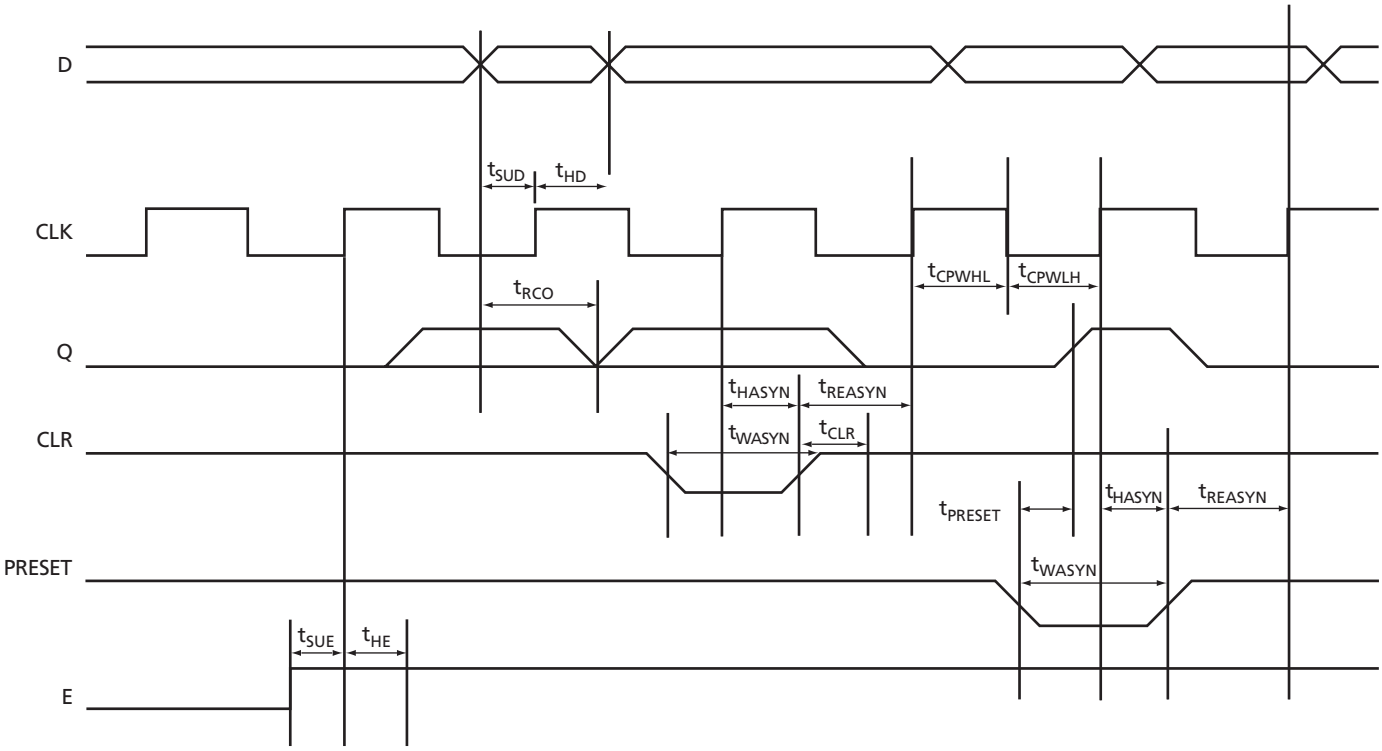


Figure 2-36 • **R-Cell Delays**

Timing Characteristics

Table 2-57 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
R-Cell Propagation Delays						
t_{RCO}	Sequential Clock to Q		0.96		1.12	ns
t_{CLR}	Asynchronous Clear to Q		0.63		0.74	ns
t_{PRESET}	Asynchronous Preset to Q		0.76		0.89	ns
t_{SUD}	FF Data input setup	0.21		0.25		ns
t_{SUE}	FF Enable input setup	0.21		0.25		ns
t_{HD}	FF Data Hold	0.00		0.00		ns
t_{HE}	FF Enable Hold time	0.00		0.00		ns
t_{WASYN}	Asynchronous Pulse width	0.48		0.48		ns
t_{REASYN}	Asynchronous Recovery time	0.00		0.00		ns
t_{HASYN}	Asynchronous Removal time	0.00		0.00		ns
t_{CPWHL}	Clock pulse width high to low	0.36		0.36		ns
t_{CPWLH}	Clock pulse width low to high	0.36		0.36		ns

Buffer Module

Introduction

An additional resource inside each SuperCluster is the Buffer (B) module (Figure 1-4 on page 1-3).

When a fanout constraint is applied to a design, the synthesis tool inserts buffers as needed. The buffer module has been added to the RTAX-S architecture to avoid logic duplication resulting from the hard fanout constraints. The router utilizes this logic resource to save area and reduce loading and delays on medium-to-high-fanout nets.

Timing Models and Waveforms

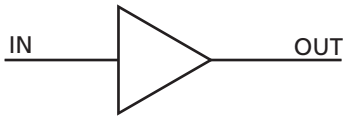


Figure 2-37 • **Buffer Module Timing Model**

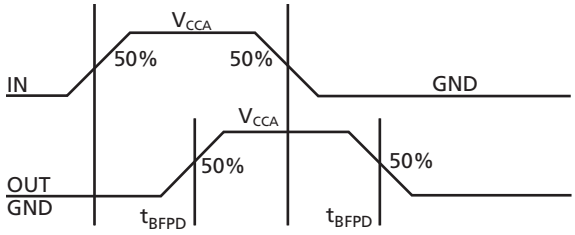


Figure 2-38 • **Buffer Module Waveform**

Timing Characteristics

Table 2-58 • **Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{BFPD}	Any input to output Y		0.17		0.20	ns

Routing Specifications

Routing Resources

The routing structure found in RTAX-S devices enables any logic module to be connected to any other logic module while retaining high performance. There are multiple paths and routing resources that can be used to route one logic module to another, both within a SuperCluster and elsewhere on the chip.

There are four primary types of routing within the RTAX-S architecture: DirectConnect, CarryConnect, FastConnect and Vertical and Horizontal Routing.

DirectConnect

DirectConnects provide a high-speed connection between an R-cell and its adjacent C-cell (Figure 2-39). This connection can be made from DCOUT of the C-cell to DCIN of the R-cell by configuring of the S1 line of the R-cell. This provides a connection that does not require an antifuse and has a delay of less than 0.1 ns.

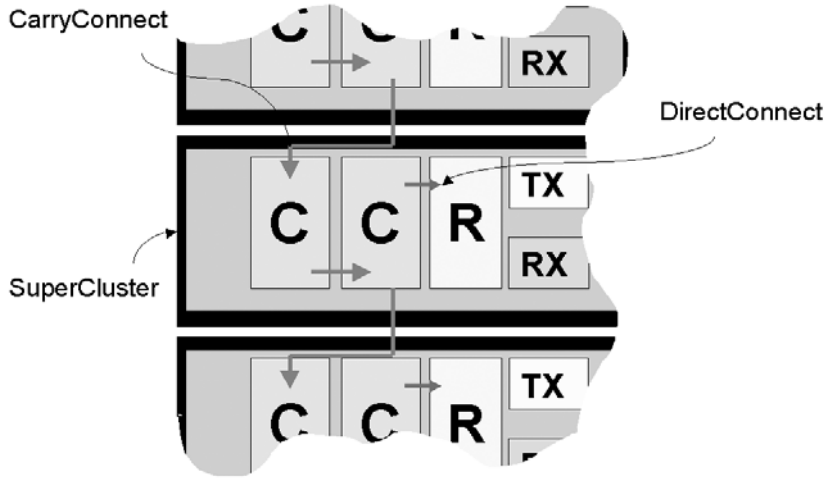


Figure 2-39 • **DirectConnect and CarryConnect**

CarryConnect

CarryConnects are used to build carry chains for arithmetic functions (Figure 2-39). The FCO output of the right C-cell of a two-C-cell Cluster drives the FCI input of the left C-cell in the two-C-cell Cluster immediately below it. This pattern continues down both sides of each SuperCluster column.

Similar to the DirectConnects, CarryConnects can be built without an antifuse connection. This connection has a delay of less than 0.1 ns from the FCO of one two-C-cell Cluster to the FCI of the two-C-cell Cluster immediately below it (see the "Carry-Chain Logic" on page 2-43 for more information).

FastConnect

For high-speed routing of logic signals, FastConnects can be used to build a short distance connection using a single antifuse (Figure 2-40 on page 2-51). FastConnects provide a maximum delay of 0.4 ns. The outputs of each logic module connect directly to the Output Tracks within a SuperCluster. Signals on the Output Tracks can then be routed through a single antifuse connection to drive the inputs of logic modules either within one SuperCluster or in the SuperCluster immediately below it.

Vertical and Horizontal Routing

Vertical and Horizontal Tracks provide both local and long distance routing (Figure 2-41 on page 2-51). These tracks are composed of both short-distance, segmented routing and across-chip routing tracks (segmented at core tile boundaries). The short-distance, segmented routing resources can be concatenated through antifuse connections to build longer routing tracks.

These short-distance routing tracks can be used within and between SuperClusters or between modules of non-adjacent SuperClusters. They can be connected to the Output Tracks and to any logic module input (R-cell, C-cell, Buffer, and TX module).

The across-chip horizontal and vertical routing provides long-distance, routing resources. These resources interface with the rest of the routing structures through

the RX and TX modules (Figure 2-41). The RX module is used to drive signals from the across-chip horizontal and vertical routing to the Output Tracks within the SuperCluster. The TX module is used to drive vertical and horizontal across-chip routing from either short-distance horizontal tracks or from Output Tracks. The TX module can also be used to drive signals from vertical across-chip tracks to horizontal across-chip tracks and vice versa.

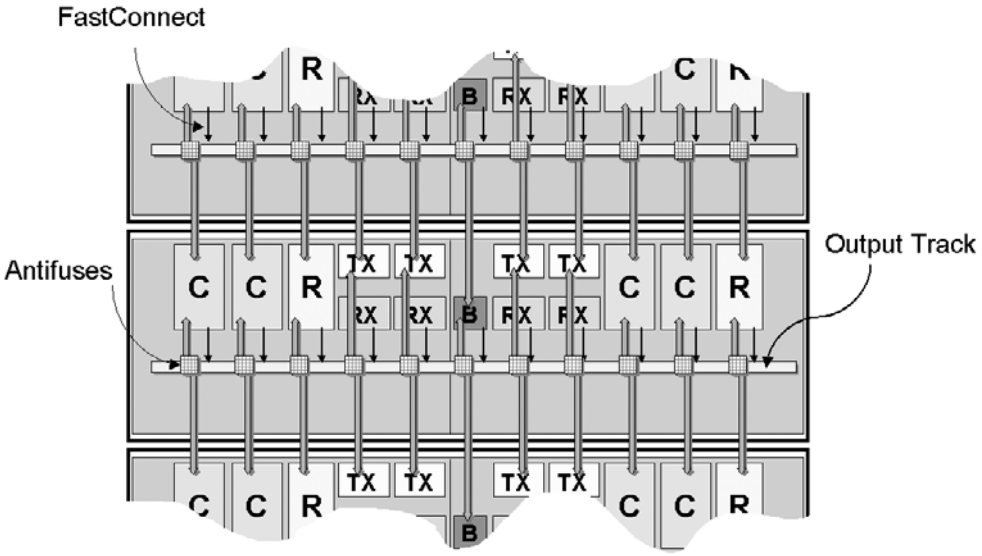


Figure 2-40 • **FastConnect Routing**

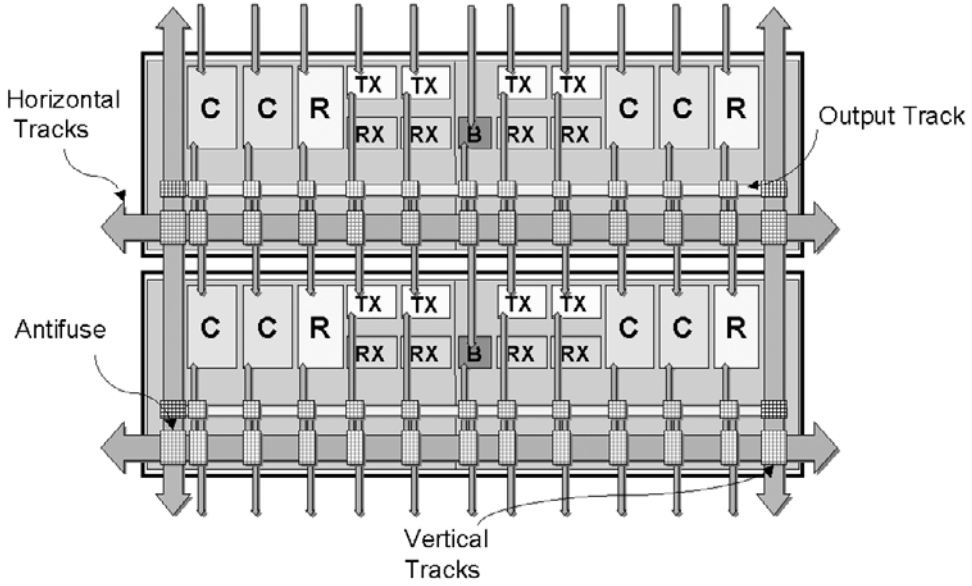


Figure 2-41 • **Horizontal and Vertical Tracks**

Timing Characteristics

Table 2-59 • **RTAX250S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.7	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.3		3.88	ns

Table 2-60 • **RTAX1000S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.7	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.3		3.88	ns

Table 2-61 • **RTAX2000S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Unit
		Min.	Max.	Min.	Max.	
Predicted Routing Delays						
t_{DC}	Direct connect		0.08		0.07	ns
t_{FC}	Fast connect F01		0.24		0.29	ns
t_{RD1}	Fanout 1		0.66		0.77	ns
t_{RD2}	Fanout 2		0.84		0.99	ns
t_{RD3}	Fanout 3		1.07		1.25	ns
t_{RD4}	Fanout 4		1.38		1.62	ns
t_{RD5}	Fanout 5		1.45		1.70	ns
t_{RD6}	Fanout 6		2.08		2.44	ns
t_{RD7}	Fanout 7		2.26		2.66	ns
t_{RD8}	Fanout 8		2.44		2.87	ns
t_{RD9}	Fanout 9		2.87		3.37	ns
t_{RD10}	Fanout 10		3.30		3.88	ns

Global Resources

One of the most important aspects of any FPGA architecture is its global resources or clocks. The RTAX-S family provides the user with flexible and easy-to-use global resources, without the limitations normally found in other FPGA architectures. In addition, these global resources have been hardened to improve SEU performance.

The RTAX-S architecture contains two types of global resources, the HCLK (hardwired clock) and CLK (routed clock). Every RTAX-S device is provided with four HCLKs and four CLKs for a total of eight clocks, regardless of device density.

Hardwired Clocks

The hardwired (HCLK) is a low-skew network that can directly drive the clock inputs of all sequential modules (R-cells, I/O registers and embedded RAM/FIFOs) in the device with no antifuse in the path. All four HCLKs are available everywhere on the chip.

Timing Characteristics

Table 2-62 • **RTAX250S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		2.76		3.24	ns
t_{HCKH}	Input High to Low		2.94		3.46	ns
t_{HPWH}	Minimum Pulse width High	0.37		0.43		ns
t_{HPWL}	Minimum Pulse width Low	0.44		0.52		ns
t_{HCKSW}	Maximum skew		TBD		TBD	ns
f_{HMAX}	Maximum frequency		TBD		TBD	MHz

Table 2-63 • **RTAX1000S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		3.48		4.09	ns
t_{HCKH}	Input High to Low		3.65		4.29	ns
t_{HPWH}	Minimum Pulse width High	0.37		0.43		ns
t_{HPWL}	Minimum Pulse width Low	0.44		0.52		ns
t_{HCKSW}	Maximum skew		TBD		TBD	ns
f_{HMAX}	Maximum frequency		TBD		TBD	MHz

Table 2-64 • **RTAX2000S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{HCKL}	Input Low to High		3.48		4.09	ns
t_{HCKH}	Input High to Low		3.65		4.29	ns
t_{HPWH}	Minimum Pulse width High	0.37		0.43		ns
t_{HPWL}	Minimum Pulse width Low	0.44		0.52		ns
t_{HCKSW}	Maximum skew		TBD		TBD	ns
f_{HMAX}	Maximum frequency		TBD		TBD	MHz

Routed Clocks

The routed clock (CLK) is a low-skew network that can drive the clock inputs of all sequential modules in the device (logically equivalent to the HCLK), but has the added flexibility in that it can drive the S0 (Enable), S1, PSET, and CLR input of a register (R-cells and I/O registers) as well as any of the inputs of any C-cell in the device. This allows CLKs to be used not only as clocks, but also for other global signals or high fanout nets. All four CLKs are available everywhere on the chip.

Timing Characteristics

Table 2-65 • **RTAX250S (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		2.78		3.27	ns
t_{RCKH}	Input High to Low		2.92		3.44	ns
tR_{PWH}	Minimum Pulse width High	0.48		0.57		ns
t_{RPWL}	Minimum Pulse width Low	0.51		0.60		ns
t_{RCKSW}	Maximum skew		0.06		0.08	ns
f_{RMAX}	Maximum frequency		TBD		TBD	MHz

Table 2-66 • **RTAX1000S (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		3.55		4.17	ns
t_{RCKH}	Input High to Low		3.73		4.38	ns
tR_{PWH}	Minimum Pulse width High	0.48		0.57		ns
t_{RPWL}	Minimum Pulse width Low	0.51		0.60		ns
t_{RCKSW}	Maximum skew		0.10		0.10	ns
f_{RMAX}	Maximum frequency		TBD		TBD	MHz

Table 2-67 • **RTAX2000S (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std.' Speed		Units
		Min.	Max.	Min.	Max.	
t_{RCKL}	Input Low to High		3.55		4.17	ns
t_{RCKH}	Input High to Low		3.73		4.38	ns
tR_{PWH}	Minimum Pulse width High	0.48		0.57		ns
t_{RPWL}	Minimum Pulse width Low	0.51		0.60		ns
t_{RCKSW}	Maximum skew		0.10		0.10	ns
f_{RMAX}	Maximum frequency		TBD		TBD	MHz

Global Resource Distribution

At the root of each global resource is a ClockDistBuffer (CDB). There are two groups of four CDBs for every device. One group, located at the center of the north edge (in the I/O ring) of the chip, sources the four HCLKs. The second group, located at the center of the south edge (again in the I/O ring), sources the four CLKs (Figure 2-42).

Regardless of the type of global resource, HCLK or CLK, each of the eight resources reach the ClockTileDist (CTD) Cluster located at the center of every core tile with zero skew. From the ClockTileDist Cluster, all four HCLKs and four CLKs are distributed through the core tile (Figure 2-43).

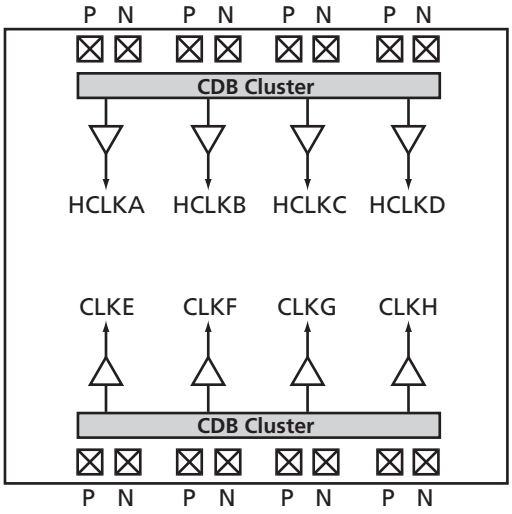


Figure 2-42 • **ClockDistBuffer Group**

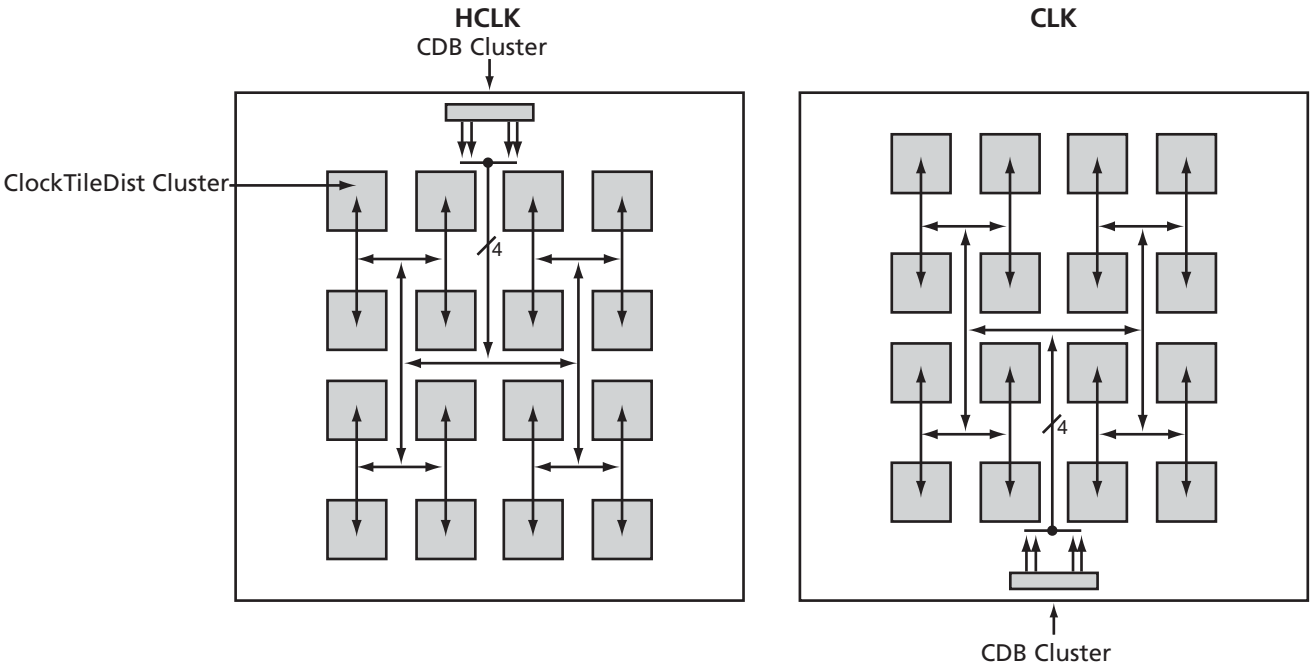


Figure 2-43 • **Example of HCLK and CLK Distributions on the RTAX2000S**

The ClockTileDist Cluster contains an HCLKMux (HM) module for each of the four HCLK trees and a CLKMux (CM) module for each of the CLK trees. The HCLK branches then propagate horizontally through the middle of the core tile to HCLKColDist (HD) modules in every SuperCluster column. The CLK branches propagate vertically through the center of the core tile to CLKRowDist (RD) modules in every SuperCluster row. Together, the HCLK and CLK branches provide for a low-skew global fanout within the core tile (Figure 2-44 and Figure 2-45).

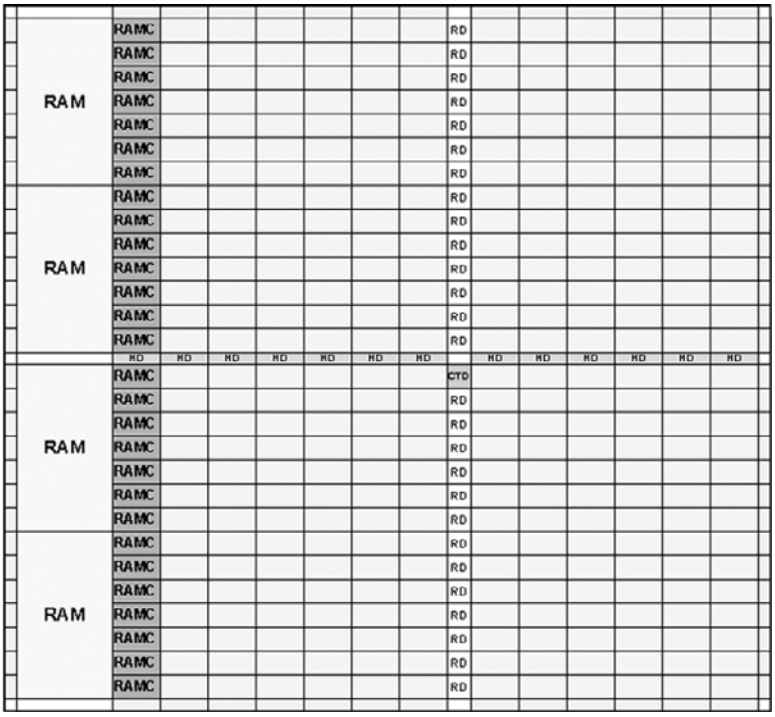


Figure 2-44 • **CTD, CD, and HD Module Layout**

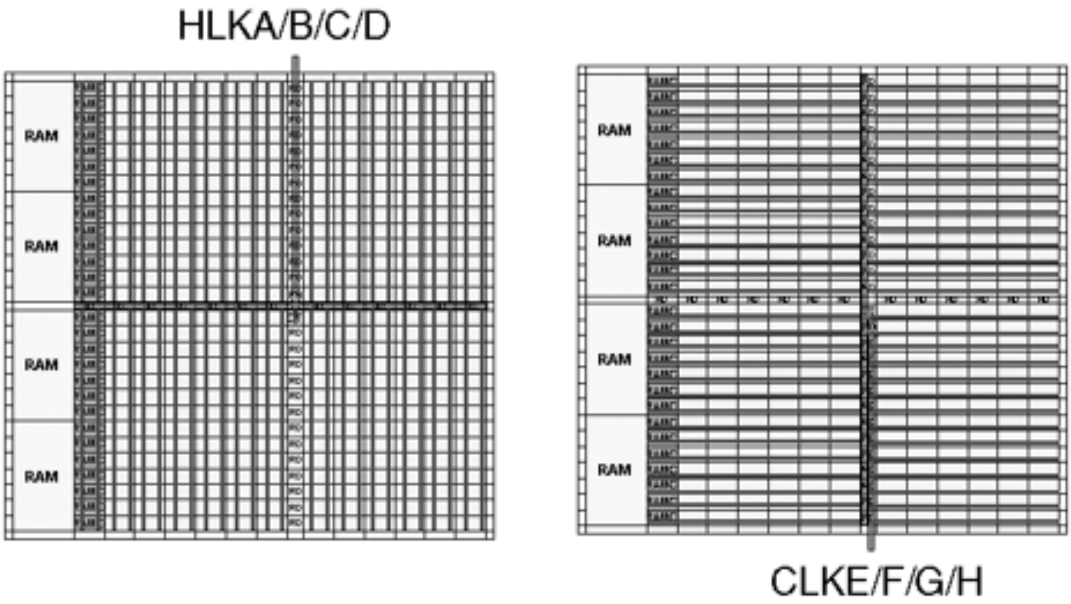


Figure 2-45 • **HCLK and CLK Distribution within a Core Tile**

The HM and CM modules can select between:

- The HCLK or CLK source
- A local signal routed on generic routing resources

This allows each core tile to have eight clocks independent of the other core tiles in the device.

Both HCLK and CLK are segmentable, meaning that individual branches of the global resource can be used independently.

Like the HM and CM modules, the HD and RD modules can select between:

- The HCLK or CLK source from the HM or CM module, respectively
- A local signal routed on generic routing resources

Again, an unused input can be tied to ground for power savings.

The RTAX-S architecture is capable of supporting a large number of local clocks – 24 segments per HCLK driving north-south and 28 segments per CLK driving east-west per core tile.

Actel's Designer software's place-and-route takes advantage of the segmented clock structure found in RTAX-S devices by turning off any unused clock segments. This results in not only better performance but also lower power consumption. Future releases of Designer will give the user greater control over these individual clock segments.

Global Resource Access Macros

Global resources can be driven by one of three sources: external pad(s) or an internal net. These connections can be made by using one of two types of macros: CLKBUF and CLKINT.

CLKBUF and HCLKBUF

CLKBUF (HCLKBUF) is used to drive a CLK (HCLK) from external pads. These macros can be used either generically or with the specific I/O standard desired (e.g. CLKBUF_LVCMOS25, HCLKBUF_LVDS, etc.) (Figure 2-46).

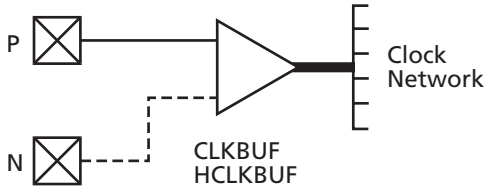


Figure 2-46 • **CLKBUF and HCLKBUF**

Package pins CLKEP and CLKEN are associated with CLKE; package pins HCLKAP and HCLKAN are associated with HCLKA, etc.

Note that when CLKBUF (HCLKBUF) is used with a single-ended I/O standard, it must be tied to the P-pad of the CLK (HCLK) package pin. In this case, the CLK (HCLK) N-pad can be used for user signals.

CLKINT and HCLKINT

CLKINT (HCLKINT) is used to access the CLK (HCLK) resource internally from the user signals (Figure 2-47).

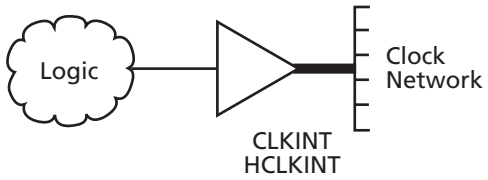


Figure 2-47 • **CLKINT and HCLKINT**

Embedded Memory

The RTAX-S architecture provides extensive, high-speed memory resources to the user. Each 4,608-bit block of RAM contains its own embedded FIFO controller, allowing the user to configure each block as either RAM or FIFO.

To meet the needs of high performance designs, the memory blocks operate in synchronous mode for both read and write operations. However, the read and write clocks are completely independent, and each may operate beyond 500 MHz.

No additional core logic resources are required to cascade the address and data buses when cascading different RAM blocks. Dedicated routing runs along each column of RAM to facilitate cascading.

The RTAX-S memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Since read and write operations can occur asynchronously to one another, special control circuitry is included to prevent metastability, overflow, and underflow. A block diagram of the memory module is illustrated in Figure 2-48.

During RAM operation, read (RA) and write (WA) addresses are sourced by user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Enables with programmable polarity are provided to create upper address bits for cascading up to 16 memory blocks. When cascading memory blocks, the bussed signals WA, WD, WEN, RA, RD, and REN are internally linked to eliminate external routing congestion.

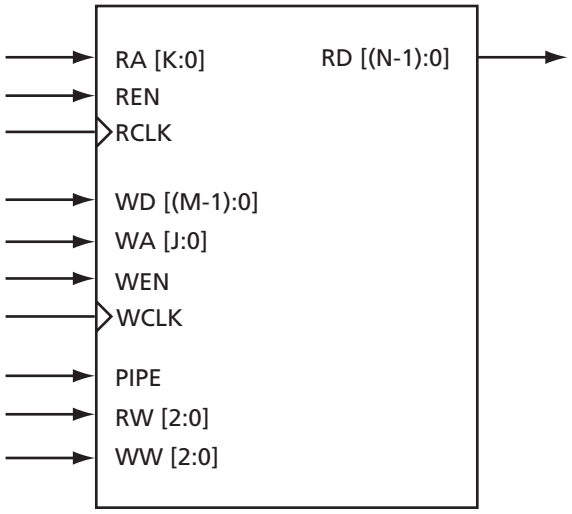


Figure 2-48 • **RTAX-S Memory Module**

RAM

Each memory block consists of 4,608 bits that can be organized as 128x36, 256x18, 512x9, 1kx4, 2kx2, or 4kx1 and are cascadable to create larger memory sizes. This allows built-in bus width conversion (Table 2-68). Each block has independent read and write ports, which enable simultaneous read and write operations. Simultaneous read and write operations to the same address is not supported.

Table 2-68 • **Memory Block WxD Options**

Data-word (in bits)	Depth	Address Bus	Data Bus
1	4,096	RA/WA[11:0]	RD/WD[0]
2	2,048	RA/WA[10:0]	RD/WD[1:0]
4	1,024	RA/WA[9:0]	RD/WD[3:0]
9	512	RA/WA[8:0]	RD/WD[8:0]
18	256	RA/WA[7:0]	RD/WD[17:0]
36	128	RA/WA[6:0]	RD/WD[35:0]

Clocks

The RCLK and the WCLK have independent source polarity selection and can be sourced by any global or local signal.

RAM Configurations

The RTAX-S architecture allows the read side and write side of RAMs to be organized independently, allowing for bus conversion. For example, the write side can be set to 256x18 and the read side to 512x9.

Both the write width and read width for the RAM blocks can be specified independently and changed dynamically with the WW (write width) and RW (read width) pins. The available DxW configurations are: 128x36, 256x18, 512x9, 1kx4, 2kx2, and 4kx1. The allowable RW and WW values are shown in Table 2-70.

When widths of one, two, and four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible. Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined.

Note that the RAM blocks employ little-endian byte order for read and write operations.

Table 2-69 • **RAM Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (can be active on either edge).
WA[J:0]	Input	Write address bus.The value J is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for J is from 6 to15.
WD[M-1:0]	Input	Write data bus. The value M is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
RCLK	Input	Read clock (can be active on either edge).
RA[K:0]	Input	Read address bus. The value K is dependent on the RAM configuration and the number of cascaded memory blocks. The valid range for K is from 6 to 15.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
REN	Input	Read enable. When this signal is valid on the active edge of the clock, data at location RA will be driven onto RD.
WEN	Input	Write enable. When this signal is valid on the active edge of the clock, WD data will be written at location WA.
RW[2:0]	Input	Width of the read operation dataword.
WW[2:0]	Input	Width of the write operation dataword.
Pipe	Input	Sets the pipeline option to be on or off.

Table 2-70 • **Allowable RW and WW Values**

RW(2:0)	WW(2:0)	D x W
000	000	4kx1
001	001	2kx2
010	010	1kx4
011	011	512x9
100	100	256x18
101	101	128x36
11x	11x	reserved

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous – one clock edge):

  In the standard read mode, new data is driven onto the RD bus in the clock cycle immediately following RA and REN valid. The read address is registered on the read-port active-clock edge and data appears at read-data after the RAM access time. Setting PIPE to OFF enables this mode.

- Read Pipelined (synchronous – two clock edges):

  The pipelined mode incurs an additional clock delay from address to data, but enables operation at a much higher frequency. The read-address is registered on the read-port active-clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.

- Write (synchronous – one clock edge):

  On the write active-clock edge, the write data are written into the SRAM at the write address when WEN is high. The setup time of the write address, write enables, and write data are minimal with respect to the write clock.

Write and read transfers are described with timing requirements beginning in "Timing Characteristics" on page 2-63.

Enhancing SEU Performance

SRAM structures are inherently susceptible to upsets caused by high-energy particles encountered in space. High-energy particles can cause an SRAM cell to change state, resulting in the loss or corruption of a valuable data bit. To allow users to achieve high levels of SEU performance, Actel has developed an intellectual property (IP) core to enhance the SEU tolerance of the embedded SRAM within RTAX-S.

This IP employs two upset-mitigation techniques:

- Error Detection and Correction (EDAC)
- A background memory-refresher, or scrubber

The EDAC IP employs the use of shortened Hamming Codes to provide the user with single-error correction/double-error detection (SEC/DED) capabilities. These shortened Hamming Codes provide the user with an implementation that has a reduced number of logic levels and less complexity than traditional Hamming Codes. The ACTgen-generated EDAC IP supports RAM widths of 8, 16, and 32 bits, with a variable RAM depth from 256 to 4k words.

The memory scrubber circuitry has also been embedded in the EDAC IP as an optional block. The scrubber circuitry periodically refreshes memory in the background to ensure that no corruption of its contents has taken place while the memory was not in use. The refresh rate can be set by the user.

The use of EDAC IP combined with the embedded memory scrubber circuitry, gives the RTAX-S an SEU radiation performance level of better than 10^{-10} errors/bit-day. See the application note *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs*.

Timing Model and Waveforms

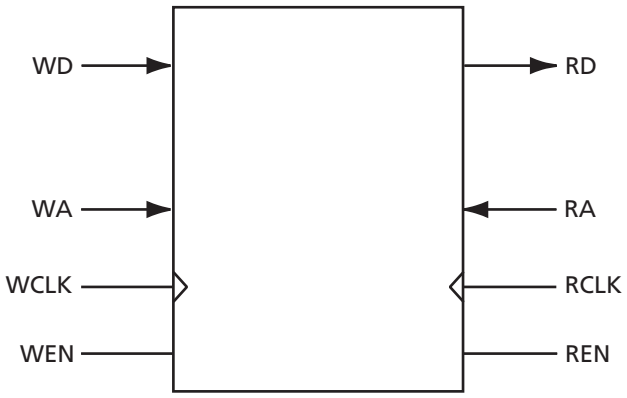


Table 2-71 • **SRAM Model**

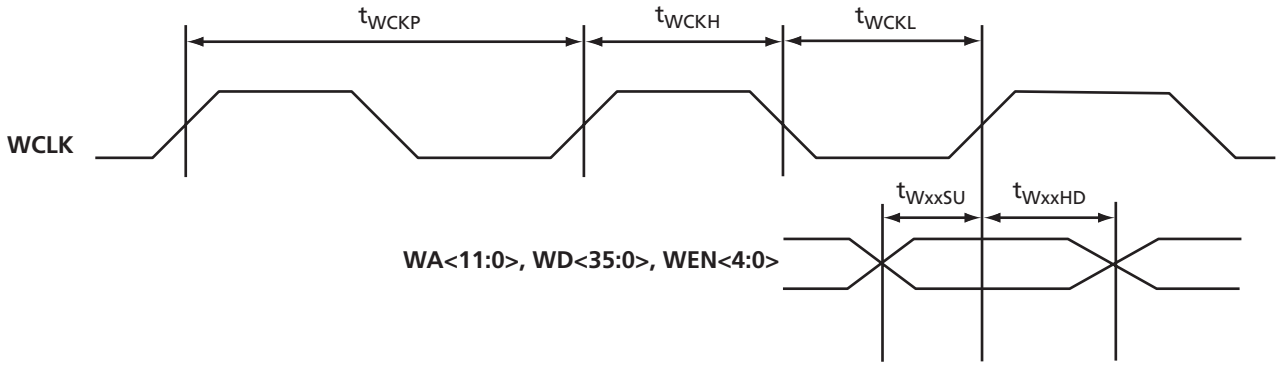


Figure 2-49 • **RAM Write Timing Waveforms**

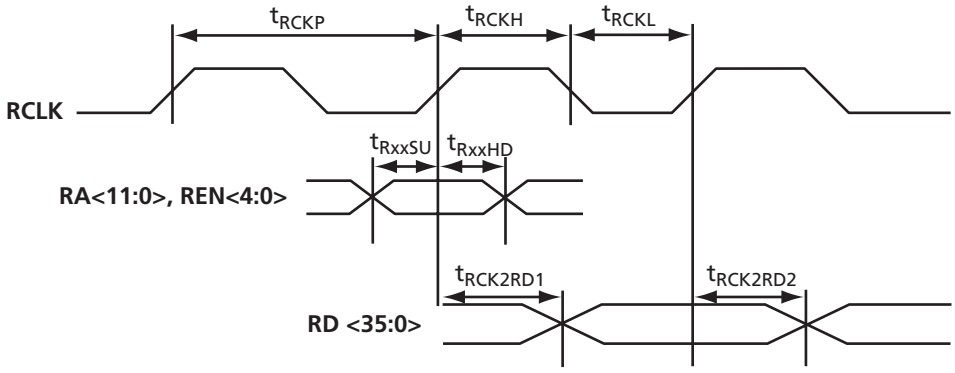


Figure 2-50 • **RAM Read Timing Waveforms**

Timing Characteristics

Table 2-72 • **One RAM Block (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C))**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	1.45		1.70		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	1.45		1.70		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	1.45		1.70		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	1.53		1.80		ns
t_{WCKP}	WCLK Minimum Period	3.07		3.60		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	1.08		1.27		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	1.08		1.27		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.86		2.19	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.50		4.12	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.34		1.58		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	1.62		1.90		ns
t_{RCKP}	RCLK Minimum Period	3.24		3.81		ns

Table 2-73 • **Two RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C))**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	1.86		2.19		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	1.86		2.19		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	1.86		2.19		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	3.07		3.60		ns
t_{WCKP}	WCLK Minimum Period	6.13		7.21		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	2.28		2.68		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	2.28		2.68		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.02		2.38	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.69		4.34	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.27		1.49		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	3.29		3.87		ns
t_{RCKP}	RCLK Minimum Period	6.58		7.74		ns

Table 2-74 • **Four RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C))**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	3.17		3.73		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	3.17		3.73		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	3.17		3.73		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	4.37		5.14		ns
t_{WCKP}	WCLK Minimum Period	8.75		10.28		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	4.13		4.85		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	4.13		4.85		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		3.33		3.91	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		4.49		5.28	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.27		1.49		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	5.16		6.06		ns
t_{RCKP}	RCLK Minimum Period	10.31		12.12		ns

Table 2-75 • **Eight RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C))**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	7.73		9.09		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	7.73		9.09		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	7.73		9.09		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	8.94		10.51		ns
t_{WCKP}	WCLK Minimum Period	17.87		21.01		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	9.04		10.63		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	9.04		10.63		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		4.77		5.61	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		7.33		8.62	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.27		1.49		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	10.05		11.82		ns
t_{RCKP}	RCLK Minimum Period	20.10		23.63		ns

Table 2-76 • **Sixteen RAM Blocks Are Cascaded (Worst-Case Military Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
Write Mode						
t_{WDASU}	Write Data Setup vs. WCLK	22.14		26.03		ns
t_{WDAHD}	Write Data Hold vs. WCLK	0.30		0.35		ns
t_{WADSU}	Write Address Setup vs. WCLK	22.14		26.03		ns
t_{WADHD}	Write Address Hold vs. WCLK	0.30		0.35		ns
t_{WENSU}	Write Enable Setup vs. WCLK	22.14		26.03		ns
t_{WENHD}	Write Enable Hold vs. WCLK	0.30		0.35		ns
t_{WCKH}	WCLK Minimum High Pulse Width	1.31		1.54		ns
t_{WCLKL}	WCLK Minimum Low Pulse Width	23.34		27.44		ns
t_{WCKP}	WCLK Minimum Period	46.69		54.88		ns
Read Mode						
t_{RADSU}	Read Address Setup vs. RCLK	24.27		28.53		ns
t_{RADHD}	Read Address Hold vs. RCLK	0.00		0.00		ns
t_{RENSU}	Read Enable Setup vs. RCLK	24.27		28.53		ns
t_{RENHD}	Read Enable Hold vs. RCLK	0.00		0.00		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		17.02		20.01	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		18.62		21.89	ns
t_{RCLKH}	RCLK Minimum High Pulse Width	1.27		1.49		ns
t_{RCLKL}	RCLK Minimum Low Pulse Width	25.10		29.51		ns
t_{RCKP}	RCLK Minimum Period	50.21		59.02		ns

FIFO

Every memory block has its own embedded FIFO controller. Each FIFO block has one read port and one write port. This embedded FIFO controller uses no internal FPGA logic and features:

- Glitch-free FIFO Flags
- Gray-code address counters/pointers to prevent metastability problems
- Overflow and underflow control

Both ports are configurable in various size from 4kx1 to 128x36, similar to the RAM block size. Each port is fully synchronous.

Read and write operations can be completely independent. Data on the appropriate WD pins are written to the FIFO on every active WCLK edge as long as WEN is high. Data is read from the FIFO and output on the appropriate RD pins on every active RCLK edge as long as REN is asserted.

The FIFO block offers programmable Almost-Empty (AEMPTY) and Almost-Full (AFULL) flags as well as EMPTY and FULL flags (Figure 2-51):

- The FULL flag is synchronous to WCLK. It allows the FIFO to inhibit writing when full.
- The EMPTY flag is synchronous to RCLK. It allows the FIFO to inhibit reading at the empty condition.

Note: Actel recommends that the WCLK and the RCLK are in phase with each other. For more information refer to the application note, *EMPTY and FULL Flag Behaviors of the Axcelerator FIFO Controller*.

Gray code counters are used to prevent metastability problems associated with flag logic. The depth of the FIFO is dependent on the data width and the number of memory blocks used to create the FIFO. The write operations to the FIFO are synchronous with respect to the WCLK, and the read operations are synchronous with respect to the RCLK.

The FIFO block may be reset to the empty state

The FIFO control unit was not implemented with SEU-hardened registers. Designs requiring high SEU tolerance should implement the FIFO control unit from hardened core logic.

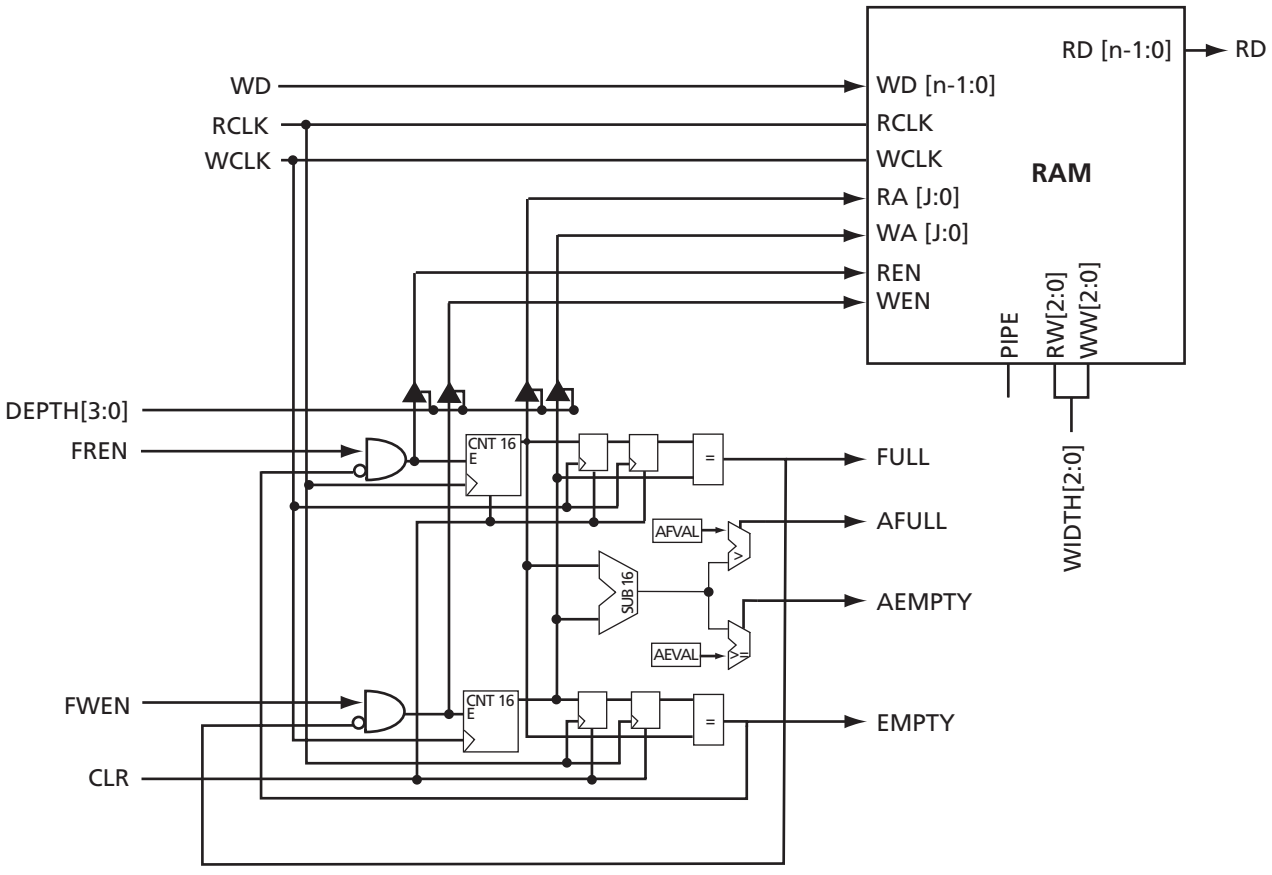


Figure 2-51 • **RTAX-S RAM with Embedded FIFO Controller**

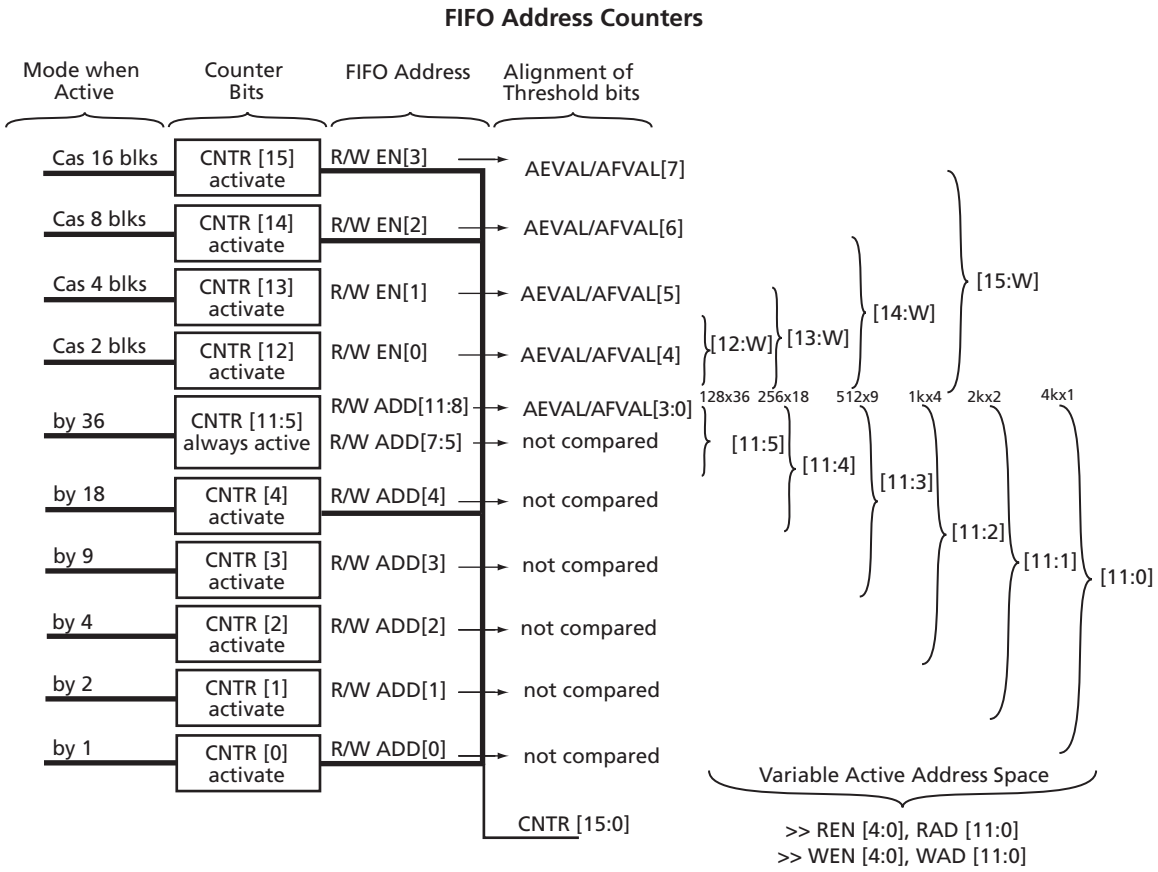
FIFO Flag Logic

The FIFO is user configurable into various depths and widths. Figure 2-52 shows the FIFO address counter details.

- Bits 11 to 5 are active for all modes.
- As the data word size is reduced, more least-significant bits are added to the address.
- As the number of cascaded blocks increases, the number of significant bits in the address increases.

For example, if four blocks are cascaded as a 1kx16 FIFO with each block having a 1kx4 aspect ratio, bits 11 to 2 of the address will be used to specify locations within each RAM block, whereas bits 13 and 12 will be used to specify the RAM block.

The AFULL and AEMPTY flag threshold values are programmable. The threshold values are AFVAL and AEVAL, respectively. Although the trigger threshold for each flag is defined with eight bits, the effective number of threshold bits in the comparison depends on the configuration. Note that the effective number of threshold bits corresponds to the range of active bits in the FIFO address space (Table 2-77).



Note: *Inactive counter bits are set to zero.*

Figure 2-52 • **FIFO Address Counters**

Table 2-77 • **FIFO Flag Logic**

Mode	Inactive AEVAL/AFVAL bits	Inactive DIFF bits (set to 0)	DIFF comparison to AFVAL/AEVAL
Non-cascade	[7:4]	[15:12]	DIFF[11:8] withAE/FVAL[3:0]
Cascade 2 blocks	[7:5]	[15:13]	DIFF[12:8] withAE/FVAL[4:0]
Cascade 4 blocks	[7:6]	[15:14]	DIFF[13:8] withAE/FVAL[5:0]
Cascade 8 blocks	[7]	[15]	DIFF[14:8] withAE/FVAL[6:0]
Cascade 16 blocks	None	None	DIFF[15:8] withAE/FVAL[7:0]

Figure 2-53 illustrates flag generation. The Verilog statements for flag assignment are:

```
assign AF = (DIFF[15:0] >={AFVAL[7:0],8'b00000000})?1:0;
assign AE = ({AEVAL[7:0],8'b00000000}>=DIFF[15:0])?1:0;
```

The number of DIFF-bits active depends on the configuration depth and width (Table 2-78). The active-high CLR pin is used to reset the FIFO to the empty state, which sets FULL and AFULL low, and EMPTY and AEMPTY high.

Assuming that the EMPTY flag is not set, new data is read from the FIFO when REN is valid on the active edge of the clock. Write and read transfers are described with timing requirements in "Timing Characteristics" on page 2-72. For more information refer to the application note, *EMPTY and FULL Flag Behaviors of the Axcelerator FIFO Controller*

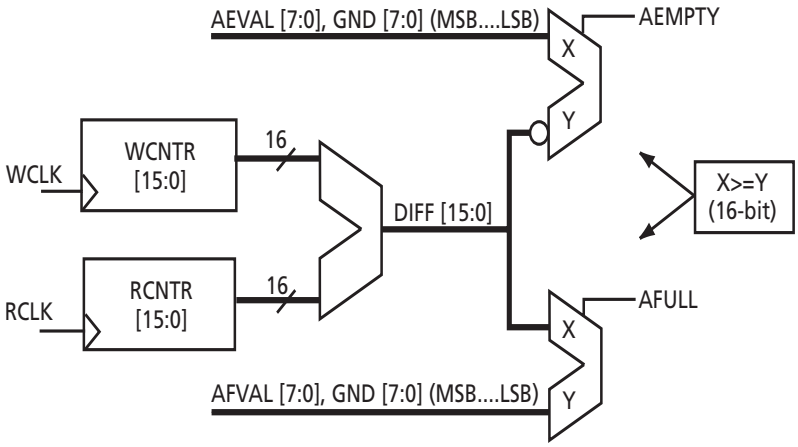


Figure 2-53 • **ALMOST-EMPTY and ALMOST-FULL Logic**

Table 2-78 • **Number of Available Configuration Bits**

Number of Blocks	Block DxW	Number of AEVAL/AFVAL Bits
1	1x1	4
2	1x2	4
2	2x1	5
4	1x4	4
4	2x2	5
4	4x1	6
8	1x8	4
8	2x4	5
8	4x2	6
8	8x1	7
16	1x16	4
16	2x8	5
16	4x4	6
16	8x2	7
16	16x1	8

Glitch Elimination

An analog filter is added to each FIFO controller to guarantee, glitch-free FIFO-flag logic.

Overflow and Underflow Control

The counter MSB keeps track of the difference between the read address (RA) and the write address (WA). The EMPTY flag is set when the read and write addresses are equal. To prevent underflow, the write address is double-sampled by the read clock prior to comparison with the read address (part A in Figure 2-54). To prevent overflow, the read address is double-sampled by the write clock prior to comparison to the write address (part B in Figure 2-54).

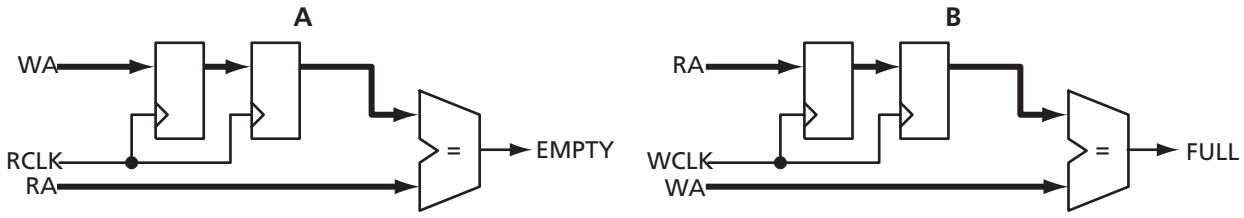


Figure 2-54 • **Overflow and Underflow Control**

FIFO Configurations

Unlike the RAM, the FIFO's write width and read width cannot be specified independently. For the FIFO, the write and read widths must be the same. The WIDTH pins are used to specify one of six allowable word widths, as shown in Table 2-79.

The DEPTH pins allow RAM cells to be cascaded to create larger FIFOs. The four pins allow depths of 2, 4, 8, and 16 to be specified. Table 2-68 on page 2-59 describes the FIFO depth options for various data width and memory blocks.

Interface

Figure 2-55 shows a logic block diagram of the RTAX-S FIFO module.

Cascading FIFO Blocks

FIFO blocks can be cascaded to create deeper FIFO functions. When building larger FIFO blocks, if the word width can be fractured in a multi-bit FIFO, the fractured word configuration is recommended over a cascaded configuration. For example, 256x36 can be configured as two blocks of 256x18. This should be taken into account when building the FIFO blocks manually. However, when using ACTgen, the user only needs to specify the depth and width of the necessary FIFO blocks. ACTgen automatically configures these blocks to optimize performance.

Clock

As with RAM configuration, the RCLK and WCLK pins have independent polarity selection

Table 2-79 • **FIFO Width Configurations**

WIDTH(2:0)	WxD
000	1x4k
001	2x2k
010	4x1k
011	9x512
100	18x256
101	36x128
11x	reserved

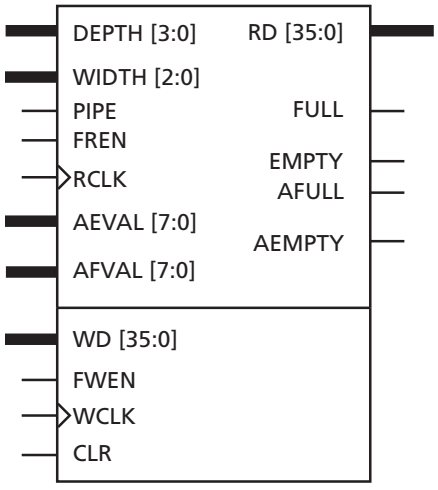


Figure 2-55 • **FIFO Block Diagram**

Table 2-80 • **FIFO Signal Description**

Signal	Direction	Description
WCLK	Input	Write clock (active either edge).
FWEN	Input	FIFO write enable. When this signal is asserted, the WD bus data is latched into the FIFO, and the internal write counters are incremented.
WD[N-1:0]	Input	Write data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
FULL	Output	Active high signal indicating that the FIFO is FULL. When this signal is set, additional write requests are ignored.
AFULL	Output	Active high signal indicating that the FIFO is AFULL.
AFVAL	Input	8-bit input defining the AFULL value of the FIFO.
RCLK	Input	Read clock (active either edge).
FREN	Input	FIFO read enable.
RD[N-1:0]	Output	Read data bus. The value N is dependent on the RAM configuration and can be 1, 2, 4, 9, 18, or 36.
EMPTY	Output	Empty flag indicating that the FIFO is EMPTY. When this signal is asserted, attempts to read the FIFO will be ignored.
AEMPTY	Output	Active high signal indicating that the FIFO is AEMPTY.
AEVAL	Input	8-bit input defining the almost-empty value of the FIFO.
PIPE	Input	Sets the pipe option on or off.
CLR	Input	Active high clear input.
DEPTH	Input	Determines the depth of the FIFO and the number of FIFOs to be cascaded.
WIDTH	Input	Determines the width of the dataword / width of the FIFO, and the number of the FIFOs to be cascaded.

Timing Characteristics

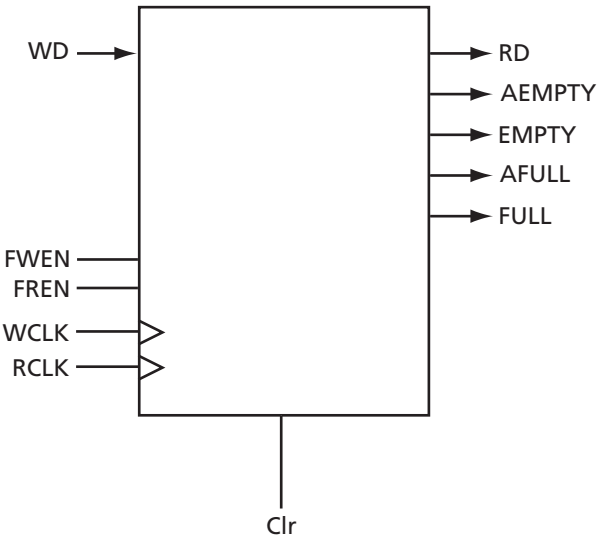


Figure 2-56 • **FIFO Model**

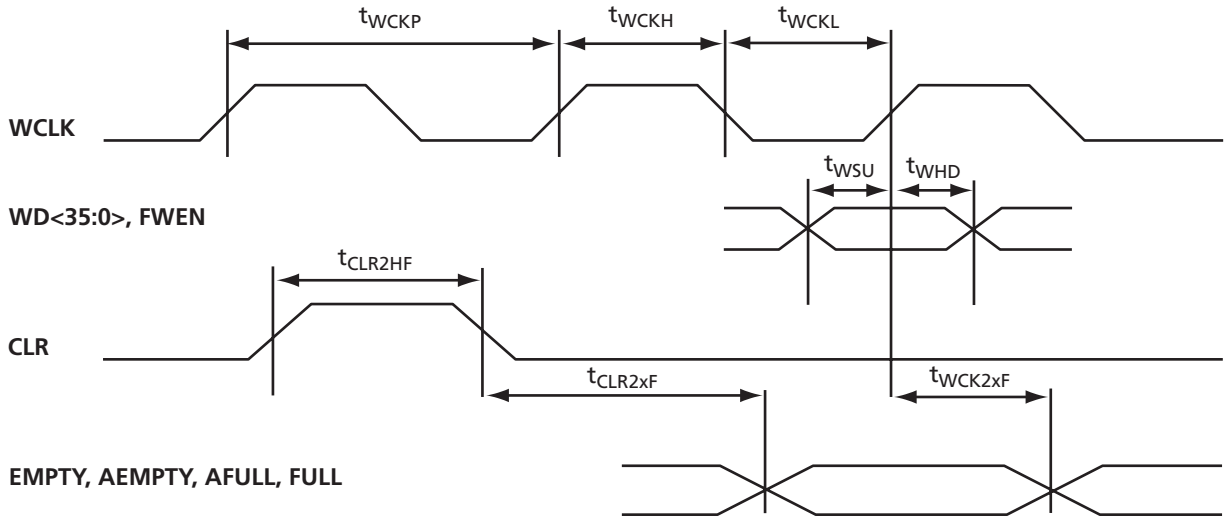


Figure 2-57 • **FIFO Write Timing**

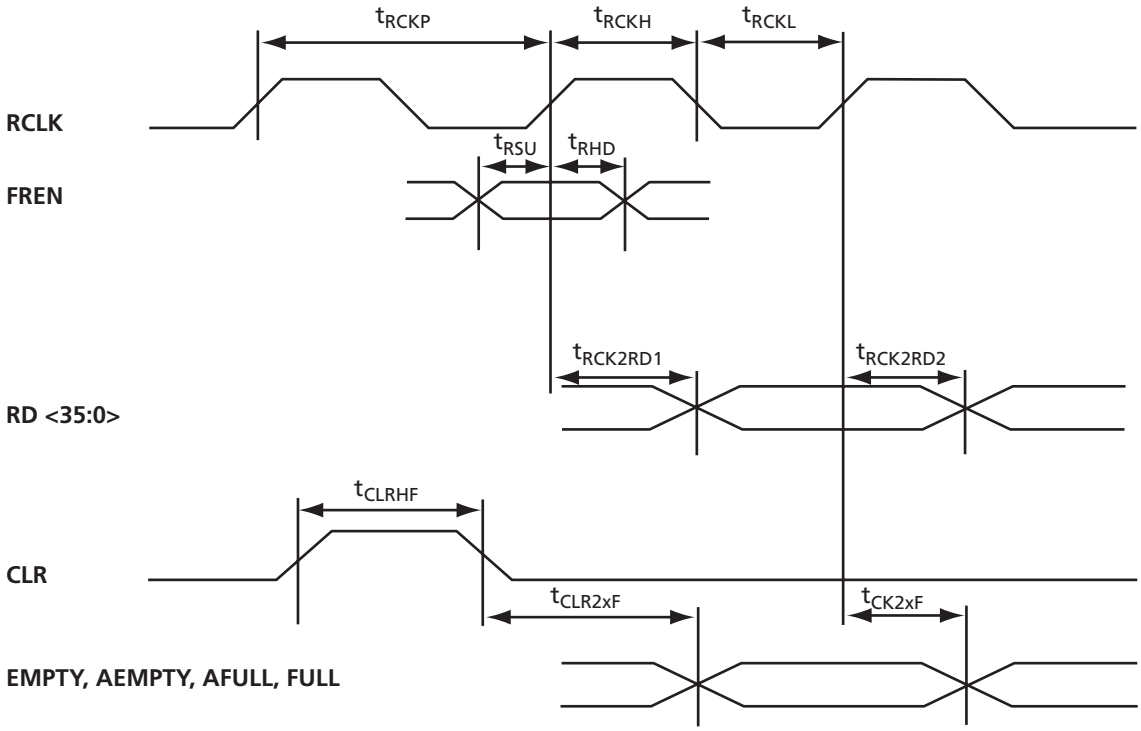


Figure 2-58 • **FIFO Read Timing**

Table 2-81 • **One FIFO Block (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	1.45		1.70		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	1.31		1.54		ns
t_{WCKL}	WCLK Low	1.53		1.80		ns
t_{WCKP}	Minimum WCLK Period					
t_{RSU}	Read Setup	1.08		1.27		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	1.34		1.58		ns
t_{RCKL}	RCLK Low	1.62		1.90		ns
t_{RCKP}	Minimum RCLK period					
t_{CLRHF}	Clear High	1.45		1.70		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.70		3.17		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	6.18		7.27		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	3.00		3.52		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	7.11		8.36		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		1.86		2.19	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.50		4.12	ns

Table 2-82 • **Two FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	1.86		2.19		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	1.31		1.54		ns
t_{WCKL}	WCLK Low	3.07		3.60		ns
t_{WCKP}	Minimum WCLK Period					
t_{RSU}	Read Setup	2.28		2.68		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	1.27		1.49		ns
t_{RCKL}	RCLK Low	3.29		3.87		ns
t_{RCKP}	Minimum RCLK period					
t_{CLRHF}	Clear High	1.45		1.70		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.70		3.17		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	6.18		7.27		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	3.00		3.52		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	7.11		8.36		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		2.02		2.38	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		3.69		4.34	ns

Table 2-83 • **Four FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	3.17		3.73		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	1.31		1.54		ns
t_{WCKL}	WCLK Low	4.37		5.14		ns
t_{WCKP}	Minimum WCLK Period					
t_{RSU}	Read Setup	4.13		4.85		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	1.27		1.49		ns
t_{RCKL}	RCLK Low	5.16		6.06		ns
t_{RCKP}	Minimum RCLK period					
t_{CLRHF}	Clear High	1.45		1.70		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.70		3.17		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	6.18		7.27		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	3.00		3.52		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	7.11		8.36		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		3.33		3.91	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		4.49		5.28	ns

Table 2-84 • **Eight FIFO Blocks Are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	7.73		9.09		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	1.31		1.54		ns
t_{WCKL}	WCLK Low	8.94		10.51		ns
t_{WCKP}	Minimum WCLK Period					
t_{RSU}	Read Setup	9.04		10.63		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	1.27		1.49		ns
t_{RCKL}	RCLK Low	10.05		11.82		ns
t_{RCKP}	Minimum RCLK period					
t_{CLRHF}	Clear High	1.45		1.70		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.70		3.17		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	6.18		7.27		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	3.00		3.52		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	7.11		8.36		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		4.77		5.61	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		7.33		8.62	ns

Table 2-85 • **Sixteen FIFO Blocks are Cascaded (Worst-Case MIlitary Conditions V_{CCA} = 1.4V, V_{CCI} = 3.0V, T_J = 125°C)**

Parameter	Description	'–1' Speed		'Std' Speed		Units
		Min.	Max.	Min.	Max.	
FIFO Module Timing						
t_{WSU}	Write Setup	22.14		26.03		ns
t_{WHD}	Write Hold	0.30		0.35		ns
t_{WCKH}	WCLK High	1.31		1.54		ns
t_{WCKL}	WCLK Low	23.34		27.44		ns
t_{WCKP}	Minimum WCLK Period					
t_{RSU}	Read Setup	24.27		28.53		ns
t_{RHD}	Read Hold	0.00		0.00		ns
t_{RCKH}	RCLK High	1.27		1.49		ns
t_{RCKL}	RCLK Low	25.10		29.51		ns
t_{RCKP}	Minimum RCLK period					
t_{CLRHF}	Clear High	1.45		1.70		ns
t_{CLR2FF}	Clear-to-flag (EMPTY/FULL)	2.70		3.17		ns
t_{CLR2AF}	Clear-to-flag (AEMPTY/AFULL)	6.18		7.27		ns
t_{CK2FF}	Clock-to-flag (EMPTY/FULL)	3.00		3.52		ns
t_{CK2AF}	Clock-to-flag (AEMPTY/AFULL)	7.11		8.36		ns
$t_{RCK2RD1}$	RCLK-To-OUT (Pipelined)		17.02		20.01	ns
$t_{RCK2RD2}$	RCLK-To-OUT (Non-Pipelined)		18.62		21.89	ns

Building RAM and FIFO Modules

RAM and FIFO modules can be generated and included in a design in two different ways:

- Using the ACTgen Macro Builder where the user defines the depth and width of the FIFO/RAM, and then instantiates this block into the design (please refer to Actel's *ACTgen Macros User's Guide* for more information).
- The alternative is to instantiate the RAM/FIFO blocks manually, using inverters for polarity control and tying all unused data bits to ground.

Other Architectural Features

Charge Pump Bypass

To reduce power consumption, the internal charge pump can be bypassed and an external power supply voltage can be used instead. This saves the internal charge-pump operating current, resulting in no DC current draw. The RTAX-S family devices have a dedicated "V_{PUMP}" pin that can be used to access an external charge pump device. In normal chip operation, when using the internal charge pump, V_{PUMP} should be tied to GND. When the voltage level on V_{PUMP} is set to 3.3V, the internal charge pump is turned off, and the V_{PUMP} voltage will be used as the charge pump voltage. Adequate voltage regulation (i.e., high drive, low output impedance, and good decoupling) should be used at V_{PUMP}.

JTAG

RTAX-S offers a JTAG interface that is compliant with the IEEE 1149.1 standard except for the device ID length which is 33 bits. The user can employ the JTAG interface for probing a design and executing any JTAG public instructions as defined in the Table 2-86. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note, which also applies to the RTAX-S family of devices.

Table 2-86 • **JTAG Instruction Code**

Instruction (IR4:IR0)	Binary Code
EXTEST	00000
PRELOAD / SAMPLE	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
DIAGNOSTIC	10000
Reserved	All others
BYPASS	11111

Interface

The interface consists of four inputs: Test Mode Select (TMS), Test Data In (TDI), Test Clock (TCK), TAP Controller Reset (TRST), and an output, Test Data Out (TDO). TMS, TDI, and TRST have on-chip pull-up resistors.

TRST

TRST (Test-Logic Reset) is an active-low asynchronous reset signal to the TAP controller. The TRST input can be used to reset the Test Access Port (TAP) Controller to the TRST state. The TAP Controller can be held at this state permanently by grounding the TRST pin. To hold the JTAG TAP controller in the TRST state, it is recommended to connect TRST directly to ground for flight.

There is an optional internal pull-up resistor available for the TRST input that can be set by the user at programming. Care should be exercised when using this option in combination with an external tie-off to ground.

An on-chip power-on-reset (POWRST) circuit is included. POWRST has the same function as "TRST," but it only occurs at power-up or during recovery from a V_{CCA} and/or V_{CCDA} voltage drop.

TDO

TDO is normally tristated, and it is active only when the TAP controller is in the "Shift_DR" state or "Shift_IR" state. The least significant bit of the selected register (i.e., IR or DR) is clocked out to TDO first by the falling edge of TCK.

TAP Controller

The TAP Controller is compliant with the IEEE Standard 1149.1. It is a state machine of 16 states that controls the Instruction Register (IR) and the Data Registers (such as Boundary-Scan Register, IDCODE, USRCODE, BYPASS, etc.). The TAP Controller steps into one of the states depending on the sequence of TMS at the rising edges of TCK.

Instruction Register (IR)

The IR has five bits (IR4 to IR0). At the TRST state, IR is reset to IDCODE. Each time when IR is selected, it goes through "select IR-Scan," "Capture-IR," "Shift-IR," all the way through "Update-IR." When there is no test error, the first five data bits coming out of TDO during the "Shift-IR" will be "10111." If a test error occurs, the last three bits will contain one to three zeroes corresponding to negatively asserted signals: "TDO_ERRORB," "PROBA_ERRORB," and "PROBB_ERRORB." The error(s) will be erased when the TAP is at the "Update-IR" or the TRST state. When in user mode start-up sequence, if the micro-probe has not been used, the "PROBA_ERRORB" is used as a "Power-up done successfully" flag.

During flight, the following configurations for all JTAG and Probe pins are recommended (Table 2-87 on page 2-78).

Table 2-87 • **JTAG and Probe Pin Recommendations for Flight**

JTAG and Probe Pins	Configurations
TCK	• Can be hardwired to V_{CCDA} or ground • Can be driven to V_{CCDA} or ground • Must not be left unterminated
TDO	Must be left unconnected
TDI	• Can be hardwired or driven to V_{CCDA} • Can be left unconnected (equipped with internal 10k pull-up resistor)
TMS	• Can be hardwired or driven to V_{CCDA} • Can be left unconnected (equipped with internal 10k pull-up resistor)
TRST	Must be hardwired to ground (equipped with optional internal 10k pull-up resistor)
PRA/B/C/D	Must be left unconnected

Data Registers (DRs)

Data registers are distributed throughout the chip. They store testing/programming vectors. The MSB of a data register is connected to TDI, while the LSB is connected to TDO. There are different types of data registers. Descriptions of the main registers are as follow:

1. IDCODE:

   The IDCODE is a 33-bit hard coded JTAG Silicon Signature. It is a hardwired device ID code, which contains the Actel identity, part number, and version number in a specific JTAG format. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note for more information.

2. USERCODE:

   The USERCODE is a 33-bit programmable JTAG Silicon Signature. It is a supplementary identity code for the user to program information to distinguish different programmed parts. USERCODE fuses will read out as "zeroes" when not programmed, so only the "1" bits need to be programmed. Refer to the *IEEE Standard 1149.1 (JTAG) in the Axcelerator Family* application note for more information.

3. Boundary-Scan Register (BSR):

   Each I/O contains three BSR Cells. Each cell has a shift register bit, a latch, and two MUXes. The boundary-scan cells are used for the Output-enable (E), Output (O), and Input (I) registers. The bit order of the boundary-scan cells for each of them is E-O-I. The boundary-scan cells are then chained serially to form the BSR. The length of the BSR is the number of I/Os in the die (not the package) multiplied by three. This excludes special function pins (TRST, TCK, TMS, TDI, TDO, PRA, PRB, PRC, PRD, and VPUMP).

4. Bypass Register (BYR):

   This is the "1-bit" register. It is used to shorten the TDI-TDO serial chain in board-level testing to only one bit per device not being tested. It is also selected for all "reserved" or unused instructions.

Probing

Internal activities of the JTAG interface can be observed via the Silicon Explorer II probes: "PRA," "PRB," "PRC," and "PRD."

Special Fuses

Security

Actel antifuse FPGAs, with FuseLock technology, offer the highest level of design security available in a programmable logic device. Since antifuse FPGAs are live at power-up, there is no bitstream that can be intercepted, and no bitstream or programming data is ever downloaded to the device during power-up, thus making device cloning impossible. In addition, special security fuses are hidden throughout the fabric of the device and may be programmed by the user to thwart attempts to reverse engineer the device by attempting to exploit either the programming or probing interfaces. Both invasive and noninvasive attacks against an RTAX-S device that access or bypass these security fuses will destroy access to the rest of the device. (refer to the *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper).

Look for this symbol to ensure your valuable IP is secure.

FuseLock™

Figure 2-59 • **FuseLock Logo**

To ensure maximum security in RTAX-S devices, it is recommended that the user program the device security fuse (SFUS). When programmed, the Silicon Explorer II testing probes are disabled to prevent internal probing, and the programming interface is also disabled. All JTAG public instructions are still accessible by the user.

For more information, refer to Actel's *Implementation of Security in Actel Antifuse FPGAs* application note.

Global Set Fuse

The Global Set Fuse determines if all R-cells and I/O Registers (InReg, OutReg, and EnReg) are either cleared or preset by driving the GCLR and GPSET inputs of all R-cells and I/O Registers ("R-cell" on page 2-45). Default setting is to clear all registers (GCLR = 0 and GPSET =1) at device power-up. When the GBSETFUS option is checked during FUSE file generation, all registers are preset (GCLR = 1 and GPSET= 0). A local CLR or PRESET will take precedence overt this setting. Both pins are pulled HIGH during normal device operation. For use details, see Libero IDE online help.

Silicon Explorer II Probe Interface

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with the Designer tools, allows users to examine any of the internal nets (except I/O registers) of the device while it is operating in a prototype or a production system. The user can probe up to four nodes at a time without changing the placement and routing of the design and without using any additional device resources. Highlighted nets in Designer's ChipPlanner can be accessed using Silicon Explorer II in order to observe their real time values.

Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle. In addition, Silicon Explorer II does not require relayout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers. By eliminating multiple place-and-route program cycles the integrity of the design is maintained throughout the debug process.

Each member of the RTAX-S family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the RTAX-S device. Each core tile can has up to two probe signals. To disallow probing, the SFUS security fuse in the silicon signature has to be programmed "Special Fuses" on page 2-78).

Silicon Explorer II connects to the host PC using a standard serial port connector. Connections to the circuit board are achieved using a nine-pin D-Sub connector (Figure 1-9 on page 1-8). Once the design has been placed-and-routed, and the RTAX-S device has been programmed, Silicon Explorer II can be connected and the Explorer software can be launched.

Silicon Explorer II comes with an additional optional PC hosted tool that emulates an 18-channel logic analyzer. Four channels are used to monitor four internal nodes, and 14 channels are available to probe external signals. The software included with the tool provides the user with an intuitive interface that allows for easy viewing and editing of signal waveforms.

Programming

Device programming is supported through the Silicon Sculptor II, a single-site, robust and compact device programmer for the PC. Up to four Silicon Sculptor IIs can be daisy-chained and controlled from a single PC host. With standalone software for the PC, Silicon Sculptor II is designed to allow concurrent programming of multiple units from the same PC when daisy-chained.

Silicon Sculptor II programs devices independently to achieve the fastest programming times possible. Each fuse is verified by Silicon Sculptor II to ensure correct programming. Furthermore, at the end of programming, there are integrity tests that are run to ensure that programming was completed properly. Not only does it test programmed and nonprogrammed fuses, Silicon Sculptor II also provides a self-test to test its own hardware extensively.

Programming an RTAX-S device using Silicon Sculptor II is similar to programming any other antifuse device. The procedure is as follows:

1. Load the .AFM file.
2. Select the device to be programmed.
3. Begin programming.

When the design is ready to go to production, Actel offers device volume-programming services either through distribution partners or via our In-House Programming Center.

For more details on programming the RTAX-S devices, please refer to the *Silicon Sculptor II User's Guide*.

Package Pin Assignments

208-Pin CQFP

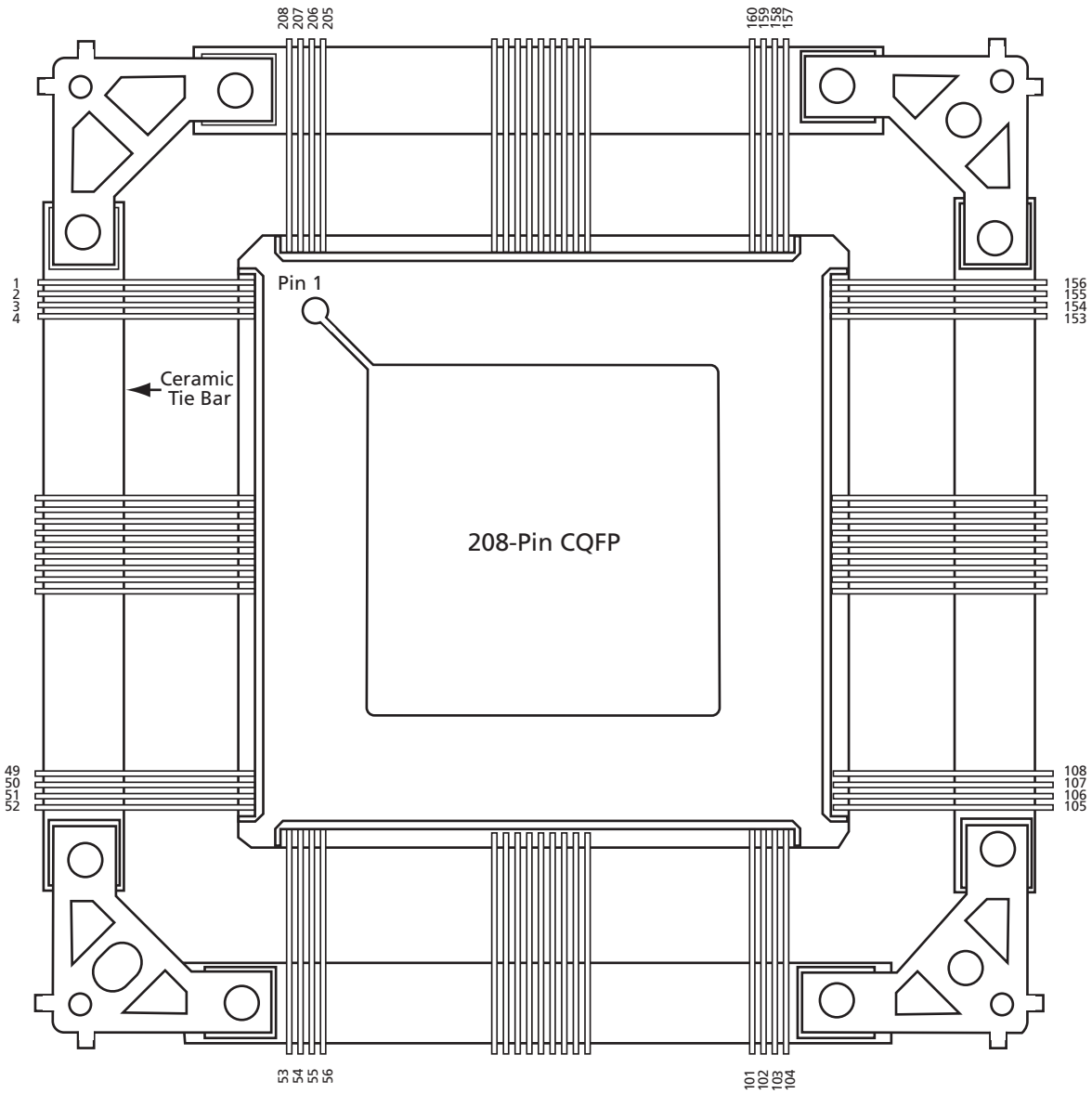


Figure 3-1 • **208-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/rescenter/package/index.html.

208 CQFP	
RTAX250S Function	**Pin Number**
Bank 0	
IO02NB0F0	197
IO03NB0F0	198
IO03PB0F0	199
IO12NB0F0/HCLKAN	191
IO12PB0F0/HCLKAP	192
IO13NB0F0/HCLKBN	185
IO13PB0F0/HCLKBP	186
Bank 1	
IO14NB1F1/HCLKCN	180
IO14PB1F1/HCLKCP	181
IO15NB1F1/HCLKDN	174
IO15PB1F1/HCLKDP	175
IO16NB1F1	170
IO16PB1F1	171
IO24NB1F1	165
IO24PB1F1	166
IO26NB1F1	161
IO26PB1F1	162
IO27NB1F1	159
IO27PB1F1	160
Bank 2	
IO29NB2F2	151
IO29PB2F2	153
IO30NB2F2	152
IO30PB2F2	154
IO31PB2F2	148
IO32NB2F2	146
IO32PB2F2	147
IO34NB2F2	144
IO34PB2F2	145
IO39NB2F2	139
IO39PB2F2	140
IO40PB2F2	141
IO41NB2F2	137
IO41PB2F2	138
IO43NB2F2	132

208 CQFP	
RTAX250S Function	**Pin Number**
IO43PB2F2	134
IO44NB2F2	131
IO44PB2F2	133
Bank 3	
IO45NB3F3	127
IO45PB3F3	129
IO46NB3F3	126
IO46PB3F3	128
IO48NB3F3	122
IO48PB3F3	123
IO50NB3F3	120
IO50PB3F3	121
IO55NB3F3	116
IO55PB3F3	117
IO57NB3F3	114
IO57PB3F3	115
IO59NB3F3	110
IO59PB3F3	111
IO60NB3F3	108
IO60PB3F3	109
IO61NB3F3	106
IO61PB3F3	107
Bank 4	
IO62NB4F4	100
IO62PB4F4	103
IO63NB4F4	101
IO63PB4F4	102
IO64NB4F4	96
IO64PB4F4	97
IO72NB4F4	91
IO72PB4F4	92
IO74NB4F4/CLKEN	87
IO74PB4F4/CLKEP	88
IO75NB4F4/CLKFN	81
IO75PB4F4/CLKFP	82
Bank 5	
IO76NB5F5/CLKGN	76

208 CQFP	
RTAX250S Function	**Pin Number**
IO76PB5F5/CLKGP	77
IO77NB5F5/CLKHN	70
IO77PB5F5/CLKHP	71
IO78NB5F5	66
IO78PB5F5	67
IO86NB5F5	62
IO87NB5F5	60
IO87PB5F5	61
IO88NB5F5	56
IO88PB5F5	57
IO89NB5F5	54
IO89PB5F5	55
Bank 6	
IO91NB6F6	47
IO91PB6F6	49
IO92NB6F6	48
IO92PB6F6	50
IO93NB6F6	42
IO93PB6F6	43
IO94PB6F6	44
IO96NB6F6	40
IO96PB6F6	41
IO101NB6F6	35
IO101PB6F6	36
IO102PB6F6	37
IO103NB6F6	33
IO103PB6F6	34
IO105NB6F6	28
IO105PB6F6	30
IO106NB6F6	27
IO106PB6F6	29
Bank 7	
IO107NB7F7	23
IO107PB7F7	25
IO108NB7F7	22
IO108PB7F7	24
IO110NB7F7	18

208 CQFP	
RTAX250S Function	**Pin Number**
IO110PB7F7	19
IO112NB7F7	16
IO112PB7F7	17
IO117NB7F7	12
IO117PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121PB7F7	7
IO122NB7F7	5
IO122PB7F7	6
IO123NB7F7	3
IO123PB7F7	4
Dedicated I/O	
GND	9
GND	15
GND	21
GND	32
GND	39
GND	46
GND	51
GND	59
GND	65
GND	69
GND	90
GND	94
GND	99
GND	104
GND	113
GND	119
GND	125
GND	136
GND	143
GND	150
GND	155
GND	164
GND	169
GND	173

208 CQFP	
RTAX250S Function	**Pin Number**
GND	194
GND	196
GND	201
GND	208
NC	72
NC	73
NC	74
NC	75
NC	83
NC	84
NC	85
NC	86
NC	176
NC	177
NC	178
NC	179
NC	187
NC	188
NC	189
NC	190
PRA	184
PRB	183
PRC	80
PRD	79
TCK	205
TDI	204
TDO	203
TMS	206
TRST	207
V_{CCA}	2
V_{CCA}	14
V_{CCA}	38
V_{CCA}	52
V_{CCA}	64
V_{CCA}	93
V_{CCA}	118
V_{CCA}	142

208 CQFP	
RTAX250S Function	**Pin Number**
V_{CCA}	156
V_{CCA}	168
V_{CCA}	195
V_{CCDA}	1
V_{CCDA}	26
V_{CCDA}	53
V_{CCDA}	63
V_{CCDA}	78
V_{CCDA}	95
V_{CCDA}	105
V_{CCDA}	130
V_{CCDA}	157
V_{CCDA}	167
V_{CCDA}	182
V_{CCDA}	202
$V_{CCI}B0$	193
$V_{CCI}B0$	200
$V_{CCI}B1$	163
$V_{CCI}B1$	172
$V_{CCI}B2$	135
$V_{CCI}B2$	149
$V_{CCI}B3$	112
$V_{CCI}B3$	124
$V_{CCI}B4$	89
$V_{CCI}B4$	98
$V_{CCI}B5$	58
$V_{CCI}B5$	68
$V_{CCI}B6$	31
$V_{CCI}B6$	45
$V_{CCI}B7$	8
$V_{CCI}B7$	20
V_{PUMP}	158

256-Pin CQFP

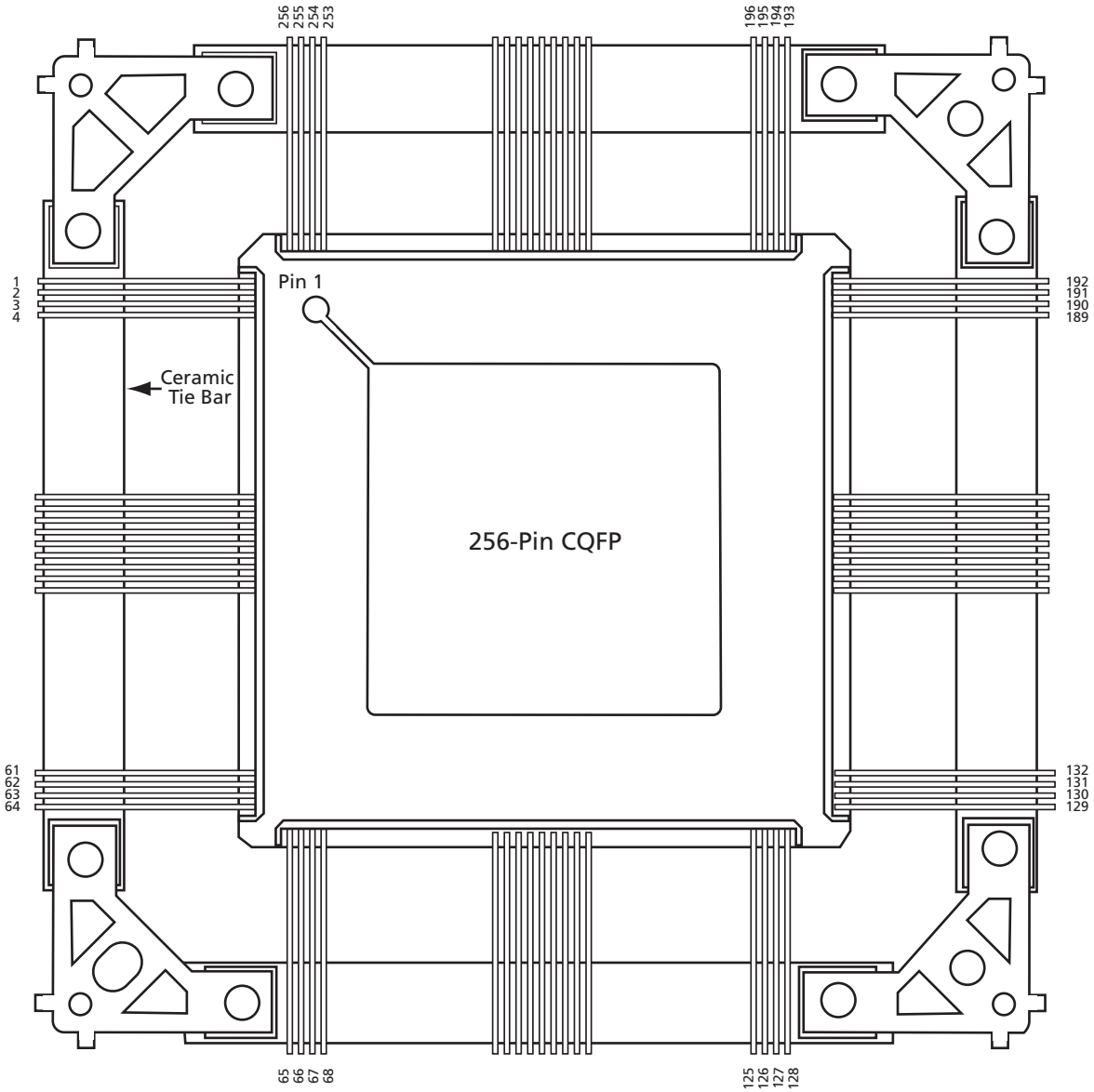


Figure 3-2 • **208-Pin CQFP (Top View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/rescenter/package/index.html.

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
Bank 0	
IO01NB0F0	248
IO01PB0F0	249
IO04NB0F0	246
IO04PB0F0	247
IO05NB0F0	242
IO05PB0F0	243
IO08NB0F0	240
IO08PB0F0	241
IO37NB0F3	234
IO37PB0F3	235
IO41NB0F3/HCLKAN	232
IO41PB0F3/HCLKAP	233
IO42NB0F3/HCLKBN	228
IO42PB0F3/HCLKBP	229
Bank 1	
IO43NB1F6/HCLKCN	220
IO43PB1F6/HCLKCP	221
IO44NB1F6/HCLKDN	216
IO44PB1F6/HCLKDP	217
IO65NB1F8	210
IO65PB1F8	211
IO69NB1F8	208
IO69PB1F8	209
IO70NB1F8	199
IO71NB1F8	204
IO71PB1F8	205
IO73NB1F8	202
IO73PB1F8	203
IO74NB1F8	197
IO74PB1F8	198
IO87NB2F12	187
IO87PB2F12	188
IO89PB2F12	186
Bank 2	
IO107NB2F14	184
IO107PB2F14	185

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO110NB2F14	180
IO110PB2F14	181
IO111NB2F14	178
IO111PB2F14	179
IO112NB2F14	174
IO112PB2F14	175
IO113NB2F14	172
IO113PB2F14	173
IO114NB2F14	168
IO114PB2F14	169
IO115NB2F14	166
IO115PB2F14	167
IO117NB2F14	162
IO117PB2F14	163
Bank 3	
IO139NB3F19	158
IO139PB3F19	159
IO141NB3F19	154
IO141PB3F19	155
IO142NB3F19	152
IO142PB3F19	153
IO145NB3F19	148
IO145PB3F19	149
IO146NB3F19	146
IO146PB3F19	147
IO147NB3F19	140
IO147PB3F19	141
IO148NB3F19	142
IO148PB3F19	143
IO149NB3F19	136
IO149PB3F19	137
IO165NB3F21	135
IO167NB3F21	133
IO167PB3F21	134
Bank 4	
IO181NB4F25	124
IO181PB4F25	125

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO182NB4F25	122
IO182PB4F25	123
IO183NB4F25	118
IO183PB4F25	119
IO184NB4F25	116
IO184PB4F25	117
IO190NB4F25	112
IO190PB4F25	113
IO192NB4F25	110
IO192PB4F25	111
IO212NB4F27/CLKEN	104
IO212PB4F27/CLKEP	105
IO213NB4F27/CLKFN	100
IO213PB4F27/CLKFP	101
Bank 5	
IO214NB5F30/CLKGN	92
IO214PB5F30/CLKGP	93
IO215NB5F30/CLKHN	88
IO215PB5F30/CLKHP	89
IO236NB5F32	82
IO236PB5F32	83
IO238NB5F32	80
IO238PB5F32	81
IO240NB5F32	76
IO240PB5F32	77
IO242NB5F32	74
IO242PB5F32	75
IO243NB5F32	70
IO243PB5F32	71
IO244NB5F32	68
IO244PB5F32	69
Bank 6	
IO257PB6F36	60
IO258NB6F36	58
IO258PB6F36	59
IO279NB6F38	56
IO279PB6F38	57

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO280NB6F38	52
IO280PB6F38	53
IO281NB6F38	50
IO281PB6F38	51
IO282NB6F38	46
IO282PB6F38	47
IO284NB6F38	44
IO284PB6F38	45
IO285NB6F38	40
IO285PB6F38	41
IO286NB6F38	38
IO286PB6F38	39
IO287NB6F38	34
IO287PB6F38	35
Bank 7	
IO310NB7F43	30
IO310PB7F43	31
IO311NB7F43	26
IO311PB7F43	27
IO312NB7F43	24
IO312PB7F43	25
IO315NB7F43	20
IO315PB7F43	21
IO316NB7F43	18
IO316PB7F43	19
IO317NB7F43	14
IO317PB7F43	15
IO318NB7F43	12
IO318PB7F43	13
IO320NB7F43	8
IO320PB7F43	9
IO341NB7F45	6
IO341PB7F45	7
Dedicated I/O	
GND	5
GND	11
GND	17

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
GND	23
GND	29
GND	33
GND	37
GND	43
GND	49
GND	55
GND	62
GND	64
GND	65
GND	73
GND	79
GND	85
GND	91
GND	97
GND	103
GND	109
GND	115
GND	121
GND	128
GND	129
GND	132
GND	139
GND	145
GND	151
GND	157
GND	161
GND	165
GND	171
GND	177
GND	183
GND	190
GND	192
GND	193
GND	201
GND	207
GND	213

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
GND	219
GND	225
GND	231
GND	239
GND	245
GND	256
PRA	227
PRB	226
PRC	99
PRD	98
TCK	253
TDI	252
TDO	250
TMS	254
TRST	255
V_{CCA}	4
V_{CCA}	22
V_{CCA}	42
V_{CCA}	61
V_{CCA}	63
V_{CCA}	84
V_{CCA}	108
V_{CCA}	127
V_{CCA}	131
V_{CCA}	150
V_{CCA}	170
V_{CCA}	189
V_{CCA}	191
V_{CCA}	212
V_{CCA}	238
V_{CCDA}	32
V_{CCDA}	66
V_{CCDA}	67
V_{CCDA}	86
V_{CCDA}	87
V_{CCDA}	94
V_{CCDA}	95

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
V_{CCDA}	96
V_{CCDA}	106
V_{CCDA}	107
V_{CCDA}	126
V_{CCDA}	130
V_{CCDA}	160
V_{CCDA}	194
V_{CCDA}	196
V_{CCDA}	214
V_{CCDA}	215
V_{CCDA}	222
V_{CCDA}	223
V_{CCDA}	224
V_{CCDA}	236
V_{CCDA}	237
V_{CCDA}	251
$V_{CCI}B0$	230
$V_{CCI}B0$	244
$V_{CCI}B1$	200
$V_{CCI}B1$	206
$V_{CCI}B1$	218
$V_{CCI}B2$	164
$V_{CCI}B2$	176
$V_{CCI}B2$	182
$V_{CCI}B3$	138
$V_{CCI}B3$	144
$V_{CCI}B3$	156
$V_{CCI}B4$	102
$V_{CCI}B4$	114
$V_{CCI}B4$	120
$V_{CCI}B5$	72
$V_{CCI}B5$	78
$V_{CCI}B5$	90
$V_{CCI}B6$	36
$V_{CCI}B6$	48
$V_{CCI}B6$	54
$V_{CCI}B7$	10

256-Pin CQFP	
RTAX2000S Function	**Pin Number**
$V_{CCI}B7$	16
$V_{CCI}B7$	28
V_{PUMP}	195

352-Pin CQFP

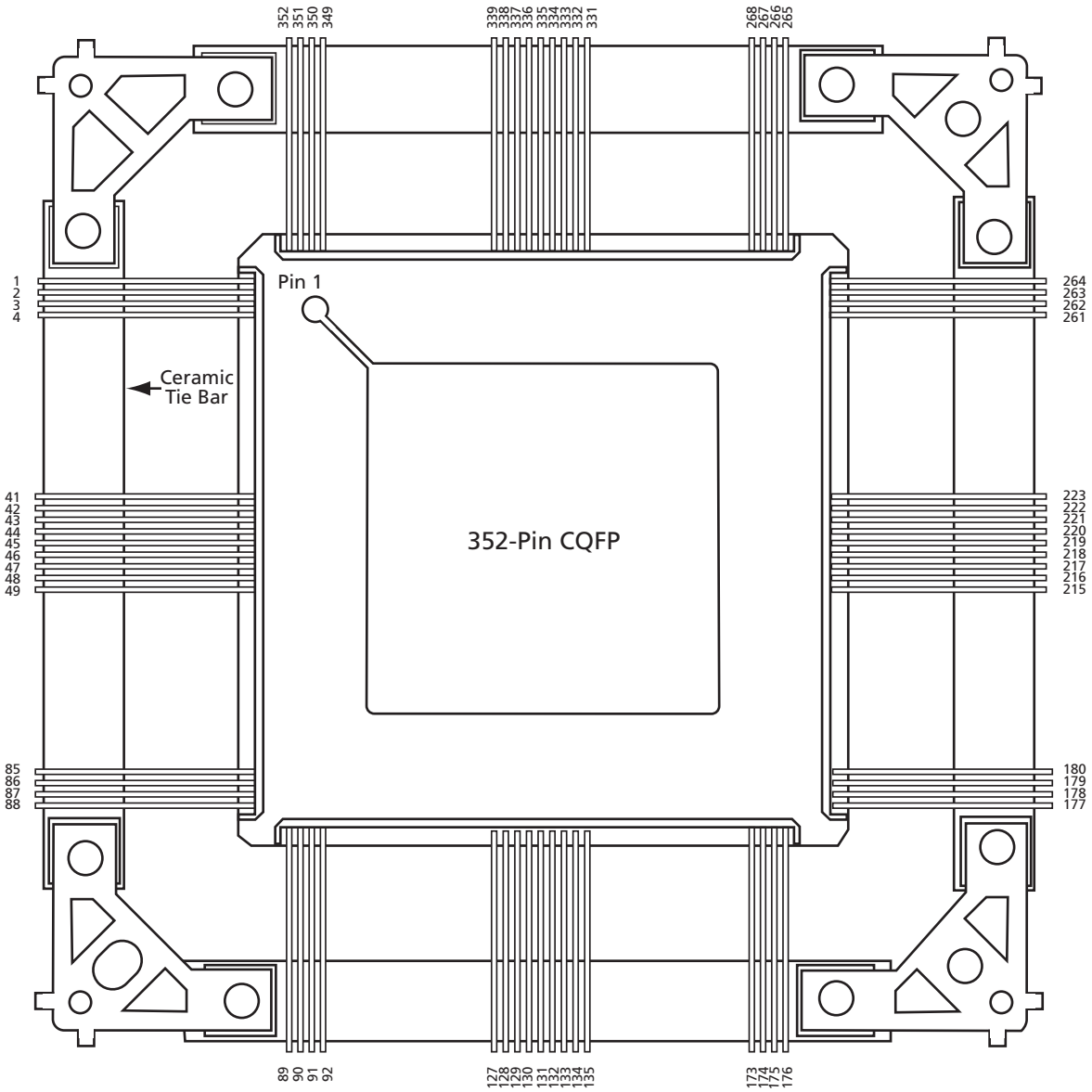


Figure 3-3 • **352-Pin CQFP**

Note:

The 352-pin CQFP pin assignments for both RTAX1000S and RTAX2000S are compatible except for the following seven pins: 91, 130, 131, 174, 268, 307, and 308. On the RTAX1000S, these pins are no connects (NC), and for RTAX2000S these pins are assigned to V_{CCDA}. Customers are therefore recommend to layout their board targeting the RTAX2000S device, in order to preserve interchangeability between the two devices.

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/rescenter/package/index.html.

352-Pin CQFP	
RTAX250S Function	**Pin Number**
Bank 0	
IO00NB0F0	341
IO00PB0F0	342
IO01NB0F0	343
IO02NB0F0	337
IO02PB0F0	338
IO04NB0F0	335
IO04PB0F0	336
IO06NB0F0	331
IO06PB0F0	332
IO08NB0F0	325
IO08PB0F0	326
IO10NB0F0	323
IO10PB0F0	324
IO12NB0F0/HCLKAN	319
IO12PB0F0/HCLKAP	320
IO13NB0F0/HCLKBN	313
IO13PB0F0/HCLKBP	314
Bank 1	
IO14NB1F1/HCLKCN	305
IO14PB1F1/HCLKCP	306
IO15NB1F1/HCLKDN	299
IO15PB1F1/HCLKDP	300
IO16NB1F1	289
IO16PB1F1	290
IO17NB1F1	295
IO17PB1F1	296
IO18NB1F1	287
IO18PB1F1	288
IO20NB1F1	283
IO20PB1F1	284
IO22NB1F1	277
IO22PB1F1	278
IO23NB1F1	281
IO23PB1F1	282
IO24NB1F1	275
IO24PB1F1	276

352-Pin CQFP	
RTAX250S Function	**Pin Number**
IO25NB1F1	271
IO25PB1F1	272
IO27NB1F1	269
IO27PB1F1	270
Bank 2	
IO29NB2F2	261
IO29PB2F2	262
IO30NB2F2	259
IO30PB2F2	260
IO31NB2F2	255
IO31PB2F2	256
IO33NB2F2	249
IO33PB2F2	250
IO34NB2F2	253
IO34PB2F2	254
IO35NB2F2	247
IO35PB2F2	248
IO36NB2F2	243
IO36PB2F2	244
IO37NB2F2	241
IO37PB2F2	242
IO38NB2F2	237
IO38PB2F2	238
IO39NB2F2	235
IO39PB2F2	236
IO41NB2F2	231
IO41PB2F2	232
IO42NB2F2	229
IO42PB2F2	230
IO43NB2F2	225
IO43PB2F2	226
IO44NB2F2	223
IO44PB2F2	224
Bank 3	
IO45NB3F3	217
IO45PB3F3	218
IO46NB3F3	219

352-Pin CQFP	
RTAX250S Function	**Pin Number**
IO46PB3F3	220
IO47NB3F3	213
IO47PB3F3	214
IO48NB3F3	211
IO48PB3F3	212
IO49NB3F3	207
IO49PB3F3	208
IO51NB3F3	205
IO51PB3F3	206
IO52NB3F3	201
IO52PB3F3	202
IO53NB3F3	199
IO53PB3F3	200
IO54NB3F3	195
IO54PB3F3	196
IO55NB3F3	193
IO55PB3F3	194
IO56NB3F3	187
IO56PB3F3	188
IO57NB3F3	189
IO57PB3F3	190
IO59NB3F3	183
IO59PB3F3	184
IO60NB3F3	181
IO60PB3F3	182
IO61NB3F3	179
IO61PB3F3	180
Bank 4	
IO62NB4F4	172
IO62PB4F4	173
IO64NB4F4	166
IO64PB4F4	167
IO65NB4F4	170
IO65PB4F4	171
IO66NB4F4	164
IO66PB4F4	165
IO67NB4F4	160

352-Pin CQFP	
RTAX250S Function	**Pin Number**
IO67PB4F4	161
IO68NB4F4	158
IO68PB4F4	159
IO70NB4F4	154
IO70PB4F4	155
IO72NB4F4	152
IO72PB4F4	153
IO73NB4F4	146
IO73PB4F4	147
IO74NB4F4/CLKEN	142
IO74PB4F4/CLKEP	143
IO75NB4F4/CLKFN	136
IO75PB4F4/CLKFP	137
Bank 5	
IO76NB5F5/CLKGN	128
IO76PB5F5/CLKGP	129
IO77NB5F5/CLKHN	122
IO77PB5F5/CLKHP	123
IO78NB5F5	112
IO78PB5F5	113
IO79NB5F5	118
IO79PB5F5	119
IO80NB5F5	110
IO80PB5F5	111
IO82NB5F5	106
IO82PB5F5	107
IO84NB5F5	100
IO84PB5F5	101
IO85NB5F5	104
IO85PB5F5	105
IO86NB5F5	98
IO86PB5F5	99
IO87NB5F5	94
IO87PB5F5	95
IO89NB5F5	92
IO89PB5F5	93
Bank 6	

352-Pin CQFP	
RTAX250S Function	**Pin Number**
IO90PB6F6	86
IO91NB6F6	84
IO91PB6F6	85
IO92NB6F6	78
IO92PB6F6	79
IO93NB6F6	82
IO93PB6F6	83
IO95NB6F6	76
IO95PB6F6	77
IO96NB6F6	72
IO96PB6F6	73
IO97NB6F6	70
IO97PB6F6	71
IO98NB6F6	66
IO98PB6F6	67
IO99NB6F6	64
IO99PB6F6	65
IO100NB6F6	60
IO100PB6F6	61
IO101NB6F6	58
IO101PB6F6	59
IO103NB6F6	54
IO103PB6F6	55
IO104NB6F6	52
IO104PB6F6	53
IO105NB6F6	48
IO105PB6F6	49
IO106NB6F6	46
IO106PB6F6	47
Bank 7	
IO107NB7F7	40
IO107PB7F7	41
IO108NB7F7	42
IO108PB7F7	43
IO109NB7F7	36
IO109PB7F7	37
IO110NB7F7	34

352-Pin CQFP	
RTAX250S Function	**Pin Number**
IO110PB7F7	35
IO111NB7F7	30
IO111PB7F7	31
IO113NB7F7	28
IO113PB7F7	29
IO114NB7F7	24
IO114PB7F7	25
IO115NB7F7	22
IO115PB7F7	23
IO116NB7F7	18
IO116PB7F7	19
IO117NB7F7	16
IO117PB7F7	17
IO118NB7F7	12
IO118PB7F7	13
IO119NB7F7	10
IO119PB7F7	11
IO121NB7F7	6
IO121PB7F7	7
IO123NB7F7	4
IO123PB7F7	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX250S Function	**Pin Number**
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX250S Function	**Pin Number**
GND	334
GND	340
GND	345
GND	352
NC	91
NC	117
NC	124
NC	125
NC	126
NC	127
NC	130
NC	131
NC	138
NC	139
NC	140
NC	141
NC	148
NC	174
NC	268
NC	294
NC	301
NC	302
NC	303
NC	304
NC	307
NC	308
NC	315
NC	316
NC	317
NC	318
NC	327
NC	328
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349

352-Pin CQFP	
RTAX250S Function	**Pin Number**
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	116
V_{CCDA}	132
V_{CCDA}	149
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	293
V_{CCDA}	309
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX250S Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
Bank 0	
IO02NB0F0	341
IO02PB0F0	342
IO03PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO08NB0F0	331
IO08PB0F0	332
IO09NB0F0	335
IO09PB0F0	336
IO24NB0F2	325
IO24PB0F2	326
IO25NB0F2	323
IO25PB0F2	324
IO30NB0F2/HCLKAN	319
IO30PB0F2/HCLKAP	320
IO31NB0F2/HCLKBN	313
IO31PB0F2/HCLKBP	314
Bank 1	
IO32NB1F3/HCLKCN	305
IO32PB1F3/HCLKCP	306
IO33NB1F3/HCLKDN	299
IO33PB1F3/HCLKDP	300
IO38NB1F3	295
IO38PB1F3	296
IO54NB1F5	287
IO54PB1F5	288
IO55NB1F5	289
IO55PB1F5	290
IO56NB1F5	281
IO56PB1F5	282
IO57NB1F5	283
IO57PB1F5	284
IO59NB1F5	277
IO59PB1F5	278
IO60NB1F5	275
IO60PB1F5	276

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
IO61NB1F5	271
IO61PB1F5	272
IO63NB1F5	269
IO63PB1F5	270
Bank 2	
IO64NB2F6	259
IO64PB2F6	260
IO67NB2F6	261
IO67PB2F6	262
IO68NB2F6	255
IO68PB2F6	256
IO69NB2F6	253
IO69PB2F6	254
IO74NB2F7	249
IO74PB2F7	250
IO75NB2F7	247
IO75PB2F7	248
IO76NB2F7	243
IO76PB2F7	244
IO77NB2F7	241
IO77PB2F7	242
IO78NB2F7	237
IO78PB2F7	238
IO79NB2F7	235
IO79PB2F7	236
IO82NB2F7	231
IO82PB2F7	232
IO83NB2F7	229
IO83PB2F7	230
IO94NB2F8	225
IO94PB2F8	226
IO95NB2F8	223
IO95PB2F8	224
Bank 3	
IO96NB3F9	217
IO96PB3F9	218
IO97NB3F9	219

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
IO97PB3F9	220
IO99NB3F9	213
IO99PB3F9	214
IO108NB3F10	211
IO108PB3F10	212
IO109NB3F10	207
IO109PB3F10	208
IO111NB3F10	205
IO111PB3F10	206
IO112NB3F10	199
IO112PB3F10	200
IO113NB3F10	201
IO113PB3F10	202
IO115NB3F10	195
IO115PB3F10	196
IO116NB3F10	193
IO116PB3F10	194
IO117NB3F10	189
IO117PB3F10	190
IO124NB3F11	183
IO124PB3F11	184
IO125NB3F11	187
IO125PB3F11	188
IO127NB3F11	181
IO127PB3F11	182
IO128NB3F11	179
IO128PB3F11	180
Bank 4	
IO130NB4F12	172
IO130PB4F12	173
IO131NB4F12	170
IO131PB4F12	171
IO132NB4F12	166
IO132PB4F12	167
IO133NB4F12	164
IO133PB4F12	165
IO134NB4F12	160

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
IO134PB4F12	161
IO136NB4F12	158
IO136PB4F12	159
IO137NB4F12	154
IO137PB4F12	155
IO138NB4F12	152
IO138PB4F12	153
IO153NB4F14	146
IO153PB4F14	147
IO159NB4F14/CLKEN	142
IO159PB4F14/CLKEP	143
IO160NB4F14/CLKFN	136
IO160PB4F14/CLKFP	137
Bank 5	
IO161NB5F15/CLKGN	128
IO161PB5F15/CLKGP	129
IO162NB5F15/CLKHN	122
IO162PB5F15/CLKHP	123
IO167NB5F15	118
IO167PB5F15	119
IO183NB5F17	110
IO183PB5F17	111
IO184NB5F17	112
IO184PB5F17	113
IO185NB5F17	104
IO185PB5F17	105
IO186NB5F17	106
IO186PB5F17	107
IO187NB5F17	98
IO187PB5F17	99
IO188NB5F17	100
IO188PB5F17	101
IO190NB5F17	94
IO190PB5F17	95
IO192NB5F17	92
IO192PB5F17	93
Bank 6	

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
IO193PB6F18	86
IO194NB6F18	84
IO194PB6F18	85
IO196NB6F18	78
IO196PB6F18	79
IO197NB6F18	82
IO197PB6F18	83
IO198NB6F18	76
IO198PB6F18	77
IO203NB6F19	72
IO203PB6F19	73
IO204NB6F19	70
IO204PB6F19	71
IO205NB6F19	66
IO205PB6F19	67
IO206NB6F19	64
IO206PB6F19	65
IO207NB6F19	60
IO207PB6F19	61
IO208NB6F19	58
IO208PB6F19	59
IO211NB6F19	54
IO211PB6F19	55
IO212NB6F19	52
IO212PB6F19	53
IO223NB6F20	48
IO223PB6F20	49
IO224NB6F20	46
IO224PB6F20	47
Bank 7	
IO225NB7F21	40
IO225PB7F21	41
IO226NB7F21	42
IO226PB7F21	43
IO237NB7F22	34
IO237PB7F22	35
IO238NB7F22	36

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
IO238PB7F22	37
IO240NB7F22	30
IO240PB7F22	31
IO241NB7F22	28
IO241PB7F22	29
IO242NB7F22	24
IO242PB7F22	25
IO244NB7F22	22
IO244PB7F22	23
IO245NB7F22	18
IO245PB7F22	19
IO246NB7F22	16
IO246PB7F22	17
IO249NB7F23	12
IO249PB7F23	13
IO250NB7F23	10
IO250PB7F23	11
IO256NB7F23	4
IO256PB7F23	5
IO257NB7F23	6
IO257PB7F23	7
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
GND	334
GND	340
GND	345
GND	352
NC	91
NC	124
NC	125
NC	126
NC	127
NC	130
NC	131
NC	138
NC	139
NC	140
NC	141
NC	174
NC	268
NC	301
NC	302
NC	303
NC	304
NC	307
NC	308
NC	315
NC	316
NC	317
NC	318
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	116
V_{CCDA}	117
V_{CCDA}	132
V_{CCDA}	148
V_{CCDA}	149
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	293
V_{CCDA}	294
V_{CCDA}	309
V_{CCDA}	327
V_{CCDA}	328
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX1000S Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
Bank 0	
IO01NB0F0	341
IO01PB0F0	342
IO02PB0F0	343
IO04NB0F0	337
IO04PB0F0	338
IO05NB0F0	335
IO05PB0F0	336
IO08NB0F0	331
IO08PB0F0	332
IO37NB0F3	325
IO37PB0F3	326
IO38NB0F3	323
IO38PB0F3	324
IO41NB0F3/HCLKAN	319
IO41PB0F3/HCLKAP	320
IO42NB0F3/HCLKBN	313
IO42PB0F3/HCLKBP	314
Bank 1	
IO43NB1F4/HCLKCN	305
IO43PB1F4/HCLKCP	306
IO44NB1F4/HCLKDN	299
IO44PB1F4/HCLKDP	300
IO48NB1F4	295
IO48PB1F4	296
IO65NB1F6	283
IO65PB1F6	284
IO66NB1F6	289
IO66PB1F6	290
IO68NB1F6	287
IO68PB1F6	288
IO69NB1F6	275
IO69PB1F6	276
IO70NB1F6	281
IO70PB1F6	282
IO71NB1F6	277
IO71PB1F6	278

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO73NB1F6	269
IO73PB1F6	270
IO74NB1F6	271
IO74PB1F6	272
Bank 2	
IO87NB2F8	261
IO87PB2F8	262
IO88NB2F8	255
IO88PB2F8	256
IO89NB2F8	259
IO89PB2F8	260
IO91NB2F8	253
IO91PB2F8	254
IO99NB2F9	249
IO99PB2F9	250
IO100NB2F9	247
IO100PB2F9	248
IO107NB2F10	243
IO107PB2F10	244
IO110NB2F10	241
IO110PB2F10	242
IO111NB2F10	237
IO111PB2F10	238
IO112NB2F10	235
IO112PB2F10	236
IO113NB2F10	231
IO113PB2F10	232
IO114NB2F10	229
IO114PB2F10	230
IO115NB2F10	225
IO115PB2F10	226
IO117NB2F10	223
IO117PB2F10	224
Bank 3	
IO129NB3F12	219
IO129PB3F12	220
IO132NB3F12	217

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO132PB3F12	218
IO137NB3F12	213
IO137PB3F12	214
IO139NB3F13	211
IO139PB3F13	212
IO141NB3F13	205
IO141PB3F13	206
IO142NB3F13	207
IO142PB3F13	208
IO145NB3F13	199
IO145PB3F13	200
IO146NB3F13	201
IO146PB3F13	202
IO147NB3F13	193
IO147PB3F13	194
IO148NB3F13	195
IO148PB3F13	196
IO149NB3F13	189
IO149PB3F13	190
IO161NB3F15	183
IO161PB3F15	184
IO163NB3F15	187
IO163PB3F15	188
IO165NB3F15	181
IO165PB3F15	182
IO167NB3F15	179
IO167PB3F15	180
Bank 4	
IO181NB4F17	172
IO181PB4F17	173
IO182NB4F17	170
IO182PB4F17	171
IO183NB4F17	166
IO183PB4F17	167
IO184NB4F17	164
IO184PB4F17	165
IO185NB4F17	160

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO185PB4F17	161
IO190NB4F17	158
IO190PB4F17	159
IO191NB4F17	154
IO191PB4F17	155
IO192NB4F17	152
IO192PB4F17	153
IO207NB4F19	146
IO207PB4F19	147
IO212NB4F19/CLKEN	142
IO212PB4F19/CLKEP	143
IO213NB4F19/CLKFN	136
IO213PB4F19/CLKFP	137
Bank 5	
IO214NB5F20/CLKGN	128
IO214PB5F20/CLKGP	129
IO215NB5F20/CLKHN	122
IO215PB5F20/CLKHP	123
IO217NB5F20	118
IO217PB5F20	119
IO236NB5F22	110
IO236PB5F22	111
IO237NB5F22	112
IO237PB5F22	113
IO238NB5F22	104
IO238PB5F22	105
IO239NB5F22	106
IO239PB5F22	107
IO240NB5F22	100
IO240PB5F22	101
IO242NB5F22	94
IO242PB5F22	95
IO243NB5F22	98
IO243PB5F22	99
IO244NB5F22	92
IO244PB5F22	93
Bank 6	

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO257PB6F24	86
IO258NB6F24	84
IO258PB6F24	85
IO261NB6F24	82
IO261PB6F24	83
IO262NB6F24	78
IO262PB6F24	79
IO265NB6F24	76
IO265PB6F24	77
IO279NB6F26	72
IO279PB6F26	73
IO280NB6F26	70
IO280PB6F26	71
IO281NB6F26	66
IO281PB6F26	67
IO282NB6F26	64
IO282PB6F26	65
IO284NB6F26	60
IO284PB6F26	61
IO285NB6F26	58
IO285PB6F26	59
IO286NB6F26	54
IO286PB6F26	55
IO287NB6F26	52
IO287PB6F26	53
IO294NB6F27	48
IO294PB6F27	49
IO296NB6F27	46
IO296PB6F27	47
Bank 7	
IO300NB7F28	42
IO300PB7F28	43
IO303NB7F28	40
IO303PB7F28	41
IO310NB7F29	34
IO310PB7F29	35
IO311NB7F29	36

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
IO311PB7F29	37
IO312NB7F29	28
IO312PB7F29	29
IO315NB7F29	30
IO315PB7F29	31
IO316NB7F29	22
IO316PB7F29	23
IO317NB7F29	24
IO317PB7F29	25
IO318NB7F29	18
IO318PB7F29	19
IO320NB7F29	16
IO320PB7F29	17
IO334NB7F31	10
IO334PB7F31	11
IO335NB7F31	12
IO335PB7F31	13
IO338NB7F31	6
IO338PB7F31	7
IO341NB7F31	4
IO341PB7F31	5
Dedicated I/O	
GND	1
GND	9
GND	15
GND	21
GND	27
GND	33
GND	39
GND	45
GND	51
GND	57
GND	63
GND	69
GND	75
GND	81
GND	88

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
GND	89
GND	97
GND	103
GND	109
GND	115
GND	121
GND	133
GND	145
GND	151
GND	157
GND	163
GND	169
GND	176
GND	177
GND	186
GND	192
GND	198
GND	204
GND	210
GND	216
GND	222
GND	228
GND	234
GND	240
GND	246
GND	252
GND	258
GND	264
GND	265
GND	274
GND	280
GND	286
GND	292
GND	298
GND	310
GND	322
GND	330

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
GND	334
GND	340
GND	345
GND	352
NC	124
NC	125
NC	126
NC	127
NC	138
NC	139
NC	140
NC	141
NC	301
NC	302
NC	303
NC	304
NC	315
NC	316
NC	317
NC	318
PRA	312
PRB	311
PRC	135
PRD	134
TCK	349
TDI	348
TDO	347
TMS	350
TRST	351
V_{CCA}	3
V_{CCA}	14
V_{CCA}	32
V_{CCA}	56
V_{CCA}	74
V_{CCA}	87
V_{CCA}	102
V_{CCA}	114

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
V_{CCA}	150
V_{CCA}	162
V_{CCA}	175
V_{CCA}	191
V_{CCA}	209
V_{CCA}	233
V_{CCA}	251
V_{CCA}	263
V_{CCA}	279
V_{CCA}	291
V_{CCA}	329
V_{CCA}	339
V_{CCDA}	2
V_{CCDA}	44
V_{CCDA}	90
V_{CCDA}	91
V_{CCDA}	116
V_{CCDA}	117
V_{CCDA}	130
V_{CCDA}	131
V_{CCDA}	132
V_{CCDA}	148
V_{CCDA}	149
V_{CCDA}	174
V_{CCDA}	178
V_{CCDA}	221
V_{CCDA}	266
V_{CCDA}	268
V_{CCDA}	293
V_{CCDA}	294
V_{CCDA}	307
V_{CCDA}	308
V_{CCDA}	309
V_{CCDA}	327
V_{CCDA}	328
V_{CCDA}	346
$V_{CCI}B0$	321

352-Pin CQFP	
RTAX2000S Function	**Pin Number**
$V_{CCI}B0$	333
$V_{CCI}B0$	344
$V_{CCI}B1$	273
$V_{CCI}B1$	285
$V_{CCI}B1$	297
$V_{CCI}B2$	227
$V_{CCI}B2$	239
$V_{CCI}B2$	245
$V_{CCI}B2$	257
$V_{CCI}B3$	185
$V_{CCI}B3$	197
$V_{CCI}B3$	203
$V_{CCI}B3$	215
$V_{CCI}B4$	144
$V_{CCI}B4$	156
$V_{CCI}B4$	168
$V_{CCI}B5$	96
$V_{CCI}B5$	108
$V_{CCI}B5$	120
$V_{CCI}B6$	50
$V_{CCI}B6$	62
$V_{CCI}B6$	68
$V_{CCI}B6$	80
$V_{CCI}B7$	8
$V_{CCI}B7$	20
$V_{CCI}B7$	26
$V_{CCI}B7$	38
V_{PUMP}	267

624-Pin CCGA/LGA

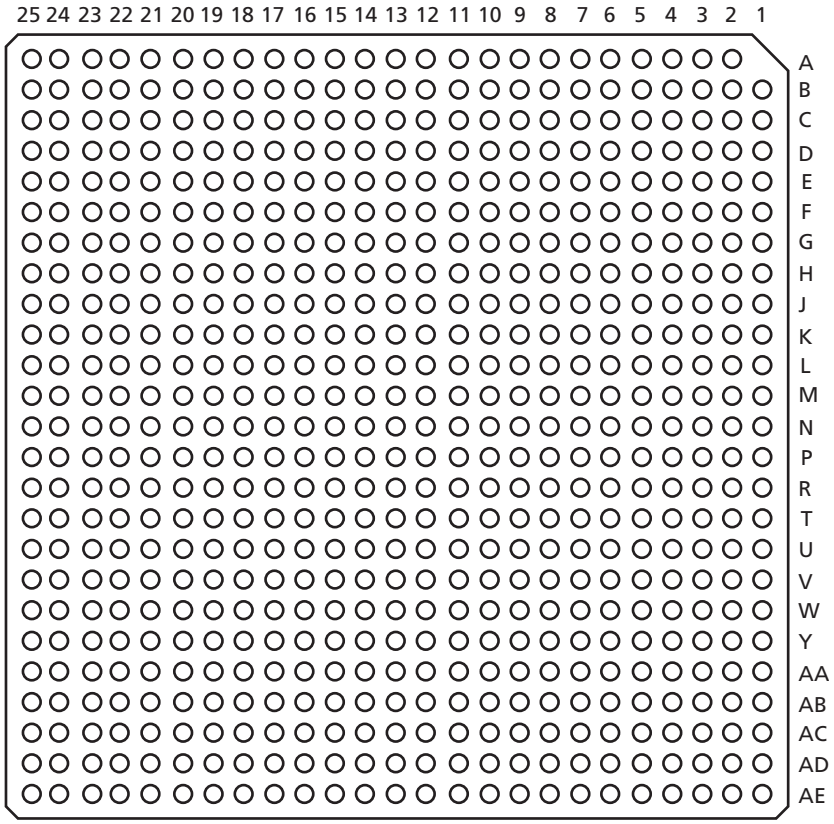


Figure 3-4 • **624-Pin CCGA/LGA (Bottom View)**

Note:

The 624-pin CCGA/LGA pin assignments for both RTAX1000S and RTAX2000S are compatible except for the following seven pins: A14, AA20, AB13, AD4, AE12, F21, G10. On the RTAX1000S, these pins are no connects (NC), and for RTAX2000S these pins are assigned to V_{CCDA}. Customers are therefore recommend to layout their board targeting the RTAX2000S device, in order to preserve interchangeability between the two devices.

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/rescenter/package/index.html.

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
Bank 0	
IO00NB0F0	F8
IO00PB0F0	F7
IO02NB0F0	G7
IO02PB0F0	G6
IO04NB0F0	E9
IO04PB0F0	D8
IO06NB0F0	G9
IO06PB0F0	G8
IO07PB0F0	B6
IO08NB0F0	F10
IO08PB0F0	F9
IO09PB0F0	C7
IO10NB0F0	H8
IO10PB0F0	H7
IO11NB0F0	D10
IO11PB0F0	D9
IO12NB0F1	B5
IO12PB0F1	B4
IO13NB0F1	A7
IO13PB0F1	A6
IO14NB0F1	C9
IO14PB0F1	C8
IO15PB0F1	B7
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	A9
IO17PB0F1	B9
IO18NB0F1	D12
IO18PB0F1	D11
IO20NB0F1	B11
IO20PB0F1	B10
IO21NB0F1	A11
IO21PB0F1	A10
IO22NB0F2	H10
IO22PB0F2	H9

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO23NB0F2	E11
IO23PB0F2	F11
IO24NB0F2	D7
IO24PB0F2	E7
IO25PB0F2	B12
IO26NB0F2	H11
IO26PB0F2	G11
IO27NB0F2	C11
IO27PB0F2	B8
IO28NB0F2	J13
IO28PB0F2	K13
IO29NB0F2	J8
IO29PB0F2	J7
IO30NB0F2/HCLKAN	G13
IO30PB0F2/HCLKAP	G12
IO31NB0F2/HCLKBN	C13
IO31PB0F2/HCLKBP	C12
Bank 1	
IO32NB1F3/HCLKCN	G15
IO32PB1F3/HCLKCP	G14
IO33NB1F3/HCLKDN	B14
IO33PB1F3/HCLKDP	B13
IO34NB1F3	G16
IO34PB1F3	H16
IO35NB1F3	C17
IO35PB1F3	B18
IO36NB1F3	H18
IO36PB1F3	H15
IO37NB1F3	H13
IO38NB1F3	E15
IO38PB1F3	F15
IO39NB1F3	D14
IO39PB1F3	C14
IO40NB1F3	D16
IO40PB1F3	D15
IO41NB1F4	F16

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO42NB1F4	G21
IO42PB1F4	G20
IO43NB1F4	A16
IO43PB1F4	A15
IO44NB1F4	A20
IO44PB1F4	A19
IO45NB1F4	B17
IO45PB1F4	B16
IO46NB1F4	G17
IO46PB1F4	H17
IO47NB1F4	A17
IO48NB1F4	C19
IO48PB1F4	C18
IO49NB1F4	B20
IO49PB1F4	B19
IO50NB1F4	H20
IO50PB1F4	H19
IO51NB1F4	A22
IO51PB1F4	A21
IO52NB1F4	C21
IO52PB1F4	C20
IO53NB1F4	B22
IO53PB1F4	B21
IO54NB1F5	J18
IO54PB1F5	J19
IO55NB1F5	D18
IO55PB1F5	D17
IO56NB1F5	F20
IO56PB1F5	F19
IO58NB1F5	E17
IO58PB1F5	F17
IO60NB1F5	D20
IO60PB1F5	D19
IO62NB1F5	E18
IO62PB1F5	F18
IO63NB1F5	G19

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO63PB1F5	G18
Bank 2	
IO64NB2F6	M17
IO64PB2F6	G22
IO65NB2F6	J21
IO65PB2F6	J20
IO66NB2F6	L23
IO66PB2F6	K20
IO67NB2F6	F23
IO67PB2F6	E23
IO68NB2F6	L18
IO68PB2F6	K18
IO70NB2F6	E24
IO70PB2F6	D24
IO71NB2F6	H23
IO71PB2F6	G23
IO72NB2F6	L19
IO72PB2F6	K19
IO74NB2F7	J22
IO74PB2F7	H22
IO75NB2F7	N23
IO75PB2F7	M23
IO76NB2F7	N17
IO76PB2F7	N16
IO77NB2F7	L22
IO77PB2F7	K22
IO78NB2F7	M19
IO78PB2F7	M18
IO79NB2F7	N19
IO79PB2F7	N18
IO80NB2F7	L21
IO80PB2F7	L20
IO82NB2F7	P18
IO82PB2F7	P17
IO83NB2F7	N22
IO83PB2F7	M22

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO84NB2F7	M20
IO84PB2F7	M21
IO86NB2F8	E25
IO86PB2F8	D25
IO87NB2F8	L24
IO87PB2F8	K24
IO88NB2F8	G24
IO88PB2F8	F24
IO89NB2F8	J25
IO90NB2F8	G25
IO90PB2F8	F25
IO91NB2F8	L25
IO91PB2F8	K25
IO92NB2F8	J24
IO92PB2F8	H24
IO93PB2F8	J23
IO94NB2F8	N24
IO94PB2F8	M24
IO95NB2F8	N25
IO95PB2F8	M25
Bank 3	
IO96NB3F9	T18
IO96PB3F9	R18
IO97NB3F9	N20
IO97PB3F9	P24
IO98NB3F9	P20
IO98PB3F9	P19
IO99NB3F9	P21
IO100NB3F9	T22
IO100PB3F9	W24
IO101NB3F9	R22
IO101PB3F9	P22
IO102NB3F9	U19
IO102PB3F9	T19
IO104NB3F9	V20
IO104PB3F9	U20

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO105NB3F9	R23
IO105PB3F9	P23
IO106NB3F9	R19
IO106PB3F9	R20
IO107NB3F10	AB24
IO108NB3F10	R25
IO108PB3F10	P25
IO109NB3F10	U25
IO109PB3F10	T25
IO110NB3F10	U24
IO110PB3F10	U23
IO112NB3F10	T24
IO112PB3F10	R24
IO113NB3F10	Y25
IO113PB3F10	W25
IO114NB3F10	V23
IO114PB3F10	V24
IO116NB3F10	AA24
IO116PB3F10	Y24
IO117NB3F10	AB25
IO117PB3F10	AA25
IO118NB3F11	T20
IO118PB3F11	R21
IO120NB3F11	W22
IO120PB3F11	W23
IO122NB3F11	V22
IO122PB3F11	U22
IO124NB3F11	Y23
IO124PB3F11	AA23
IO126NB3F11	V21
IO126PB3F11	U21
IO128NB3F11	Y22
IO128PB3F11	Y21
Bank 4	
IO129NB4F12	W20
IO129PB4F12	Y20

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO131NB4F12	V19
IO131PB4F12	W19
IO133NB4F12	Y18
IO133PB4F12	Y19
IO135NB4F12	W18
IO135PB4F12	V18
IO137NB4F12	Y17
IO137PB4F12	AA17
IO138NB4F12	AB19
IO138PB4F12	AB18
IO139NB4F13	AA19
IO139PB4F13	U18
IO140NB4F13	AC20
IO140PB4F13	AC21
IO141NB4F13	AD17
IO141PB4F13	AD18
IO142NB4F13	AD21
IO142PB4F13	AD22
IO143NB4F13	AB17
IO143PB4F13	AC17
IO144PB4F13	AE22
IO145NB4F13	AE15
IO145PB4F13	AE16
IO146NB4F13	AD19
IO146PB4F13	AD20
IO147NB4F13	AD15
IO147PB4F13	AD16
IO148PB4F13	AE21
IO149NB4F13	AD14
IO149PB4F13	AC14
IO150NB4F13	AE19
IO150PB4F13	AE20
IO151NB4F13	V17
IO151PB4F13	W17
IO152NB4F14	AB16
IO152PB4F14	W16

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO153NB4F14	Y15
IO153PB4F14	Y16
IO155NB4F14	V15
IO155PB4F14	V16
IO156NB4F14	AB14
IO156PB4F14	AB15
IO157NB4F14	AE14
IO157PB4F14	AC18
IO158NB4F14	AC15
IO158PB4F14	AC19
IO159NB4F14/CLKEN	W14
IO159PB4F14/CLKEP	W15
IO160NB4F14/CLKFN	AC13
IO160PB4F14/CLKFP	AD13
Bank 5	
IO161NB5F15/CLKGN	W13
IO161PB5F15/CLKGP	Y13
IO162NB5F15/CLKHN	AC12
IO162PB5F15/CLKHP	AD12
IO163NB5F15	V9
IO163PB5F15	V10
IO164NB5F15	V11
IO164PB5F15	T13
IO165NB5F15	U13
IO165PB5F15	V13
IO167NB5F15	W11
IO167PB5F15	W12
IO168NB5F15	AB6
IO168PB5F15	AA6
IO169NB5F15	V8
IO169PB5F15	V7
IO171NB5F16	W8
IO171PB5F16	W9
IO172NB5F16	AB8
IO172PB5F16	AC8
IO173NB5F16	AA11

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO173PB5F16	Y11
IO174NB5F16	AB10
IO174PB5F16	AB11
IO175NB5F16	AC9
IO175PB5F16	AE9
IO177NB5F16	AA8
IO177PB5F16	Y8
IO178NB5F16	Y6
IO178PB5F16	W6
IO179NB5F16	Y10
IO179PB5F16	W10
IO180NB5F16	Y7
IO180PB5F16	W7
IO181NB5F17	AD9
IO181PB5F17	AD10
IO182NB5F17	AE10
IO182PB5F17	AE11
IO183NB5F17	AD7
IO183PB5F17	AD8
IO184NB5F17	AB9
IO185NB5F17	AE6
IO185PB5F17	AE7
IO186NB5F17	AE4
IO186PB5F17	AE5
IO187NB5F17	AA9
IO187PB5F17	Y9
IO188NB5F17	U8
IO189NB5F17	AD5
IO189PB5F17	AD6
IO191NB5F17	AC5
IO191PB5F17	AC6
IO192NB5F17	AB7
IO192PB5F17	AC7
Bank 6	
IO193NB6F18	U6
IO193PB6F18	U5

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO194NB6F18	Y3
IO194PB6F18	AA3
IO195NB6F18	V6
IO195PB6F18	W4
IO197NB6F18	R5
IO197PB6F18	U3
IO198NB6F18	P6
IO199NB6F18	Y5
IO199PB6F18	W5
IO200NB6F18	V3
IO200PB6F18	W3
IO201NB6F18	T7
IO201PB6F18	U7
IO202NB6F18	V2
IO203NB6F19	W2
IO203PB6F19	Y2
IO204NB6F19	AA1
IO204PB6F19	AB1
IO205NB6F19	R6
IO205PB6F19	T6
IO206NB6F19	W1
IO206PB6F19	Y1
IO207NB6F19	T2
IO207PB6F19	U2
IO208NB6F19	T1
IO208PB6F19	U1
IO209NB6F19	AA2
IO209PB6F19	AB2
IO210NB6F19	P5
IO211NB6F19	M1
IO211PB6F19	N1
IO212NB6F19	P1
IO212PB6F19	R1
IO213NB6F19	R8
IO213PB6F19	T8
IO215NB6F20	U4

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO215PB6F20	V4
IO216NB6F20	P8
IO216PB6F20	R3
IO217NB6F20	P7
IO217PB6F20	R7
IO219NB6F20	R4
IO219PB6F20	T4
IO220NB6F20	P2
IO220PB6F20	R2
IO221NB6F20	N4
IO221PB6F20	P4
IO223NB6F20	M2
IO223PB6F20	N2
IO224NB6F20	N3
IO224PB6F20	P3
Bank 7	
IO225NB7F21	J2
IO225PB7F21	J1
IO226PB7F21	G2
IO227NB7F21	H3
IO227PB7F21	H2
IO229NB7F21	K2
IO229PB7F21	L2
IO230NB7F21	K1
IO230PB7F21	L1
IO231NB7F21	E2
IO231PB7F21	F2
IO232NB7F21	F1
IO232PB7F21	G1
IO233NB7F21	L3
IO233PB7F21	M3
IO234NB7F21	D1
IO234PB7F21	E1
IO235NB7F21	K4
IO235PB7F21	L4
IO236NB7F22	M6

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
IO237NB7F22	N8
IO237PB7F22	N7
IO238NB7F22	M5
IO239NB7F22	L6
IO239PB7F22	L5
IO240NB7F22	M4
IO241NB7F22	L7
IO241PB7F22	M7
IO242NB7F22	J3
IO243NB7F22	M9
IO243PB7F22	M8
IO244NB7F22	P9
IO244PB7F22	N6
IO245NB7F22	K8
IO245PB7F22	L8
IO246NB7F22	F3
IO246PB7F22	E3
IO247NB7F23	K7
IO247PB7F23	K6
IO248NB7F23	D2
IO249NB7F23	G4
IO249PB7F23	G3
IO251NB7F23	N10
IO251PB7F23	N9
IO253NB7F23	H4
IO253PB7F23	J4
IO255NB7F23	J6
IO255PB7F23	J5
IO257NB7F23	H5
IO257PB7F23	H6
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
GND	V1
GND	V25
GND	V5
NC	A14
NC	AA12
NC	AA14
NC	AA20
NC	AB13
NC	AD4
NC	AE12
NC	E12
NC	E14
NC	F12
NC	F14
NC	F21
NC	G10
NC	H12
NC	H14
NC	J12
NC	J14
NC	U12
NC	U14
NC	V12
NC	V14
NC	Y12
NC	Y14
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
V_{CCA}	AB20

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
V_{CCA}	F22
V_{CCA}	F4
V_{CCA}	J17
V_{CCA}	J9
V_{CCA}	K10
V_{CCA}	K11
V_{CCA}	K15
V_{CCA}	K16
V_{CCA}	L10
V_{CCA}	L16
V_{CCA}	R10
V_{CCA}	R16
V_{CCA}	T10
V_{CCA}	T11
V_{CCA}	T15
V_{CCA}	T16
V_{CCA}	U17
V_{CCA}	U9
V_{CCA}	Y4
V_{CCDA}	A12
V_{CCDA}	AA13
V_{CCDA}	AA15
V_{CCDA}	AA7
V_{CCDA}	AC11
V_{CCDA}	AD11
V_{CCDA}	AE17
V_{CCDA}	B15
V_{CCDA}	C15
V_{CCDA}	C6
V_{CCDA}	D13
V_{CCDA}	E13
V_{CCDA}	E19
V_{CCDA}	G5
V_{CCDA}	N21
V_{CCDA}	N5
V_{CCDA}	W21

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
$V_{CCI}B0$	A3
$V_{CCI}B0$	B3
$V_{CCI}B0$	C4
$V_{CCI}B0$	D5
$V_{CCI}B0$	J10
$V_{CCI}B0$	J11
$V_{CCI}B0$	K12
$V_{CCI}B1$	A23
$V_{CCI}B1$	B23
$V_{CCI}B1$	C22
$V_{CCI}B1$	D21
$V_{CCI}B1$	J15
$V_{CCI}B1$	J16
$V_{CCI}B1$	K14
$V_{CCI}B2$	C24
$V_{CCI}B2$	C25
$V_{CCI}B2$	D23
$V_{CCI}B2$	E22
$V_{CCI}B2$	K17
$V_{CCI}B2$	L17
$V_{CCI}B2$	M16
$V_{CCI}B3$	AA22
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AC25
$V_{CCI}B3$	P16
$V_{CCI}B3$	R17
$V_{CCI}B3$	T17
$V_{CCI}B4$	AB21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AE23
$V_{CCI}B4$	T14
$V_{CCI}B4$	U15
$V_{CCI}B4$	U16
$V_{CCI}B5$	AB5

624-Pin CCGA/LGA	
RTAX1000S Function	**Pin Number**
$V_{CCI}B5$	AC4
$V_{CCI}B5$	AD3
$V_{CCI}B5$	AE3
$V_{CCI}B5$	T12
$V_{CCI}B5$	U10
$V_{CCI}B5$	U11
$V_{CCI}B6$	AA4
$V_{CCI}B6$	AB3
$V_{CCI}B6$	AC1
$V_{CCI}B6$	AC2
$V_{CCI}B6$	P10
$V_{CCI}B6$	R9
$V_{CCI}B6$	T9
$V_{CCI}B7$	C1
$V_{CCI}B7$	C2
$V_{CCI}B7$	D3
$V_{CCI}B7$	E4
$V_{CCI}B7$	K9
$V_{CCI}B7$	L9
$V_{CCI}B7$	M10
V_{PUMP}	E20

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
Bank 0	
IO00NB0F0	D7
IO00PB0F0	E7
IO01NB0F0	G7
IO01PB0F0	G6
IO02NB0F0	B5
IO02PB0F0	B4
IO04PB0F0	C7
IO05NB0F0	F8
IO05PB0F0	F7
IO06NB0F0	H8
IO06PB0F0	H7
IO11NB0F0	J8
IO11PB0F0	J7
IO12PB0F1	B6
IO13NB0F1	E9
IO13PB0F1	D8
IO15NB0F1	C9
IO15PB0F1	C8
IO16NB0F1	A5
IO16PB0F1	A4
IO17NB0F1	D10
IO17PB0F1	D9
IO18NB0F1	A7
IO18PB0F1	A6
IO19NB0F1	G9
IO19PB0F1	G8
IO20PB0F1	B7
IO23NB0F2	F10
IO23PB0F2	F9
IO26NB0F2	C11
IO26PB0F2	B8
IO27NB0F2	H10
IO27PB0F2	H9
IO28NB0F2	A9
IO28PB0F2	B9

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO30NB0F2	B11
IO30PB0F2	B10
IO31NB0F2	E11
IO31PB0F2	F11
IO33NB0F2	D12
IO33PB0F2	D11
IO34NB0F3	A11
IO34PB0F3	A10
IO37NB0F3	J13
IO37PB0F3	K13
IO38NB0F3	H11
IO38PB0F3	G11
IO40PB0F3	B12
IO41NB0F3/HCLKAN	G13
IO41PB0F3/HCLKAP	G12
IO42NB0F3/HCLKBN	C13
IO42PB0F3/HCLKBP	C12
Bank 1	
IO43NB1F4/HCLKCN	G15
IO43PB1F4/HCLKCP	G14
IO44NB1F4/HCLKDN	B14
IO44PB1F4/HCLKDP	B13
IO45NB1F4	H13
IO47NB1F4	D14
IO47PB1F4	C14
IO48NB1F4	A16
IO48PB1F4	A15
IO49PB1F4	H15
IO51NB1F4	E15
IO51PB1F4	F15
IO52NB1F4	A17
IO55NB1F5	G16
IO55PB1F5	H16
IO56NB1F5	A20
IO56PB1F5	A19
IO57NB1F5	D16

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO57PB1F5	D15
IO58NB1F5	A22
IO58PB1F5	A21
IO59NB1F5	F16
IO61NB1F5	G17
IO61PB1F5	H17
IO62NB1F5	B17
IO62PB1F5	B16
IO63NB1F5	H18
IO65NB1F6	C17
IO66PB1F6	B18
IO67NB1F6	J18
IO67PB1F6	J19
IO68NB1F6	B20
IO68PB1F6	B19
IO69NB1F6	E17
IO69PB1F6	F17
IO70NB1F6	B22
IO70PB1F6	B21
IO71PB1F6	G18
IO73NB1F6	G19
IO74NB1F6	C19
IO74PB1F6	C18
IO75NB1F6	D18
IO75PB1F6	D17
IO76NB1F7	C21
IO76PB1F7	C20
IO79NB1F7	H20
IO79PB1F7	H19
IO80NB1F7	E18
IO80PB1F7	F18
IO81NB1F7	G21
IO81PB1F7	G20
IO82NB1F7	F20
IO82PB1F7	F19
IO85NB1F7	D20

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO85PB1F7	D19
Bank 2	
IO86NB2F8	F23
IO86PB2F8	E23
IO87NB2F8	H23
IO87PB2F8	G23
IO88NB2F8	E24
IO88PB2F8	D24
IO89NB2F8	M17
IO89PB2F8	G22
IO91NB2F8	J22
IO91PB2F8	H22
IO92NB2F8	L18
IO92PB2F8	K18
IO96NB2F9	G24
IO96PB2F9	F24
IO97NB2F9	J21
IO97PB2F9	J20
IO98PB2F9	J23
IO99NB2F9	L19
IO99PB2F9	K19
IO100NB2F9	E25
IO100PB2F9	D25
IO103PB2F9	K20
IO105NB2F9	M19
IO105PB2F9	M18
IO106NB2F9	J24
IO106PB2F9	H24
IO107NB2F10	L23
IO107PB2F10	N16
IO109NB2F10	L22
IO109PB2F10	K22
IO110NB2F10	G25
IO110PB2F10	F25
IO111NB2F10	L21
IO111PB2F10	L20

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO112NB2F10	L24
IO112PB2F10	K24
IO113NB2F10	N17
IO115NB2F10	M20
IO115PB2F10	M21
IO117NB2F10	N19
IO117PB2F10	N18
IO118NB2F11	J25
IO121NB2F11	N24
IO121PB2F11	M24
IO122NB2F11	L25
IO122PB2F11	K25
IO123NB2F11	N22
IO123PB2F11	M22
IO124NB2F11	N23
IO124PB2F11	M23
IO127NB2F11	P18
IO127PB2F11	P17
IO128NB2F11	N25
IO128PB2F11	M25
Bank 3	
IO129NB3F12	N20
IO130PB3F12	P24
IO131NB3F12	P21
IO133NB3F12	P20
IO133PB3F12	P19
IO138NB3F12	R23
IO138PB3F12	P23
IO139NB3F13	R22
IO139PB3F13	P22
IO141NB3F13	R19
IO142NB3F13	R25
IO142PB3F13	P25
IO143PB3F13	R21
IO145NB3F13	T18
IO145PB3F13	R18

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO146NB3F13	T24
IO146PB3F13	R24
IO147NB3F13	T20
IO147PB3F13	R20
IO148NB3F13	U25
IO148PB3F13	T25
IO149NB3F13	T22
IO153NB3F14	U19
IO153PB3F14	T19
IO154NB3F14	Y25
IO154PB3F14	W25
IO157NB3F14	V20
IO157PB3F14	U20
IO158NB3F14	AB25
IO158PB3F14	AA25
IO160PB3F14	W24
IO161NB3F15	U24
IO161PB3F15	U23
IO162NB3F15	AA24
IO162PB3F15	Y24
IO163NB3F15	V22
IO163PB3F15	U22
IO164NB3F15	V23
IO164PB3F15	V24
IO166NB3F15	AB24
IO167NB3F15	V21
IO167PB3F15	U21
IO168NB3F15	Y23
IO168PB3F15	AA23
IO169NB3F15	W22
IO169PB3F15	W23
IO170NB3F15	Y22
IO170PB3F15	Y21
Bank 4	
IO171NB4F16	AC20
IO171PB4F16	AC21

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO172NB4F16	W20
IO172PB4F16	Y20
IO173NB4F16	AD21
IO173PB4F16	AD22
IO174NB4F16	AA19
IO176NB4F16	Y18
IO176PB4F16	Y19
IO177NB4F16	AB19
IO177PB4F16	AB18
IO182NB4F17	V19
IO182PB4F17	W19
IO183PB4F17	AC19
IO184NB4F17	AB17
IO184PB4F17	AC17
IO185NB4F17	AD19
IO185PB4F17	AD20
IO187PB4F17	AC18
IO188NB4F17	Y17
IO188PB4F17	AA17
IO189PB4F17	AE22
IO191NB4F17	W18
IO191PB4F17	V18
IO192PB4F17	U18
IO195PB4F18	AE21
IO196NB4F18	AB16
IO197NB4F18	AD17
IO197PB4F18	AD18
IO198NB4F18	V17
IO198PB4F18	W17
IO199NB4F18	AE19
IO199PB4F18	AE20
IO200NB4F18	AC15
IO201NB4F18	AD15
IO201PB4F18	AD16
IO202NB4F18	Y15
IO202PB4F18	Y16

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO206NB4F19	AB14
IO206PB4F19	AB15
IO207NB4F19	AE15
IO207PB4F19	AE16
IO208PB4F19	W16
IO209NB4F19	AE14
IO210NB4F19	V15
IO210PB4F19	V16
IO211NB4F19	AD14
IO211PB4F19	AC14
IO212NB4F19/CLKEN	W14
IO212PB4F19/CLKEP	W15
IO213NB4F19/CLKFN	AC13
IO213PB4F19/CLKFP	AD13
Bank 5	
IO214NB5F20/CLKGN	W13
IO214PB5F20/CLKGP	Y13
IO215NB5F20/CLKHN	AC12
IO215PB5F20/CLKHP	AD12
IO216NB5F20	U13
IO216PB5F20	V13
IO217NB5F20	AE10
IO217PB5F20	AE11
IO218NB5F20	W11
IO218PB5F20	W12
IO222NB5F20	AA11
IO222PB5F20	Y11
IO223PB5F21	AE9
IO225NB5F21	AE6
IO225PB5F21	AE7
IO226NB5F21	Y10
IO226PB5F21	W10
IO227PB5F21	T13
IO228NB5F21	AB10
IO228PB5F21	AB11
IO229NB5F21	AD9

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO229PB5F21	AD10
IO230NB5F21	V11
IO233NB5F21	AD7
IO233PB5F21	AD8
IO234NB5F21	V9
IO234PB5F21	V10
IO236NB5F22	AC9
IO238NB5F22	W8
IO238PB5F22	W9
IO239NB5F22	AE4
IO239PB5F22	AE5
IO240NB5F22	AB9
IO242NB5F22	AA9
IO242PB5F22	Y9
IO243NB5F22	AD5
IO243PB5F22	AD6
IO244NB5F22	U8
IO246NB5F23	AB8
IO246PB5F23	AC8
IO247NB5F23	AB7
IO247PB5F23	AC7
IO250NB5F23	AA8
IO250PB5F23	Y8
IO251NB5F23	V8
IO251PB5F23	V7
IO252NB5F23	Y7
IO252PB5F23	W7
IO253NB5F23	AC5
IO253PB5F23	AC6
IO254NB5F23	Y6
IO254PB5F23	W6
IO256NB5F23	AB6
IO256PB5F23	AA6
Bank 6	
IO257NB6F24	Y3
IO257PB6F24	AA3

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO258NB6F24	V3
IO258PB6F24	W3
IO259NB6F24	AA2
IO259PB6F24	AB2
IO260NB6F24	V6
IO260PB6F24	W4
IO262NB6F24	U4
IO262PB6F24	V4
IO263NB6F24	Y5
IO263PB6F24	W5
IO268NB6F25	U6
IO268PB6F25	U5
IO269PB6F25	U3
IO272NB6F25	T2
IO272PB6F25	U2
IO273NB6F25	W2
IO273PB6F25	Y2
IO274NB6F25	R6
IO274PB6F25	T6
IO275NB6F25	T7
IO275PB6F25	U7
IO277NB6F25	V2
IO278NB6F26	R4
IO278PB6F26	T4
IO279PB6F26	R3
IO280NB6F26	R5
IO281NB6F26	AA1
IO281PB6F26	AB1
IO284NB6F26	R8
IO284PB6F26	T8
IO285NB6F26	W1
IO285PB6F26	Y1
IO286NB6F26	P2
IO286PB6F26	R2
IO287NB6F26	T1
IO287PB6F26	U1

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO288NB6F26	P5
IO290NB6F27	P6
IO291NB6F27	P1
IO291PB6F27	R1
IO292NB6F27	P7
IO292PB6F27	R7
IO293NB6F27	M1
IO293PB6F27	N1
IO294NB6F27	P8
IO296NB6F27	N3
IO296PB6F27	P3
IO298NB6F27	N4
IO298PB6F27	P4
IO299NB6F27	M2
IO299PB6F27	N2
Bank 7	
IO300NB7F28	P9
IO300PB7F28	N6
IO302NB7F28	M6
IO304NB7F28	N8
IO304PB7F28	N7
IO308NB7F28	M4
IO309NB7F28	L3
IO309PB7F28	M3
IO310NB7F29	N10
IO310PB7F29	N9
IO311NB7F29	K1
IO311PB7F29	L1
IO313NB7F29	M5
IO316NB7F29	L6
IO316PB7F29	L5
IO317NB7F29	K2
IO317PB7F29	L2
IO318NB7F29	K4
IO318PB7F29	L4
IO320NB7F29	J3

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO321NB7F30	J2
IO321PB7F30	J1
IO323NB7F30	L7
IO323PB7F30	M7
IO324NB7F30	M9
IO324PB7F30	M8
IO327NB7F30	F1
IO327PB7F30	G1
IO328NB7F30	K7
IO328PB7F30	K6
IO329NB7F30	D1
IO329PB7F30	E1
IO331PB7F30	G2
IO332NB7F31	H3
IO332PB7F31	H2
IO333NB7F31	E2
IO333PB7F31	F2
IO334NB7F31	H4
IO334PB7F31	J4
IO335NB7F31	H5
IO335PB7F31	H6
IO337NB7F31	D2
IO338NB7F31	J6
IO338PB7F31	J5
IO339NB7F31	F3
IO339PB7F31	E3
IO340NB7F31	G4
IO340PB7F31	G3
IO341NB7F31	K8
IO341PB7F31	L8
Dedicated I/O	
GND	K5
GND	A18
GND	A2
GND	A24
GND	A25

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
GND	A8
GND	AA10
GND	AA16
GND	AA18
GND	AA21
GND	AA5
GND	AB22
GND	AB4
GND	AC10
GND	AC16
GND	AC23
GND	AC3
GND	AD1
GND	AD2
GND	AD24
GND	AD25
GND	AE1
GND	AE18
GND	AE2
GND	AE24
GND	AE25
GND	AE8
GND	B1
GND	B2
GND	B24
GND	B25
GND	C10
GND	C16
GND	C23
GND	C3
GND	D22
GND	D4
GND	E10
GND	E16
GND	E21
GND	E5

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
GND	E8
GND	H1
GND	H21
GND	H25
GND	K21
GND	K23
GND	K3
GND	L11
GND	L12
GND	L13
GND	L14
GND	L15
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N11
GND	N12
GND	N13
GND	N14
GND	N15
GND	P11
GND	P12
GND	P13
GND	P14
GND	P15
GND	R11
GND	R12
GND	R13
GND	R14
GND	R15
GND	T21
GND	T23
GND	T3
GND	T5

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
GND	V1
GND	V25
GND	V5
NC	AA12
NC	AA14
NC	E12
NC	E14
NC	F12
NC	F14
NC	H12
NC	H14
NC	J12
NC	J14
NC	U12
NC	U14
NC	V12
NC	V14
NC	Y12
NC	Y14
PRA	F13
PRB	A13
PRC	AB12
PRD	AE13
TCK	F5
TDI	C5
TDO	F6
TMS	D6
TRST	E6
V_{CCA}	AB20
V_{CCA}	F22
V_{CCA}	F4
V_{CCA}	J17
V_{CCA}	J9
V_{CCA}	K10
V_{CCA}	K11
V_{CCA}	K15

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
V_{CCA}	K16
V_{CCA}	L10
V_{CCA}	L16
V_{CCA}	R10
V_{CCA}	R16
V_{CCA}	T10
V_{CCA}	T11
V_{CCA}	T15
V_{CCA}	T16
V_{CCA}	U17
V_{CCA}	U9
V_{CCA}	Y4
V_{CCDA}	A12
V_{CCDA}	A14
V_{CCDA}	AA13
V_{CCDA}	AA15
V_{CCDA}	AA20
V_{CCDA}	AA7
V_{CCDA}	AB13
V_{CCDA}	AC11
V_{CCDA}	AD11
V_{CCDA}	AD4
V_{CCDA}	AE12
V_{CCDA}	AE17
V_{CCDA}	B15
V_{CCDA}	C15
V_{CCDA}	C6
V_{CCDA}	D13
V_{CCDA}	E13
V_{CCDA}	E19
V_{CCDA}	F21
V_{CCDA}	G10
V_{CCDA}	G5
V_{CCDA}	N21
V_{CCDA}	N5
V_{CCDA}	W21

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
$V_{CCI}B0$	A3
$V_{CCI}B0$	B3
$V_{CCI}B0$	C4
$V_{CCI}B0$	D5
$V_{CCI}B0$	J10
$V_{CCI}B0$	J11
$V_{CCI}B0$	K12
$V_{CCI}B1$	A23
$V_{CCI}B1$	B23
$V_{CCI}B1$	C22
$V_{CCI}B1$	D21
$V_{CCI}B1$	J15
$V_{CCI}B1$	J16
$V_{CCI}B1$	K14
$V_{CCI}B2$	C24
$V_{CCI}B2$	C25
$V_{CCI}B2$	D23
$V_{CCI}B2$	E22
$V_{CCI}B2$	K17
$V_{CCI}B2$	L17
$V_{CCI}B2$	M16
$V_{CCI}B3$	AA22
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AC25
$V_{CCI}B3$	P16
$V_{CCI}B3$	R17
$V_{CCI}B3$	T17
$V_{CCI}B4$	AB21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AE23
$V_{CCI}B4$	T14
$V_{CCI}B4$	U15
$V_{CCI}B4$	U16
$V_{CCI}B5$	AB5

624-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
$V_{CCI}B5$	AC4
$V_{CCI}B5$	AD3
$V_{CCI}B5$	AE3
$V_{CCI}B5$	T12
$V_{CCI}B5$	U10
$V_{CCI}B5$	U11
$V_{CCI}B6$	AA4
$V_{CCI}B6$	AB3
$V_{CCI}B6$	AC1
$V_{CCI}B6$	AC2
$V_{CCI}B6$	P10
$V_{CCI}B6$	R9
$V_{CCI}B6$	T9
$V_{CCI}B7$	C1
$V_{CCI}B7$	C2
$V_{CCI}B7$	D3
$V_{CCI}B7$	E4
$V_{CCI}B7$	K9
$V_{CCI}B7$	L9
$V_{CCI}B7$	M10
V_{PUMP}	E20

1152-Pin CCGA/LGA

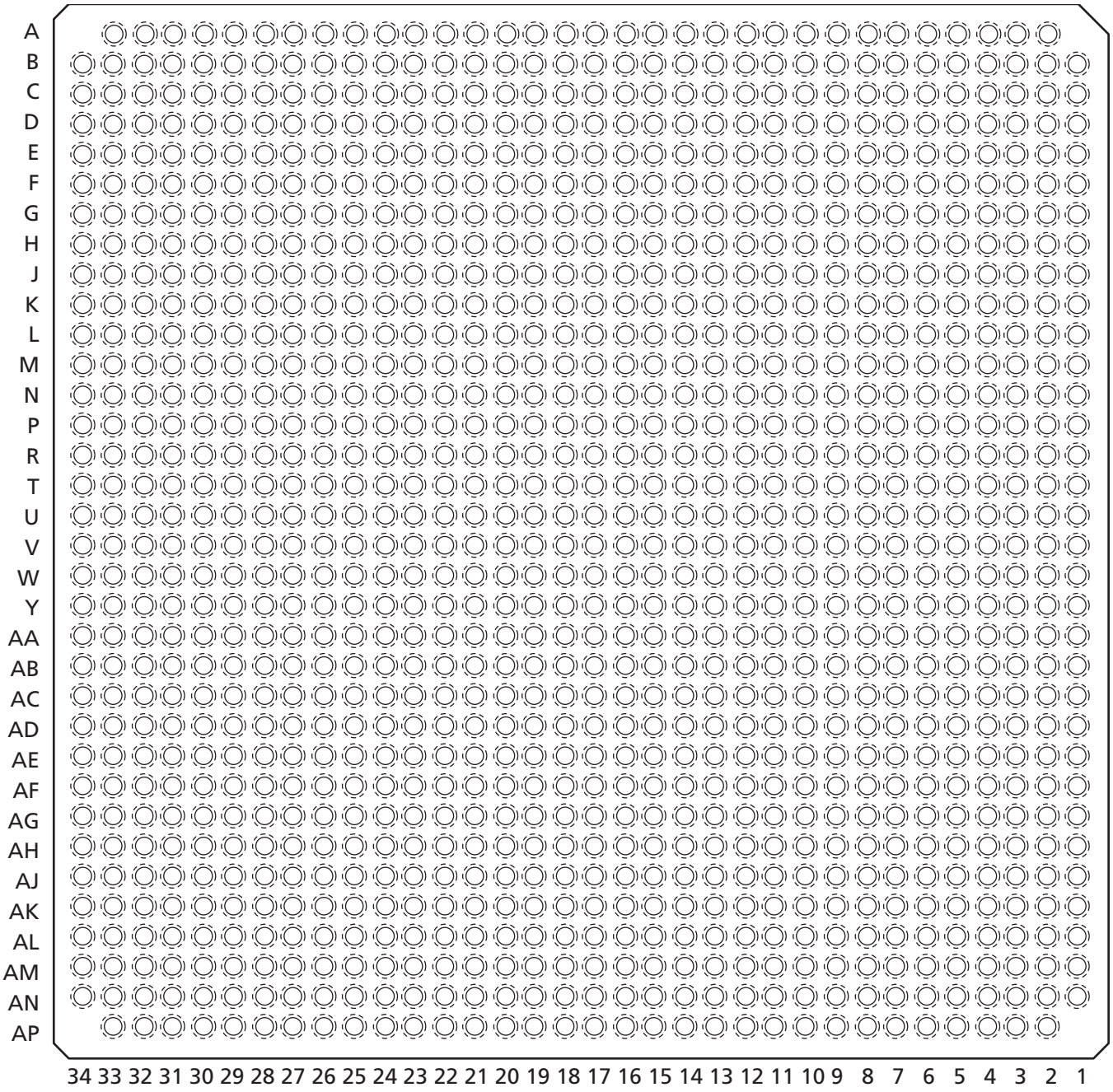


Figure 3-5 • **1152-Pin CCGA/LGA (Bottom View)**

Note

For Package Manufacturing and Environmental information, visit the Resource center at http://www.actel.com/products/rescenter/package/index.html.

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
Bank 0	
IO00NB0F0	D6
IO00PB0F0	C6
IO01NB0F0	H10
IO01PB0F0	H9
IO02NB0F0	F8
IO02PB0F0	G8
IO03NB0F0	A6
IO03PB0F0	B6
IO04NB0F0	C7
IO04PB0F0	D7
IO05NB0F0	K10
IO05PB0F0	J10
IO06NB0F0	F9
IO06PB0F0	G9
IO07NB0F0	F10
IO07PB0F0	G10
IO08NB0F0	E9
IO08PB0F0	E8
IO09NB0F0	J11
IO09PB0F0	K11
IO10NB0F0	C8
IO10PB0F0	D8
IO11NB0F0	K12
IO11PB0F0	J12
IO12NB0F1	G11
IO12PB0F1	H11
IO13NB0F1	G12
IO13PB0F1	H12
IO14NB0F1	A7
IO14PB0F1	B7
IO15NB0F1	H13
IO15PB0F1	J13
IO16NB0F1	C9
IO16PB0F1	D9
IO17NB0F1	F12
IO17PB0F1	F11

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO18NB0F1	E11
IO18PB0F1	E10
IO19NB0F1	F13
IO19PB0F1	G13
IO20NB0F1	A10
IO20PB0F1	A9
IO21NB0F1	K14
IO21PB0F1	K13
IO22NB0F2	B11
IO22PB0F2	B10
IO23NB0F2	C12
IO23PB0F2	C11
IO24NB0F2	A12
IO24PB0F2	A11
IO25NB0F2	H14
IO25PB0F2	J14
IO26NB0F2	D13
IO26PB0F2	D12
IO27NB0F2	F14
IO27PB0F2	G14
IO28NB0F2	E14
IO28PB0F2	E13
IO29NB0F2	B13
IO29PB0F2	B12
IO30NB0F2	C14
IO30PB0F2	C13
IO31NB0F2	H15
IO31PB0F2	J15
IO32NB0F2	A14
IO32PB0F2	B14
IO33NB0F2	K15
IO33PB0F2	L15
IO34NB0F3	D15
IO34PB0F3	D14
IO35NB0F3	A15
IO35PB0F3	B15
IO36NB0F3	B16

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO36PB0F3	A16
IO37NB0F3	G16
IO37PB0F3	G15
IO38NB0F3	D16
IO38PB0F3	C16
IO39NB0F3	K16
IO39PB0F3	L16
IO40NB0F3	D17
IO40PB0F3	C17
IO41NB0F3/HCLKAN	E16
IO41PB0F3/HCLKAP	F16
IO42NB0F3/HCLKBN	G17
IO42PB0F3/HCLKBP	F17
Bank 1	
IO43NB1F4/HCLKCN	G19
IO43PB1F4/HCLKCP	G18
IO44NB1F4/HCLKDN	E19
IO44PB1F4/HCLKDP	F19
IO45NB1F4	C18
IO45PB1F4	D18
IO46NB1F4	A18
IO46PB1F4	B18
IO47NB1F4	K19
IO47PB1F4	L19
IO48NB1F4	C19
IO48PB1F4	D19
IO49NB1F4	K20
IO49PB1F4	L20
IO50NB1F4	A19
IO50PB1F4	B19
IO51NB1F4	H20
IO51PB1F4	J20
IO52NB1F4	B20
IO52PB1F4	A20
IO53NB1F4	F20
IO53PB1F4	E20
IO54NB1F5	B21

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO54PB1F5	A21
IO55NB1F5	K21
IO55PB1F5	J21
IO56NB1F5	D21
IO56PB1F5	C21
IO57NB1F5	G22
IO57PB1F5	G21
IO58NB1F5	E22
IO58PB1F5	E21
IO59NB1F5	D22
IO59PB1F5	C22
IO60NB1F5	B23
IO60PB1F5	A23
IO61NB1F5	H22
IO61PB1F5	H21
IO62NB1F5	C24
IO62PB1F5	C23
IO63NB1F5	F23
IO63PB1F5	F22
IO64NB1F6	B24
IO64PB1F6	A24
IO65NB1F6	J22
IO65PB1F6	K22
IO66NB1F6	B25
IO66PB1F6	A25
IO67NB1F6	K23
IO67PB1F6	J23
IO68NB1F6	F24
IO68PB1F6	E24
IO69NB1F6	C27
IO69PB1F6	C26
IO70NB1F6	H24
IO70PB1F6	G24
IO71NB1F6	H23
IO71PB1F6	G23
IO72NB1F6	B28
IO72PB1F6	A28

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO73NB1F6	E26
IO73PB1F6	E25
IO74NB1F6	F26
IO74PB1F6	F25
IO75NB1F6	K25
IO75PB1F6	K24
IO76NB1F7	D27
IO76PB1F7	D26
IO77NB1F7	B29
IO77PB1F7	A29
IO78NB1F7	D28
IO78PB1F7	C28
IO79NB1F7	H25
IO79PB1F7	G25
IO80NB1F7	F27
IO80PB1F7	E27
IO81NB1F7	J25
IO81PB1F7	J24
IO82NB1F7	D29
IO82PB1F7	C29
IO83NB1F7	H26
IO83PB1F7	G26
IO84NB1F7	F28
IO84PB1F7	E28
IO85NB1F7	H27
IO85PB1F7	G27
Bank 2	
IO86NB2F8	J28
IO86PB2F8	J27
IO87NB2F8	M25
IO87PB2F8	L25
IO88NB2F8	L26
IO88PB2F8	K26
IO89NB2F8	G31
IO89PB2F8	F31
IO90NB2F8	H29
IO90PB2F8	G29

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO91NB2F8	K28
IO91PB2F8	K27
IO92NB2F8	J30
IO92PB2F8	H30
IO93NB2F8	L28
IO93PB2F8	L27
IO94NB2F8	K29
IO94PB2F8	J29
IO95NB2F8	K31
IO95PB2F8	J31
IO96NB2F9	J32
IO96PB2F9	H32
IO97NB2F9	M27
IO97PB2F9	M26
IO98NB2F9	L30
IO98PB2F9	K30
IO99NB2F9	N25
IO99PB2F9	N26
IO100NB2F9	M29
IO100PB2F9	L29
IO101NB2F9	L33
IO101PB2F9	L32
IO102NB2F9	K34
IO102PB2F9	K33
IO103NB2F9	N28
IO103PB2F9	M28
IO104NB2F9	M34
IO104PB2F9	L34
IO105NB2F9	P27
IO105PB2F9	N27
IO106NB2F9	M32
IO106PB2F9	M31
IO107NB2F10	P25
IO107PB2F10	P26
IO108NB2F10	N33
IO108PB2F10	M33
IO109NB2F10	P29

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO109PB2F10	N29
IO110NB2F10	P30
IO110PB2F10	N30
IO111NB2F10	R24
IO111PB2F10	R25
IO112NB2F10	P31
IO112PB2F10	N31
IO113NB2F10	R28
IO113PB2F10	P28
IO114NB2F10	P32
IO114PB2F10	N32
IO115NB2F10	R30
IO115PB2F10	R29
IO116NB2F10	P34
IO116PB2F10	P33
IO117NB2F10	R27
IO117PB2F10	R26
IO118NB2F11	R34
IO118PB2F11	R33
IO119NB2F11	T24
IO119PB2F11	T25
IO120NB2F11	T33
IO120PB2F11	T34
IO121NB2F11	T27
IO121PB2F11	T26
IO122NB2F11	T30
IO122PB2F11	T29
IO123NB2F11	U28
IO123PB2F11	T28
IO124NB2F11	T31
IO124PB2F11	T32
IO125NB2F11	U24
IO125PB2F11	U25
IO126NB2F11	U33
IO126PB2F11	U34
IO127NB2F11	U26
IO127PB2F11	U27

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO128NB2F11	U31
IO128PB2F11	U32
Bank 3	
IO129NB3F12	V29
IO129PB3F12	U29
IO130NB3F12	V31
IO130PB3F12	V32
IO131NB3F12	V24
IO131PB3F12	V25
IO132NB3F12	W28
IO132PB3F12	V28
IO133NB3F12	W26
IO133PB3F12	V26
IO134NB3F12	W33
IO134PB3F12	V33
IO135NB3F12	W25
IO135PB3F12	W24
IO136NB3F12	W31
IO136PB3F12	W32
IO137NB3F12	Y30
IO137PB3F12	W30
IO138NB3F12	Y29
IO138PB3F12	W29
IO139NB3F13	Y27
IO139PB3F13	W27
IO140NB3F13	AA33
IO140PB3F13	Y33
IO141NB3F13	Y25
IO141PB3F13	Y24
IO142NB3F13	AA31
IO142PB3F13	Y31
IO143NB3F13	AA28
IO143PB3F13	Y28
IO144NB3F13	AA34
IO144PB3F13	Y34
IO145NB3F13	AA26
IO145PB3F13	Y26

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO146NB3F13	AA29
IO146PB3F13	AA30
IO147NB3F13	AB30
IO147PB3F13	AB29
IO148NB3F13	AB32
IO148PB3F13	AA32
IO149NB3F13	AB27
IO149PB3F13	AA27
IO150NB3F14	AC31
IO150PB3F14	AB31
IO151NB3F14	AD33
IO151PB3F14	AC33
IO152NB3F14	AC28
IO152PB3F14	AB28
IO153NB3F14	AB25
IO153PB3F14	AA25
IO154NB3F14	AD32
IO154PB3F14	AC32
IO155NB3F14	AD29
IO155PB3F14	AC29
IO156NB3F14	AE30
IO156PB3F14	AD30
IO157NB3F14	AC26
IO157PB3F14	AB26
IO158NB3F14	AH33
IO158PB3F14	AG33
IO159NB3F14	AD27
IO159PB3F14	AC27
IO160NB3F14	AG32
IO160PB3F14	AF32
IO161NB3F15	AG31
IO161PB3F15	AF31
IO162NB3F15	AF29
IO162PB3F15	AE29
IO163NB3F15	AE28
IO163PB3F15	AD28
IO164NB3F15	AG30

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO164PB3F15	AF30
IO165NB3F15	AE26
IO165PB3F15	AD26
IO166NB3F15	AJ30
IO166PB3F15	AH30
IO167NB3F15	AG28
IO167PB3F15	AF28
IO168NB3F15	AF27
IO168PB3F15	AE27
IO169NB3F15	AH29
IO169PB3F15	AG29
IO170NB3F15	AD25
IO170PB3F15	AC25
Bank 4	
IO171NB4F16	AP29
IO171PB4F16	AN29
IO172NB4F16	AH26
IO172PB4F16	AH27
IO173NB4F16	AJ27
IO173PB4F16	AJ28
IO174NB4F16	AL27
IO174PB4F16	AL28
IO175NB4F16	AM28
IO175PB4F16	AM29
IO176NB4F16	AG25
IO176PB4F16	AG26
IO177NB4F16	AK26
IO177PB4F16	AK27
IO178NB4F16	AF25
IO178PB4F16	AE25
IO179NB4F16	AP28
IO179PB4F16	AN28
IO180NB4F16	AJ25
IO180PB4F16	AJ26
IO181NB4F17	AM26
IO181PB4F17	AM27
IO182NB4F17	AF24

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO182PB4F17	AE24
IO183NB4F17	AH24
IO183PB4F17	AH25
IO184NB4F17	AG23
IO184PB4F17	AG24
IO185NB4F17	AL25
IO185PB4F17	AL26
IO186NB4F17	AP25
IO186PB4F17	AP26
IO187NB4F17	AK24
IO187PB4F17	AK25
IO188NB4F17	AF23
IO188PB4F17	AE23
IO189NB4F17	AN24
IO189PB4F17	AM24
IO190NB4F17	AH22
IO190PB4F17	AH23
IO191NB4F17	AJ23
IO191PB4F17	AJ24
IO192NB4F17	AG21
IO192PB4F17	AG22
IO193NB4F18	AP23
IO193PB4F18	AP24
IO194NB4F18	AN22
IO194PB4F18	AN23
IO195NB4F18	AM23
IO195PB4F18	AL23
IO196NB4F18	AF21
IO196PB4F18	AF22
IO197NB4F18	AL22
IO197PB4F18	AM22
IO198NB4F18	AE21
IO198PB4F18	AE22
IO199NB4F18	AJ21
IO199PB4F18	AJ22
IO200NB4F18	AK21
IO200PB4F18	AK22

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO201NB4F18	AM21
IO201PB4F18	AL21
IO202NB4F18	AE20
IO202PB4F18	AD20
IO203NB4F19	AN21
IO203PB4F19	AP21
IO204NB4F19	AP20
IO204PB4F19	AN20
IO205NB4F19	AN19
IO205PB4F19	AP19
IO206NB4F19	AG20
IO206PB4F19	AF20
IO207NB4F19	AL19
IO207PB4F19	AL20
IO208NB4F19	AG19
IO208PB4F19	AF19
IO209NB4F19	AN18
IO209PB4F19	AP18
IO210NB4F19	AE19
IO210PB4F19	AD19
IO211NB4F19	AL18
IO211PB4F19	AM18
IO212NB4F19/CLKEN	AJ20
IO212PB4F19/CLKEP	AK20
IO213NB4F19/CLKFN	AJ18
IO213PB4F19/CLKFP	AJ19
Bank 5	
IO214NB5F20/CLKGN	AJ16
IO214PB5F20/CLKGP	AJ17
IO215NB5F20/CLKHN	AJ15
IO215PB5F20/CLKHP	AK15
IO216NB5F20	AD16
IO216PB5F20	AE17
IO217NB5F20	AM17
IO217PB5F20	AL17
IO218NB5F20	AG16
IO218PB5F20	AF16

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO219NB5F20	AM16
IO219PB5F20	AL16
IO220NB5F20	AP16
IO220PB5F20	AN16
IO221NB5F20	AN15
IO221PB5F20	AP15
IO222NB5F20	AD15
IO222PB5F20	AE16
IO223NB5F21	AL14
IO223PB5F21	AL15
IO224NB5F21	AN14
IO224PB5F21	AP14
IO225NB5F21	AK13
IO225PB5F21	AK14
IO226NB5F21	AE15
IO226PB5F21	AF15
IO227NB5F21	AG14
IO227PB5F21	AG15
IO228NB5F21	AJ13
IO228PB5F21	AJ14
IO229NB5F21	AM13
IO229PB5F21	AM14
IO230NB5F21	AE14
IO230PB5F21	AF14
IO231NB5F21	AN12
IO231PB5F21	AP12
IO232NB5F21	AG13
IO232PB5F21	AH13
IO233NB5F21	AL12
IO233PB5F21	AL13
IO234NB5F21	AE13
IO234PB5F21	AF13
IO235NB5F22	AN11
IO235PB5F22	AP11
IO236NB5F22	AM11
IO236PB5F22	AM12
IO237NB5F22	AJ11

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO237PB5F22	AJ12
IO238NB5F22	AH11
IO238PB5F22	AH12
IO239NB5F22	AK10
IO239PB5F22	AK11
IO240NB5F22	AE12
IO240PB5F22	AF12
IO241NB5F22	AN10
IO241PB5F22	AP10
IO242NB5F22	AG11
IO242PB5F22	AG12
IO243NB5F22	AL9
IO243PB5F22	AL10
IO244NB5F22	AM8
IO244PB5F22	AM9
IO245NB5F23	AH10
IO245PB5F23	AJ10
IO246NB5F23	AF10
IO246PB5F23	AF11
IO247NB5F23	AJ9
IO247PB5F23	AK9
IO248NB5F23	AN7
IO248PB5F23	AP7
IO249NB5F23	AL7
IO249PB5F23	AL8
IO250NB5F23	AE10
IO250PB5F23	AE11
IO251NB5F23	AK8
IO251PB5F23	AJ8
IO252NB5F23	AH8
IO252PB5F23	AH9
IO253NB5F23	AN6
IO253PB5F23	AP6
IO254NB5F23	AG9
IO254PB5F23	AG10
IO255NB5F23	AJ7
IO255PB5F23	AK7

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO256NB5F23	AL6
IO256PB5F23	AM6
Bank 6	
IO257NB6F24	AG6
IO257PB6F24	AH6
IO258NB6F24	AD9
IO258PB6F24	AE9
IO259NB6F24	AF7
IO259PB6F24	AG7
IO260NB6F24	AH3
IO260PB6F24	AH4
IO261NB6F24	AH5
IO261PB6F24	AJ5
IO262NB6F24	AE6
IO262PB6F24	AF6
IO263NB6F24	AF5
IO263PB6F24	AG5
IO264NB6F24	AD8
IO264PB6F24	AE8
IO265NB6F24	AF3
IO265PB6F24	AG3
IO266NB6F24	AC10
IO266PB6F24	AD10
IO267NB6F25	AD7
IO267PB6F25	AE7
IO268NB6F25	AD5
IO268PB6F25	AE5
IO269NB6F25	AE4
IO269PB6F25	AF4
IO270NB6F25	AB9
IO270PB6F25	AC9
IO271NB6F25	AC6
IO271PB6F25	AD6
IO272NB6F25	AB8
IO272PB6F25	AC8
IO273NB6F25	AE1
IO273PB6F25	AE2

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO274NB6F25	AA10
IO274PB6F25	AB10
IO275NB6F25	AB7
IO275PB6F25	AC7
IO276NB6F25	AD1
IO276PB6F25	AD2
IO277NB6F25	AC4
IO277PB6F25	AC3
IO278NB6F26	AA8
IO278PB6F26	AA9
IO279NB6F26	AB5
IO279PB6F26	AB6
IO280NB6F26	Y10
IO280PB6F26	Y11
IO281NB6F26	AB3
IO281PB6F26	AB4
IO282NB6F26	Y7
IO282PB6F26	AA7
IO283NB6F26	AC2
IO283PB6F26	AC1
IO284NB6F26	Y9
IO284PB6F26	Y8
IO285NB6F26	AA5
IO285PB6F26	AA6
IO286NB6F26	W10
IO286PB6F26	W11
IO287NB6F26	AA3
IO287PB6F26	AA4
IO288NB6F26	W9
IO288PB6F26	W8
IO289NB6F27	AA1
IO289PB6F27	AA2
IO290NB6F27	W6
IO290PB6F27	Y6
IO291NB6F27	W5
IO291PB6F27	Y5
IO292NB6F27	V7

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO292PB6F27	W7
IO293NB6F27	W4
IO293PB6F27	Y4
IO294NB6F27	V10
IO294PB6F27	V11
IO295NB6F27	Y1
IO295PB6F27	Y2
IO296NB6F27	W1
IO296PB6F27	W2
IO297NB6F27	V1
IO297PB6F27	V2
IO298NB6F27	V9
IO298PB6F27	V8
IO299NB6F27	U4
IO299PB6F27	V4
Bank 7	
IO300NB7F28	U10
IO300PB7F28	U11
IO301NB7F28	U2
IO301PB7F28	U1
IO302NB7F28	U6
IO302PB7F28	U7
IO303NB7F28	T3
IO303PB7F28	U3
IO304NB7F28	U9
IO304PB7F28	U8
IO305NB7F28	R2
IO305PB7F28	R1
IO306NB7F28	R4
IO306PB7F28	T4
IO307NB7F28	R5
IO307PB7F28	T5
IO308NB7F28	T11
IO308PB7F28	T10
IO309NB7F28	T6
IO309PB7F28	T7
IO310NB7F29	T9

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO310PB7F29	T8
IO311NB7F29	N3
IO311PB7F29	P3
IO312NB7F29	P7
IO312PB7F29	R7
IO313NB7F29	P6
IO313PB7F29	R6
IO314NB7F29	M2
IO314PB7F29	N2
IO315NB7F29	N4
IO315PB7F29	P4
IO316NB7F29	R9
IO316PB7F29	R8
IO317NB7F29	N5
IO317PB7F29	P5
IO318NB7F29	R10
IO318PB7F29	R11
IO319NB7F29	L2
IO319PB7F29	L1
IO320NB7F29	N8
IO320PB7F29	P8
IO321NB7F30	M6
IO321PB7F30	N6
IO322NB7F30	P10
IO322PB7F30	P9
IO323NB7F30	L3
IO323PB7F30	M3
IO324NB7F30	M7
IO324PB7F30	N7
IO325NB7F30	K2
IO325PB7F30	K1
IO326NB7F30	G2
IO326PB7F30	H2
IO327NB7F30	L6
IO327PB7F30	L5
IO328NB7F30	N10
IO328PB7F30	N9

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
IO329NB7F30	J4
IO329PB7F30	K4
IO330NB7F30	J5
IO330PB7F30	K5
IO331NB7F30	M10
IO331PB7F30	M9
IO332NB7F31	L8
IO332PB7F31	M8
IO333NB7F31	F2
IO333PB7F31	F1
IO334NB7F31	J6
IO334PB7F31	K6
IO335NB7F31	H4
IO335PB7F31	H3
IO336NB7F31	K7
IO336PB7F31	L7
IO337NB7F31	G4
IO337PB7F31	G3
IO338NB7F31	K9
IO338PB7F31	L9
IO339NB7F31	H6
IO339PB7F31	H5
IO340NB7F31	H7
IO340PB7F31	J7
IO341NB7F31	J8
IO341PB7F31	K8
Dedicated I/O	
GND	A13
GND	A2
GND	A22
GND	A27
GND	A3
GND	A31
GND	A32
GND	A33
GND	A4
GND	A8

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
GND	AA14
GND	AA15
GND	AA16
GND	AA17
GND	AA18
GND	AA19
GND	AA20
GND	AA21
GND	AB1
GND	AB13
GND	AB22
GND	AB34
GND	AC12
GND	AC23
GND	AC30
GND	AC5
GND	AD11
GND	AD24
GND	AD31
GND	AD4
GND	AE3
GND	AE32
GND	AF2
GND	AF33
GND	AG1
GND	AG27
GND	AG34
GND	AG8
GND	AH28
GND	AH7
GND	AJ29
GND	AJ6
GND	AK12
GND	AK17
GND	AK18
GND	AK23
GND	AK30

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
GND	AK5
GND	AL1
GND	AL11
GND	AL2
GND	AL24
GND	AL3
GND	AL31
GND	AL32
GND	AL33
GND	AL34
GND	AL4
GND	AM1
GND	AM10
GND	AM15
GND	AM2
GND	AM20
GND	AM25
GND	AM3
GND	AM31
GND	AM32
GND	AM33
GND	AM34
GND	AM4
GND	AN1
GND	AN2
GND	AN26
GND	AN3
GND	AN31
GND	AN32
GND	AN33
GND	AN34
GND	AN4
GND	AN9
GND	AP13
GND	AP2
GND	AP22
GND	AP27

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
GND	AP3
GND	AP31
GND	AP32
GND	AP33
GND	AP4
GND	AP8
GND	B1
GND	B2
GND	B26
GND	B3
GND	B31
GND	B32
GND	B33
GND	B34
GND	B4
GND	B9
GND	C1
GND	C10
GND	C15
GND	C2
GND	C20
GND	C25
GND	C3
GND	C31
GND	C32
GND	C33
GND	C34
GND	C4
GND	D1
GND	D11
GND	D2
GND	D24
GND	D3
GND	D31
GND	D32
GND	D33
GND	D34

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
GND	D4
GND	E12
GND	E17
GND	E18
GND	E23
GND	E30
GND	E5
GND	F29
GND	F30
GND	F6
GND	G28
GND	G6
GND	G7
GND	H1
GND	H34
GND	J2
GND	J33
GND	K3
GND	K32
GND	L11
GND	L24
GND	L31
GND	L4
GND	M12
GND	M23
GND	M30
GND	M5
GND	N1
GND	N13
GND	N22
GND	N34
GND	P14
GND	P15
GND	P16
GND	P17
GND	P18
GND	P19

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
GND	P20
GND	P21
GND	R14
GND	R15
GND	R16
GND	R17
GND	R18
GND	R19
GND	R20
GND	R21
GND	R3
GND	R32
GND	T14
GND	T15
GND	T16
GND	T17
GND	T18
GND	T19
GND	T20
GND	T21
GND	U14
GND	U15
GND	U16
GND	U17
GND	U18
GND	U19
GND	U20
GND	U21
GND	U30
GND	U5
GND	V14
GND	V15
GND	V16
GND	V17
GND	V18
GND	V19
GND	V20

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
GND	V21
GND	V30
GND	V5
GND	W14
GND	W15
GND	W16
GND	W17
GND	W18
GND	W19
GND	W20
GND	W21
GND	Y14
GND	Y15
GND	Y16
GND	Y17
GND	Y18
GND	Y19
GND	Y20
GND	Y21
GND	Y3
GND	Y32
NC	A17
NC	A26
NC	AB2
NC	AB33
NC	AC34
NC	AD17
NC	AD3
NC	AD34
NC	AE18
NC	AE31
NC	AE33
NC	AE34
NC	AF1
NC	AF17
NC	AF18
NC	AF34

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
NC	AG2
NC	AG4
NC	AH1
NC	AH16
NC	AH19
NC	AH2
NC	AH31
NC	AH32
NC	AH34
NC	AJ1
NC	AJ2
NC	AJ3
NC	AJ31
NC	AJ32
NC	AJ33
NC	AJ34
NC	AJ4
NC	AK16
NC	AK19
NC	AL29
NC	AM19
NC	AM7
NC	AN13
NC	AN17
NC	AN25
NC	AN27
NC	AN8
NC	AP17
NC	AP9
NC	B17
NC	B22
NC	B27
NC	B8
NC	D10
NC	D20
NC	D23
NC	D25

1152-Pin CCGA/LGA	
RTAX2000S Function	Pin Number
NC	F3
NC	F32
NC	F33
NC	F34
NC	F4
NC	G1
NC	G32
NC	G33
NC	G34
NC	H16
NC	H19
NC	H31
NC	H33
NC	J1
NC	J16
NC	J19
NC	J3
NC	J34
NC	K17
NC	K18
NC	L17
NC	L18
NC	M1
NC	M4
NC	P1
NC	P2
NC	R31
NC	T1
NC	T2
NC	V3
NC	V34
NC	W3
NC	W34
PRA	J17
PRB	F18
PRC	AD18
PRD	AH18

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
TCK	J9
TDI	F7
TDO	L10
TMS	H8
TRST	E6
V_{CCA}	AA13
V_{CCA}	AA22
V_{CCA}	AB14
V_{CCA}	AB15
V_{CCA}	AB16
V_{CCA}	AB17
V_{CCA}	AB18
V_{CCA}	AB19
V_{CCA}	AB20
V_{CCA}	AB21
V_{CCA}	AF8
V_{CCA}	AK28
V_{CCA}	G30
V_{CCA}	G5
V_{CCA}	N14
V_{CCA}	N15
V_{CCA}	N16
V_{CCA}	N17
V_{CCA}	N18
V_{CCA}	N19
V_{CCA}	N20
V_{CCA}	N21
V_{CCA}	P13
V_{CCA}	P22
V_{CCA}	R13
V_{CCA}	R22
V_{CCA}	T13
V_{CCA}	T22
V_{CCA}	U13
V_{CCA}	U22
V_{CCA}	V13
V_{CCA}	V22

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
V_{CCA}	W13
V_{CCA}	W22
V_{CCA}	Y13
V_{CCA}	Y22
V_{CCDA}	AF26
V_{CCDA}	AF9
V_{CCDA}	AG17
V_{CCDA}	AG18
V_{CCDA}	AH14
V_{CCDA}	AH15
V_{CCDA}	AH17
V_{CCDA}	AH20
V_{CCDA}	AH21
V_{CCDA}	AK29
V_{CCDA}	AK6
V_{CCDA}	E15
V_{CCDA}	E29
V_{CCDA}	E7
V_{CCDA}	F15
V_{CCDA}	F21
V_{CCDA}	F5
V_{CCDA}	G20
V_{CCDA}	H17
V_{CCDA}	H18
V_{CCDA}	H28
V_{CCDA}	J18
V_{CCDA}	V27
V_{CCDA}	V6
$V_{CCI}B0$	A5
$V_{CCI}B0$	B5
$V_{CCI}B0$	C5
$V_{CCI}B0$	D5
$V_{CCI}B0$	L12
$V_{CCI}B0$	L13
$V_{CCI}B0$	L14
$V_{CCI}B0$	M13
$V_{CCI}B0$	M14

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
$V_{CCI}B0$	M15
$V_{CCI}B0$	M16
$V_{CCI}B0$	M17
$V_{CCI}B1$	A30
$V_{CCI}B1$	B30
$V_{CCI}B1$	C30
$V_{CCI}B1$	D30
$V_{CCI}B1$	L21
$V_{CCI}B1$	L22
$V_{CCI}B1$	L23
$V_{CCI}B1$	M18
$V_{CCI}B1$	M19
$V_{CCI}B1$	M20
$V_{CCI}B1$	M21
$V_{CCI}B1$	M22
$V_{CCI}B2$	E31
$V_{CCI}B2$	E32
$V_{CCI}B2$	E33
$V_{CCI}B2$	E34
$V_{CCI}B2$	M24
$V_{CCI}B2$	N23
$V_{CCI}B2$	N24
$V_{CCI}B2$	P23
$V_{CCI}B2$	P24
$V_{CCI}B2$	R23
$V_{CCI}B2$	T23
$V_{CCI}B2$	U23
$V_{CCI}B3$	AA23
$V_{CCI}B3$	AA24
$V_{CCI}B3$	AB23
$V_{CCI}B3$	AB24
$V_{CCI}B3$	AC24
$V_{CCI}B3$	AK31
$V_{CCI}B3$	AK32
$V_{CCI}B3$	AK33
$V_{CCI}B3$	AK34
$V_{CCI}B3$	V23

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
$V_{CCI}B3$	W23
$V_{CCI}B3$	Y23
$V_{CCI}B4$	AC18
$V_{CCI}B4$	AC19
$V_{CCI}B4$	AC20
$V_{CCI}B4$	AC21
$V_{CCI}B4$	AC22
$V_{CCI}B4$	AD21
$V_{CCI}B4$	AD22
$V_{CCI}B4$	AD23
$V_{CCI}B4$	AL30
$V_{CCI}B4$	AM30
$V_{CCI}B4$	AN30
$V_{CCI}B4$	AP30
$V_{CCI}B5$	AC13
$V_{CCI}B5$	AC14
$V_{CCI}B5$	AC15
$V_{CCI}B5$	AC16
$V_{CCI}B5$	AC17
$V_{CCI}B5$	AD12
$V_{CCI}B5$	AD13
$V_{CCI}B5$	AD14
$V_{CCI}B5$	AL5
$V_{CCI}B5$	AM5
$V_{CCI}B5$	AN5
$V_{CCI}B5$	AP5
$V_{CCI}B6$	AA11
$V_{CCI}B6$	AA12
$V_{CCI}B6$	AB11
$V_{CCI}B6$	AB12
$V_{CCI}B6$	AC11
$V_{CCI}B6$	AK1
$V_{CCI}B6$	AK2
$V_{CCI}B6$	AK3
$V_{CCI}B6$	AK4
$V_{CCI}B6$	V12
$V_{CCI}B6$	W12

1152-Pin CCGA/LGA	
RTAX2000S Function	**Pin Number**
$V_{CCI}B6$	Y12
$V_{CCI}B7$	E1
$V_{CCI}B7$	E2
$V_{CCI}B7$	E3
$V_{CCI}B7$	E4
$V_{CCI}B7$	M11
$V_{CCI}B7$	N11
$V_{CCI}B7$	N12
$V_{CCI}B7$	P11
$V_{CCI}B7$	P12
$V_{CCI}B7$	R12
$V_{CCI}B7$	T12
$V_{CCI}B7$	U12
V_{PUMP}	J26

Datasheet Information

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v2.2)	Page
v2.1 October 2005	The LVDS Capable I/O specification was added to "Leading-Edge Performance".	i-i
	Table 1 • RTAX-S Family Product Profile was updated to include CQ256.	i-i
	CQ256 was added to the "Temperature Grade Offerings" table.	i-ii
	CQ256 was is new and CQ352 for the RTAX1000S device was updated in the "Device Resources" table.	i-ii
	The "Overshoot/Undershoot Limits" section is new.	2-2
	Table 2-2 • Absolute Maximum Ratings was updated.	2-2
	Table 2-3 • Recommended Operating Conditions was updated.	2-2
	The "Timing Model" was updated.	2-8
	The "Hardwired Clock" equations were updated.	2-8
	The "Routed Clock" equations were updated.	2-8
	This sentence was updated in the "CLKE/F/G/H Global Clocks E, F, G, and H" section: When the CLK pins are unused, Actel recommends that they are tied to a known state.	2-9
	Figure 2-27 • LVPECL Circuit was updated. The following labels were corrected: INBUF_LVPECL OUTBUF_LVPECL	2-39
	The following sentence was removed from "Global Resource Distribution": An unused input can be tied to ground for power savings.	2-56
	The "RAM" section was updated.	2-59
	The "256-Pin CQFP" package figure and is new.	3-4
v2.0	In Table 2-4, the I_{CCA} column heading was changed to I_{CCDA} and note 3 is new.	2-3
Advanced v0.5	The "Designed for Space" section was updated.	i-i
	Table 1 was updated to include 1152 CCGA/LGA.	i-i
	The "Temperature Grade Offerings" table was updated to include the 1152 CCGA.	i-ii
	The RTAX1000S and the RTAX2000S columns were updated in the "Device Resources" table.	i-ii
	Figure 1-9 was updated and a note was added to the figure.	1-8
	Table 2-4 was updated.	2-3
	In Table 2-5 the LVPECL and LVDS specifications were updated. A note was also added to the table.	2-3
	The "Global Resource Access Macros" section was updated.	2-58
	The "JTAG" section was updated.	2-77

Previous version	Changes in current version (v2.2)	Page
Advanced v0.5 (continued)	In the "Data Registers (DRs)" section the IDCODE and USERCODE were changed from 32 bits to 33 bits.	2-77
	150°C was changed to 125°C in the "Package Thermal Characteristics" section.	2-6
	Table 2-7 was updated to include the 1152 CCGA.	2-6
	Table 2-8 was updated.	2-7
	A note was added to the "FIFO" section.	2-68
	Table 2-6 was updated.	2-4
	Table 2-15 was updated.	2-17
	All Timing Characteristic tables from Table 2-19 to Table 2-68 were updated.	2-22 to 2-59
	In the "Actel MIL-STD-883 Class B Product Flow" table, #3 for the 883 Method was updated. A note was also added to the table.	i-iii
	In the "Actel Extended Flow1" table, #5 for the Method column was updated. The notes were also added to the table.	i-iii
	In the "Pin Descriptions" section, the descriptions for the "HCLKA/B/C/D Dedicated (Hardwired) Clocks A, B, C, and D" and "CLKE/F/G/H Global Clocks E, F, G, and H" were updated.	2-9
	A footnote was added to the "PRA/B/C/D Probes A, B, C, and D", "TCK2 Test Clock", "TDI2 Test Data Input", "TDO2 Test Data Output", and "TDO2 Test Data Output" descriptions.	2-10
	The "1152-Pin CCGA/LGA" section is new.	3-34
Advanced v0.4	LET_{TH} values for SEU and SEL updated under "Designed for Space".	i-i
	"Ordering Information" was updated/ The "Temperature Grade Offerings", "Speed Grade and Temperature Grade Matrix"tables are new and the "Device Resources" was updated.	i-ii
	Sections "Actel MIL-STD-883 Class B Product Flow" and "Actel Extended Flow1" are new.	i-iii, i-iv
	"General Description" was updated.	1-1
	Table 2-6 was updated.	2-4
	The"Thermal Characteristics" section was updated.	2-6
	Figure 2-4, the "Hardwired Clock"section and the "Routed Clock" section were updated.	2-8
	The "Introduction" section under "User I/Os" was updated to give details regarding V_{REF} usage.	2-11
	The "Simultaneous Switching Outputs (SSO)" section under "User I/Os" was updated.	2-12
	"Using DDR (Double Data Rate)" is new.	2-15
	Table 2-16 was updated.	2-19
	All Timing Characteristic Tables were updated.	2-22 to 2-76
	"Introduction" was updated.	2-45
	The "SEU Hardened D Flip-Flop (DFF)" section was moved under "R-Cell" and updated.	2-46
	The "Global Resource Distribution" section is new.	2-56
	The "Enhancing SEU Performance" section is new.	2-61
	Figure 2-49 and Figure 2-50 were updated.	2-62
	Figure 2-57 and Figure 2-58 were updated.	2-73
	The "Charge Pump Bypass" section is new.	2-77
	The "TRST" section was updated.	2-77

Previous version	Changes in current version (v2.2)	Page
Advanced v0.4 (continued)	The "Global Set Fuse" section is new.	2-79
	The "208-Pin CQFP" for both the RTAX250S and RTAX1000S were added.	3-1
	The "352-Pin CQFP" pin tables for both the RTAX1000S and RTAX2000S were updated.	3-8
	The "624-Pin CCGA/LGA" pin tables for both the RTAX1000S and RTAX2000S were updated.	3-21
Advanced v0.3	The "Designed for Space" section was updated.	i
	A new device, the RTAX250S, was added to the "Designed for Space", "Ordering Information", "Temperature Grade Offerings" and "Device Resources" sections.	i to ii
	2.5V GTL+ support across full military range was removed.	n/a
	Table 1-1 • Number of Core Tiles per Device was updated.	1-4
	Table 2-5 • Standby Power and Table 2-6 • Default Cload/VCCI were updated.	2-3
	Table 2-7 • Different Components Contributing to the Total Power Consumption in RTAX-S Devices was updated.	2-4
	Table 2-12 • Legal I/O Usage Matrix was updated.	2-13
	Table 2-16 • I/O Macros for Voltage-Referenced I/O Standards	2-15
Advanced v0.2	In the 352-Pin CQFP for the RTAX1000S, pin 80 has been changed from VCCI to VCCIB6.	3-2
	In the 352-Pin CQFP and 352-Pin CQFP, the NC (V_{PP}) was changed to NC for all pins.	3-2 to 3-5
Advanced v0.1	The 352-Pin CQFP for the RTAX1000S is new.	3-2
	Pins 14 and 32 have been changed from VCCA to VCCI for the RTAX2000S in the 352-Pin CQFP.	3-5
	The 624-Pin CCGA for the RTAX1000S is new.	3-10

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," "Production," and "Datasheet Supplement." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advanced or production) containing general product information. This brief gives an overview of specific device and family information.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

Datasheet Supplement

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