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Convolutional Neural Network for Subharmonics Detection in Hardware-in-the-Loop

Marina Yushkova[1], Joseph Zambreno[2], Alberto Sanchez[1] and Angel de Castro[1]

[1]HCTLab Research Group, Universidad Autonoma de Madrid, Madrid 28049, Spain; [2]Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011, USA

ABSTRACT

Hardware-In-the-Loop has become a popular technique for testing real-time complex systems. One of its possible applications is power converter modeling to test digital controllers. When a switching converter model is used, the output of the controller can be read incorrectly. Therefore, undesirable oscillations can appear in the output due to the aliasing effects, which prevent the twin model from its normal functionality. While there are various solutions present in academic and industrial research to address this arising problem, there is no automatic algorithm to detect it when a reference model is not available. In this paper, a one-dimensional convolutional neural network which allows detecting the aliasing distortions is implemented. The network was chosen due to the kind of signals to be classified – an inductor current of the converter model, which is in effect a 1D time sequence. The proposed CNN architecture is shallow and consists of 27 layers only. Despite its simplicity, it shows remarkable performance of more than 99% for both validation and testing datasets, and for the post-training characteristics. Moreover, it makes the architecture implementable in embedded systems, like real-time Hardware-In-the-Loop systems.

KEYWORDS

Convolutional neural network; Hardware-In-The-Loop; Power electronics; Real-time simulation; Switching converter

1. INTRODUCTION

1.1 State of the Art

Deep Learning has become an extremely powerful tool for wide range of tasks in all scientific areas. Unlike machine learning, deep learning performs automatic feature selection and extraction during the training process. This can drastically simplify the development process when feature operations are not obvious or require a large effort.

One of the fastest growing deep learning architectures is convolutional neural networks (CNNs). Their computation is based on applying filters (kernels) layer by layer to an input instance performing convolutions and building a feature map. The feature map is used for the response in the output, for example, for classifying the instance. The math inside the hidden layers is usually done by machine, which is why CNN calculations are often referred to as a black box. The most intuitive CNNs application is image recognition [1,2], which implies the usage of multidimensional neural networks. For example, some famous multidimensional convolutional networks for processing 2D and 3D objects are AlexNet, ResNet, VGGNet. AlexNet is used in [3] for handwritten digits recognition. In [4], ResNet is applied for the detection of melanoma cancer by classifying skin images. In [4], VGG-16 and VGG-19 architectures are used to classify dementia types by MRI images.

However, the need for artificial intelligence in various one-dimensional tasks has provoked the popularity of adapting classical multidimensional CNNs to one-dimensional ones, or creating them ad-hoc. Such numerous tasks include the detection of series arc faults [5], diagnosis of cardiological diseases [6], mosquito classification [7], transmission line fault detection [8], *etc*. Dealing with one-dimensional signals is what unites these dissimilar problems in contexts of convolutional neural networks. In [5], the authors use 1D voltage vectors for the detection and classification of series arc faults in photovoltaic systems applying a 1D CNN. In [6], the input dataset consists of electrocardiogram (ECG) signals, which are essentially 1D timing sequences. In [7], a 1D CNN is used for the classification of mosquito types by analyzing 1D audio recordings of their wings. In [8], a one-dimensional array of sampled three-phase line currents is fed to a 1D CNN. All developed 1D CNN architectures in the aforementioned papers are considered as potentially good candidates for embedded devices. This is due to their simple array operations and low computational burden.

In this work, 1D CNN usage for the detection of undesirable oscillations in Hardware-In-the-Loop (HIL) switched models is proposed. A modified version of the CNN proposed by Lu *et al.* in [6] which was inspired by VGG-16 neural network is applied. Unlike the application of 1D CNNs in [6], such as ECG classification in healthcare wearables, our work focuses on detecting aliasing distortions in Hardware-In-the-Loop (HIL) simulations for power electronics. This issue was not previously addressed with CNN-based solutions. To further clarify the distinctions between our work and prior research, including Lu *et al.*, a comparative analysis is provided in Section 1.2, highlighting key differences in application domain, preprocessing methodology, and deployment considerations.

The choice of the network is justified by its potential for hardware implementations (proven in [9]) and conceptual similarity of ECG signals used in [6] to the Hardware-In-the-Loop model outputs under research. Typical signals present in HIL systems are 1D time sequences which are used to imitate the behavior of real power converters [10]. These are state variable waves, such as inductor current and capacitor voltage. Due to occasional appearance of aliasing effects, the waves receive certain distortions that can affect the functionality of the system. This phenomenon is well-studied and analyzed for various applications [11–13]. Its appearance in the case of digital sampling in switched Hardware-In-the-Loop models was described in [14]. In that case, aliasing occurs when the control signal in the input of the model is read inaccurately provoking undesirable subharmonics in the output. While different engineering approaches from both academia and industry – such as simulation step reduction [15], parallel oversampling [16], integration oversampling [17], and gate drive signal (GDS) oversampling as implemented in commercial platforms like Typhoon HIL [18,19] – have been proposed to mitigate aliasing distortions, all these methods rely on structural or system-level adjustments to reduce the aliasing effect. However, none of these strategies include an automatic, data-driven detection mechanism capable of identifying aliasing-induced subharmonics in real time. In contrast, this work introduces the first application of a CNN-based model to detect aliasing distortions in digitally controlled switching converters within HIL simulations, providing a missing link between manual corrective actions and intelligent, automated detection solutions.

An effective CNN application to automatizing tracing of the oscillations in HIL models is presented. The dataset collection of 21k signals and its preprocessing were performed by the authors. The trained network obtains more than 99% for testing and validation accuracy, recall, precision, specificity, and F1 scores. The simple 1D CNN architecture makes possible its future implementation to integrated circuits such as Field-Programmable Gate Arrays (FPGAs).

The rest of this paper is organized as follows. Section 2 introduces the background of the problem to be solved and provides details on the dataset collection with examples of normal and abnormal behaviors. Section 3 describes the data preprocessing and the structure of the proposed 1D CNN. Section 4 provides the training options and plots along with the confusion matrix, final post-training characteristics and discussion on future work. The conclusion is given in Section 5.

1.2 Comparison with Related Work

Table 1 presents a structured comparison between our work and prior CNN applications, illustrating the unique aspects of our approach in aliasing detection within Hardware-In-the-Loop power electronics simulations. Specifically, it highlights the differences between our work and the study that inspired our neural network [6], demonstrating how our approach has been adapted and applied to a new problem domain. Table 1 provides a comparative overview between our work and previous CNN applications, as well as traditional aliasing mitigation strategies typically employed in HIL systems. Specifically, while prior CNN applications (*e.g.* ECG classification) operate on biomedical signals with segmentation and normalization as preprocessing steps, our approach introduces a dedicated preprocessing pipeline that extracts steady-state segments and removes high-frequency switching noise specific to power converter signals. Furthermore, unlike prior works focused on wearable or low-power devices [6], our model is optimized for real-time FPGA-based deployment in HIL environments.

The table also emphasizes that our work is the first to employ CNN-based methods for aliasing detection in power electronics HIL simulations, filling a gap left by engineering solutions that focus on aliasing prevention, rather than detection. By embedding intelligence into the detection process, more dynamic and adaptive control strategies for addressing subharmonic oscillations are enabled, paving the way for future closed-loop corrective frameworks.

Table 1: Comparison with related work

Feature	ECG classification [6]	HIL aliasing detection (this work)
Application	ECG classification in wearable devices	Aliasing detection in power electronics HIL models
Signal type	ECG waveforms	Inductor current waveforms from HIL simulations
Preprocessing	Segmentation and normalization	Steady-state extraction and switching ripple removal
CNN architecture	1D CNN inspired by VGG16 with GAP	1D CNN with 27 layers optimized for real-time FPGA deployment
Hardware implementation	Optimized for low-power wearables (Zynq ZC706)	Designed for real-time integration in HIL systems
Novel contribution	Efficient CNN for ECG classification	First CNN-based detection of aliasing effects in power electronics

2. PROBLEM STATEMENT AND DATASET COLLECTION

HIL models are created to emulate the behavior of a real plant in an HIL system to test digital controllers. The output of a digital controller is passed to the input of the model defining the way of variables calculation, since it depends on the state of switches (Figure 1). However, internal digital clocks of the controller and the clock of the model are usually not synchronized since they are designed in different boards. Besides, both the digital control and the HIL models have finite temporal resolution (for instance, modern HIL platform Typhoon HIL 606 uses 200 ns model clock cycle). Therefore, the model cannot detect the exact moment of the transition and for some time continues to calculate state variables as for the previous state, as it is shown on the top of Figure 1. This can cause appearance of undesirable subharmonics which do not exist in real plants, also known as aliasing. The aliasing problem in Hardware-In-the-Loop switching converters is explained in detail in [14]. In brief, aliasing distortion occurrence depends on the relation of parameters that define how the controller signal is read. Changing T_{sw} or dt is potentially problematic since they are set up in the design stage of the HIL system. Influencing the duty cycle D is not feasible; because it is regulated by the controller, its value can change during the simulation.

In this research, an asynchronous buck converter model controlled by a pulse-width modulation (PWM) signal is used as an example of a switching power converter. The operation of the converter can be explained using the following set of equations:

$$\begin{aligned} \frac{di_L}{dt} &= \frac{v_L}{L} \\ \frac{dv_C}{dt} &= \frac{i_C}{C} \end{aligned} \tag{1}$$

where i_L is the inductor current and v_C is the capacitor voltage – interdependent state variables of the model. The calculation mode varies depending on the potential states of the system. There are four possible states, such as closed switch, open switch with positive i_L, open switch

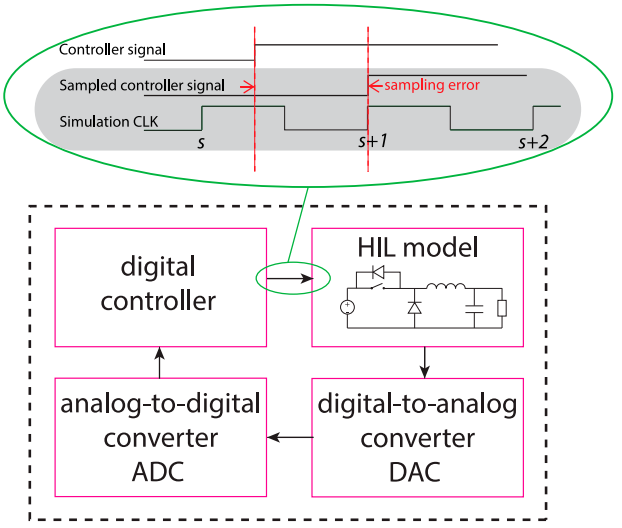

Figure 1: Reading of the controller signal in an HIL system

with slightly negative i_L and open switch with zero i_L:

$$\left.\begin{aligned} i_C &= i_L - \frac{v_C}{R} \\ v_L &= v_{in} - v_C \end{aligned}\right\} \textit{closed } S$$

$$\left.\begin{aligned} i_C &= i_L - \frac{v_C}{R} \\ v_L &= -v_C \end{aligned}\right\} \textit{open } S, i_L > 0$$

$$\left.\begin{aligned} i_C &= i_L - \frac{v_C}{R} \\ v_L &= v_{in} - v_C \end{aligned}\right\} \textit{open } S, i_L < 0$$

$$\left.\begin{aligned} i_C &= i_L - \frac{v_C}{R} \\ v_L &= 0 \end{aligned}\right\} \textit{open } S, i_L = 0 \tag{2}$$

where i_C is the current through the capacitor, v_L is the voltage across the inductor, and v_{in} is the input voltage. However, it is proven in [14] that the aliasing distortion does not depend on the topology of the switching model, so any model could have been used.

In Figure 2, two plots of normal behavior (a., b.) and two plots of undesirable behavior (c., d.) of the converter model are presented. The plots represent the state variables of the model – inductor current and capacitor voltage. As illustrated in Figure 2, the "abnormal"

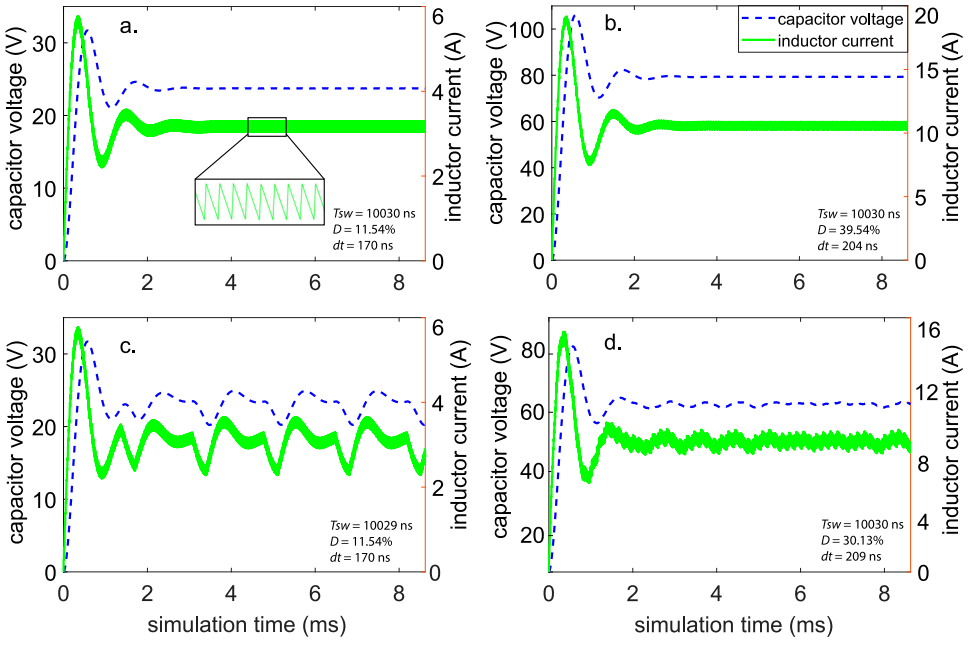

Figure 2: Examples of normal (a., b.) and abnormal (c., d.) behaviors of the converter simulation

signals detected by the CNN are characterized by the appearance of low-frequency subharmonic oscillations superimposed on the nominal switching ripple of the inductor current and capacitor voltage. For example, in Figure 2(c.), a small change in the switching period from 10,030 ns to 10,029 ns compared to Figure 2(a.) triggers a pronounced oscillatory behavior, which is not present in the normal case. These subharmonics are a direct result of aliasing distortions caused by improper sampling synchronization between the digital controller and the HIL model.

In real-world systems, such distortions would not occur due to continuous-time behavior in physical plants; however, in HIL setups, where sampling is performed discretely, the asynchronous interaction leads to incorrect PWM signal interpretation and causes these aliasing artifacts. The abnormal class, therefore, corresponds to signals where this undesired dynamic is present. In contrast, the normal class (Figure 2a. and b.) exhibits expected switching ripple behavior without additional low-frequency components.

This behavior has significant implications in the power electronics HIL community, as subharmonic distortions may compromise the fidelity of the models used in controller testing and validation. Our detection system is designed to automatically distinguish between these two scenarios based on the waveform characteristics, even in cases where the distortions are subtle or triggered by small parameter variations.

For future CNN design, 21,413 data samples were collected during simulations and classified into two classes (normal and abnormal). The classification was done using the MAE (Mean Absolute Error) formula divided by the reference value:

$$\frac{MAE}{Ref} = \frac{1}{n \cdot Ref} \sum_{j=1}^{n} |y_j - x_j| \tag{3}$$

MAE represents the difference between the measured value and the "true" reference value all over the simulation. Dividing by the reference value is necessary to normalize the errors for further classification, *i.e.* receive their error in percentage, not in absolute values. It can be noted from Figure 2 that the absolute value is not the same for different cases. Obtaining the reference value is not possible in online scenarios, because the unrealistically small time-step of 1 ns is used in the reference simulation to reach maximum precision. Thus the initial classification for teaching a neural network can be made only offline. However, once the CNN has been trained, it may be executed in real time, not needing any reference model.

The state variables of power converters are interdependent, so voltage distortion immediately causes current distortion, and vice versa. Therefore, to estimate abnormalities it is enough to analyze one variable, and only inductor current signals are used in this work to feed into the CNN, since it is more sensitive than capacitor voltage. To collect all possible patterns of abnormalities

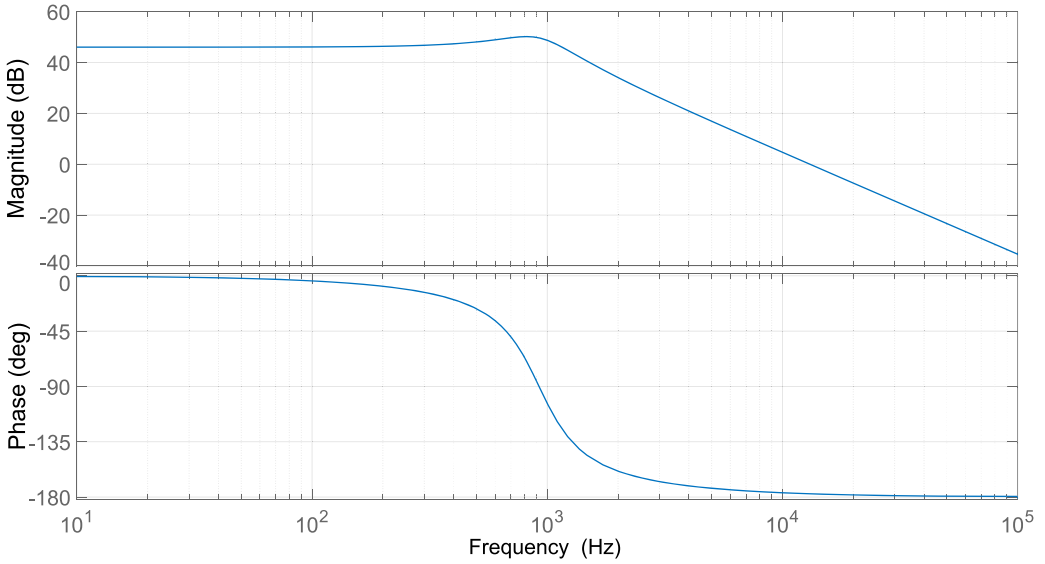

Figure 3: Bode diagram (duty cycle to output voltage) of the converter used in the study

Table 2: Parameters of the model used in the study

v_{in}	v_{out}	C	L	R	f_{sw}	D	dt
200 V	100 V	35 µF	850 µF	7.5 Ω	2–50 kHz	10–90%	100–1000 ns

in the dataset, different combinations of T_{sw}, D, and dt were applied during the dataset generation. The range of switching periods T_{sw} is defined from the Bode plot of the asynchronous buck converter, since it is a low-pass filter. The Bode diagram of the transfer function of the used converter in open loop is shown in Figure 3 (from duty cycle to output voltage). To discard the frequencies where the converter attenuates too much or not enough, f_{sw} are chosen in the range of 2–50 kHz. Though the converter was designed to operate at 10 kHz nominal frequency, various switching periods around it are considered to increase the number of points and create a generalized dataset with different resulting voltage and current ripples.

The duty cycle values D are within 10–90% range, and the simulation steps are within 100–1000 ns – typical simulation steps in Hardware-In-the-Loop applications in power electronics nowadays. These values along with the parameters of the buck converter model are presented in Table 2. In the following section, details on dataset preprocessing and the CNN architecture developed in the study will be discussed.

3. PREPROCESSING AND CNN ARCHITECTURE

3.1 Preprocessing

Preprocessing the inputs of CNNs is important because it helps to normalize the inputs, remove noise, and extract important features, all of which can lead to improved performance of the model. As can be seen in Figure 2 from the previous section, the dynamic of state variables can be divided by two segments: transient and steady state. Unlike other classification tasks, such as ECG classifications where waveform morphology is critical, aliasing detection requires isolating steady-state oscillations. Therefore, actual preprocessing approach focuses on filtering high-frequency switching noise and extracting only the relevant portions of inductor current waveforms.

To preprocess the original inductor current signals for the CNN input, only values in steady state are captured, since undesirable subharmonics can be masked during the transient by its natural oscillation. By definition, the steady state occurs when the characteristic values of the system (state variables) are unchanging in time [20]. In this work, it is considered that a signal is in steady state when its reference fluctuation is not higher than 2%. In addition, the signals for the dataset were filtered by their switching frequencies, not to merge switching ripple (which is part of correct working operation) with subharmonic oscillations.

Figure 4 shows a segment of the inductor current wave before and after the preprocessing. To facilitate the CNN teaching process, the high-frequency switching ripple was filtered capturing only lower peaks of the signal as it is shown in the figure. The high-frequency ripple does not bring importance to the final classification by normal and

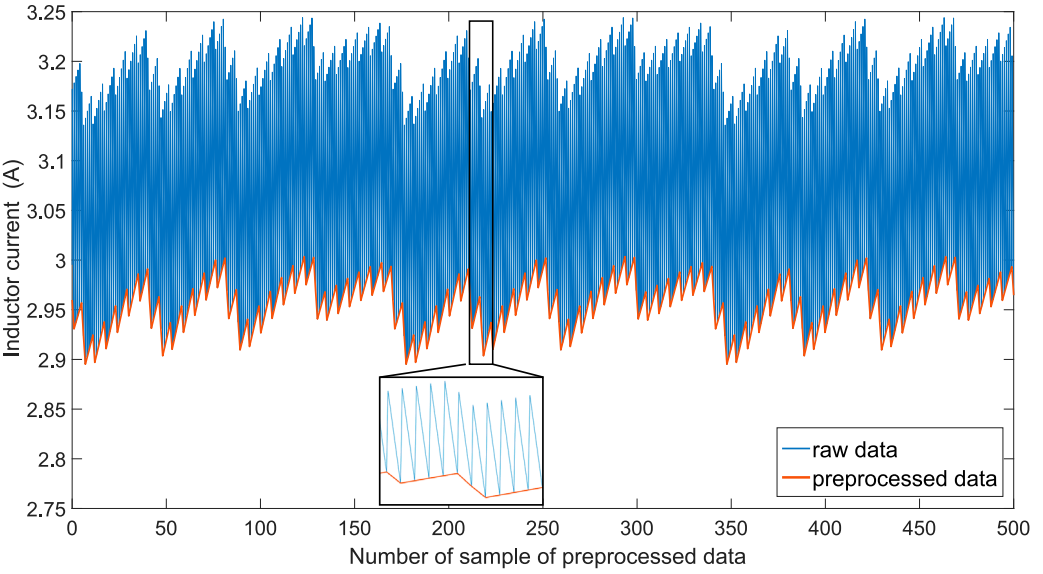

Figure 4: Example of the inductor current signal before and after preprocessing

abnormal classes, since the undesirable subharmonic is the low-frequency oscillation. Finally, to scale the inputs only the last 500 points of each signal were taken to be presented to the CNN classifier.

3.2 Convolutional Neural Network

1D CNNs have advantages over traditional multidimensional CNNs when dealing with 1D signals. Recent 1D CNNs show great efficiency having limited number of learnables (up to 10k) while their 2D analogs have 1M parameters and above [21]. This simplifies the design process of one-dimensional models. The computational complexity is proportional to the number of dimensions: for 1D CNN an $N \cdot N$ dimensional input convolves with $K \cdot K$ filter with computational complexity $O(NK)$, while for 2D CNN it is $O(N^2K^2)$. This reduction in the time and cost of developing 1D CNNs allows them to be implemented even on standard computers.

One-dimensional CNNs are used to automatically extract feature maps and classify 1D sequences, such as the state variable signals studied in this article. They mainly consist in convolutional, pooling, and fully connected layers. Convolutional layers are basic blocks of CNNs, they perform mathematical operations by applying various filters to an input instance and extracting features. Pooling layers are added to the outputs of convolutional layers to compress them, performing operations similar to convolution (max pooling, average pooling, *etc.*). Fully connected layers are used to flatter previous layers (turn them into a single vector) or to get final probabilities for the classification in the output.

Figure 5 shows the 1D feedforward CNN architecture used in this work. In the figure, Conv stands for convolutional, MP for maximum pooling, GAP for global average pooling, FC for fully connected layers. The input of the proposed CNN receives preprocessed inductor current signals of the size 500 × 1 and classifies it into two classes in the output: normal NORM and abnormal ABNR. In total, it consists of 27 layers, including 8 convolutional, 5 pooling, and 2 fully connected layers. For the convolutional layers, filter size of 5 × 1 is applied with the sliding stride 1. ReLU activation function is used all over the architecture except for the last fully connected layer, where Softmax function is applied. Training options, final results, and discussion will be presented in the following section.

4. TRAINING RESULTS AND DISCUSSION

The 1D convolutional neural network was implemented using the MATLAB environment. The preprocessed dataset of 21k samples was divided into 70% for training, 15% for validation, and 15% for independent testing. The training and validation parts were used exclusively for model training, while the final performance metrics were computed solely on the test set, which was never seen by the model during training. The following set of training options using the Adam optimizer was applied: the maximum number of epochs for training was set to 100, the mini-batch size is 64 observations at each iteration, and the initial learning rate was chosen as 0.0001. The best-validation-loss neural network is returned when the training is completed.

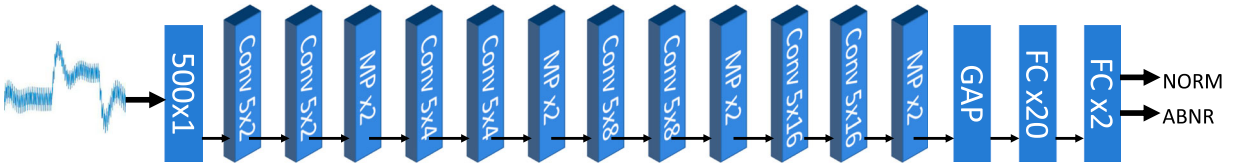

Figure 5: Architecture of 1D CNN implemented in the study

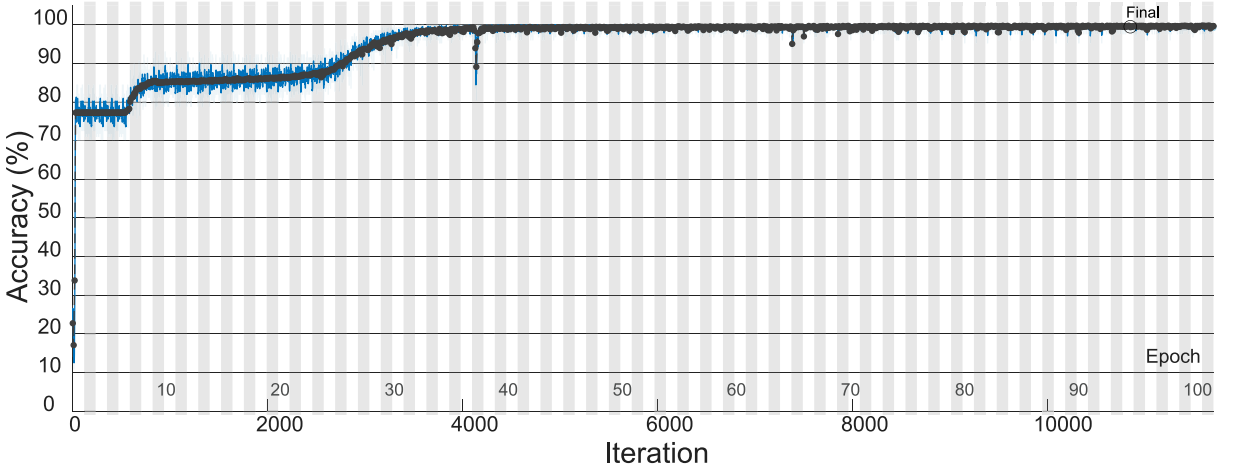

Figure 6: 1D CNN training **accuracy** plot

Table 3: Post-training characteristics

Testing accuracy	99.35%
Precision	99.92%
Recall	99.24%
Specificity	99.72%
F1	99.58%

Figures 6 and 7 show the training and validation accuracy and loss curves. As it can be noted from the figures, the accuracy increases to more than 70% initially in the first epoch, while the loss decreases to 0.4. Then, after the epoch 8 another accuracy peak is reached, up to 90%. Finally, after the epoch 30 the accuracy achieves a maximum and in epoch 93 defines the return model according to the best validation/loss proportion. After the training is done, 1D CNN obtained the validation accuracy of 99.38% and testing accuracy of 99.35%. The confusion matrix of the model is shown in Figure 8. Only 21 samples from 3212 testing dataset were misclassified. After analyzing the misclassified signals, it is concluded that there is no specific reason for their misclassification, so the 0.65% testing error is the error of the CNN. Post-training characteristics are presented in Table 3. As it can be seen, all the parameters such as precision, recall, specificity, and F1 get outstanding scores of more than 99%.

The proposed 1D CNN model is ready to use in software environment: any inductor current signal or batch of signals can be analyzed for the presence of undesirable oscillations automatically and without a need for a reference model. However, the CNN is specifically designed for real-time FPGA implementation within HIL systems. The architecture comprises only 2.9k parameters (learnables), making it highly efficient for hardware and real-time applications. Training was completed in approximately 90 minutes on a standard CPU (Intel Core i7-4790, 3.6 GHz), while inference for a single signal classification occurs within milliseconds, ensuring real-time suitability. Additionally, its compact 27-layer structure is optimized for embedded deployment, making it a practical choice for FPGA-based implementations. Its lightweight architecture ensures that it can be deployed in embedded environments for real-time aliasing detection and potential closed-loop correction strategies. Unlike traditional engineering solutions that rely on predefined mitigation techniques (*e.g.* oversampling [16–18], or step reduction [15]), our method introduces an automatic, data-driven detection layer using a CNN model, filling a notable gap in the state-of-the-art. Existing strategies aim to prevent aliasing distortions but do not include a mechanism to autonomously identify when these distortions occur. The novelty of our approach lies in integrating anomaly detection into the real-time workflow of HIL systems, enabling dynamic and automated responses to aliasing effects. To the best of our knowledge, this is the first implementation of CNN-based detection for aliasing distortions within real-time power electronics HIL simulations. Furthermore, this automated detection capability could improve system adaptability by selectively triggering corrective measures (*e.g.* activating oversampling only when necessary), thereby optimizing

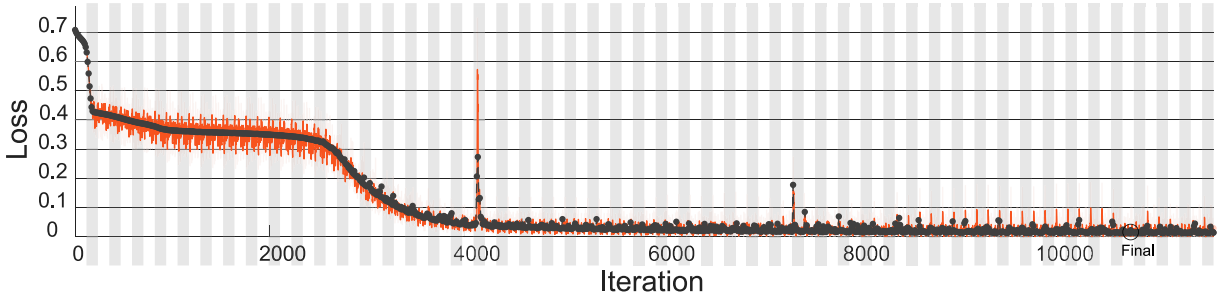

Figure 7: 1D CNN training **loss** plot

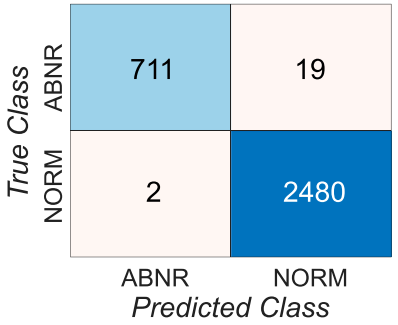

Figure 8: Confusion matrix of the testing dataset

resource usage and simulation performance. Thus one of the future work ideas is integrating the CNN into an HIL model to detect subharmonics in a real time simulations. Depending on the subharmonics appearance in closed loop, the CNN output would define if it is necessary to apply an algorithm for their removal (like GDS oversampling used by Typhoon HIL [18] or input oversampling proposed by the authors in [16]). Disabling oversampling when there is no need for it can reduce the simulation step – which implies better accuracy, since when oversampling is enabled, the calculation delay increases.

Beyond the current approach of enabling or disabling oversampling, an additional strategy can be considered. If subharmonics persist despite oversampling, an alternative mitigation technique based on the findings in [14] can be employed. Instead of reducing the sampling period – which may already be at its practical limit – a slight variation in the sampling period of the HIL system can be introduced. This adjustment would modify the relationship between the HIL sampling period (which is controllable) and the switching or PWM period (which is not directly controllable), thereby significantly reducing aliasing-induced oscillations without requiring a substantial increase in computational load.

5. CONCLUSION

This paper presents a lightweight and efficient one-dimensional convolutional neural network designed for aliasing detection in Hardware-In-the-Loop power electronics simulations. Unlike previous CNN applications, which have been widely used in fields such as image recognition, biomedical signal processing, and fault detection, this work applies deep learning to detect undesirable oscillations in digitally controlled power converters within Hardware-In-the-Loop simulations – a novel application that has not been explored before.

To achieve this, a dataset of 21,413 inductor current waveforms was developed, classified signals into normal and abnormal categories, and applied a tailored preprocessing pipeline to isolate steady-state behavior and remove high-frequency switching noise. Our CNN model achieves 99.38% validation accuracy and 99.35% testing accuracy, with all key performance metrics – including precision, recall, specificity, and F1-score – exceeding 99%.

In addition to software implementation, the study establishes a foundation for future real-time deployment in FPGA-based HIL systems. Apart from its lightweight structure and low computational cost, the key contribution of this work is the introduction of an automatic CNN-based detection framework for aliasing distortions – an area previously overlooked in power electronics HIL simulations. Although this study centers on detection, future research will investigate embedding the model within closed-loop control systems to facilitate real-time countermeasures against aliasing distortions.

DISCLOSURE STATEMENT

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AUTHORS

Marina Yushkova was born in Korsakov, Russia, in 1995. She received MSc degree in applied physics from Karazin Kharkiv National University, Ukraine, in 2018. She received PhD degree in computer science and telecommunication engineering from the Universidad Autónoma de Madrid, Madrid, in 2023. She is currently an assistant professor at the Technology for Electronics and Communications Department, Universidad Autónoma de Madrid. Her current research interests include simulation and control of mixed digital and analog systems, and applied artificial intelligence.

Corresponding author. Email: marina.yushkova@uam.es

Joseph Zambreno received the BS degree (summa cum laude) in computer engineering in 2001, the MS and PhD degrees in electrical and computer engineering in 2002 and 2006, respectively. He has been with the Department of Electrical and Computer Engineering, Iowa State University, since 2006, where he is currently a professor, the associate chair, and the director of the Reconfigurable Computing Laboratory (RCL). Prior to joining ISU, he was with Northwestern University, Evanston, IL, USA. While with Northwestern University, he was a recipient of the National Science Foundation (NSF) Graduate Research Fellowship, the Northwestern University Graduate School Fellowship, the Walter P. Murphy Fellowship, and the EECS Department Best Dissertation Award for his PhD dissertation titled "Compiler and Architectural Approaches to Software Protection and Security". He was a recipient of the NSF Career Award (2012), the ISU Award for Early Achievement in Teaching (2012), the College of Engineering Outstanding Achievement in Teaching Award (2019), and the ECpE Department's Warren B. Boast Undergraduate Teaching Award (2009, 2011, and 2016).

Email: zambreno@iastate.edu

Alberto Sanchez was born in Madrid, Spain, in 1986. He received his MSc degree in computer science engineering and PhD degree in computer science and telecommunication engineering from the Universidad Autónoma de Madrid, Madrid, in 2010 and 2013, respectively. He is currently an assistant professor at the Technology for Electronics and Communications Department, Universidad Autónoma de Madrid. He has published over 25 articles in peer-review journals. His current research interests include digital control of switching mode power supplies and the simulation of mixed digital and analog systems.

Email: alberto.sanchezgonzalez@uam.es

Angel de Castro (M'08, SM'21) received the MSc and PhD degrees in electrical engineering from the Universidad Politecnica de Madrid, Madrid, Spain, in 1999 and 2004, respectively. He started as an assistant professor in the Universidad Politecnica de Madrid in 2003. Then he moved to the Universidad Autonoma de Madrid in 2006, where he has been a professor since 2022. He is the director of the HCTLab (Hardware and Control Technology Laboratory) research group. He has published over 40 articles in peer-review journals. His research interests include digital control of switching mode power supplies, field programmable gate arrays, and hardware-in-the-loop (HIL).

Email: angel.decastro@uam.es