Faculty Vita: Promotion and Tenure

Date: 11/1/2015
Name: Phillip H. Jones III
Department: Electrical and Computer Engineering
Current Rank: Assistant Professor

I. Personal History and Professional Experience

A. Educational Background

- Washington University (St. Louis), PhD, Computer Engineering, May 2008
- University of Illinois (Urbana-Champaign), MS, Electrical Engineering, May 2002
- University of Illinois (Urbana-Champaign), BS, Electrical Engineering, May 1999

B. List of Academic Positions since Final Degree

8/2008 - Present: Assistant Professor, Iowa State University
2/2008 - 8/2008: Postdoc, Washington University (St. Louis)

C. Other Professional Employment

6/1996 - 8/2005, Summer Intern, Intel Corporation (Hillsboro, OR)
2/2002 - 8/2003, Intern, Intel Corporation (Chandler, AZ)
6/2001 – 8/2001, Summer Intern, Jet Propulsion Lab (Pasadena, CA)

D. Honors, Recognitions, and Outstanding Achievements

- Individual:
    - Warren B. Boast Undergraduate Teaching Award, Department of Electrical and Computer Engineering: 2014
    - Best Paper Award, IEEE International Conference on VLSI Design (VLSI Design): 2007
    - Graduate Engineering Minority (GEM) Fellowship: 1999-2000, 2003-2004
    - Intel Minority Scholarship: 1996-1999

- Student Advised Awards:
    - MemoCODE Design Competition: 1st place (international design competition): 2014
    - MemoCODE Design Competition: 1st place (international design competition): 2012

E. Formally Invited Lectures and Invited Conference Presentations

N/A

F. Offices Held in Professional Societies

N/A

G. Editorships of Journals or Other Learned Publications
N/A

H. Grants and Contracts Received Since Last Promotion at ISU

1. PI: Phillip Jones

   Title: "An FPGA-based Exploration and Feasibility Study of Hardware Approaches to Software Protection"
   Agency: Security and Software Engineering Research Center (S2ERC) with support from Boeing
   Dates: 9/2015 - 8/2016
   Amount: $40,000

2. Purpose: 15 High Performance Virtext-5 FPGAs

   PIs: Phillip Jones (with Joseph Zambreno)
   Company: Xilinx Corporation
   Dates: 2014
   Amount: equipment donation: commercial value $64,410

3. Xilinx Corporate equipment donation (with Joseph Zambreno)

   Dates: 2013
   Amount: 4 Zedboards for CPRE 488 course development: Commercial value $1,196

4. PI: Phillip Jones

   Co-PIs: Joseph Zambreno, Ron Cytron, Chris Gill, Nicola Elia
   Title: "An Adaptive Property-Aware HW/SW Framework for DDDAS"
   Agency: Air Force Office of Scientific Research (AFOSR)
   Dates: 9/2011 - 9/2013 (NCE to 9/2014)
   Amount: $299,987: $168,656 ISU share, Jones share: $67,000
   Roles & Responsibilities: Grant administration, provide research vision, advise supported PhD students (Chetan N-Govindaiah, Matt Rich).

5. PI: Phillip Jones

   Co-PIs: Joseph Zambreno, Ron Cytron, Chris Gill
   Title: "Seamless Integration of Conjoined Cyber-Physical System Properties"
   Agency: NSF: EArly Grants for Exploratory Research (EAGER)
   Dates: 10/2010 - 10/2013 (NCE to 12/2014)
   Amount: $299,917: $149,928 ISU share, Jones share: $74,964
   Roles & Responsibilities: Grant administration, provide research vision, advise supported PhD student (Sudhanshu Vyas).

6. PI: Phillip Jones

   Title: "Toward Mission Automation: Command and Control of Autonomous Vehicles through Advanced Human Computer Interfaces"
   Agency: NASA Iowa Experimental Program to Stimulate Competitive Research (EPSCoR) Research Fellowship
   Dates: 6/2010 - 8/2010
   Amount: $16,000
   Roles & Responsibilities: Create and strengthen contacts with NASA, guide research of one of my graduate students during their summer research fellowship at NASA, Ames, CA.

7. Xilinx Corporate equipment donation (with Joseph Zambreno)
   Dates: 2010
   Amount: 15 High Performance Virtext-5 FPGAs: Commercial value $57,268

8. ECpE Strategic Planning and Execution Committee (SPEC) funding: "Green Information Technology" (with Morris Change, Akhilesh Tyagi, Ahmed Kamal)
   Dates: 2010
   Amount: $30,000

9. Information Infrastructure Institute (ICube) internal funding: "Real-Time Management of Integrated Information, Physical, and Human Networks" (with Joseph Zambreno)
   Dates: 2009
   Amount: $5,000

I. Proposals for Grant and Contracts Pending

1. Title: "Computer Architecture Design for Deeply Embedded Control"
   PI: Phillip Jones
   Co-PIs: Nicola Elia, Joseph Zambreno
   Agency: NSF: Computer and Network Systems (CNS): Computer Systems Research (CSR)
   Submission date: 9/16/2015
   Amount: $1,213,943.00

2. Title: "WI-ECSEL Scholarship Program (Women in Electrical, Computer, and Software Engineering as Leaders)"
   PI: Joseph Zambreno
   Co-PIs: Diane Rover, Doug Jacobson, Mack Shelley, Sara Rajala, Lisa Larson, Phillip Jones, Mani Mina, Sarah Rodriquez,
   Agency: NSF: Division of Undergraduate Education (DUE): S-STEM
   Submission date: 9/22/2015
   Amount: $5,000,000: ISU share: 4,054,576

J. Proposals for Grants and Contracts not Funded Since Last Promotion at ISU.

1. Title: "IUSE/PFE:RED: Reinventing the Instructional and Departmental Enterprise (RIDE) to Advance the Professional Formation of Electrical and Computer Engineers
   PI: David Jiles
   Co-PIs: Diane Rover, Mani Mina, Phillip Jones, Joseph Zambreno
   Agency: NSF: EEC : Engineering Education
   Submission date: 11/26/2014
   Amount: $1,999,991

2. Title: "An Integrated Architecture, Real-time Systems, and Controls Design approach"
   PI: Phillip Jones
   Agency: NSF: Computer and Network Systems (CNS): Computer Systems Research (CSR)
   Submission date: 1/14/2015
   Amount: $503,799.00

3. Title: "Genomics Boost: Custom Hardware Acceleration Libraries for High-Throughput DNA Processing"
   PI: Phillip Jones
   Co-PIs: Joseph Zambreno
   Agency: NSF: Computer and Network Systems (CNS): Computer Systems Research (CSR)
   Submission date: 1/14/2015
   Amount: $514,190.00

4. Title: "CPS:Synergy:Collaborative Research: Control, Hardware, and Software Integration for Mixed-Criticality Cyber-Physical Systems"
   PI: Phillip Jones
   Co-PIs: Ron Cytron, Christopher Gill, Joseph Zambreno
   Agency: NSF: Cyber Physical Systems (CPS)
   Submission date: 6/2/2014
   Amount: $1,024,140: ISU share $415,400.00

5. Title: "Genomics Boost: Custom Hardware Acceleration Libraries for High-Throughput DNA Processing"
   PI: Phillip Jones
   Co-PI: Joseph Zambreno
   Agency: NSF: Computing and Communication Foundations (CCF): SW/HW Foundations (SHF)
   Submission date: 1/14/2014
   Amount: $511,062

6. Title: "TAURUS – Terrestrial Advanced UHF Radar on University SmallSat"
   Number of PIs: 7
   Agency: NASA: SmallSat Technology Partnerships CAN
   Submission date: 6/5/2013

Amount: $298,061

7. Title: “Cyber Physical Platform Design using a Holistic approach to Architecture, Real-time systems, and Controls”
   Number of PIs: 1
   Agency: NSF: Cyber Physical Systems (CPS)
   Submission date: 1/29/2013
   Amount: $494,470

8. Title: “A Computational Framework for Tightly Constrained Cyber-Physical Systems”
   Number of PIs: 4
   Agency: NSF: Cyber Physical Systems (CPS)
   Submission date: 1/29/2013
   Amount: $996,997: ISU share $550,210

9. Title: “Autonomous Robot for Complex Plant Phenotyping”
   Agency: NSF: National Robotics Initiative (NRI)
   Number of PIs: 5
   Submission date: 12/11/2012
   Amount: $1,021,344

10. Title: “Synergetic Micro-Robotics Laboratory (SMRL)”
    Number of PIs: 4
    Agency: NSF: Computing and Communication Foundations (CCF): CRI
    Submission date: 10/23/2012
    Amount: $440,000

11. Title: “Genomics Boost: Custom Hardware Acceleration Libraries for High-Throughput DNA Processing”
    Number of PIs: 2
    Agency: NSF: Computing and Communication Foundations (CCF): SW/HW Foundations (SHF)
    Submission date: 12/17/2012
    Amount: $495,598

12. Title: “An Adaptive Computational Stack for Highly Constrained Cyber-Physical Systems”
    Agency: NSF: Faculty Early Career Development (CAREER) Program
    Number of PIs: 1
    Submission date: 7/23/2012
    Amount: $401,961

13. Title: High-Assurance Cyber Military Systems (HACMS)
    Agency: DARPA
    Number of PIs: Senior Personal
    Submission date: 4/10/2012
    Amount: $4,555,020

14. Title: “Autonomous Robotic Platforms to Assist Plant Phenomics”
    Agency: NSF: National Robotics Initiative (NRI)

Number of PIs: 4
Submission date: 11/3/2011
Amount: $998,240

15. Title: “Energy Management using a Reliable and Aggressive Framework”
    Agency: NSF: Computing and Communication Foundations (CCF)
    Number of PIs: 2
    Submission date: 9/29/2011
    Amount: $603,121

16. Title: “Hardware Architecture Support for Small Autonomous Vehicles”
    Agency: NSF: Faculty Early Career Development (CAREER) Program
    Number of PIs: 1
    Submission date: 7/25/2011
    Amount: $402,306

17. Title: “RAKSHA: Reliable and Aggressive frameworK for System design using High Integrity Approaches”
    Agency: NSF: Computing and Communication Foundations (CCF)
    Number of PIs: 2
    Submission date: 9/14/2010
    Amount: $810,263

18. Title: “RA-CAS^{2}T: Reconfigurable Architecture Customization and Adaptation for Small Scale Technologies”
    Agency: NSF: Faculty Early Career Development (CAREER) Program
    Number of PIs: 1
    Submission date: 7/20/2010
    Amount: $409,665

19. Title: “Seamless Integration of Conjoined Cyber-Physical System Properties”
    Agency: NSF: Cyber Physical Systems (CPS)
    Number of PIs: 4
    Submission date: 3/11/2010
    Amount: $695,869

20. Title: “A Reconfigurable Autonomous Vehicle Infrastructure (RAVI) based on Field Programmable Gate Array Technology”
    Agency: NFS: Broadening Participation in Engineering (BRIGE)
    Number of PIs: 1
    Submission date: $170,843
    Amount: 2/25/2010

21. Title: “Toward Mission Automation: Command and Control of Autonomous Vehicles through Advanced Human Computer Interfaces”
    Agency: NASA EPSCoR (Iowa NASA EPSCoR selection competition semi-finalist)
    Number of PIs: 1 (coordinating NASA Ames, Boeing, John Deere, Rockwell Collins, VRAC)
    Submission date: 11/30/2009

Amount: $1,380,000

22. Title: “Seamless Integration of Conjoined Cyber-Physical System Properties”
    Agency: NSF: Cyber Physical Systems (CPS)
    Number of PIs: 4
    Submission date: 2/27/2009
    Amount: $644,224

K. Grant Review Panels

1. NSF Panelist, Cyber Physical Systems (CPS) – Break Through: July 2012
2. NSF Panelist, Computer & Information Science & Engineering (CISE) - Computing Research Infrastructure (CRI): January 2012
3. NSF Panelist, Computer and Network Systems (CNS) - Computer Systems Research (CSR): May 2011

L. Policy, Advisory or Corporate Panels or Boards (e.g., for Governmental Agencies, Educational Institutions, Companies)

N/A

II. PUBLICATIONS AND CREATIVE WORKS

A. Doctoral thesis title

Optimizing application performance using temperature feedback
by *Jones, Phillip H., III*, Ph.D.,
Washington University in St. Louis, 2008

B. Books Authored or Co-Authored
N/A

C. Books Edited or Co-Edited
N/A

D. Chapters in Books (in print or accepted)
N/A

E. Monographs (in print or accepted)
N/A

F. Articles in Journals (in print or accepted)

1. RAMPS: A Reconfigurable Architecture for Minimal Perfect Sequencing,
by C. Nelson, K. Townsend, O. Attia, P. Jones, and J. Zambreno;
IEEE Transactions on Parallel and Distributed Systems (TPDS), (Accepted with minor revision)

2. A Scalable Unsegmented Multi-port Memory for FPGA-based Systems,
by K. Townsend, O. Attia, P. Jones and J. Zambreno;
International Journal of Reconfigurable Computing (IJRC) (Accepted with minor revision)

3. A Reconfigurable Architecture for the Detection of Strongly Connected Components,
by O. Attia, P. Jones, J. Zambreno;
ACM Transactions on Reconfigurable Technology and Systems (TRETS) (To appear)

4. A Configurable Architecture for Sparse LU Decomposition on Matrices with Arbitrary Patterns,
by X. Wang, P. Jones and J. Zambreno;
ACM SIGARCH Computer Architecture News (To appear).

5. A Fault-aware Toolchain Approach for FPGA Fault Tolerance,
by Adwait Gupte, Sudhanshu Vyas and Phillip Jones;
ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 20, no. 2, 2015

6. An FPGA Architecture for the Recovery of WPA/WPA2 Keys,
by T. Johnson, D. Roggow, P. Jones and J. Zambreno;
Journal of Circuits, Systems, and Computers (JCSC), vol. 24, no. 7, 2015

7. Hardware-Software Architecture for Priority Queue Management in Real-time and Embedded Systems,
by C. Kumar, S. Vyas, J. Shidal, R. Cytron, C. Gill, J. Zambreno and P. Jones;
International Journal of Embedded Systems(IJES), vol. 6, no. 4 pp. 319-334, 2014

8. An FPGA-based Plant-on-Chip Platform for Cyber-Physical System Analysis,
by S. Vyas, C. Kumar, J. Zambreno, C. Gill, R. Cytron, P. Jones;
IEEE Embedded Systems Letters (ESL), vol. 6, no 1., pp. 4-7, 2014

9. Hardware Architectural Support for Control Systems and Sensor Processing,
by Sudhanshu Vyas, Adwait Gupte, Christopher Gill, Ron Cytron, Joseph Zambreno, Phillip H. Jones;
ACM Transactions on Embedded Computing Systems (TECS), vol. 13, no. 2, 2013

10. An I/O Bandwidth-Sensitive Sparse Matrix-Vector Multiplication Engine on FPGAs,
by S. Sun, M. Monga, P. Jones, and J. Zambreno; I
IEEE Transactions on Circuits and Systems-I (TCAS-I), Volume 59, no. 1, January 2012, Pages 113-123.

11. Extracting and Improving Microarchitecture Performance on Reconfigurable Architectures,
by Shobana Padmanabhan, Phillip Jones, David V. Schuehler, Scott J. Friedman, Praveen Krishnamurthy, Huakai Zhang, Roger Chamberlain, Ron K. Cytron, Jason Fritts, and John W. Lockwood;
International Journal of Parallel Programming, Volume 33, Issue 2 - 3, June 2005, Pages 115 - 136.

12. The Effects of an ARMOR-based SIFT Environment on the Performance and Dependability of User Applications,
by K. Whisnant, R.K. Iyer, Z.T. Kalbarczyk, P.H. Jones III, D.A. Rennels, R. Some;
IEEE Transactions on Software Engineering (TSE), Volume 30, Issue 4, April 2004, Pages 257 - 277.

G. Creative Works

N/A

H. Highly Competitive **(<= 34% Acceptance Rate)** Conference Proceedings that have undergone stringent editorial review by peers

13. A Software Configurable and Parallelized Coprocessor for LQR Control,
by Pei Zhang, Aaron Mills, Joseph Zambreno, and Phillip H. Jones
IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig), Cancun, Mexico, December, 2015. **(Acceptance Rate 34%)**

14. A Software Configurable Coprocessor-Based State-Space Controller,
by Aaron Mills, Pei Zhang, Sudhanshu Vyas, Joseph Zambreno, and Phillip H. Jones
IEEE International Conference on Field Programmable Logic and Applications (FPL), London, England, September, 2015. **(Acceptance Rate 22%)**

15. A Reconfigurable Architecture for QR Decomposition Using A Hybrid Approach,
by X. Wang, P. Jones and J. Zambreno;
Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July, 2014
(Acceptance Rate 32.3%)

16. CyGraph: A Reconfigurable Architecture for Parallel Breadth-First Search,
by O. Attia, T. Johnson, K. Townsend, P. Jones and J. Zambreno;
Proceedings of the Reconfigurable Architectures Workshop (RAW), Phoenix, AZ, May, 2014 (**Acceptance Rate 28.8%**)

17. Design and Evaluation of a Delay-Based FPGA Physically Unclonable Function,
by A. Mills, S. Vyas, M. Patterson, C. Sabotta, P. Jones and J. Zambreno;
Proceedings of the International Conference on Computer Design (ICCD), September, 2012.
(Acceptance Rate 25%)

18. Shepard: A Fast Exact Match Short Read Aligner,
by C. Nelson, K. Townsend, B S. Rao, P. Jones and J. Zambreno;
Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE), July, 2012 **(Acceptance Rate 32%**: included in proceedings as design competition champion)

19. Circumventing a Ring Oscillator Approach to FPGA-Based Hardware Trojan Detection ,
by J. Rilling, D. Graziano, J. Hitchcock, T. Meyer, X. Wang, P. Jones and J. Zambreno;
Proceedings of the International Conference on Computer Design (ICCD), October, 2011
(Acceptance Rate 28%)

20. Teaching Graphics Processing and Architecture using a Hardware Prototyping Approach ,
by M. Steffen, P. Jones and J. Zambreno;
Proceedings of the International Conference on Microelectronic Systems Education (MSE), June, 2011 **(Acceptance Rate 24%)**

21. An Evaluation of a Slice Fault Aware Tool Chain ,
by Adwait Gupte, and Phillip Jones;
Proceedings of Design, Automation, and Test in Europe (DATE), Dresden, Germany, Mar 8-12, 2010. **(Acceptance Rate 30%)**

22. Hotspot Mitigation using Dynamic Partial Reconfiguration for Improved Performance ,
by Adwait Gupte, and Phillip H. Jones;
IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig), Cancun, Mexico, Dec 9-11, 2009. **(Acceptance Rate 32%)**

23. Adaptive Thermoregulation for Applications on Reconfigurable Devices,
by Phillip H. Jones, James Moscola, Young H. Cho, and John W. Lockwood;
IEEE International Conference on Field Programmable Logic and Applications (FPL), Amsterdam, Netherlands, Aug 27-29, 2007. **(Acceptance Rate 21%)**

24. Dynamically Optimizing FPGA Applications by Monitoring Temperature and Workloads,
by Phillip H. Jones, Young H. Cho, and John W. Lockwood;
IEEE International Conference on VLSI Design (VLSI Design), Bangalore, India, Jan 6-10, 2007. **(Acceptance Rate 32%)**
(Best Paper Award)

25. An Adaptive Frequency Control Method Using Thermal Feedback for Reconfigurable Hardware Applications,
by Phillip H. Jones, Young H. Cho, and John W. Lockwood;
IEEE International Conference on Field Programmable Technology (FPT), Bangkok, Thailand, Dec 13-15, 2006. **(Acceptance Rate 20%)**

26. A Thermal Management and Profiling Method for Reconfigurable Hardware Applications,
by Phillip H. Jones, John W. Lockwood, and Young H. Cho;
IEEE International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, Aug 28-30, 2006. **(Acceptance Rate 30%)**

27. An Experimental Evaluation of the REE SIFT Environment for Spaceborne Applications,
by K. Whisnant, R.K. Iyer, P. Jones, R. Some, D. Rennels;
International Conference on Dependable Systems and Networks (DSN), Washington, D.C., USA, 2002 **(Acceptance Rate 31%)**

28. NFTAPE: Networked Fault Tolerance and Performance Evaluator,
by D. Stott, P.H. Jones, M. Hamman, Z. Kalbarczyk, R.K. Iyer;
International Conference on Dependable Systems and Networks (DSN), Washington, D.C., USA, 2002 **(Acceptance Rate 31%)**

I. Conference Proceedings that have undergone stringent editorial review by peers

29. Accelerating All-Pairs Shortest Path Using A Message-Passing Reconfigurable Architecture,
by Osama Attia, Alex Grieve, Kevin Townsend, Phillip H. Jones and Joseph Zambreno
IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig), Cancun, Mexico, December, 2015, 2015. (Short paper)

30. A Project-Based Embedded Systems Design Course Using a Reconfigurable SoC Platform,
by D. Roggow, P. Uhing, P. Jones and J. Zambreno;
Proceedings of the International Conference on Microelectronic Systems Education (MSE), May, 2015.

31. k-NN Text Classification using an FPGA-Based Sparse Matrix Vector Multiplication Accelerator,
by K. Townsend, S. Sun, T. Johnson, O. Attia, P. Jones and J. Zambreno;
Proceedings of the IEEE International Conference on Electro/Information Technology (EIT), May, 2015.

32. Cache Design for Mixed Critical Real-Time Systems,
by C. Kumar, S. Vyas, R. Cytron, C. Gill, J. Zambreno and P. Jones;
Proceedings of the International Conference on Computer Design (ICCD), Seoul, Korea, October, 2014 **(Acceptance Rate 37.6%)**

33. A High Performance Systolic Architecture for k-NN Classification,
by K. Townsend, P. Jones and J. Zambreno;
Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE), Lausanne, Switzerland, October, 2014 **(Acceptance Rate 42.5%**)

34. Design and Implementation of an H-infinity Controller for a Quadrotor Helicopter,
by M. Rich, N. Elia, P. Jones;
21st Conference on Control & Automation (MED), IBSN: 978-1-4799-0995-7, pp. 1189-1198, June 2013.

35. Scheduling Challenges in Mixed Critical Real-time Heterogeneous Computing Platforms,
by C. Kumar, S. Vyas, R. Cytron, C. Gill, J. Zambreno and P. Jones;
Proceedings of the International Conference on Computational Science (ICCS), *Dynamic Data Driven Application Systems (DDDAS) Workshop*, pp. 1891-1898, June, 2013.

36. Introducing Graphics Processing from a Systems Perspective: A Hardware / Software Approach,
by M. Steffen, P. Jones, J. Zambreno;
Proceedings of the Annual Conference of American Society for Engineering Education (ASEE), June, 2012

37. Improving System Predictability and Performance via Hardware Accelerated Data Structures,
by C. Kumar, S. Vyas, J. Shidal, R. Cytron, C. Gill, J. Zambreno and P. Jones,
Proceedings of the International Conference on Computational Science (ICCS), Dynamic Data Driven Application Systems (DDDAS) Workshop, June, 2012.

38. Characterizing Non-Ideal Impacts of Reconfigurable Hardware Workloads on Ring Oscillator-based Thermometers,
by Moinuddin Sayed and Phillip Jones;
IEEE International Conference on Reconfigurable Computing and FPGAs (Reconfig), Cancun, Mexico, Nov 3-Dec 2, 2011. **(Acceptance Rate 35%)**

39. Towards Hardware Support for Common Sensor Processing Tasks ,
by Adwait Gupte, and Phillip Jones;
15th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA) , Beijing, China, August 2009. **(Acceptance Rate: 47%)**

40. Changing Output Quality for Thermal Management,
by Phillip H. Jones, James Moscola, Young H. Cho, John W. Lockwood;
IEEE International Symposium on Field-Programmable Custom Computing Machines(FCCM), Napa Valley, CA, April 2007. (short paper)

41. Cycle-Accurate Microarchitecture Performance Evaluation,
by Richard Hough, Phillip Jones, Scott Friedman, Roger Chamberlain, Jason Fritts, John Lockwood, Ron Cytron;
IEEE Workshop on Introspective Architecture (WISA), Austin, TX, February 2006.

42. Use of a Soft-Core Processor in a Hardware/Software Codesign Laboratory,
by Roger Chamberlain, John Lockwood, Saurabh Gayen, Richard Hough, and Phillip Jones;
IEEE Intl. Conf. on Microelectronic Systems Education, June, 2005.

43. Extracting and Improving Microarchitecture Performance on Reconfigurable Architectures, by Shobana Padmanabhan, Phillip Jones, David V. Schuehler, Scott J. Friedman, Praveen Krishnamurthy, Huakai Zhang, Roger Chamberlain, Ron K. Cytron, Jason Fritts, and John W. Lockwood;
International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), Workshop on Compilers and Tools for Constrained Embedded Systems (CTCES), Washington DC, September 22, 2004.

J. Bulletins, Reports, or Conference Proceedings That Have Not Undergone Stringent Editorial Review by Peers

44. Team [Ii][Ss][Uu][0-2]\{4\} Design Overview: MEMOCODE 2010 Design Contest, by Sudhanshu Vyas, Pooja Mhapsekar, Aditya Ashok, Moinuddin Sayed, Avinash Srinivasa, Gunjan Pandey, Adam Jackson, Matthew Nelson, Anand Saggi, Harini Sundararaman, Phillip H. Jones;
8th IEEE/ACM International Conference on Formal Methods and Models for Codesign (MEMOCODE), Grenoble, France, July 2010.

45. CANSCID-CUDA,
by Michael Steffen, Veerendra Allada, Phillip Jones and Joseph Zambreno;
8th IEEE/ACM International Conference on Formal Methods and Models for Codesign (MEMOCODE), Grenoble, France, July 2010.

46. Liquid Architecture,
by Phillip Jones, Shobana Padmanabhan, Daniel Rymarz, John Maschmeyer, David V. Schuehler, John W. Lockwood, and Ron K. Cytron;
IEEE International Parallel and Distributed Symposium (IPDPS), Next Generation Software (NGS) Workshop, Santa Fe, New Mexico, April 26, 2004.

K. Abstracts Technical Presentations

N/A

L. Book and Paper Reviews

N/A

M. Patents, Disclosures and Technology Transfer Activities

N/A

N. Consulting Activities

N/A

O. Other (Publications Under Review)

47. A Cache Architecture for Mixed Criticality Real-Time Systems,
by C. Kumar, S. Vyas, R. Cytron, C. Gill, J. Zambreno and P. Jones;
ACM Transactions on Embedded Computing Systems (TECS), (Under review)

P. Publications and Creative Works Submitted but Not Accepted:

III. INSTRUCTION AND SUPERVISION

A. Instruction for ISU

- Embedded Systems Design: CPRE 488 (Spring 2014), 4 credits (3-3)
  (1 Lecture section = 12 students)
  (Teaching Eval: 4.5/5.0, std: .90, # replies 12/12)

- Introduction to Embedded Systems: CPRE 288 (Spring 2015), 4 credits (3-2)
  (1 Lecture section = 90 students)
  (Teaching Eval: 4.13/5.0, std: .71, # replies 52/90)

- Introduction to Embedded Systems: CPRE 288 (Fall 2014), 4 credits (3-2)
  (1 Lecture section = 47 students)
  (Teaching Eval: 4.48/5.0, std: .92, # replies 29/47)

- Introduction to Embedded Systems: CPRE 288 (Spring 2014), 4 credits (3-2)
  (1 Lecture section = 67 students)
  (Teaching Eval: 4.3/5.0, std: .81, # replies 47/67)

- Embedded Systems Design: CPRE 488 (Spring 2014), 4 credits (3-3)
  (1 Lecture section = 27 students)
  (Teaching Eval: 4.52/5.0, std: .95, # replies 23/27)

- Introduction to Embedded Systems: CPRE 288 (Fall 2013), 4 credits (3-2)
  (1 Lecture section = 50 students)
  (Teaching Eval: 4.79/5.0, std: .5, # replies 28/50)

- Introduction to Embedded Systems: CPRE 288 (Summer 2013), 4 credits (3-2)
  (1 Lecture section = 35 students)
  (Teaching Eval: 4.5/5.0, std: .99, # replies 18/35)
  Note: 29/35 students were EE's

- Models and Techniques in Embedded Systems: CPRE 584 (Spring 2013), 3 credits
  (8 students)
  (Teaching Eval: 4.67/5.0, std: .71, # of replies 9/10)

- Introduction to Embedded Systems: CPRE 288 (Spring 2013), 4 credits (3-2)
  (1 Lecture section = 142 students)
  (Teaching Eval: 4.01/5.0, std: 1.0, # replies 75/142)

- Introduction to Embedded Systems: CPRE 288 (Fall 2012), 4 credits (3-2)
  (1 Lecture section = 48 students)
  (Teaching Eval: 4.48/5.0, std: .79, # replies 23/48)

- Models and Techniques in Embedded Systems: CPRE 584 (Spring 2012), 3 credits
  (8 students)
  (Teaching Eval: 4.75/5.0, std: .46, # of replies 7/8)

- Introduction to Embedded Systems: CPRE 288 (Fall 2011), 4 credits (3-2)
  (1 Lecture section = 45 students)
  (Teaching Eval: 4.42/5.0, std: .83, # replies 26/45)

- Reconfigurable Computing: CPRE 583 (Fall 2011), 3 credits
  (15 Students = 9 on campus + 6 Distance Education)
  (Teaching Eval: 5.0/5.0, std: 0.0, # replies 9/9)

- Introduction to Embedded Systems(Jones:Course Advisor, Chad Nelson:Taught):CPRE 288 (Summer 2011), 4 credits (3-2)
  (29 students)
  (Eval: N/A)

- Introduction to Embedded Systems (Lab instructor): CPRE 288 (Spring 2011), 4 credits (3-2)
  (3 Lab sections = 23 (with 1 TA) + 18 + 17 = 58)
  (Teaching Eval: 4.63, std: .43, # of replies 46/58)

- Reconfigurable Computing: CPRE 583 (Fall 2010), 3 credits
  (20 Students = 14 on campus + 6 Distance Education)
  (Teaching Eval: 4.91/5.0, std: .30, # of replies 11/14)

- Models and Techniques in Embedded Systems: CPRE 584X (Spring 2010), 3 credits
  (10 students)
  (Teaching Eval: 4.89/5.0, std: .33, # of replies 9/10)

- Reconfigurable Computing: CPRE 583 (Fall 2009), 3 credits
  (16 Students = 14 on campus + 2 Distance Education)
  (Teaching Eval: 4.58/5.0, std: .50, # of replies 13/14)

- Embedded Systems Research Skills: CPRE 594 (Now CPRE 584X)(Spring 2009, Co-taught with Joseph Zambreno), 3 credits
  (9 students)
  (Teaching Eval: 4.83/5.0, std: .41, # of replies 6/9)

- Reconfigurable Computing: CPRE 583 (Fall 2008), 1/4 TA, 3 credits
  (21 students = 11 on campus + 10 Distance Education)
  (Teaching Eval: 4.18/5.0, std: 1.08, # of replies 11/11)

B. Non-ISU Instruction

Washington University in St. Louis: Introduction to Computing Tools: CSE100 (Fall 2007)

C. Curricular Development Activity

- Embedded Systems Design CPRE 488 (Summer 2013)
    - Reworking course to update lab infrastructure and lectures
    - Integrating micro-Unmanned Aerial Vehicles (UAVs)
    - Collaboration with Joseph Zambreno

- Introduction to Embedded Systems CPRE 288 (Summer 2013):
    - Upgrading lab infrastructure and reworking lectures
    - Collaboration with Zhao Zhang, and Akhilesh Tyagi

- Models and Techniques in Embedded Systems CPRE 584X (Spring 2009)
    - New course co-developed with Joseph Zambreno

- Reconfigurable Computing CPRE 583 (Fall 2008):
    - Reworked course to add a major hands-on component.
    - Set up an infrastructure to allow distance students to participate equally well as on-campus students in the new hands-on component of the course

D. Supervision of Graduate Student Research for which Candidate is Primary Advisor or Co-Advisor

- Pei Zhang, PhD, Aug 2014 - Present, (PhD qualification: planned Spring 2016)
    - Supported by : Department Teaching Assistantship.

- Murad Qasaimeh, PhD, Aug 2015 - Present, (PhD qualification: planned Spring 2017)
    - Supported by : Department Teaching Assistantship.

- Matthew Nelson, MS, May 2010 - Present, (degree expected December 2015)

- N-Govindaiah, Chetan, PhD, Aug 2011 – December 2015
    - "Hardware Architecture Support for Mixed Criticality and Real-Time Systems"
    - Supported by the "An Adaptive Property-Aware HW/SW Framework for DDDAS", Air Force Office of Scientific Research (AFOSR) to 12/2015.
    - Nvidia, Portland, OR

- Sudhanshu Vyas, PhD, Jan 2010 - December 2015
    - "Design Exploration of Hardware Accelerators for Mitigating the Effects of Computational Delay on Digital Control Loops"
    - Supported by the "Seamless Integration of Conjoined Cyber-Physical System Properties", NSF EAGER to 5/2014.

- Pooja Mhapsekar, MS, Jan 2010 - May 2013
    - "FPGA-based Acceleration of the RMAP Short Read Mapping Tool"
    - Currently working at Micron

- Moinuddin Sayed, MS, Jan 2010 – Dec 2012
    - "Mitigating impacts of Workload Variation on Ring Oscillator-based Thermometers"
    - Currently working at NetApp Inc., Boulder CO

- Adwait Gupte, MS, Jan 2009 - May 2011
    - "A Slice Fault-aware Toolchain for FPGAs"
    - Currently working at Algo-Logic

- Ejiofor Odo, MS with Creative Component, Distance Education from Intel Corporation
    - Graduated December 2009
    - Advised final two semesters of Creative Component

- Ben Armfield, MS with Creative Component, Distance Education from Rockwell Collins
    - Graduated December 2008
    - Advised final semester of Creative Component

E. Service on Thesis Committees Other than Own Advisees

PhD committees: Gang Wu, Aaron Mills, Osama Attia, Jungmin Park, Matt Rich, Elizabeth, Amit Pande, Avinash Srinivasa, Prasad Avirneni, Ji Li, Vaibhav Sundriyal, Mihir Awatramani, Chad Nelson, Kevin Townsend, Pavan Kumar

MS committees: Ashish Daga, Ravi, Yasa, Matt Rich, Mengduo Ma, Kiran Tondehal, Alex Baumgarten, Adam Jackson, Jay Roltgen, Matthew Clausman

F. Supervision of Post-Doctoral Students and Professional Staff

N/A

G. Supervision of Undergraduate Research and Independent Study
- Modeste Kenne, Quinn Murphy, Joe Avey, Brian Anderson: 2015
- Matt Vitale, Paul Danner: 2014
- Nathan Hemmings, James Honzatko, Kevin Engel, Paul Danner: 2013
- Nathan Hemmings, Damek Svec: 2012

H. Other Contributions to Instructional Programs
Senior Design Advisor:
- Microprocessor Controlled Aerial Robotics Team (F2015 – S2016)
    - Joseph Avey, Amy Seibert, Cal Fisher, John Eganhouse, Garrett Lassek, Shemin Gong (Co-advise with Nicola Elia)

- Aerial Land Inspection System (ALIS) (F2015 – S2016)
    - Quinn Murphy, Brian Gillenwater, Jonathan Schlueter, Bryce Poellet, Nathan Kent (Co-advise with Joseph Zambreno)

- Video Display MicroZed (F2015 – S2016)
    - Trevor Goodpasture, Joe Jiang, Kai Ching (Co-advise with Joseph Zambreno)

- Microprocessor Controlled Aerial Robotics Team (F2014 – S2015)
    - Matt Vitale, Paul Gerver, Jacob Rigdon, Tyler Kurtz, Joe Benedict, Adam Campbell, Ravi Nagaraju, Matt Post (Co-advise with Nicola Elia)

- Plant Cooperative Robotics Team (OmniCoor) (F2014 – S2015)
    - Alberto Di Martino, Dylan Gransee, Robert Larsen, Ian McInerney, Aaron Pederson, Rohit Zambre, Fengxing Zhu (Co-advise with Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2013 – S2014)
    - Kevin Engel, Nathan Ferris, William Franey, Michael Johnson, Kelsey Moore, Lucas Mulkey, Aaron Peterson (Co-advise with Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2012 – S2013)
    - Rachana Kaul, James Honzatko, Christina Kuhfal, Collin Bartels, Alex Sturgeon, Andria Osborne, Alex Denny,Mathew Huss(Co-adviser Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2011 – Spring 2012)
    - Jeff Wick, Peter Ha, Victor Lin, Pengqing Xie (Co-advise with Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2010 - S2011)
    - Jared Hagemann, Roy Lycke, Kyle Teske, Preston Webster, Shibing Zhao (Co-advise with Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2009 - S2010)
    - Kollin Moore, Michael Peat, Alex Reifert, Matt Rich (Co-adviser Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (S2009 - F2010)
    - Andrew Erdman, Taoran Li, Chris Sade (Co-advise with Nicola Elia)

- Microprocessor Controlled Aerial Robotics Team (F2008 - S2009)
    - Wade Paustain, Muhammad Ali Riaz, Jay Roltgen, Kyle Rutledge, Ryan Steffens (Co-advise with Nicola Elia)

- Power over Ethernet (PoE) (F2012- Present)
    - Eric Greenley, John Ryan, Michael Carter, Stephen Brossart, Matthew Boyce

- Virtual Pinball Experience (F2011- S2012)
    - Kevin Pope, Steven Bruening, MatthewDavid Grove, Max Mayfield, Michael Yeager (Co-advise with Joseph Zambreno)

- FPGA-based Arcade Emulation System (F2010–S2011)
    - David Gartner, John Alexander, Danny Funk, Tony Milosch, Cory Mohling (Co-advise with Joseph Zambreno)

- FPGA-based Emulation of the Nintendo Entertainment System (F2009 - S2010)
    - Ashley Good, David Graziano, Tim Meyer, Matt Saladin (Co-Adiser Joseph Zambreno)

IV. SERVICE (PUBLIC, PROFESSIONAL/DISCIPLINARY, AND UNIVERSITY)

A. Public Service

- United Way Volunteer, Reading to Kindergarten - 2nd graders: 2013, 2014, 2015
- State Science + Technology Fair of Iowa, Judge: 2015

B. Service to Disciplinary and Professional Societies or Associations

Grant Review Panels:

- NSF Panelist, Cyber Physical Systems (CPS) – Break Through: July 2012
- NSF Panelist, Computer & Information Science & Engineering (CISE) - Computing Research Infrastructure (CRI): January 2012
- NSF Panelist, Computer and Network Systems (CNS) - Computer Systems Research (CSR): May 2011

Conference Organization:

- Program committee member: IEEE International Conf. on Reconfigurable Computing and FPGAs(ReConFig) : 2014, 2015
- Co-chair of Systems track: International Conference on Contemporary Computing (IC3): 2011

Journal and Conference paper reviewer:

- IEEE Transactions on Computers (TC): 2008, 2013, 2014
- ACM Transactions on Reconfigurable Technology and Systems (TRETS): 2013
- IEEE Transactions on Parallel and Distributed Systems (TPDS): 2013, 2014
- IEEE International Conf. on Reconfigurable Computing and FPGAs(ReConFig): 2014, 2015
- IEEE Midwest Symposium on Circuits and Systems (MWSCAS): 2014
- IEEE International Conference on Networking, Architecture, and Storage(NAS): 2013
- IEEE International Parallel and Distributed Symposium (IPDPS): 2009, 2012
- Embedded Hardware Design (MICPRO): 2008, 2009, 2010, 2011, 2014
- ACM Transactions on Design Automation of Electronic Systems (TODAES): 2011
- International Symposium on Circuits and Systems (ISCAS): 2011

C. University/Campus Service

N/A

D. Other Service

Department level service:

- Senior Design Advisor: Fall 2008 - Present
- IEEE student chapter advisor: Fall 2013 - Present
- Graduate College Diversity and Inclusion Workshop: ECE Faculty Representative: 2013
- ABET subcommittee for Rubric development Fall 2011
- Graduate Committee: Spring 2011 – Spring 2014
- Computer and Network Systems Area Chair: Spring 2011 – Spring 2014

- Curriculum Committee: Fall 2009 – Spring 2013, Fall 2015 - Present
- ECE Department Head Search Committee: Fall 2009 - Spring 2010
- Graduate Admission Committee: Fall 2008 - Spring 2009

Educational outreach service:

- IT-Olympics Programming Competition, volunteer: (2009, 2010, 2011, 2012, 2013, 2014, 2015)
- Leadership through Engineering Academic Diversity (LEAD):
    - Spoken at multicultural student meetings to encourage, and share experiences (2008, 2009, 2010,2011,2012,2013,2014, 2015)
    - Attended farewell dinners for recruiting prospective multicultural high school students (2009, 2010)
- Digital Women: Faculty Advisor (11/2012 – Present)
- Howard Hughes Medical Institute (HHMI) Project:
    - Hosted community college student in my laboratory: 2015

Miscellaneous:

- 24 hour IEEE Extreme Programming Competition, proctor (2010, 2011, 2012, 2013)