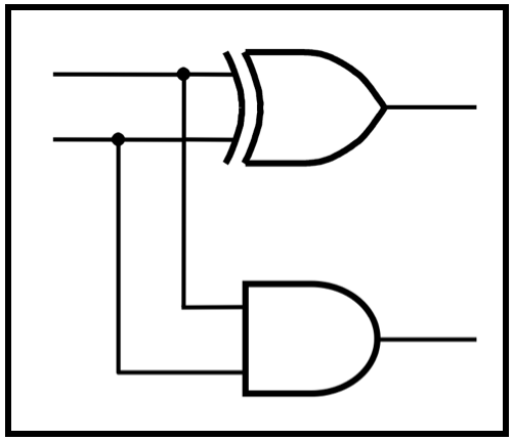


CprE 2810: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Mealy State Model

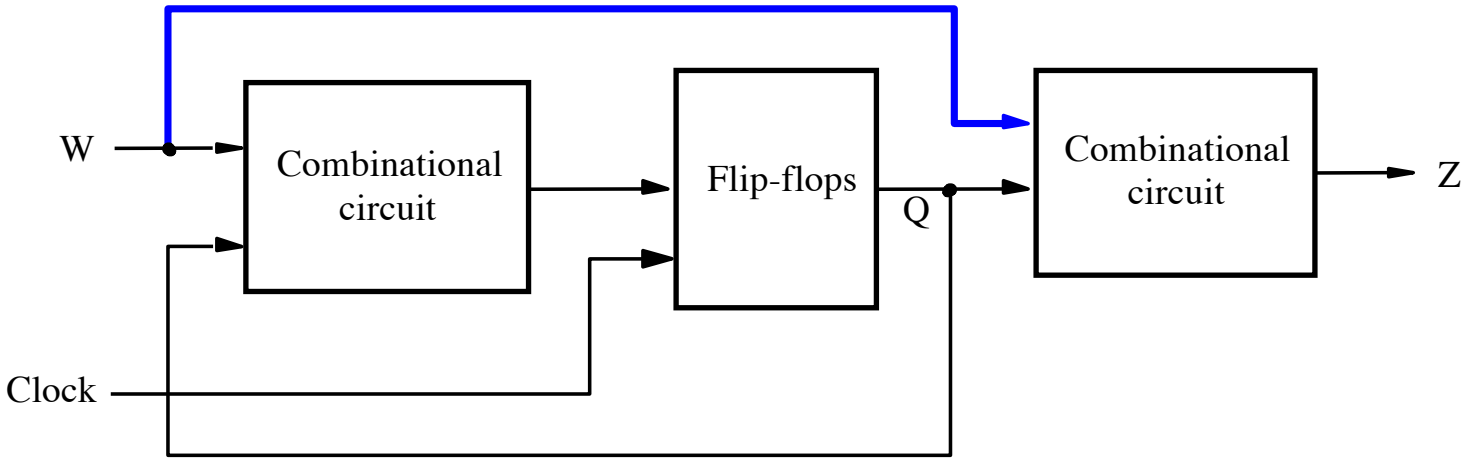
CprE 2810: Digital Logic
Iowa State University, Ames, IA

Administrative Stuff

- **Homework 10 is due on Monday Nov 10 @ 10 pm**

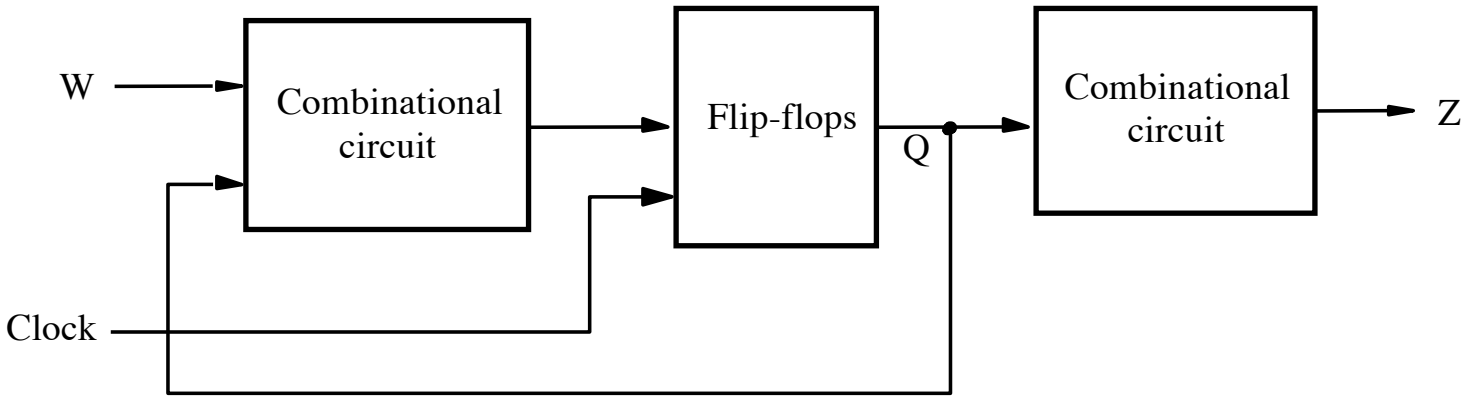
- **Homework 11 is due on Monday Nov 17 @ 10 pm**

The general form of a synchronous sequential circuit

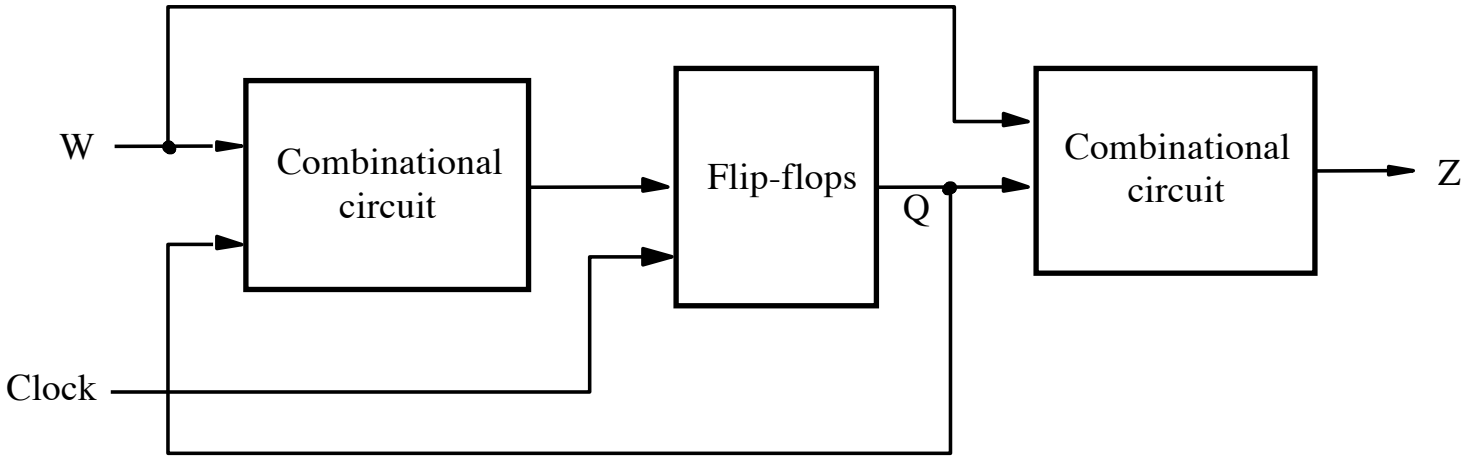


[Figure 6.1 from the textbook]

Moore Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Mealy Type

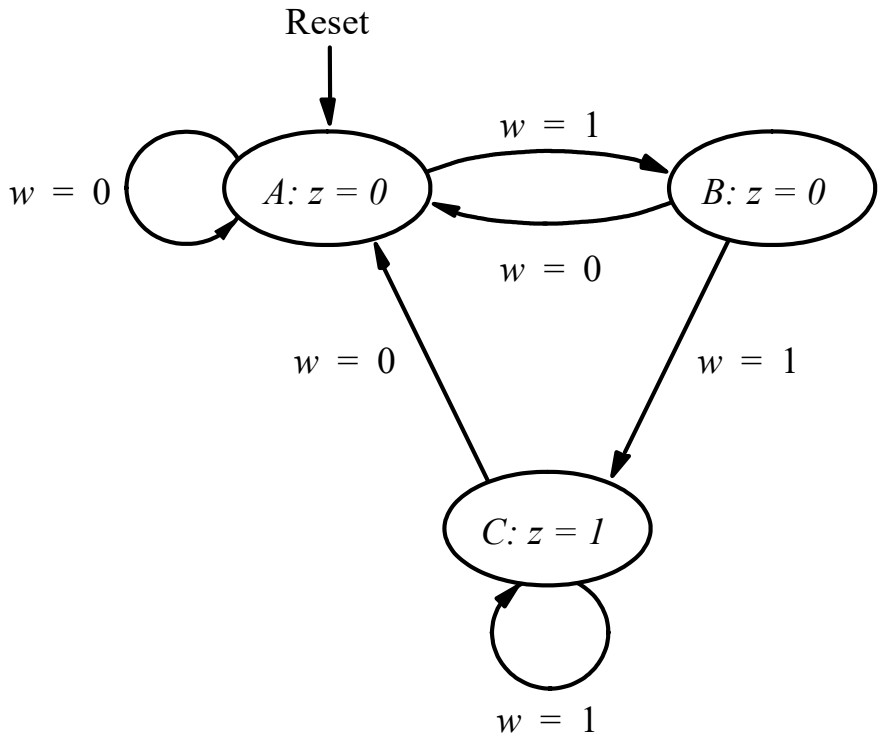

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Sample Problem

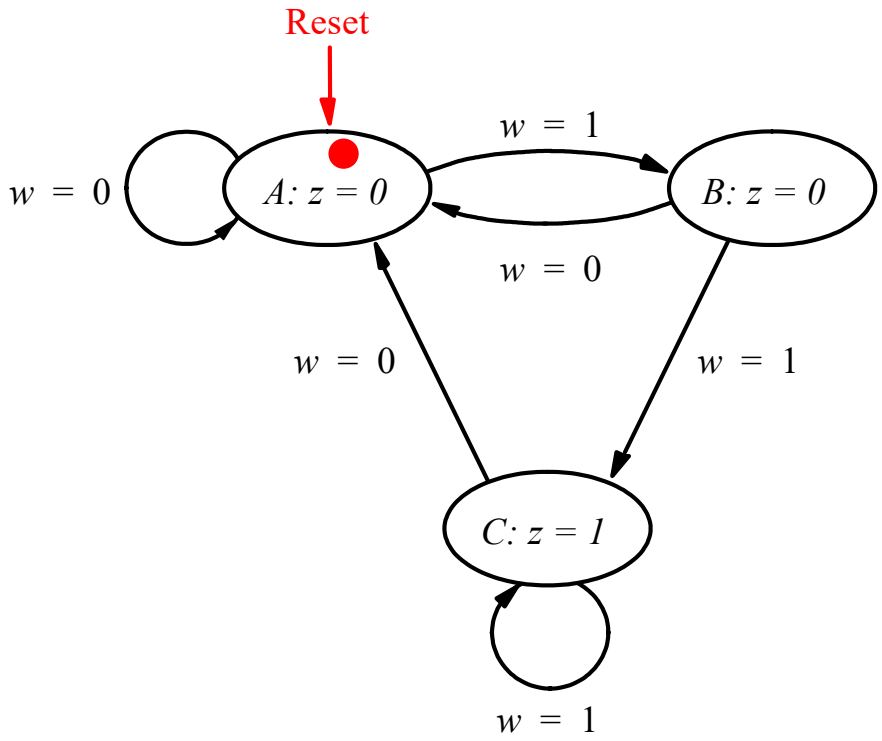
Implement a 11 detector. In other words, the output should be equal to 1 if two consecutive 1's have been detected on the input line.

The output should become 1 as soon as the second 1 is detected in the input.

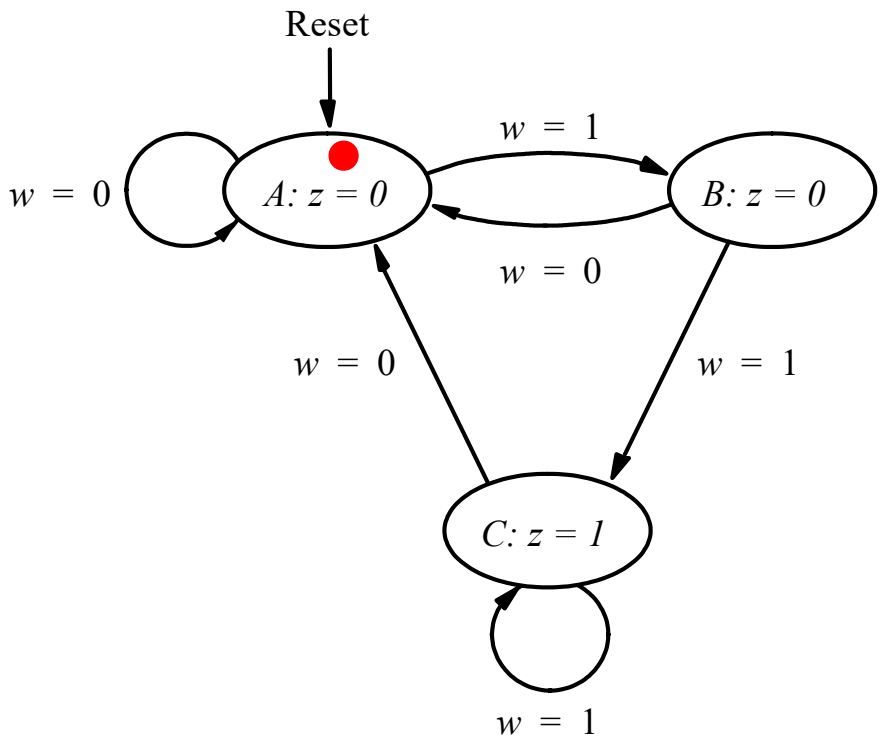
Moore Machine Implementation



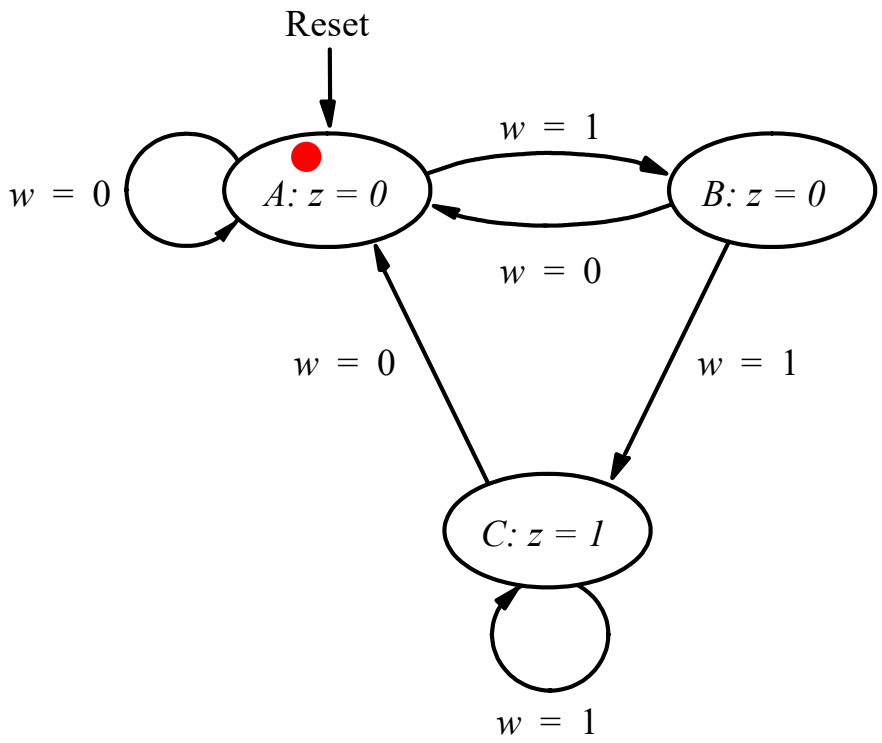
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



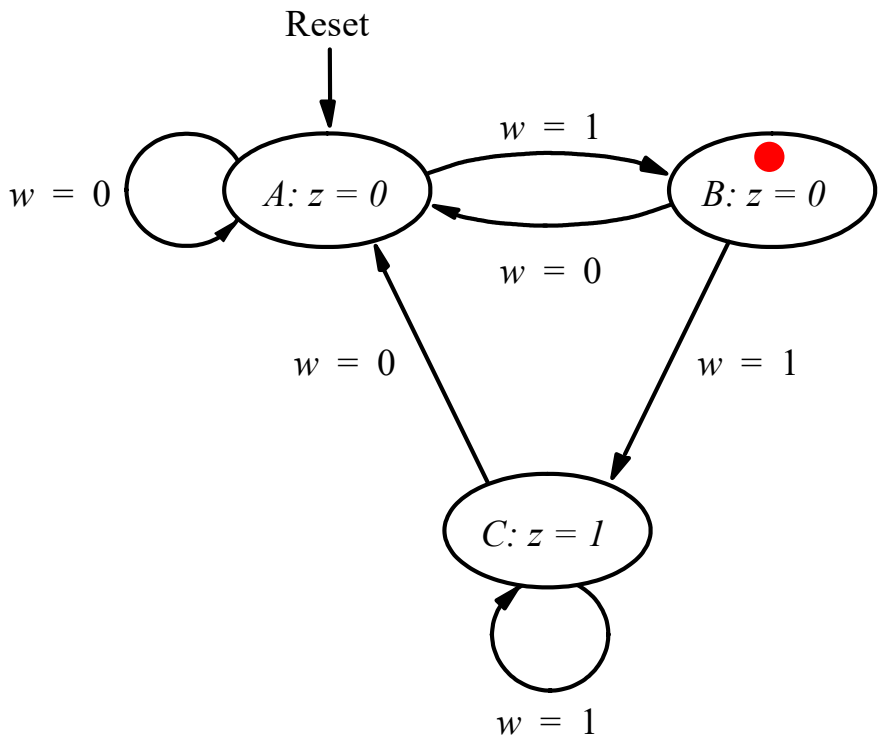
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



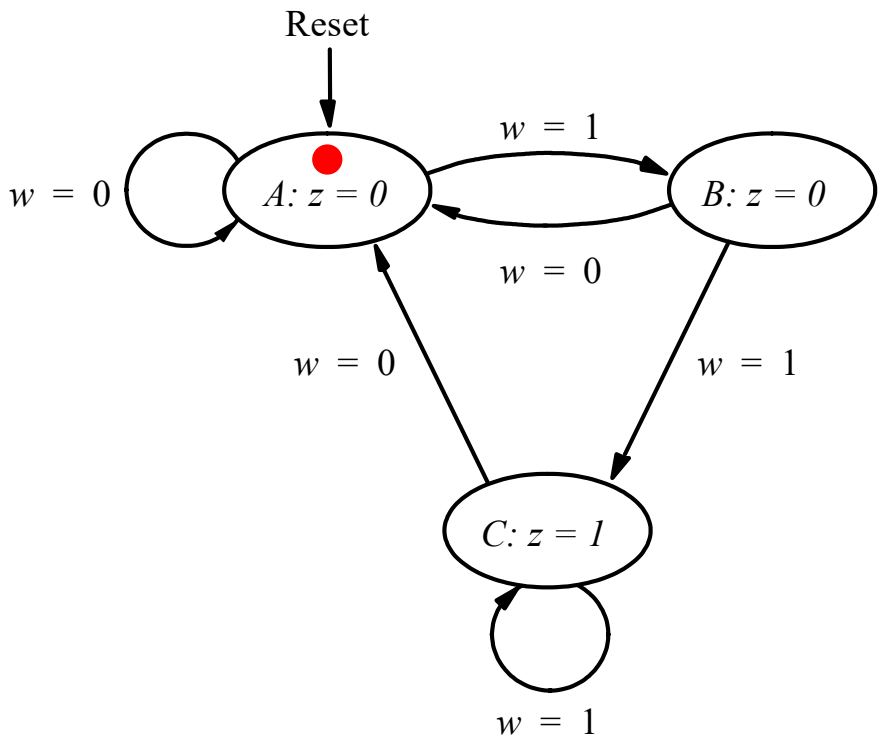
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



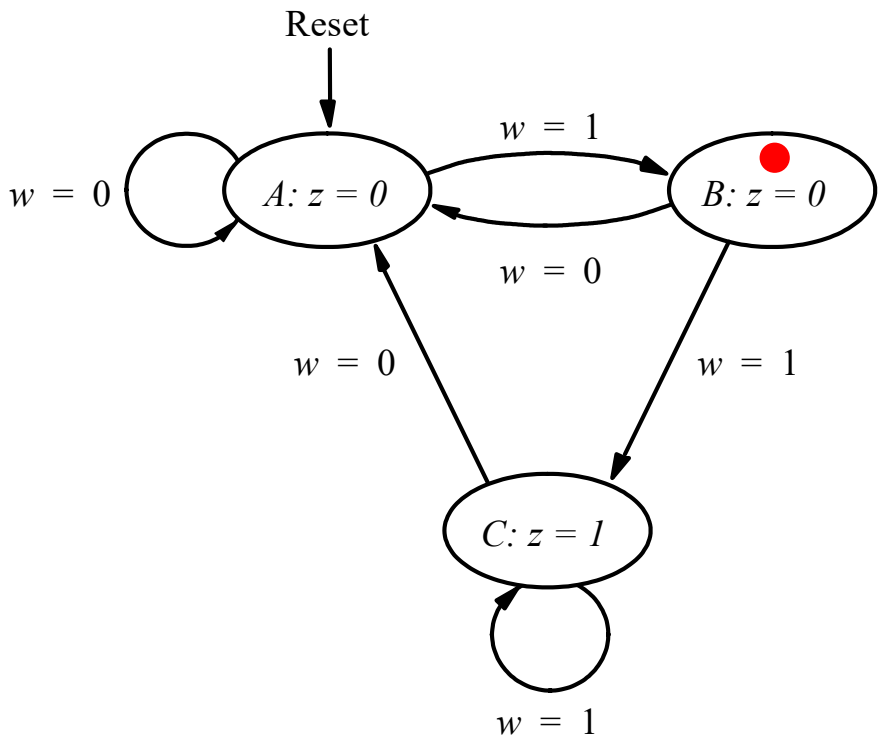
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



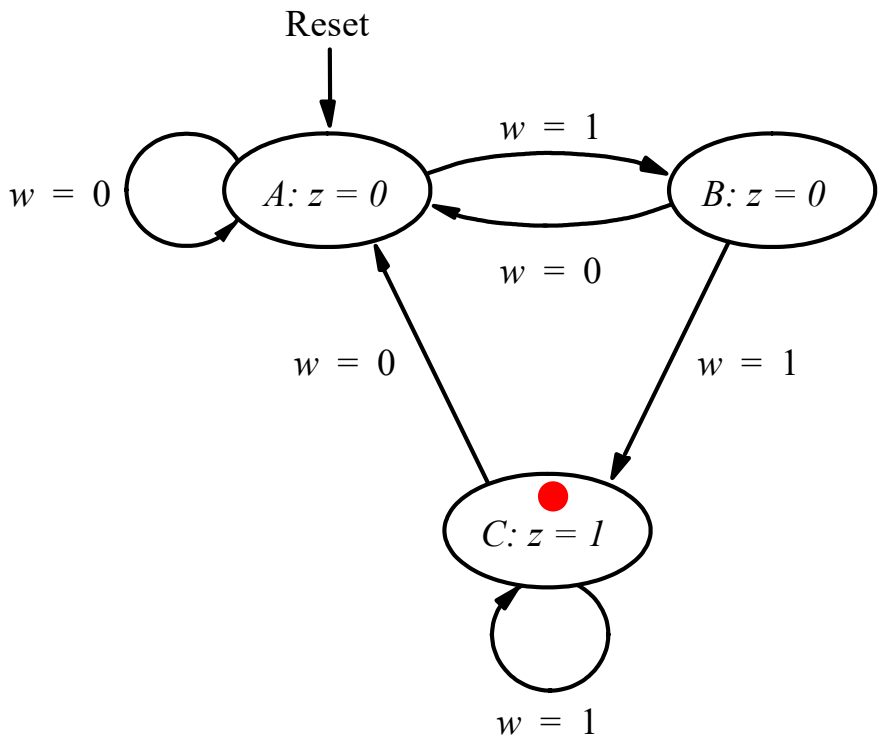
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



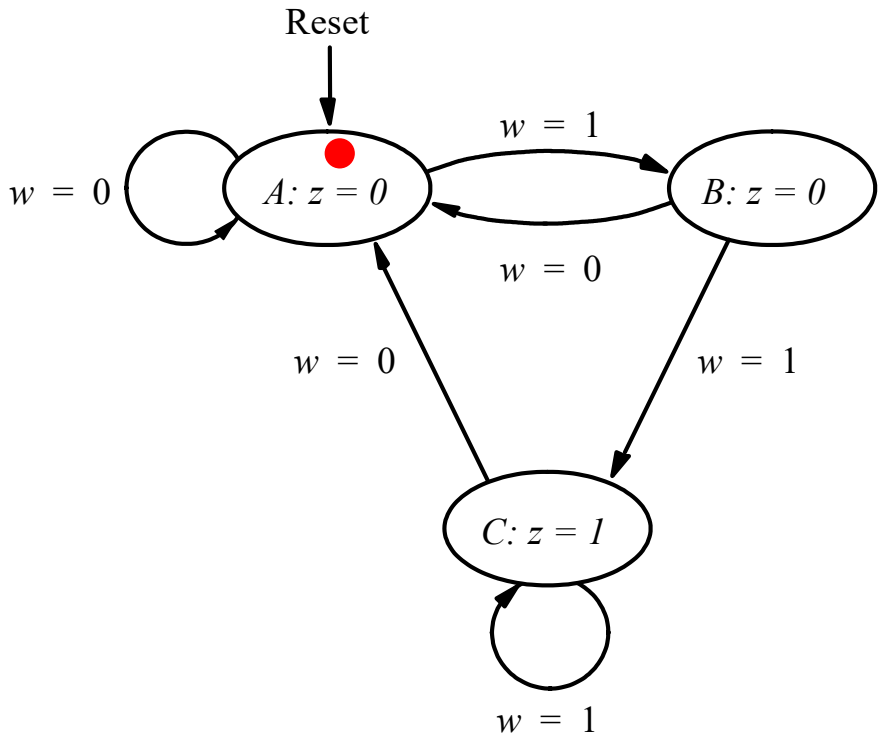
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



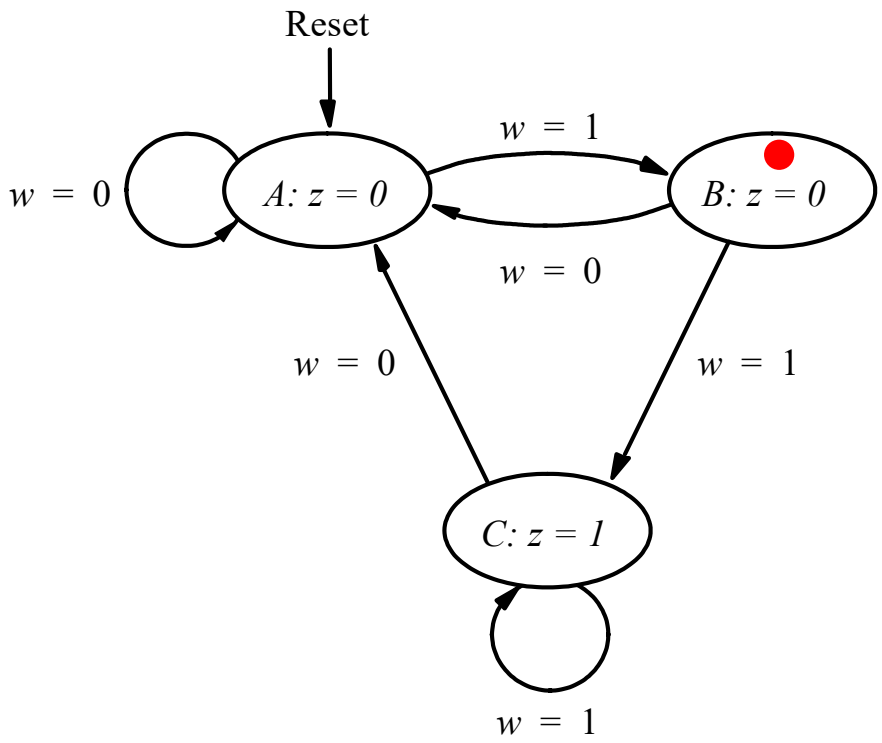
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



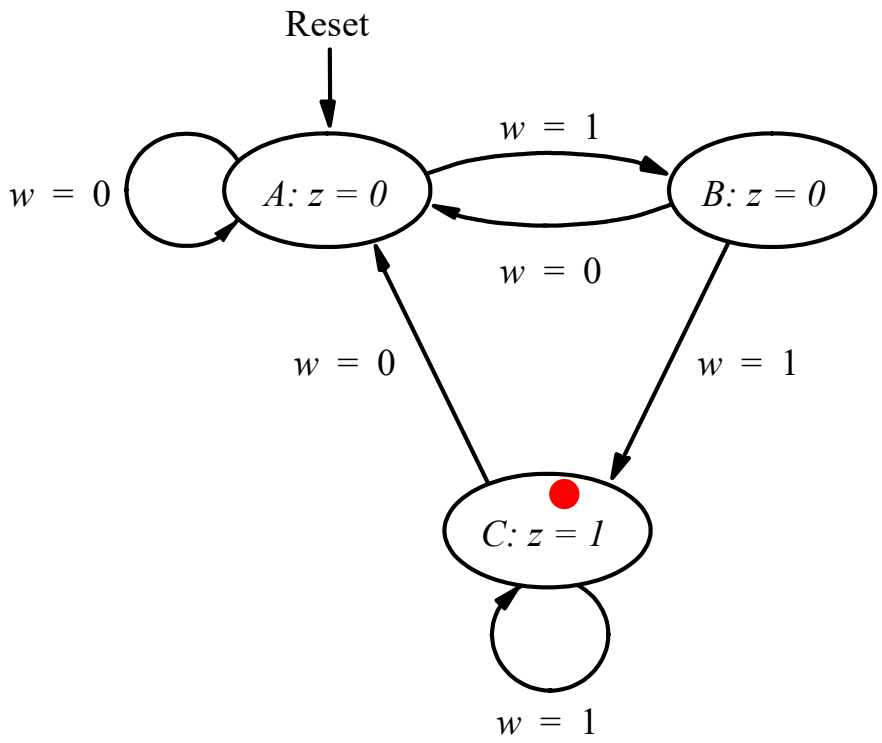
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



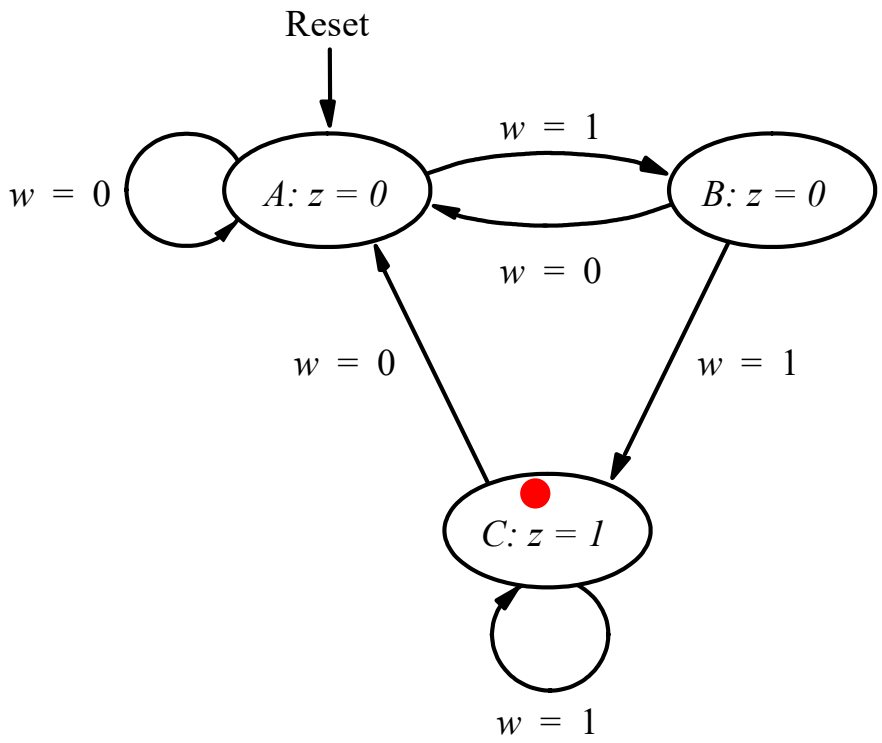
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



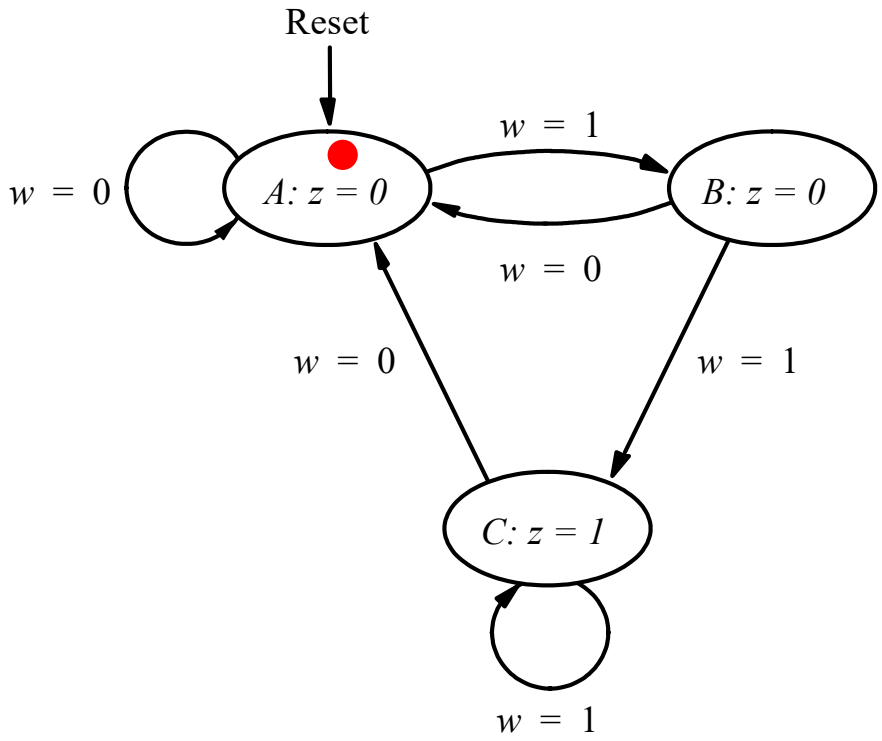
Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0

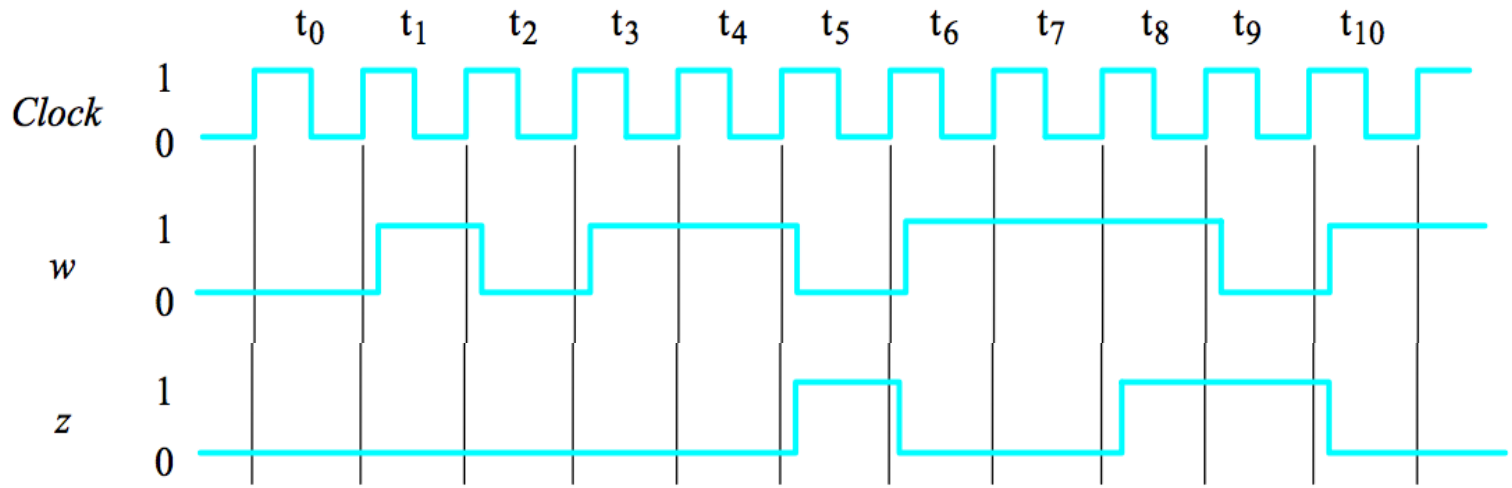


Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0



Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0

Inferring the States

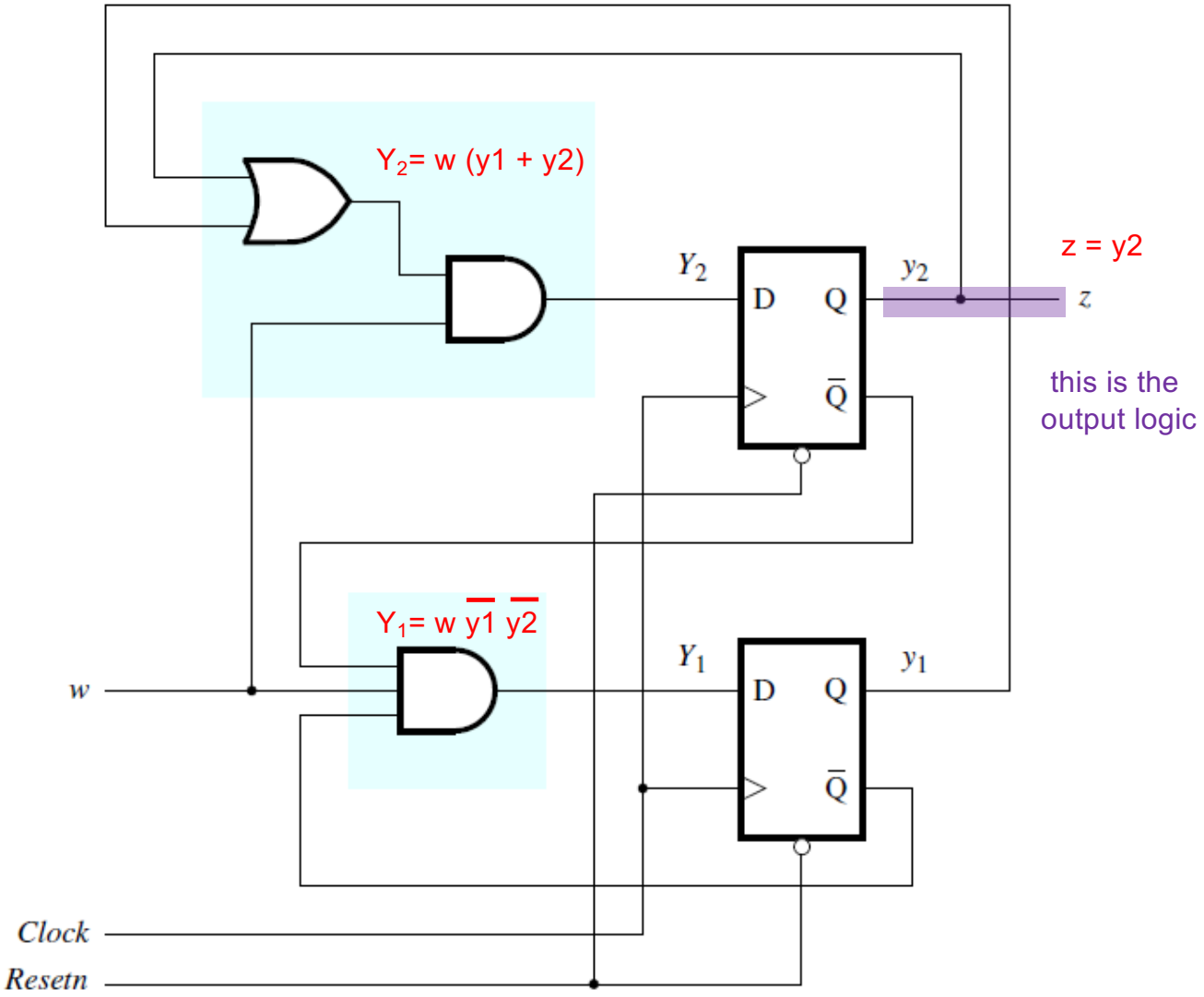


Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w:	0	1	0	1	1	0	1	1	1	0	1
z:	0	0	0	0	0	1	0	0	1	1	0

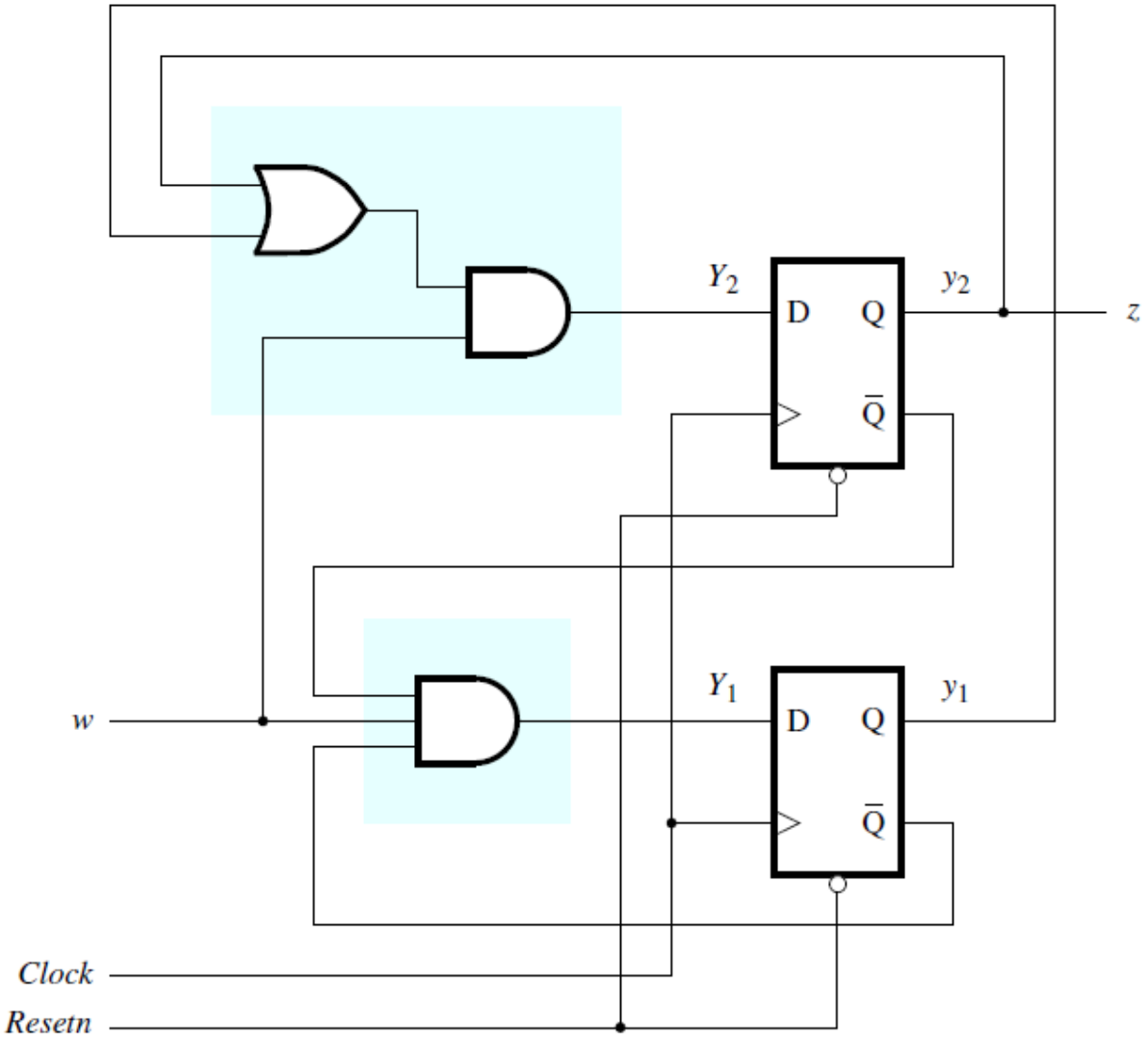
State Encoding for Example #1: A=00, B=01, C=10

(Uses Two Flip-Flops)

The Circuit Diagram



[Figure 6.8 from the textbook]



[Figure 6.8 from the textbook]

Alternative State Encoding for Example #1:
A=00, B=01, C=11

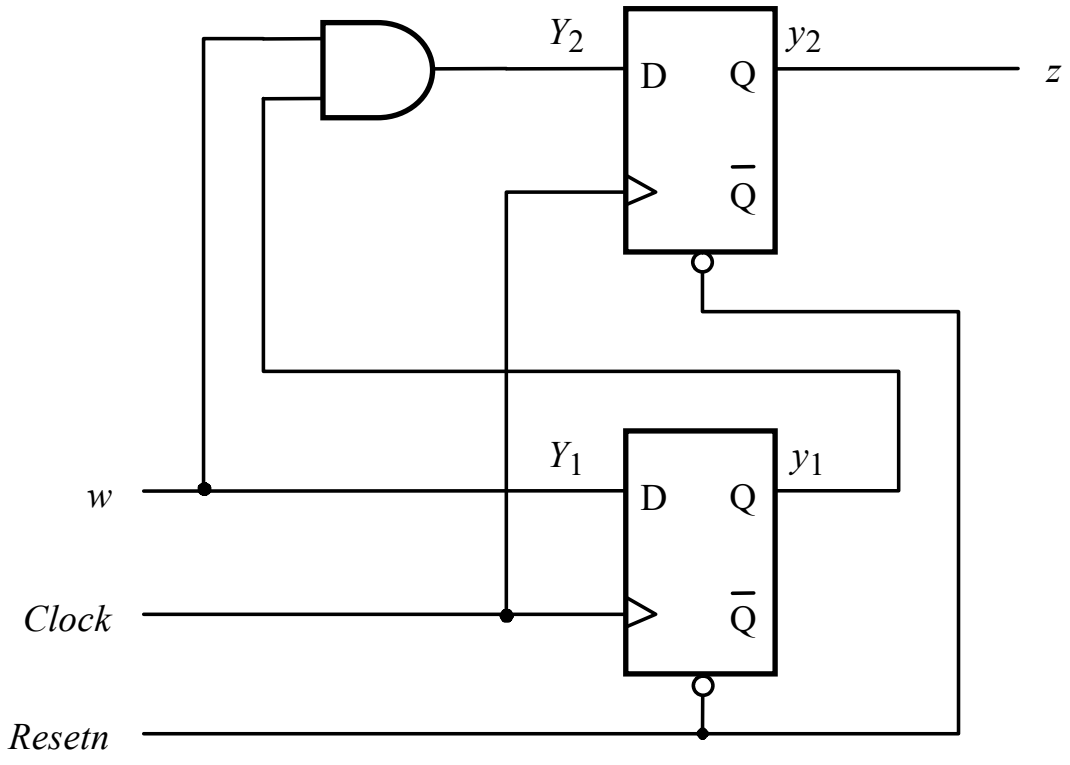
(Also Uses Two Flip-Flops)

The New and Improved Circuit Diagram

$$Y_1(w, y_2, y_1) = w$$

$$Y_2(w, y_2, y_1) = wy_1$$

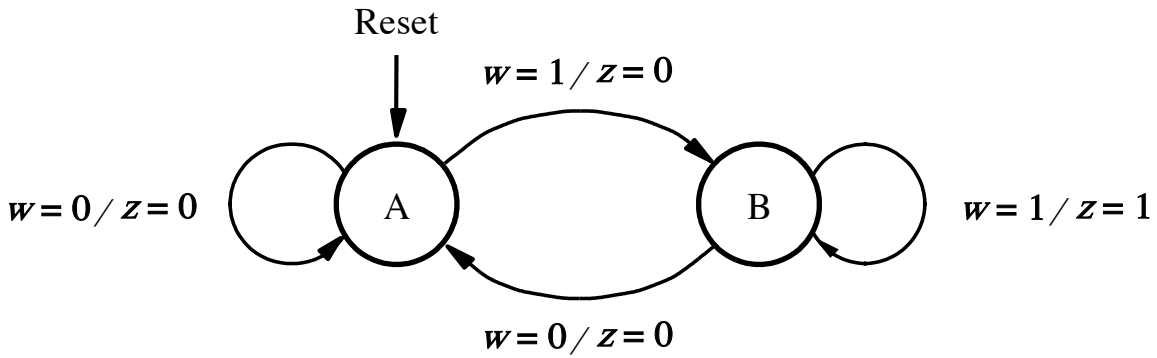
$$z(y_2, y_1) = y_2$$



[Figure 6.17 from the textbook]

Mealy Machine Implementation

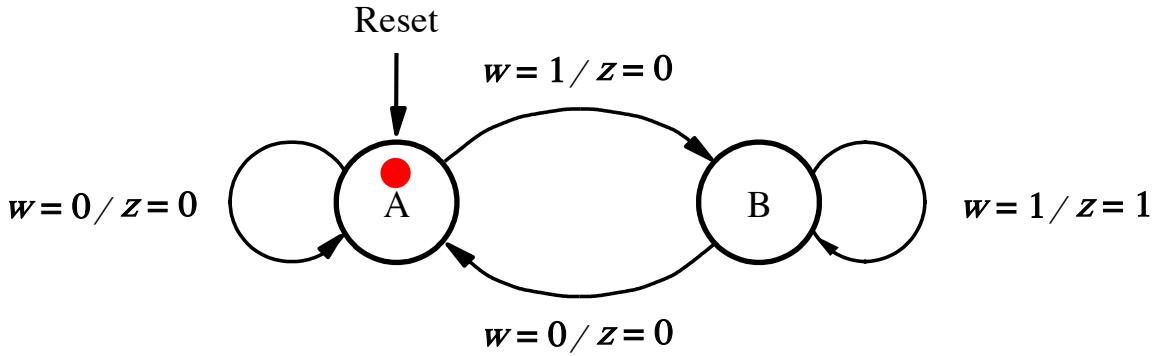
State diagram of an FSM that realizes the task



[Figure 6.23 from the textbook]

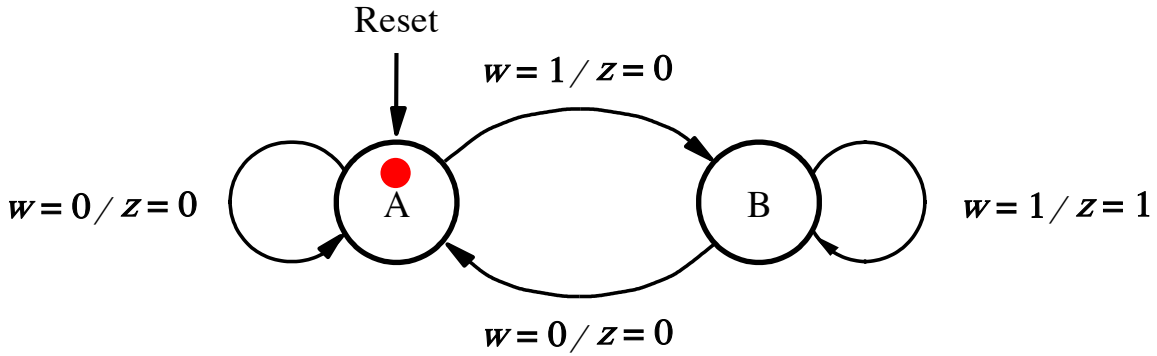
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



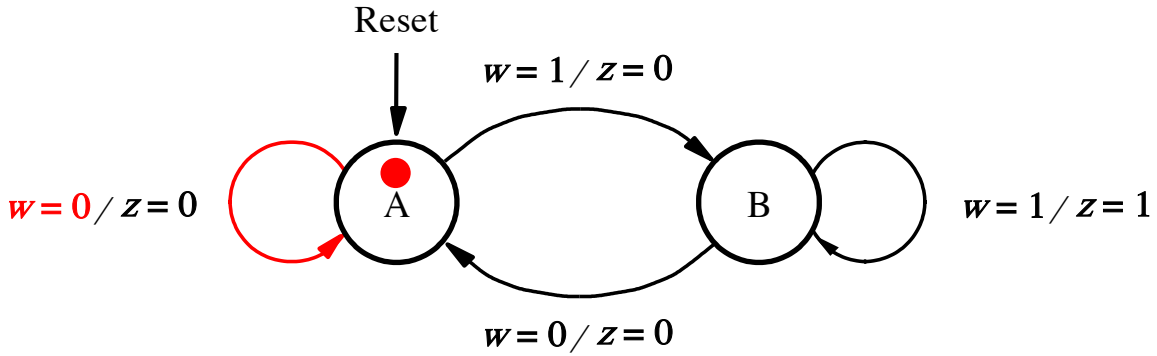
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



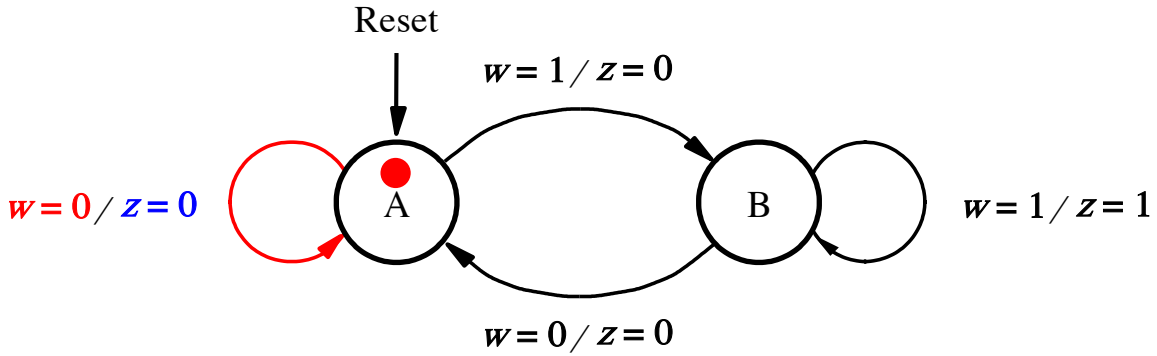
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



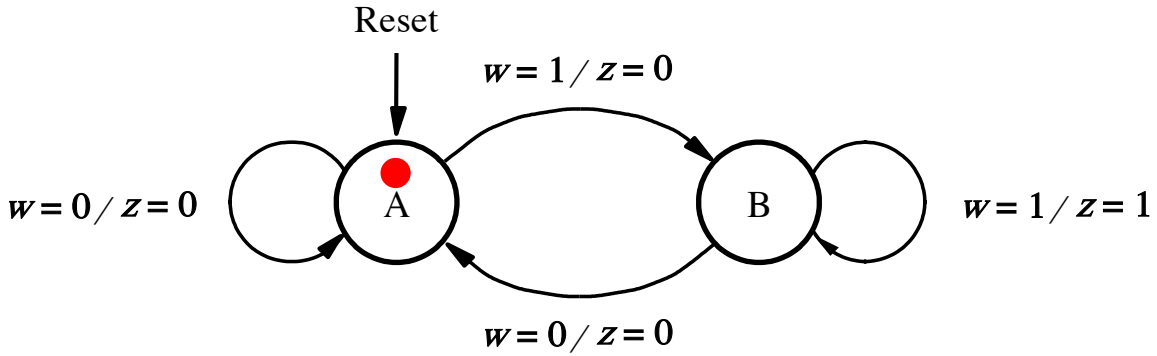
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



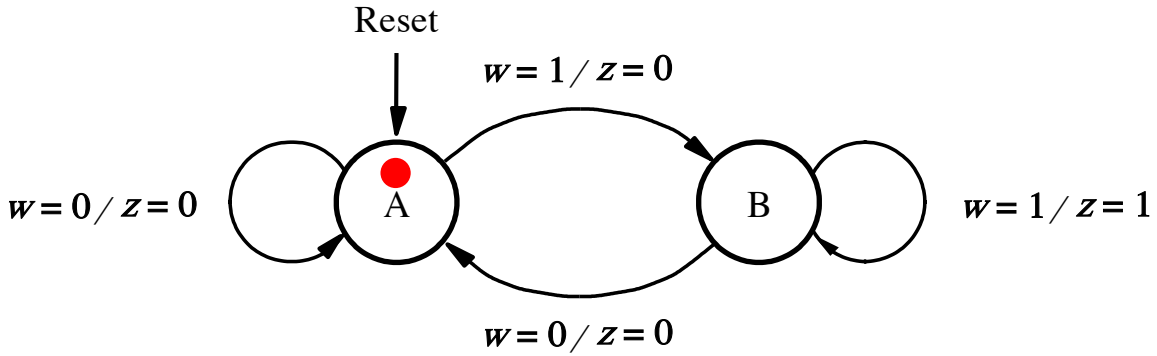
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



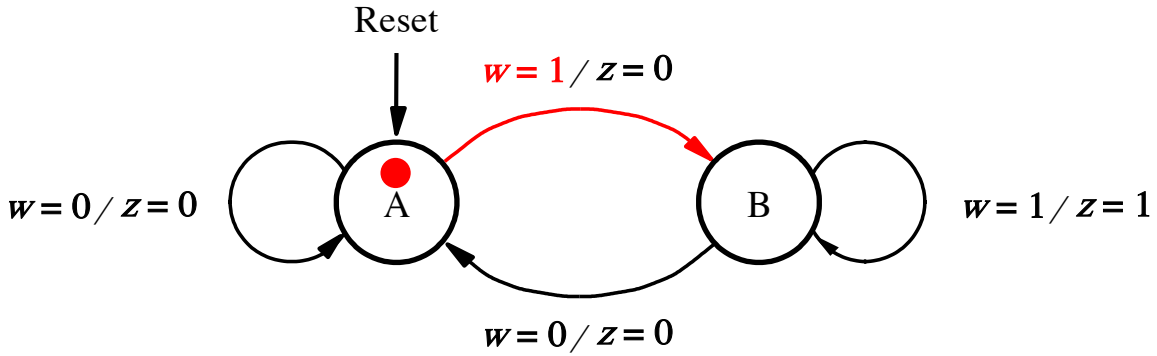
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



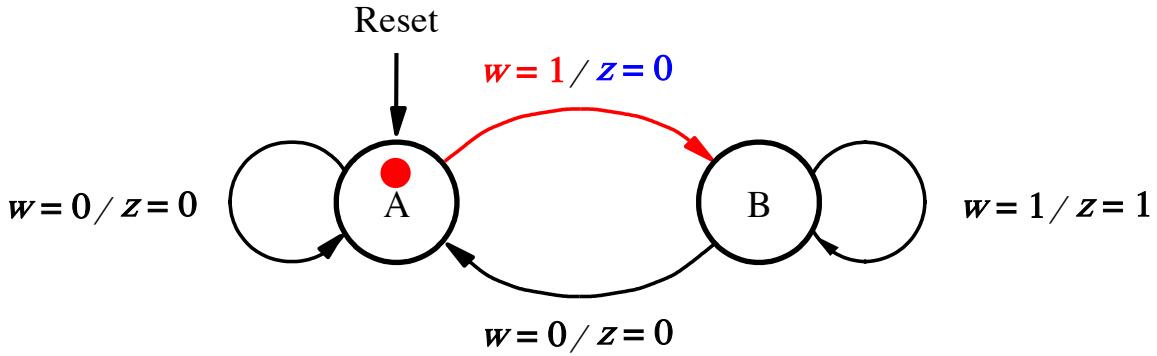
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



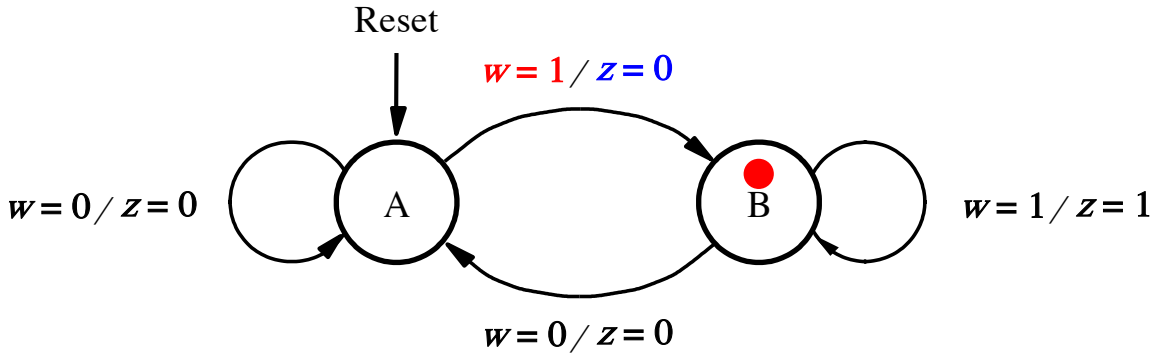
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



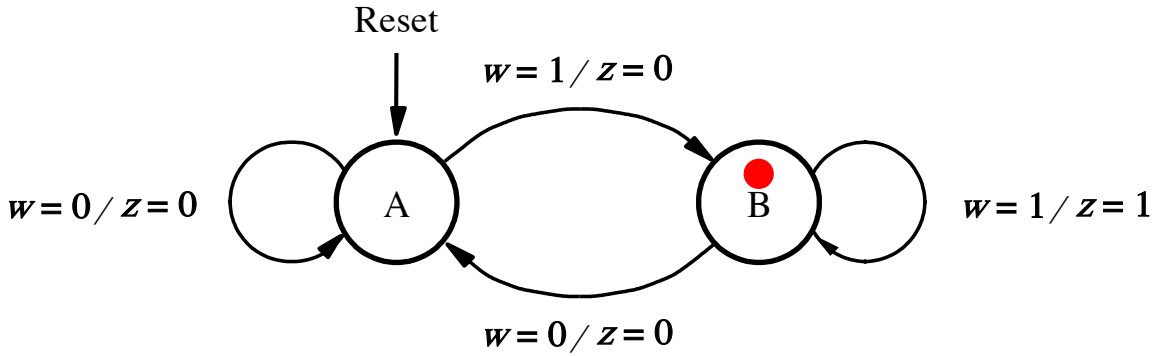
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



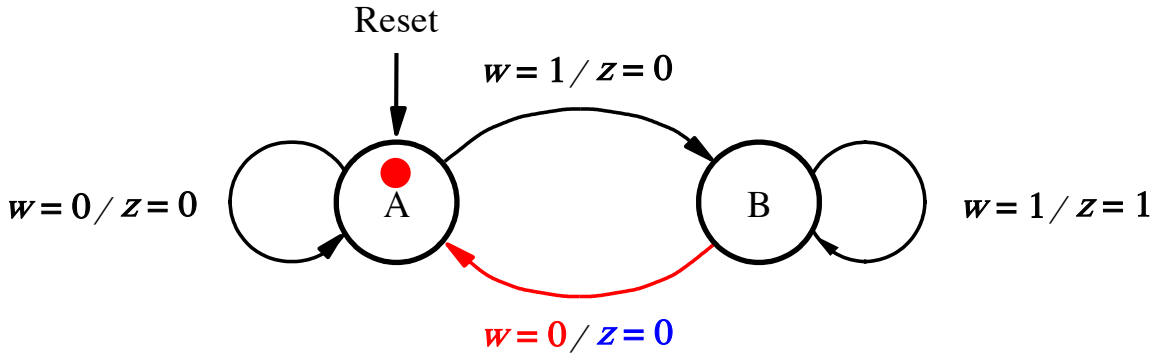
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



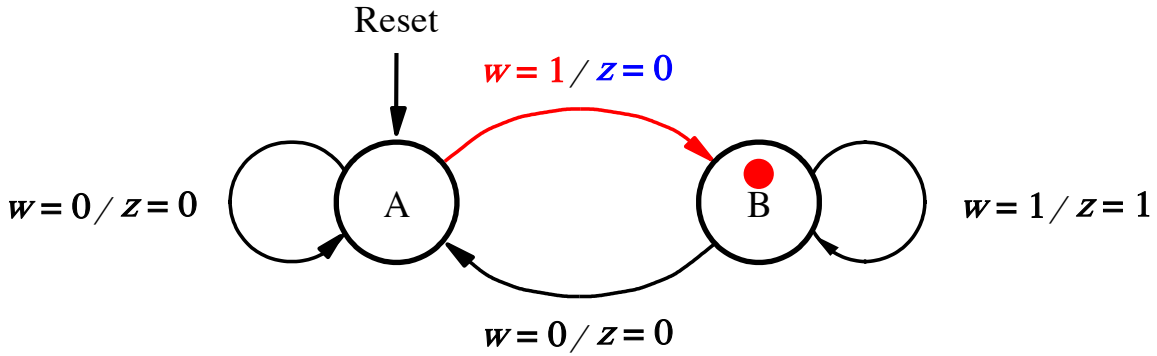
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0



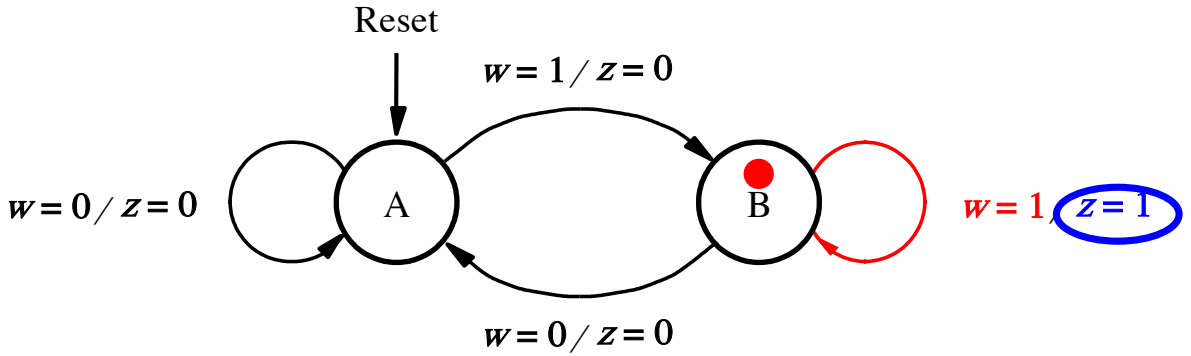
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



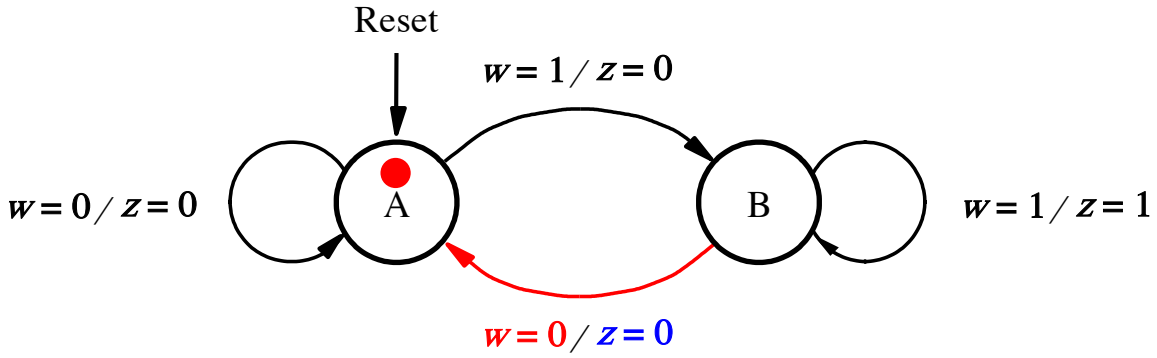
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



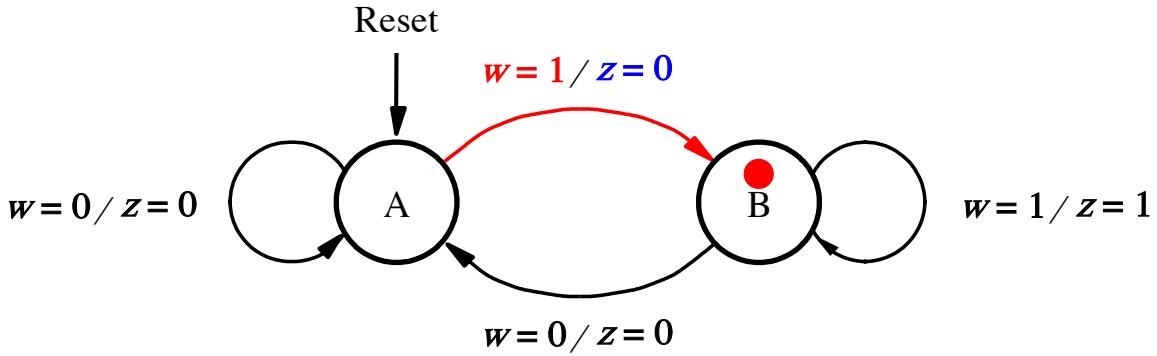
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



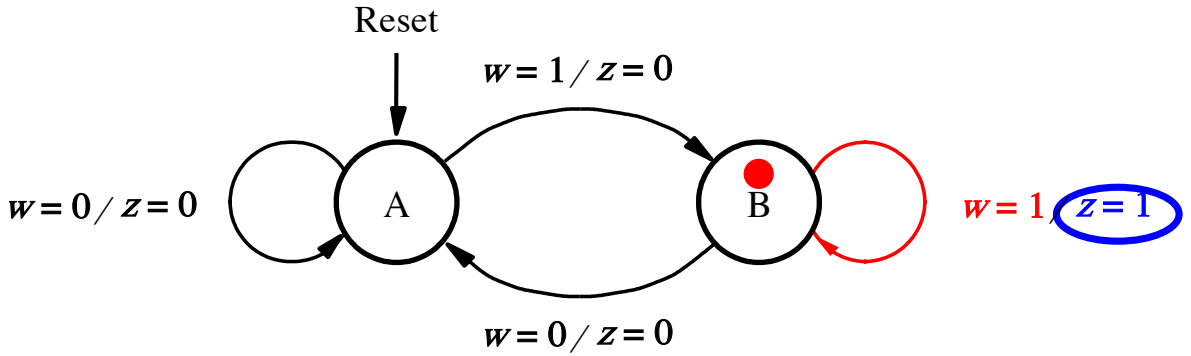
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



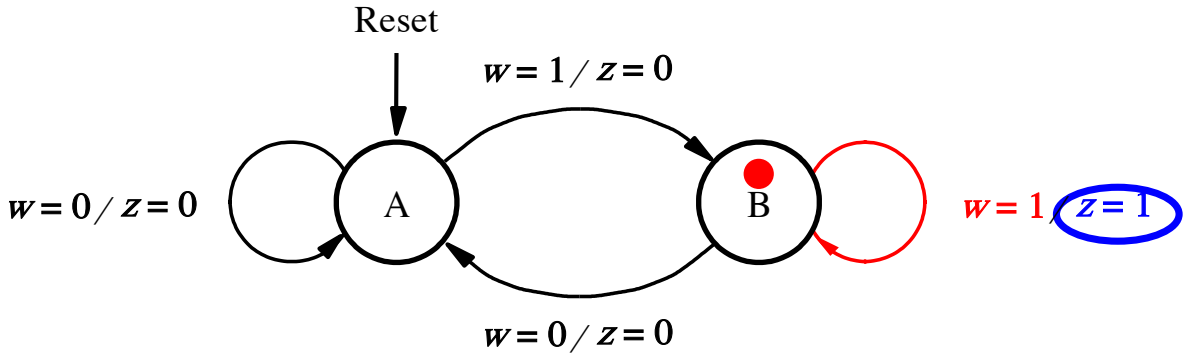
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



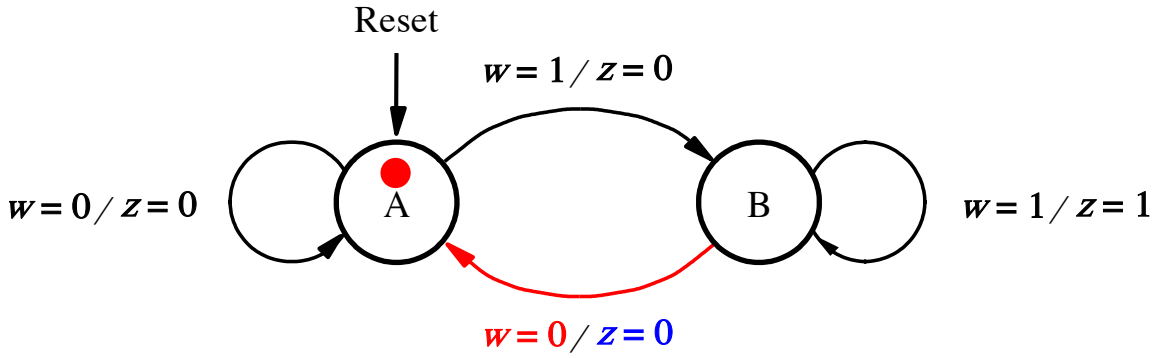
Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0



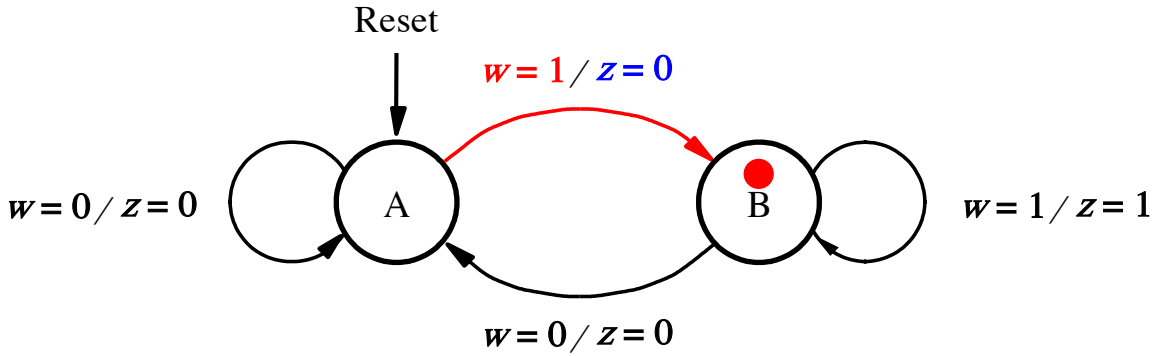
Let's Do a Simulation

Clock cycle:		t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input	w:	0	1	0	1	1	0	1	1	1	0	1
output	z:	0	0	0	0	1	0	0	1	1	0	0

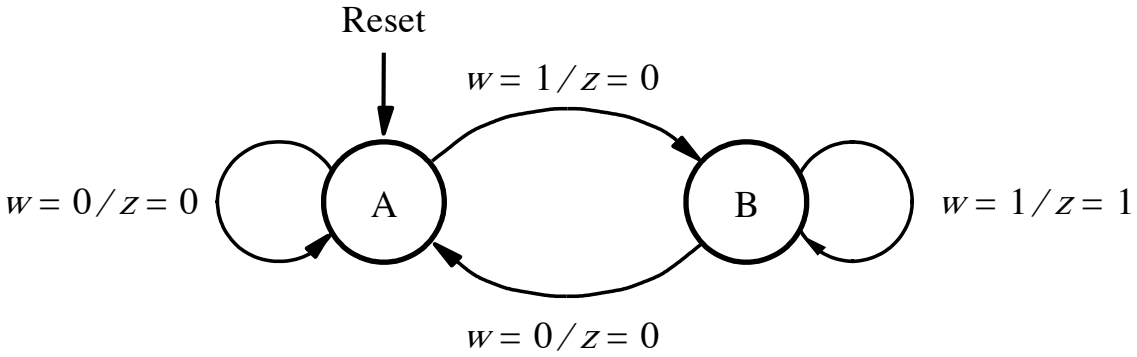


Let's Do a Simulation

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0

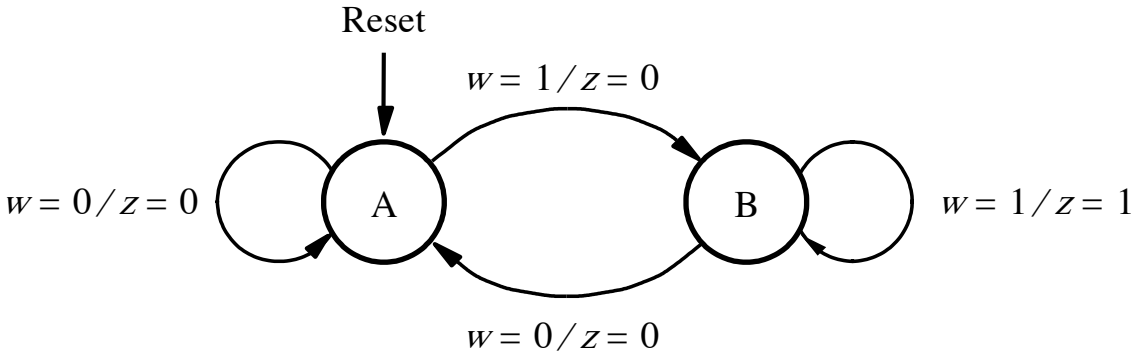


Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A				
B				

Now Let's Do the State Table for this FSM



Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

The State Table for this FSM

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

[Figure 6.24 from the textbook]

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0				
B	1				

Let's Do the State-assigned Table

Present state	Next state		Output z	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	A	B	0	0
B	A	B	0	1

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

[Figure 6.25 from the textbook]

The State-assigned Table

	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

$$Y = D = w \qquad z = wy$$

[Figure 6.25 from the textbook]

The State-assigned Table

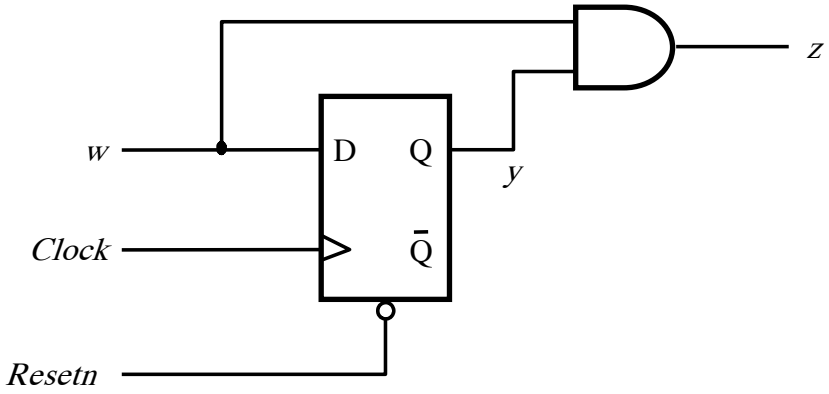
	Present state	Next state		Output	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
	y	Y	Y	z	z
A	0	0	1	0	0
B	1	0	1	0	1

$Y = D = w$ $\quad$ $z = wy$

This assumes D flip-flop

[Figure 6.25 from the textbook]

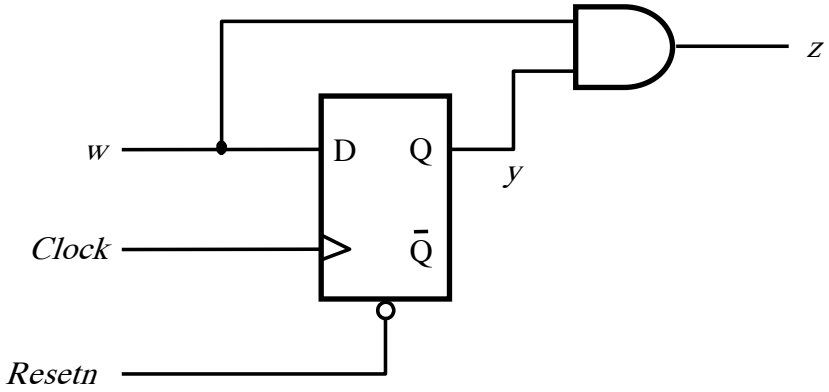
Circuit Implementation of the FSM



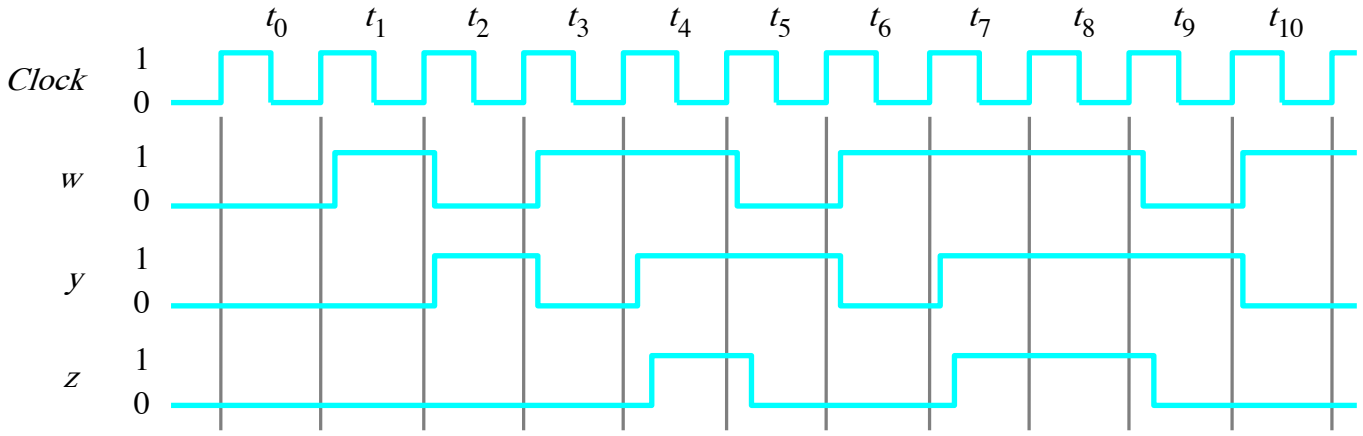
$$Y = D = w \qquad z = wy$$

[Figure 6.26 from the textbook]

Circuit & Timing Diagram



(a) Circuit

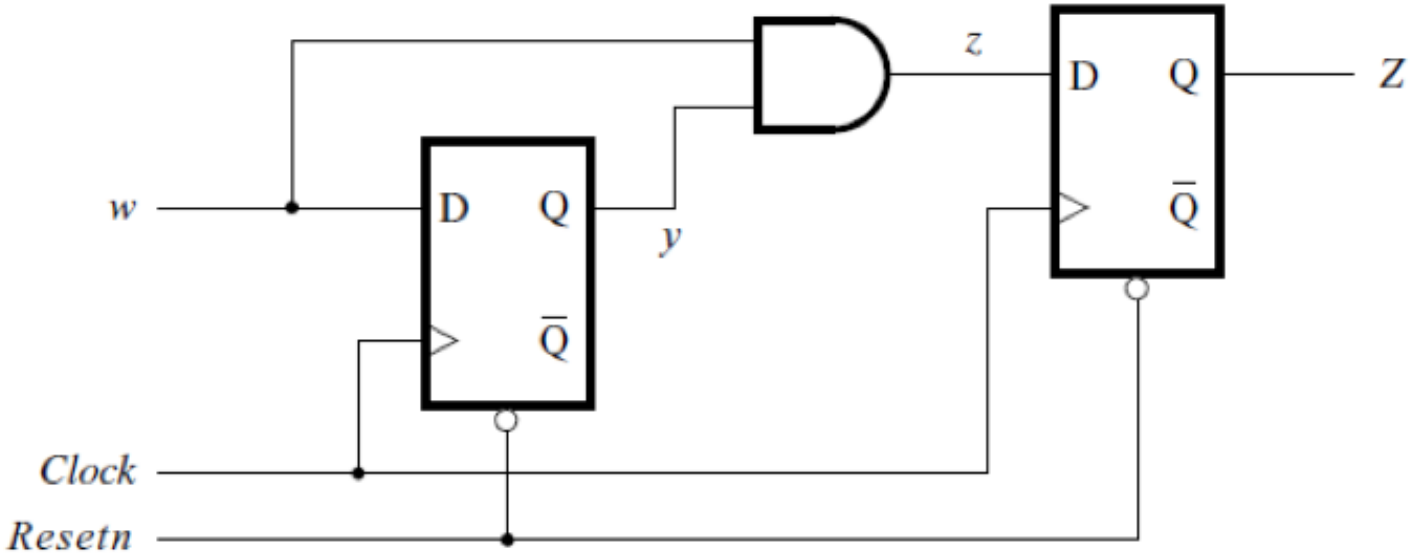


(b) Timing diagram

[Figure 6.26 from the textbook]

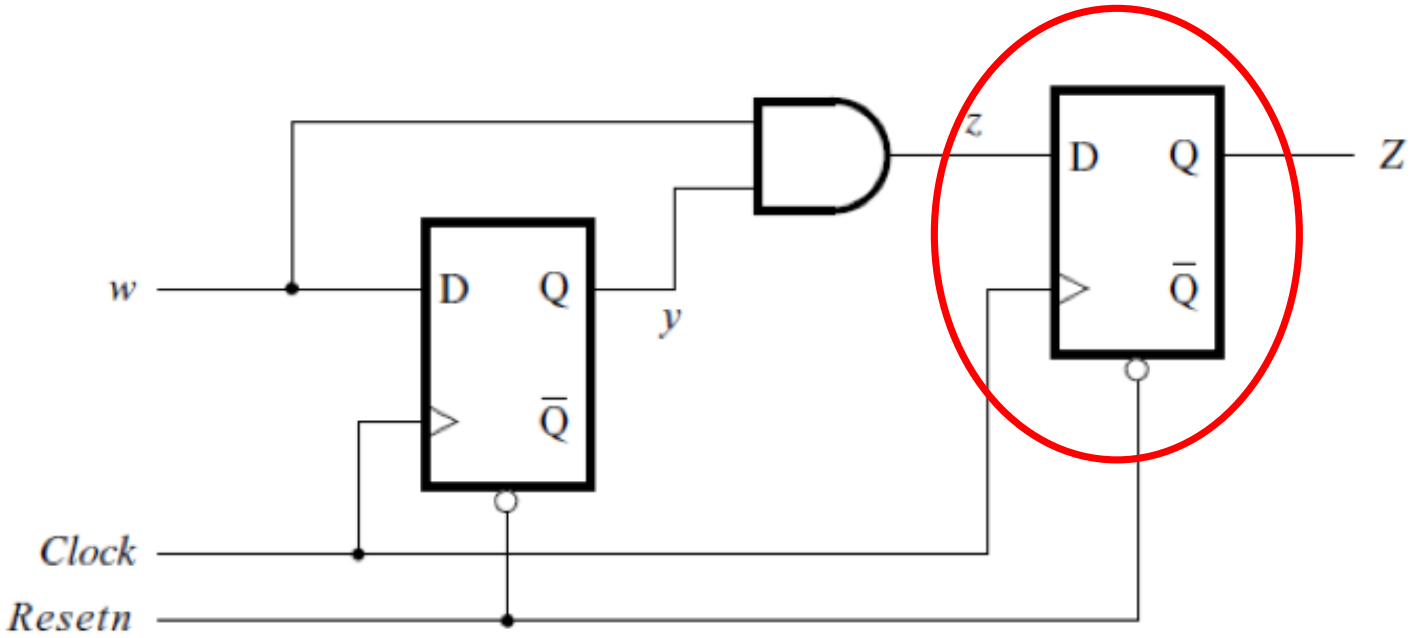
What if we wanted the output signal to be delayed by 1 clock cycle?

Circuit Implementation of the Modified FSM



[Figure 6.27a from the textbook]

Circuit Implementation of the Modified FSM



This flip-flop delays the
output signal by one clock cycle

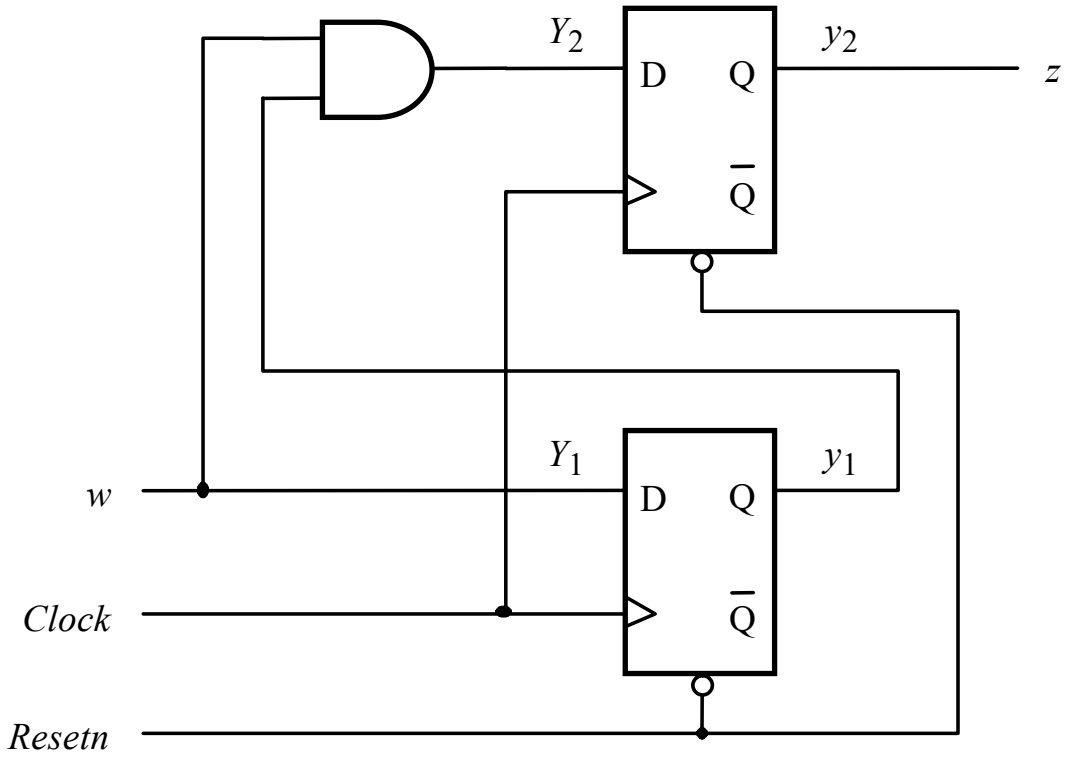
[Figure 6.27a from the textbook]

We Have Seen This Diagram Before

$$Y_1(w, y_2, y_1) = w$$

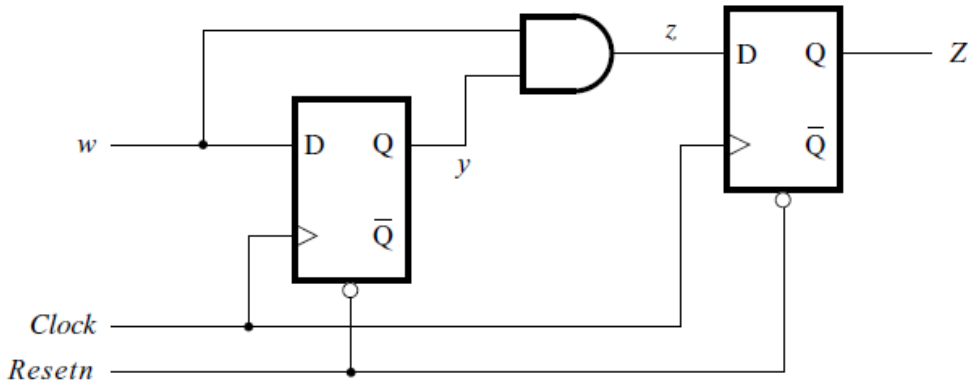
$$Y_2(w, y_2, y_1) = wy_1$$

$$z(y_2, y_1) = y_2$$

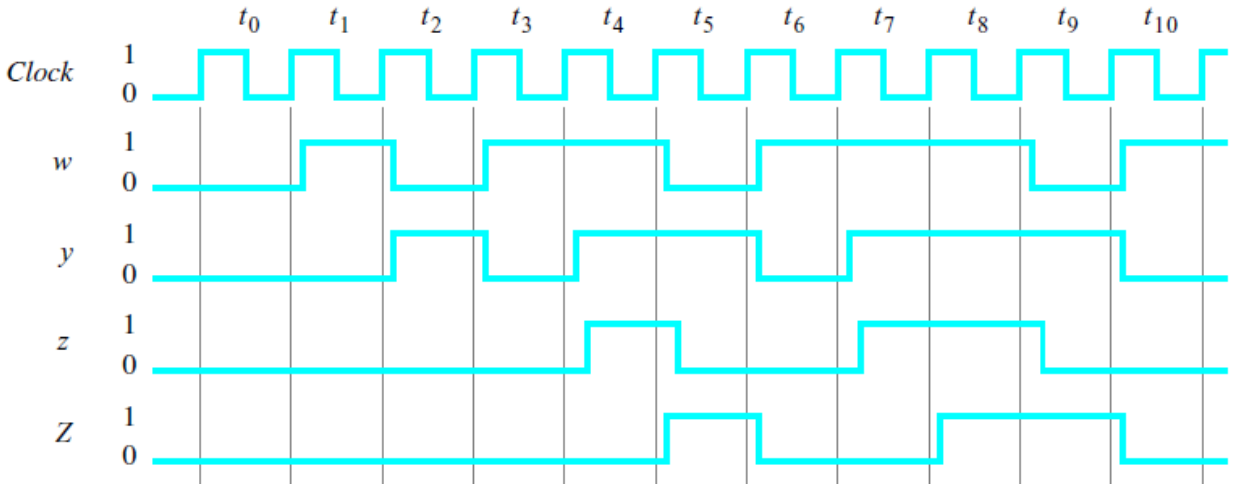


[Figure 6.17 from the textbook]

Circuit & Timing Diagram

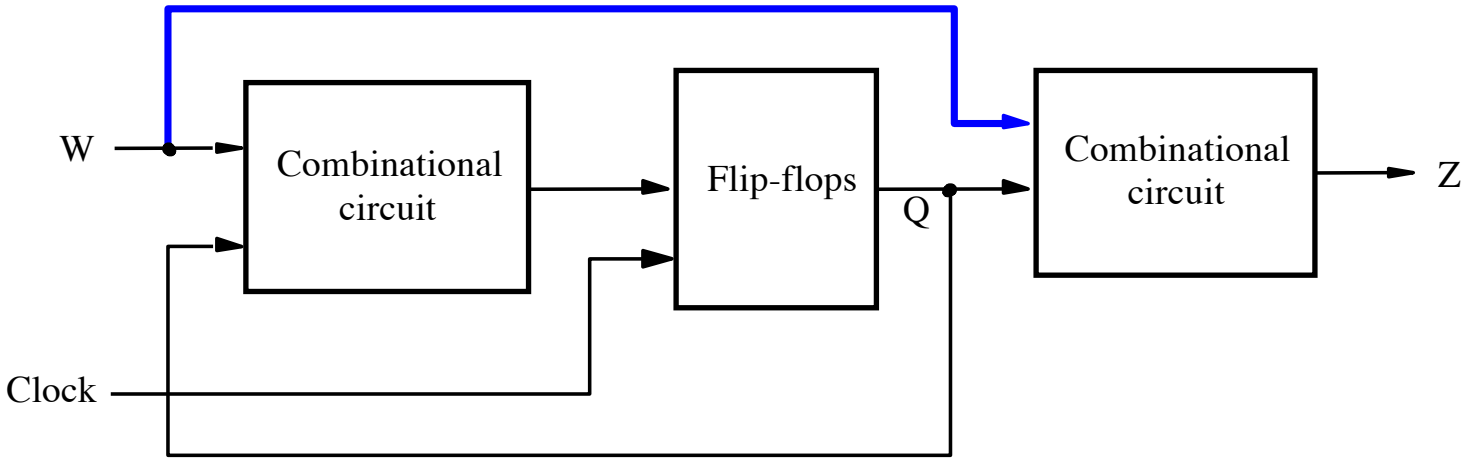


(a) Circuit



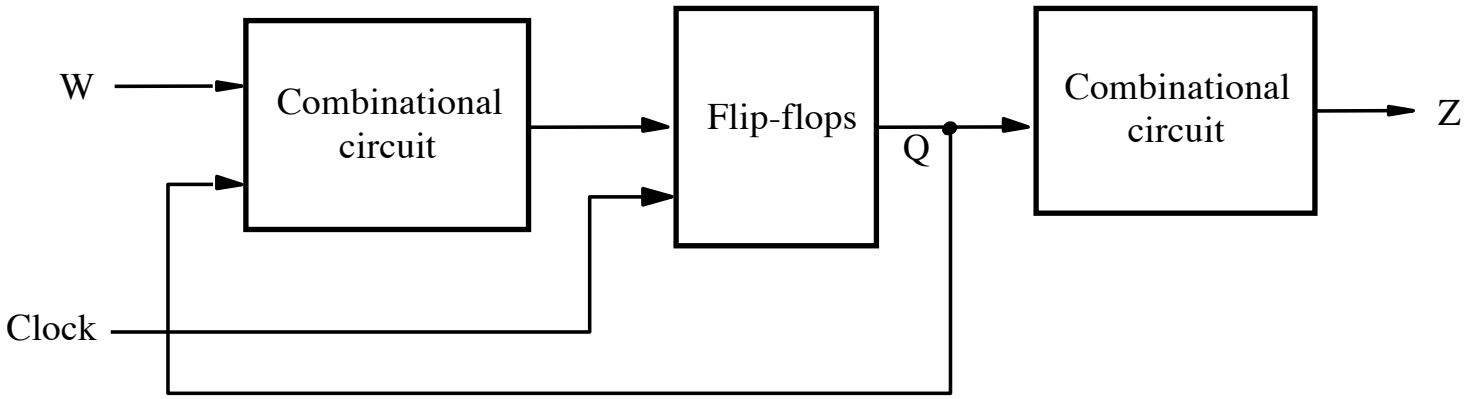
[Figure 6.27 from the textbook]

The general form of a synchronous sequential circuit

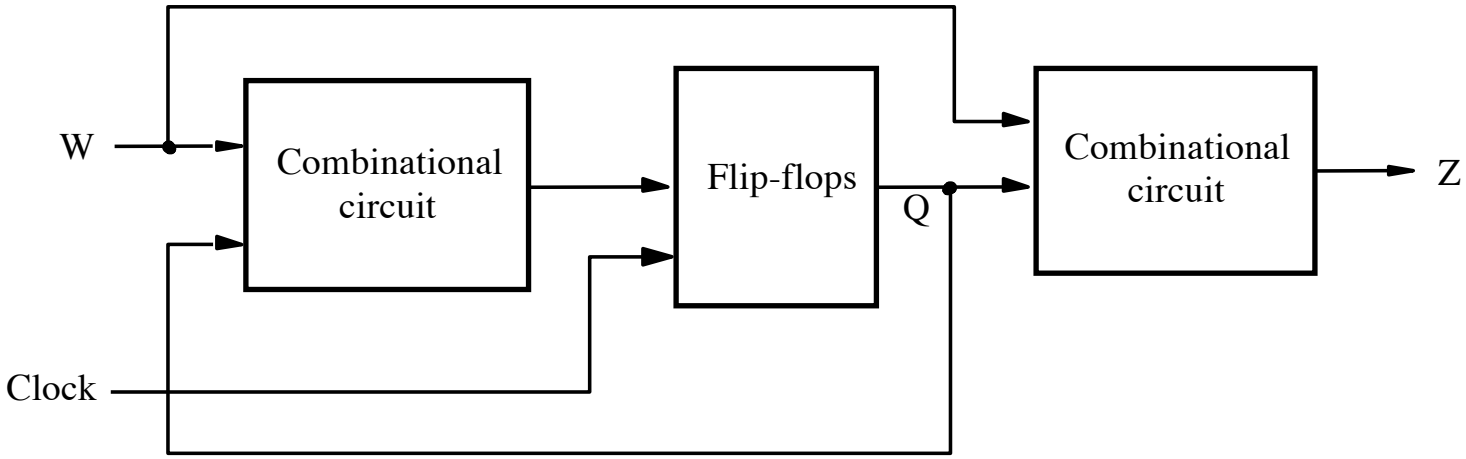


[Figure 6.1 from the textbook]

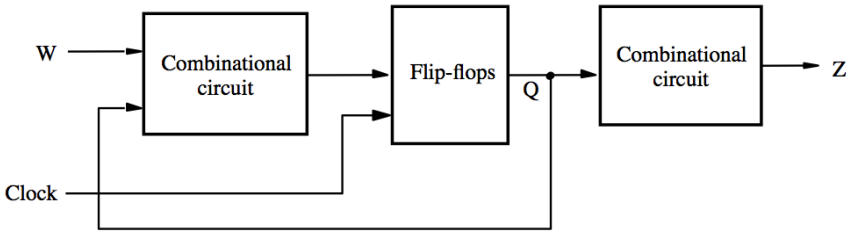
Moore Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

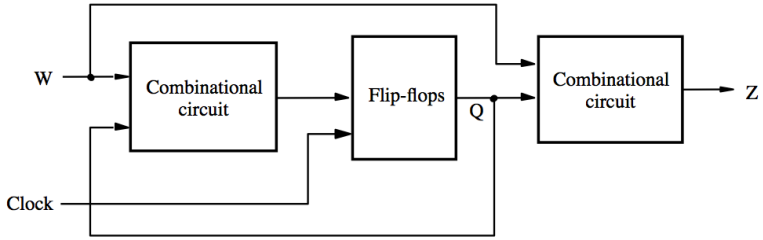
Mealy Type


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

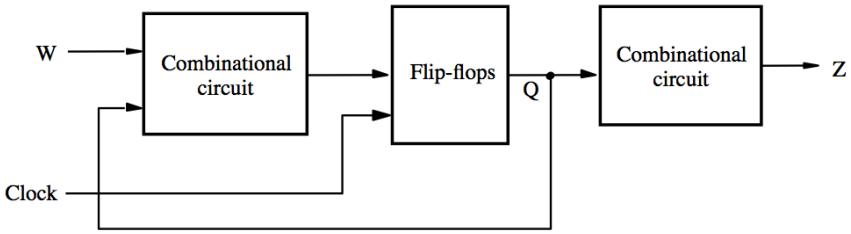
Moore

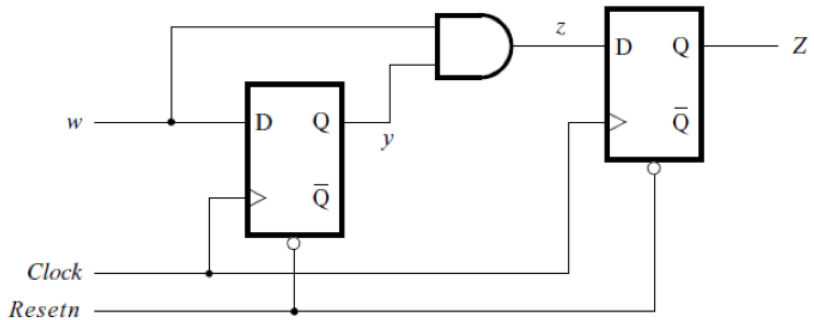

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

Mealy

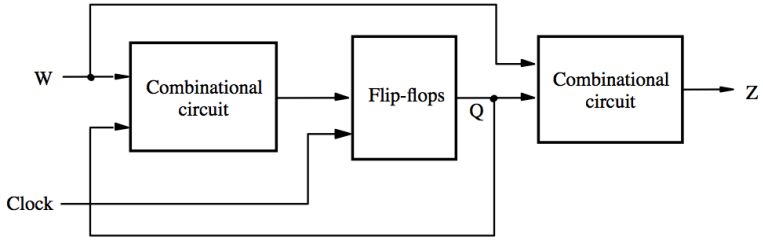

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

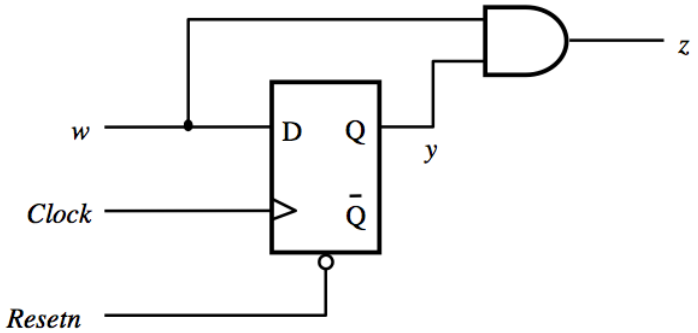
Moore


W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock

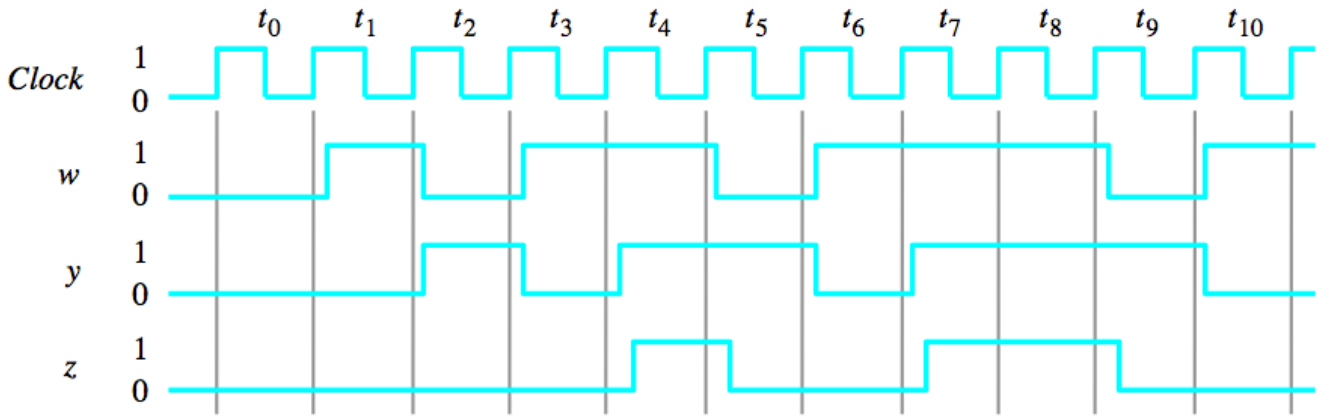

z
D
Q
Z
w
y
Clock
Resetn

Mealy

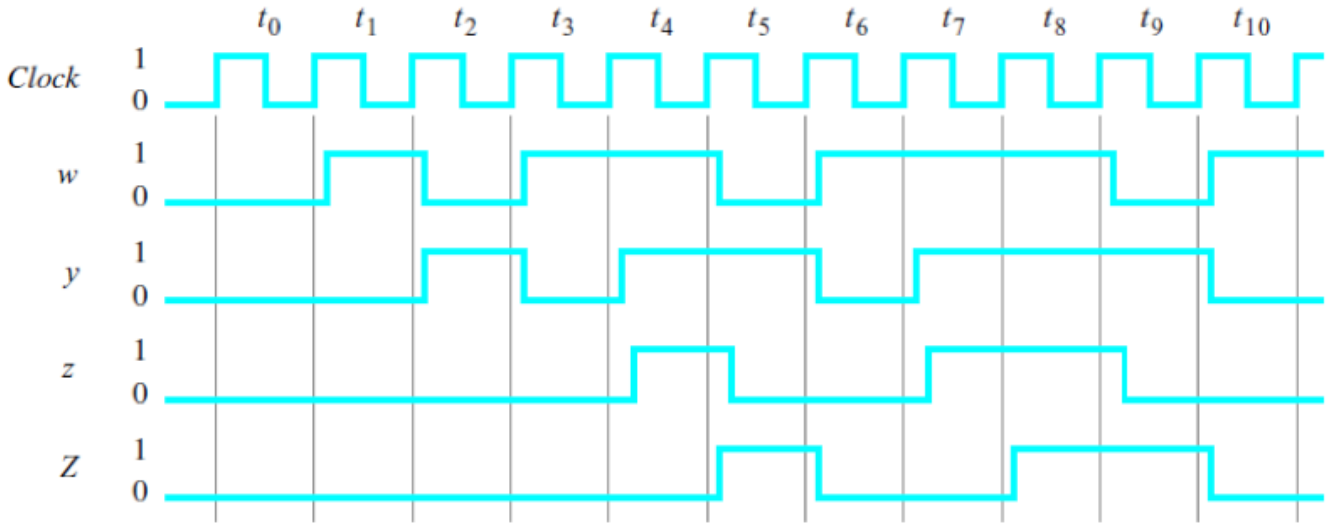

W
Combinational circuit
Flip-flops
Q
Combinational circuit
Z
Clock


z
w
D
Q
y
Clock
Resetn

Mealy

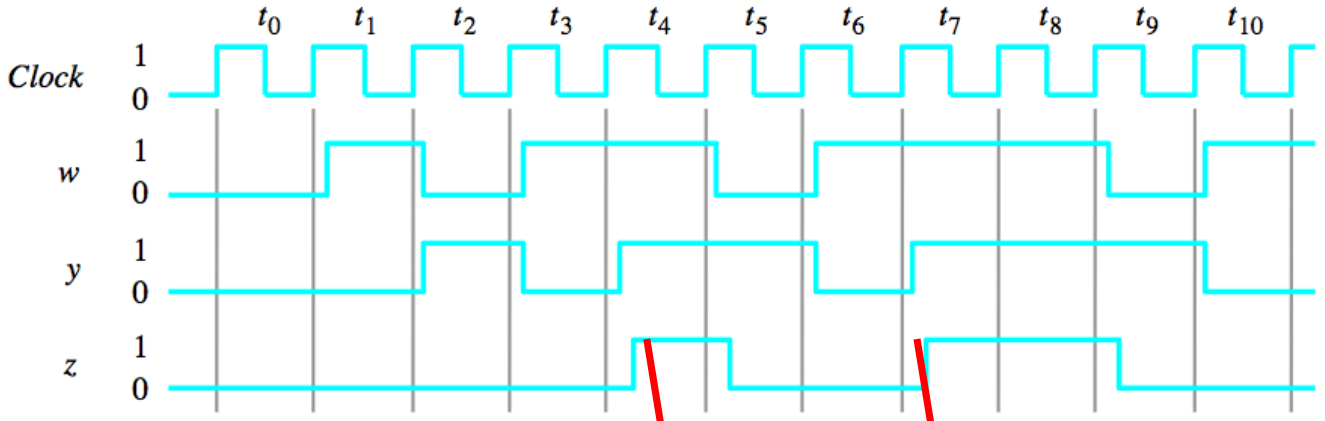

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10}
Clock
w
y
z
1
0

Moore

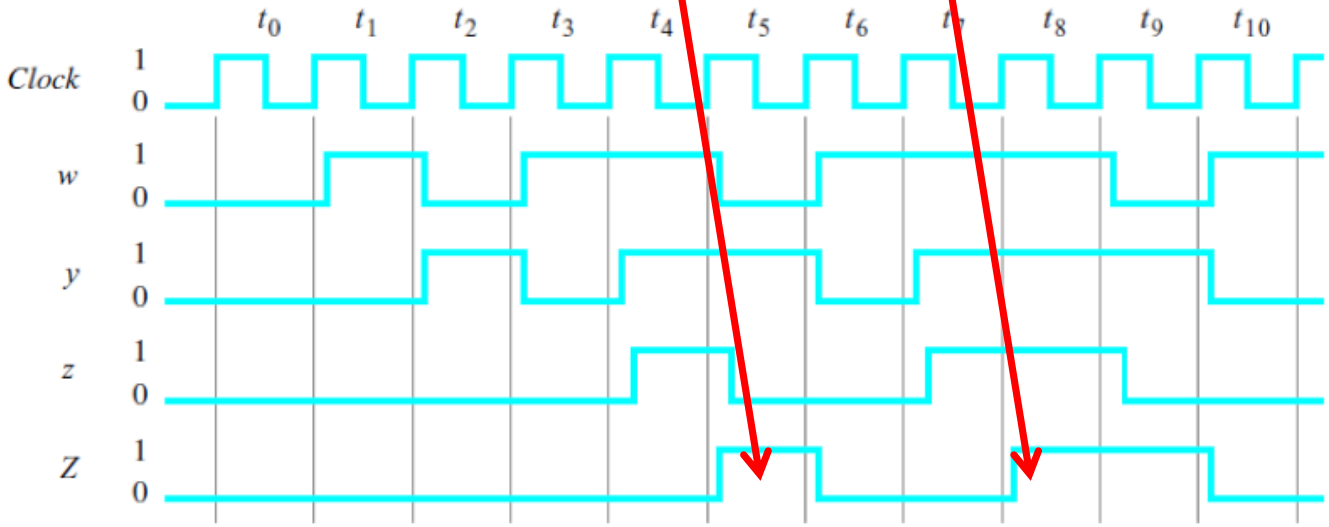

t_0 t_1 t_2 t_3 t_4 t_5 t_6 t_7 t_8 t_9 t_{10}
Clock
w
y
z
Z
1
0

Notice that the output of the Moore machine is delayed by one clock cycle

Mealy



Moore



Notice that the output of the Moore machine is delayed by one clock cycle

Mealy

Clock cycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	1	0	0	1	1	0	0

Moore

Clockcycle:	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
input w:	0	1	0	1	1	0	1	1	1	0	1
output z:	0	0	0	0	0	1	0	0	1	1	0

Questions?

THE END