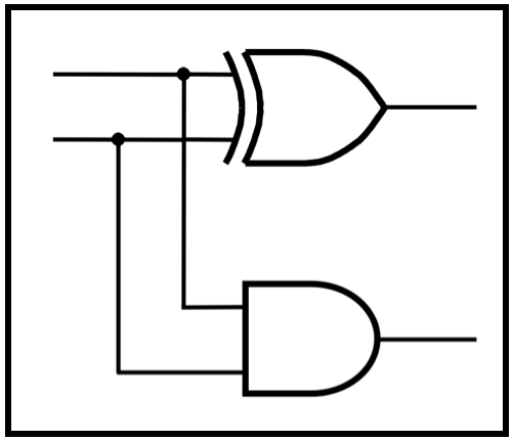


CprE 2810: Digital Logic

Instructor: Alexander Stoytchev

http://www.ece.iastate.edu/~alexs/classes/

Logic Gates

CprE 2810: Digital Logic
Iowa State University, Ames, IA

Administrative Stuff

- **HW1 is out. It is due on Wednesday Sep 3 @ 10pm.**
- **Submit it as a PDF upload on Canvas before the deadline.**
- **You can write the solutions on paper and then scan the pages to make **one** PDF file.**
- **No late homeworks will be accepted.**
- **Please write clearly on the first page:**
  - **your name**
  - **student ID**
  - **lab section number**

Labs Next Week

- **Please download and read the lab assignment for next week before you go to your lab section.**

- **https://www.ece.iastate.edu/~alexs/classes/2025_Fall_2810/labs/Lab_01/**

- **You must print and complete the prelab before you go to the lab.**

- **The TAs will check your prelab answers at the beginning of the recitation. If you don't have it done, you'll lose 20% of the lab grade for that lab.**

www.ece.iastate.edu/~alexs/classes/2025_Fall_2810/

CprE 2810: Digital Logic (Fall 2025)

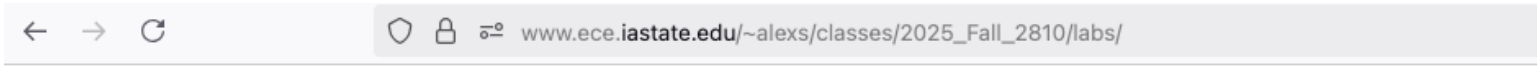
4:25 - 5:15 pm (Mondays, Wednesdays, and Fridays)
Hoover Hall, Room 2055
Instructor: Alexander Stoytchev

- Syllabus
- Class Schedule (Tentative)
- Lecture Notes (also in PDF)
- Labs
- Recitations

- Extra Readings

- Verilog Stuff
- Verilog Reference

- i281 CPU
- i281 CPU Simulator



CprE 2810: Digital Logic (Lab Assignments)

- Lab 1
- Lab 2
- Lab 3
- Lab 4
- Lab 5
- Mini Project
- Lab 6
- Lab 7
- Lab 8
- Lab 9
- Lab 10
- Lab 11
- Lab 12
- Lab 13

- Remote Access Instructions

Index

Name	Last modified	Size
Parent Directory		-
CPRE281_LAB01(Answer_Sheet).docx	2021-08-27 14:02	26K
CPRE281_LAB01(Answer_Sheet).pdf	2021-08-27 14:03	338K
CPRE281_LAB01.docx	2021-08-27 14:04	1.9M
CPRE281_LAB01.pdf	2021-08-27 14:04	1.4M
lab1.zip	2021-08-27 13:56	5.4M

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lab1.zip	2021-08-27 13:56	5.4M

READ one of these at home.
This is the lab assignment.

Index

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lab1.zip	2021-08-27 13:56	5.4M

During the lab next week,
download this ZIP file and
follow the instructions.

Index

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CPRE281_LAB01.pdf	2021-08-27 14:04	1.4M
lab1.zip	2021-08-27 13:56	5.4M

Print this file,
complete the prelab,
and bring it with you
to the lab.

Index

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lab1.zip	2021-08-27 13:56	5.4M

This is the same,
but in Word format.

Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 1 Answer Sheet

Name and Student ID:_____ **Lab Section:**___

Date:_____

PRELAB:

Q1. Fill in the Truth Table below for an AND gate:

A	B	C
0	0	
0	1	
1	0	
1	1	

Q2. What does the .bdf file extension stand for?

Q3. What is the name of the FPGA on the DE2-115 board?

TA Initials: _____

LAB:

2.0 Fill in the Truth Table for *lab1step1*:

A	B	C
0	0	
0	1	
1	0	
1	1	

Logic Expression: _____

This is the prelab for lab #1.

Cpr E 281 LAB1
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 1 Answer Sheet

Quartus Simulation TA Initials: _____ Questa ModelSim TA Initials: _____

4.0 Fill in the Truth Table for *lab1step2*:

W	X	Y	Z
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Logic Expression: _____

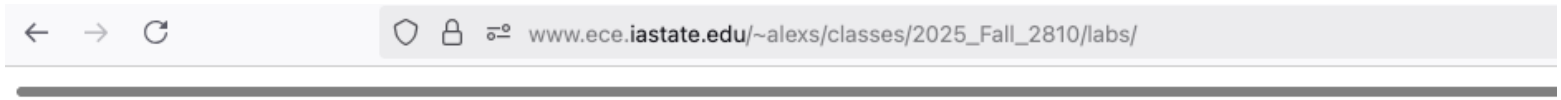
TA Initials: _____

4.0 Fill in the Truth Table for *lab1step3*:

A	B	C	F

Logic Expression: _____

TA Initials: _____



CprE 2810: Digital Logic (Lab Assignments)

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- Lab 13

- Remote Access Instructions

Lab Safety

This class has a substantial hands-on laboratory section. Students will be using expensive, sensitive, and potentially hazardous equipment. Safety in the lab is a number one priority for students and instructors and to ensure a safe laboratory experience, a brief safety presentation will be given during the first lab session. It is mandatory that all students attend this presentation. Moreover, it is expected that students follow any and all posted safety guidelines. All students must sign the lab safety form (posted in the syllabus).

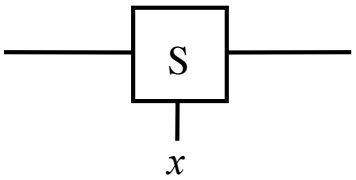
For reference, a copy of the University Laboratory Safety Manual can be found at:
www.ehs.iastate.edu/sites/default/files/uploads/publications/manuals/labsm.pdf

See also the safety page of the ECpE Department:

http://www.ece.iastate.edu/the-department/safety/

A Binary Switch

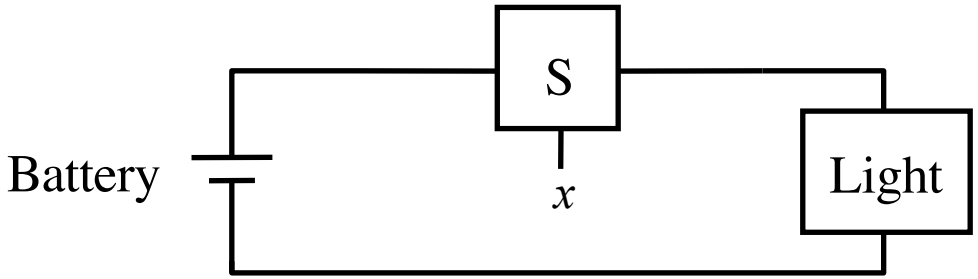
(a) Two states of a switch



(b) Symbol for a switch

[Figure 2.1 from the textbook]

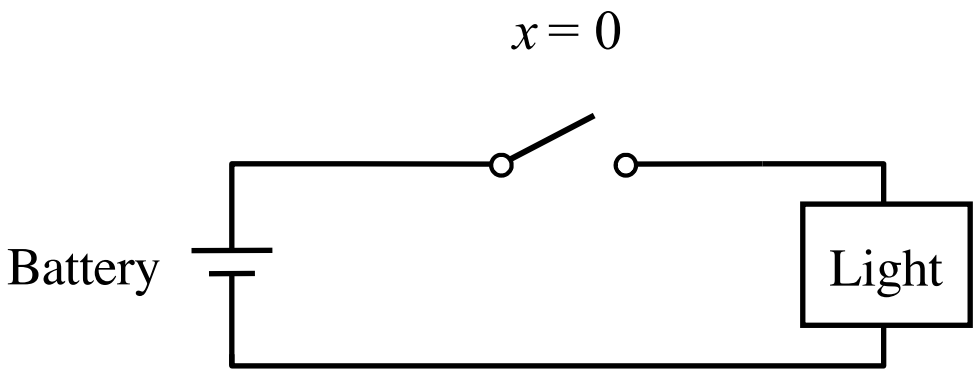
A Light Controlled by a Switch



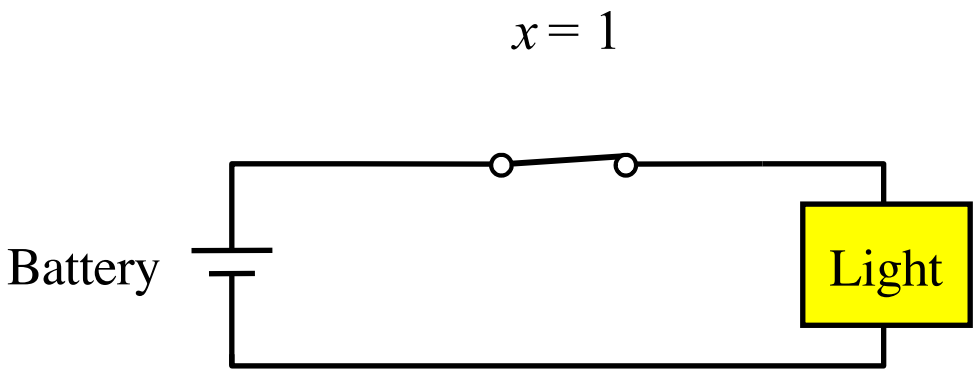
(a) Simple connection to a battery

[Figure 2.2a from the textbook]

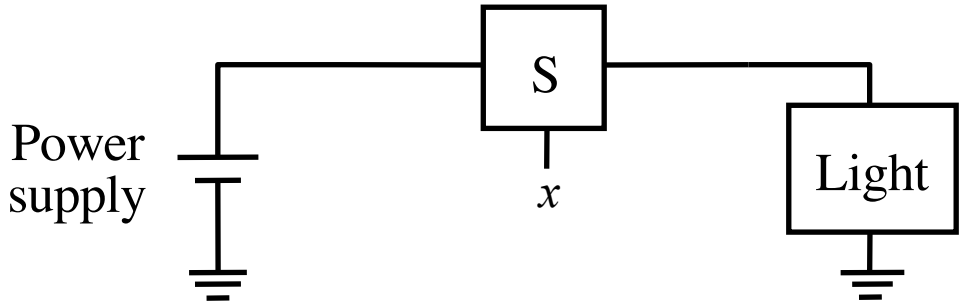
A Light Controlled by a Switch



A Light Controlled by a Switch



A Light Controlled by a Switch

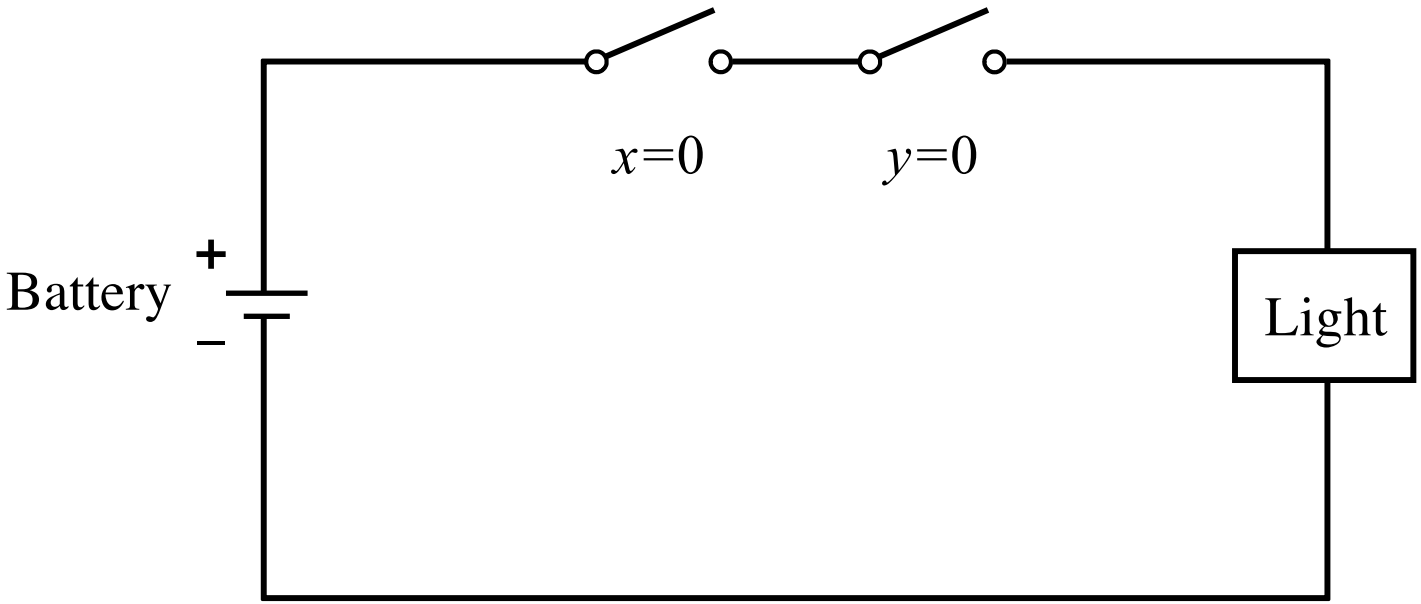


(b) Using a ground connection as the return path

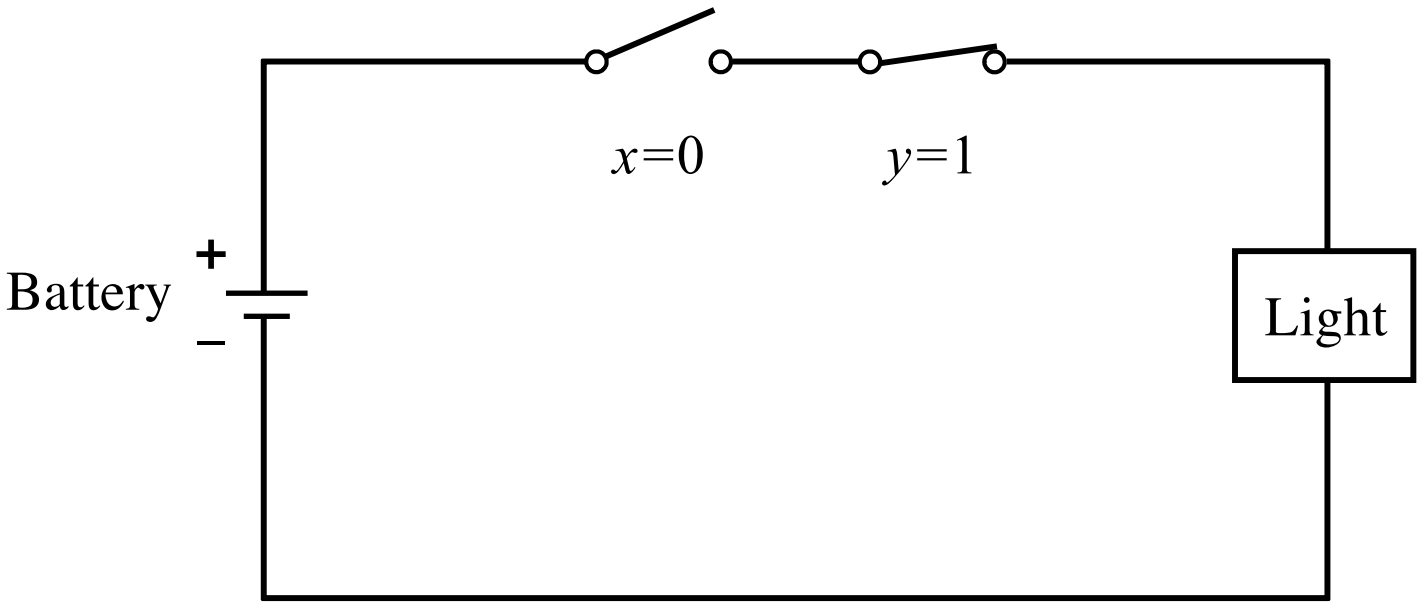
[Figure 2.2b from the textbook]

Logic AND with Switches
(series connection of the switches)

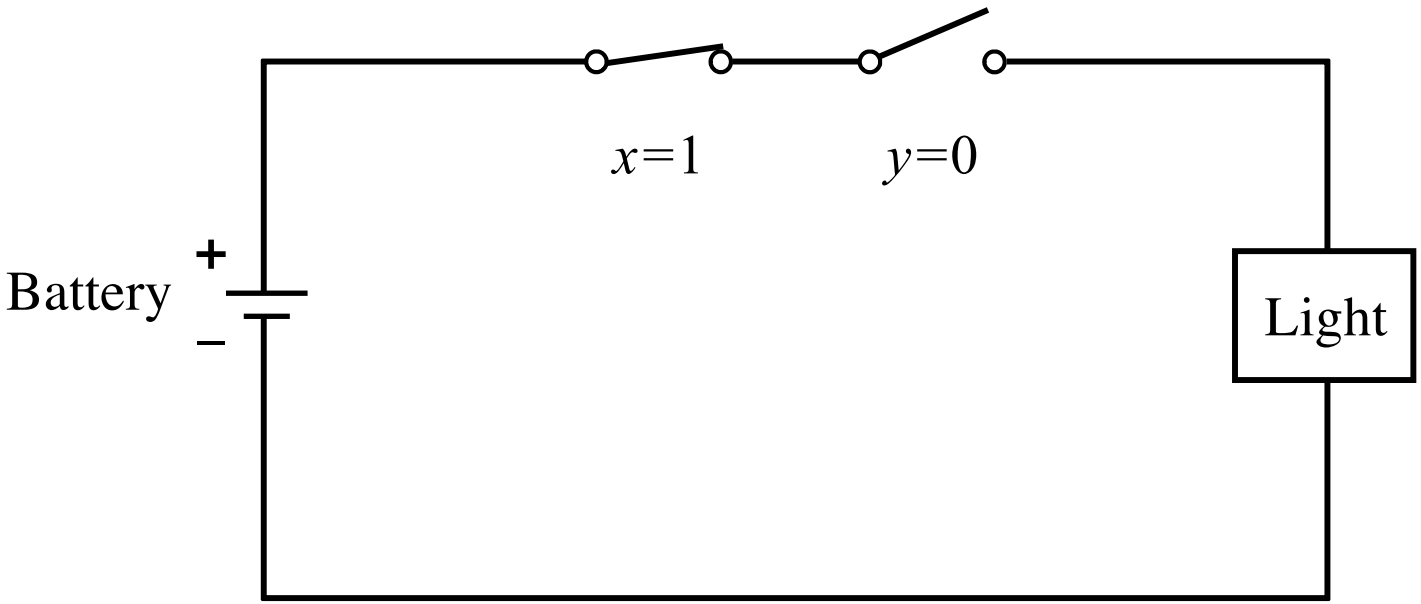
AND Circuit



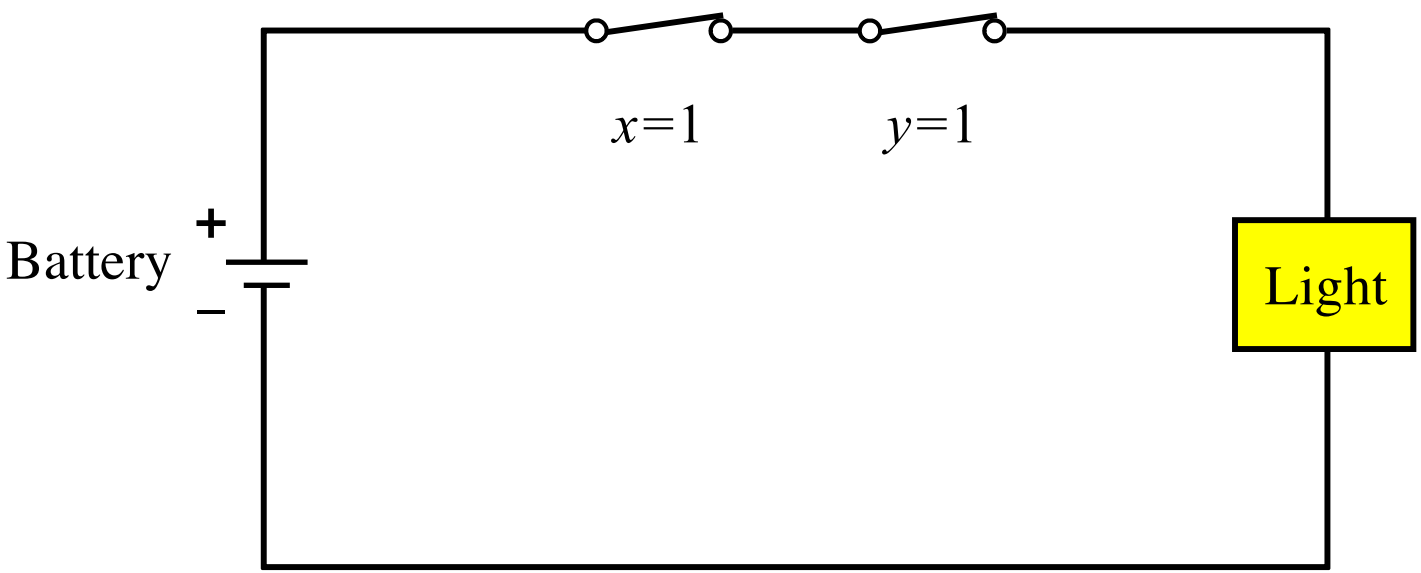
AND Circuit



AND Circuit

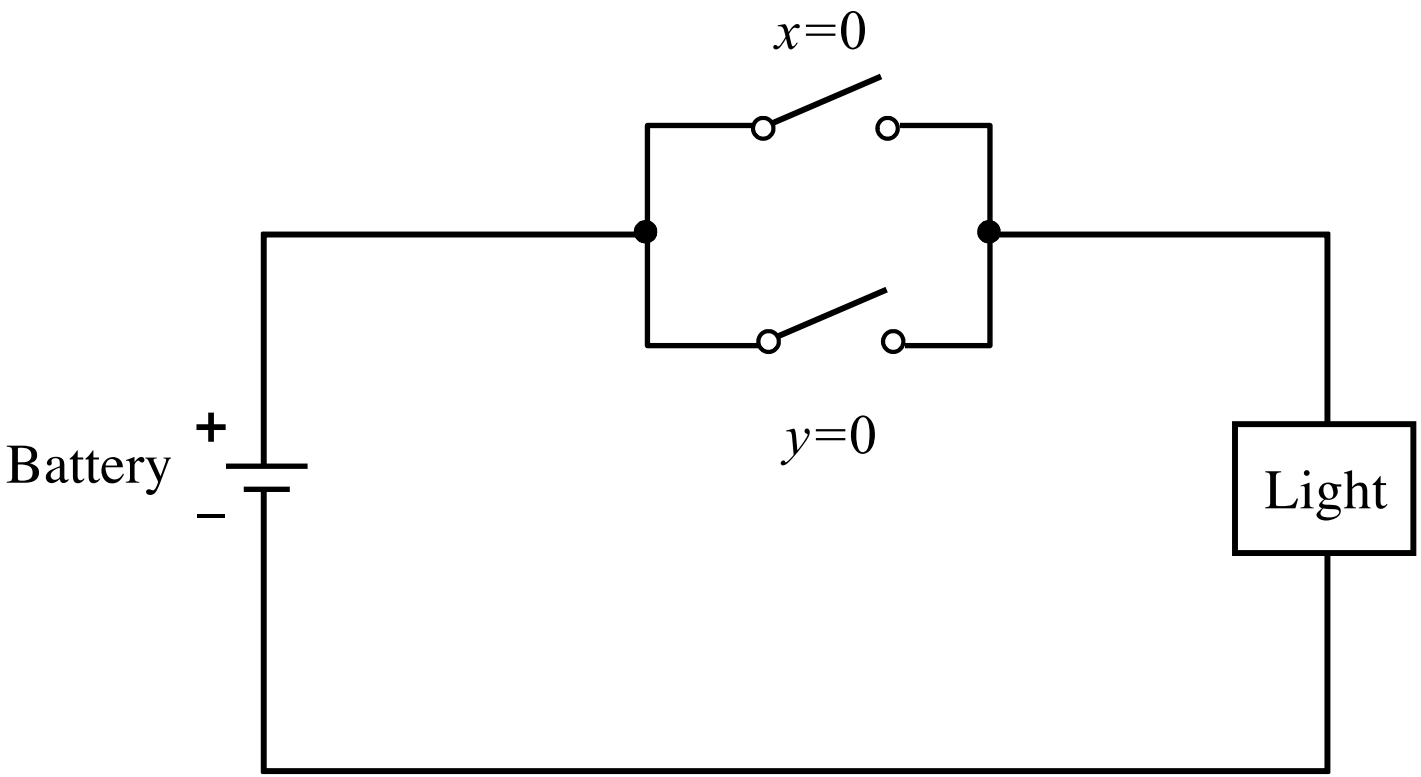


AND Circuit

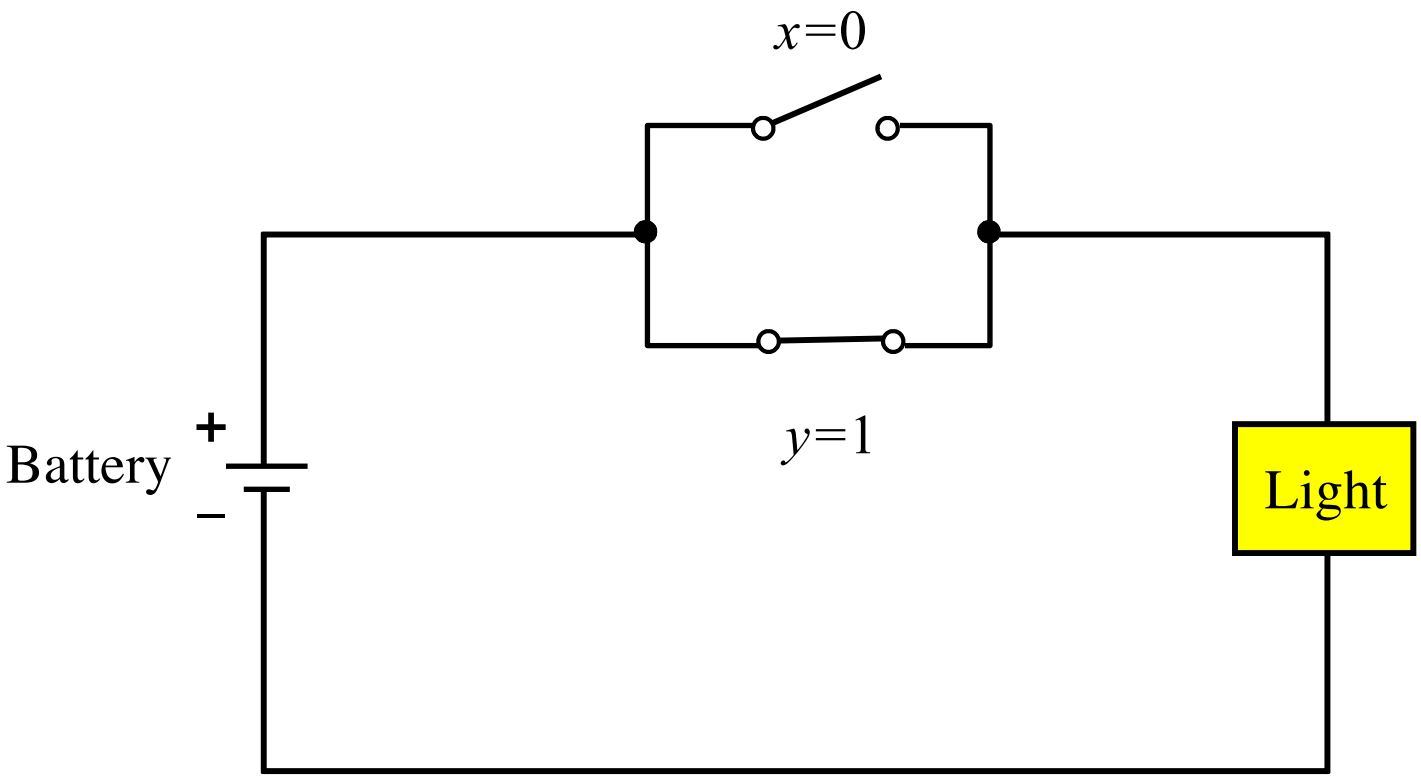


Logic OR with Switches
(parallel connection of the switches)

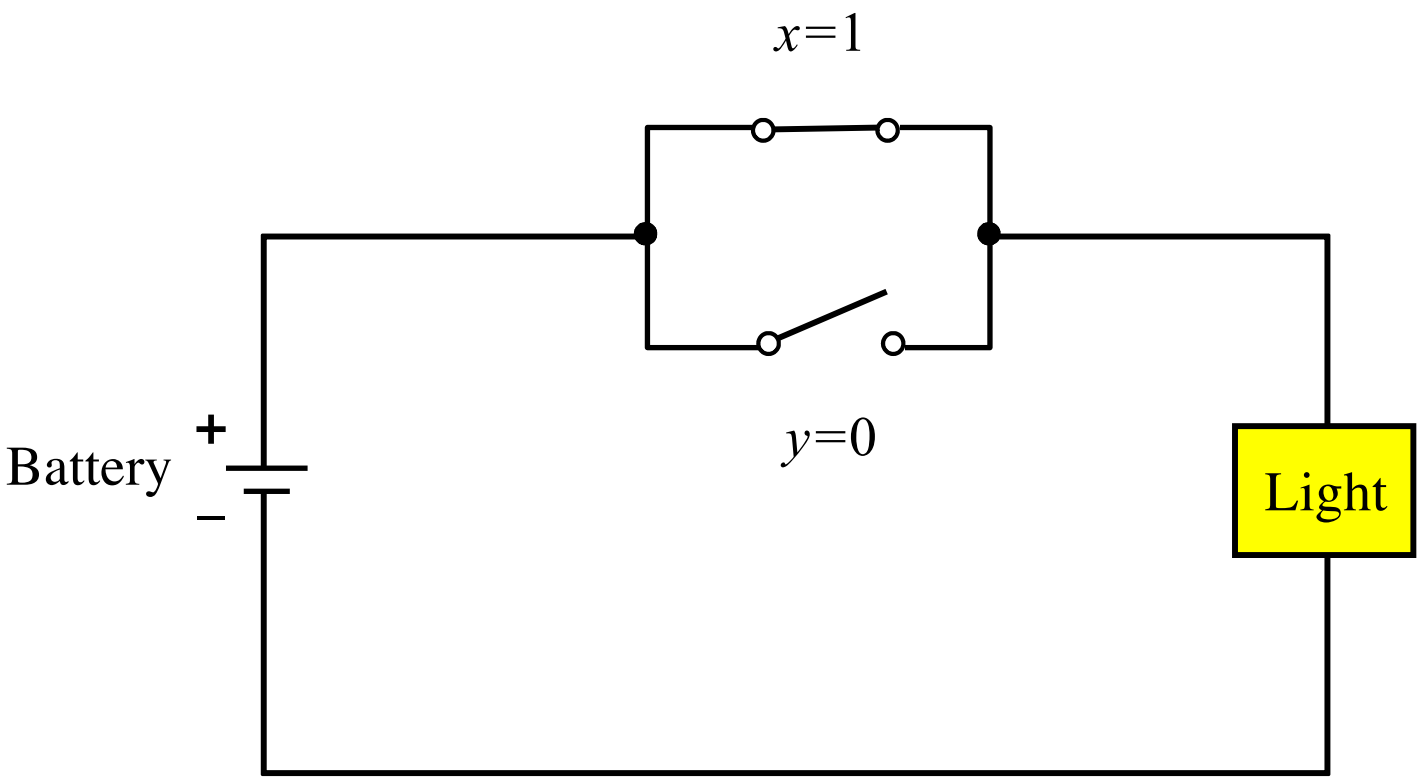
OR Circuit



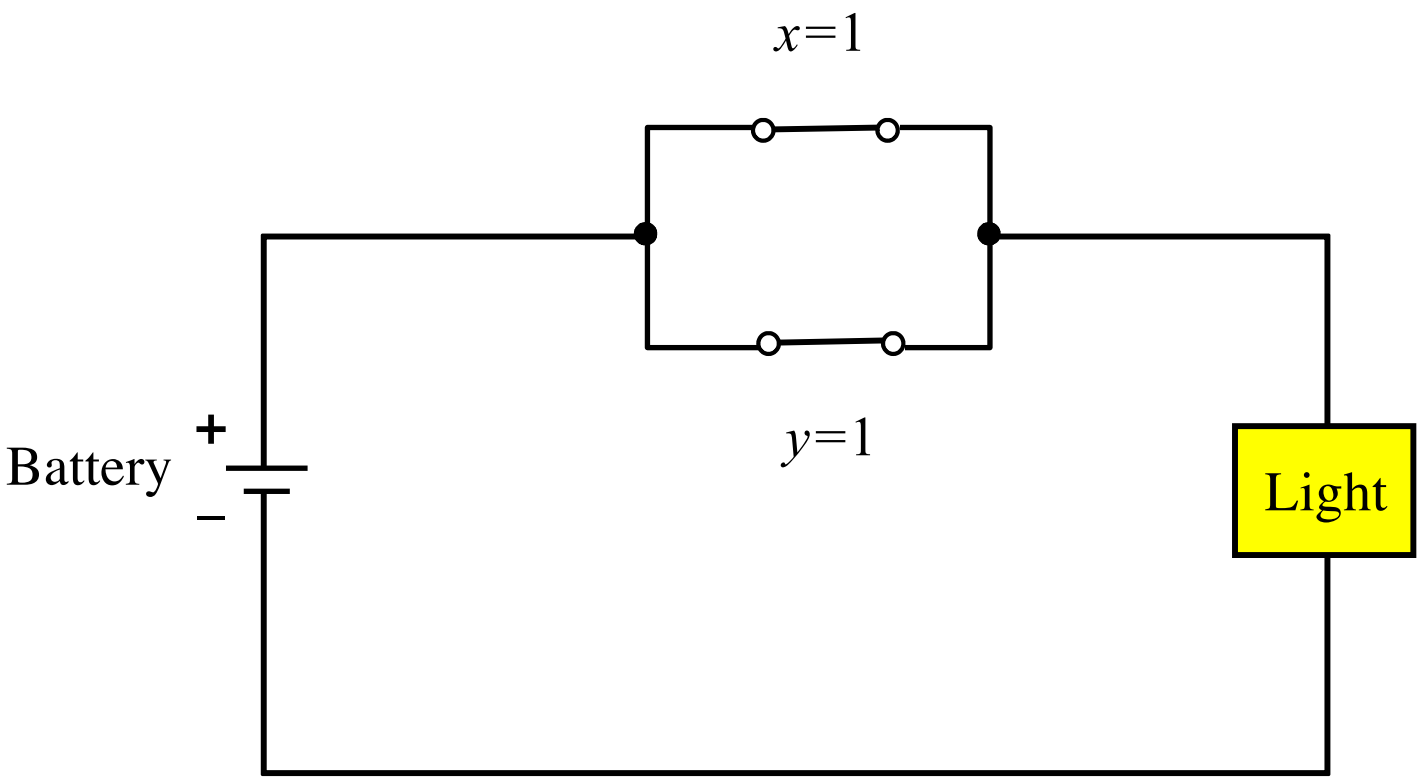
OR Circuit



OR Circuit

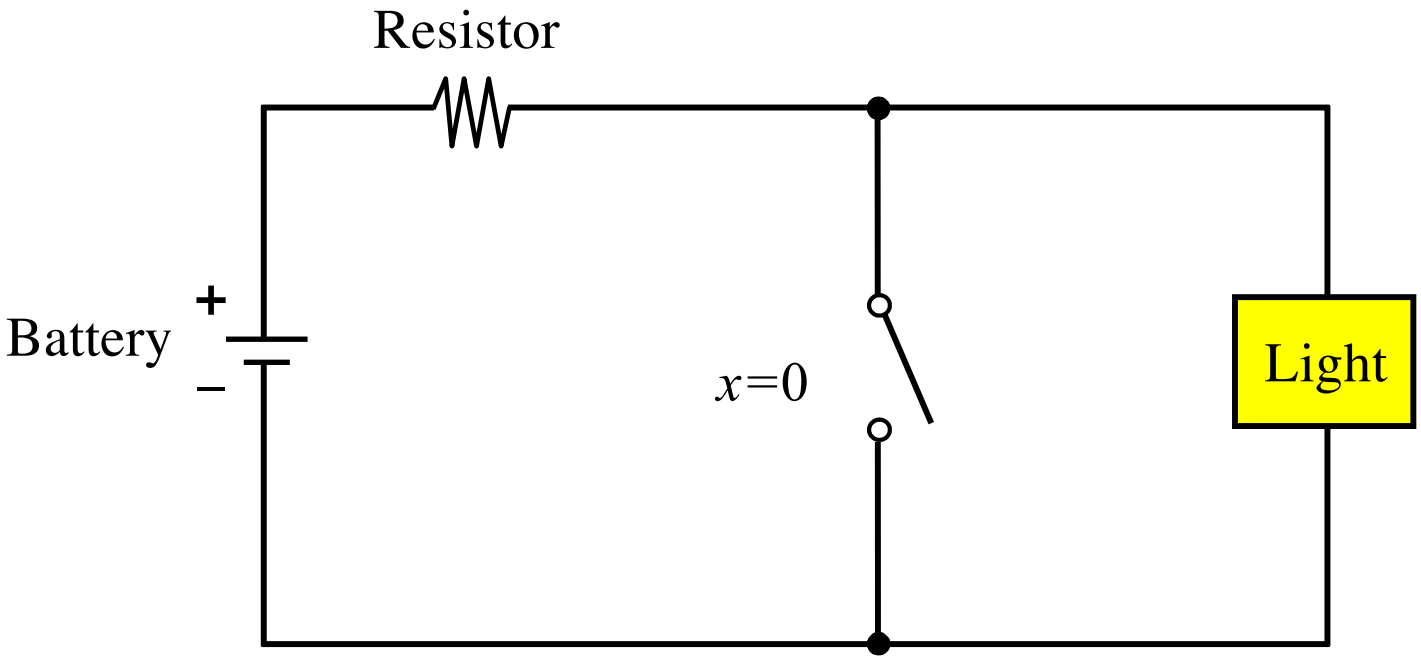


OR Circuit

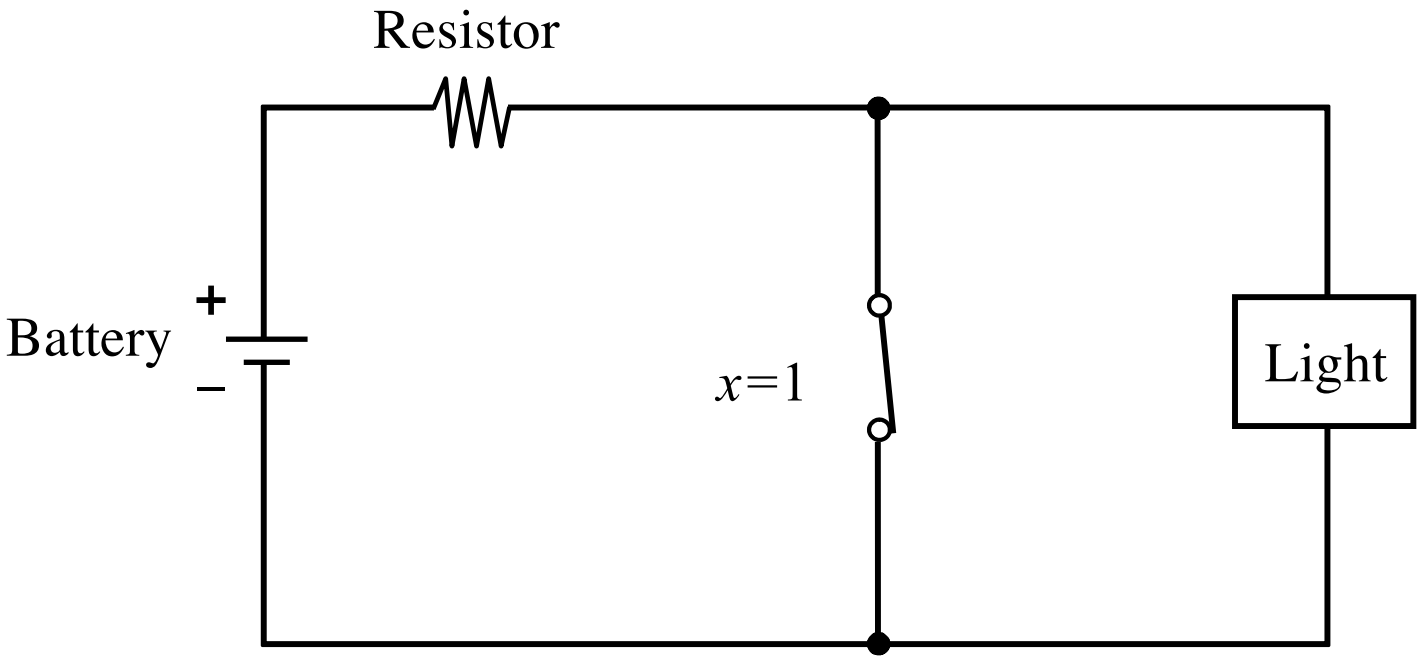


Logic NOT with a Switch
(an inverting circuit)

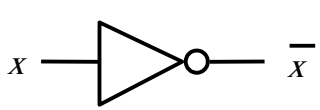
NOT Circuit



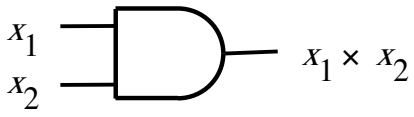
NOT Circuit



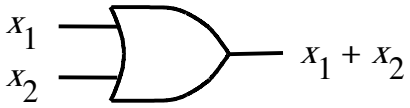
The Three Basic Logic Gates



NOT gate



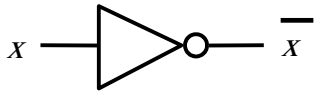
AND gate



OR gate

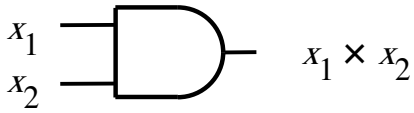
[Figure 2.8 from the textbook]

Truth Table for NOT



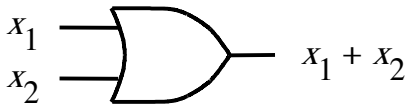
x	$\overline{x}$
0	1
1	0

Truth Table for AND



x_1	x_2	$x_1 \cdot x_2$
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table for OR



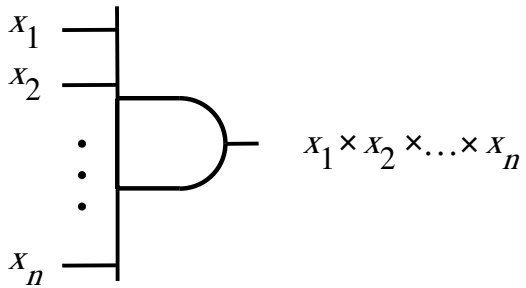
x_1	x_2	$x_1 + x_2$
0	0	0
0	1	1
1	0	1
1	1	1

Truth Tables for AND and OR

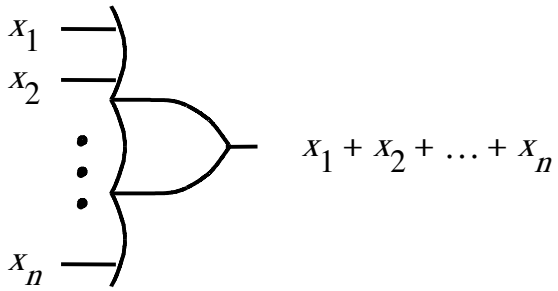
x_1	x_2	$x_1 \cdot x_2$	$x_1 + x_2$
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	1
		AND	OR

[Figure 2.6b from the textbook]

Logic Gates with n Inputs



AND gate



OR gate

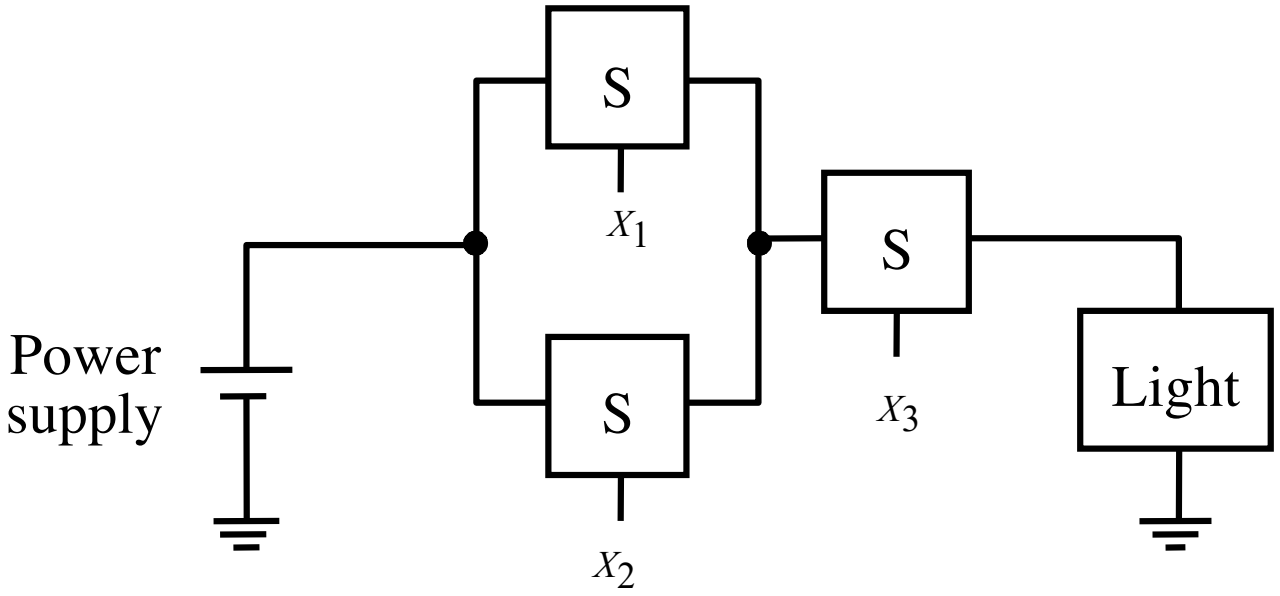
[Figure 2.8 from the textbook]

Truth Table for 3-input AND and OR

x_1	x_2	x_3	$x_1 \cdot x_2 \cdot x_3$	$x_1 + x_2 + x_3$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

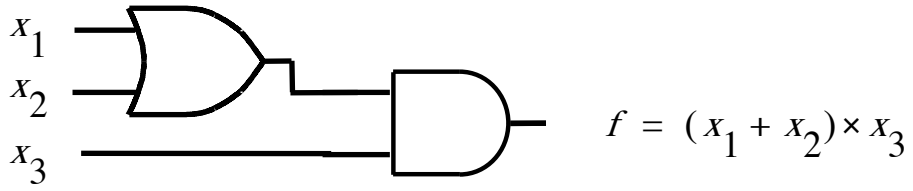
[Figure 2.7 from the textbook]

A series-parallel connection of the switches



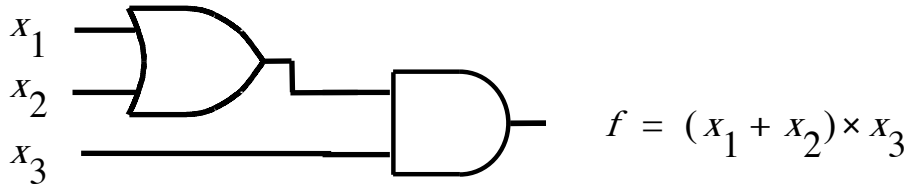
[Figure 2.4 from the textbook]

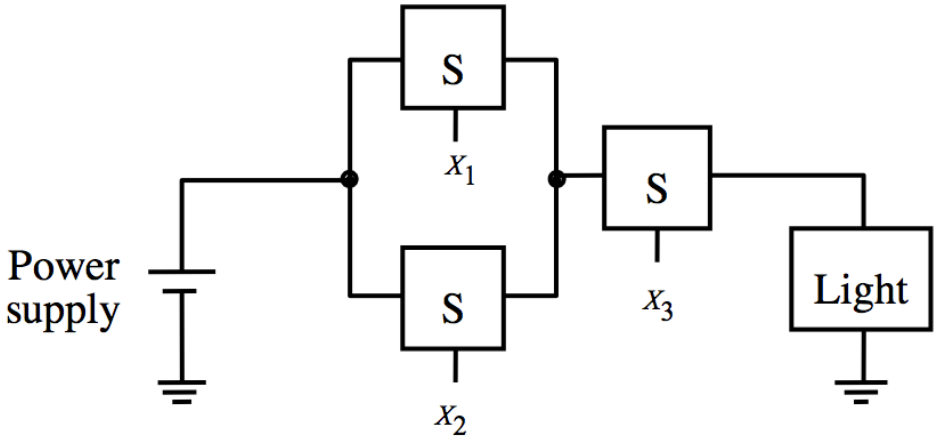
Example of a Logic Circuit Implemented with Logic Gates



[Figure 2.8 from the textbook]

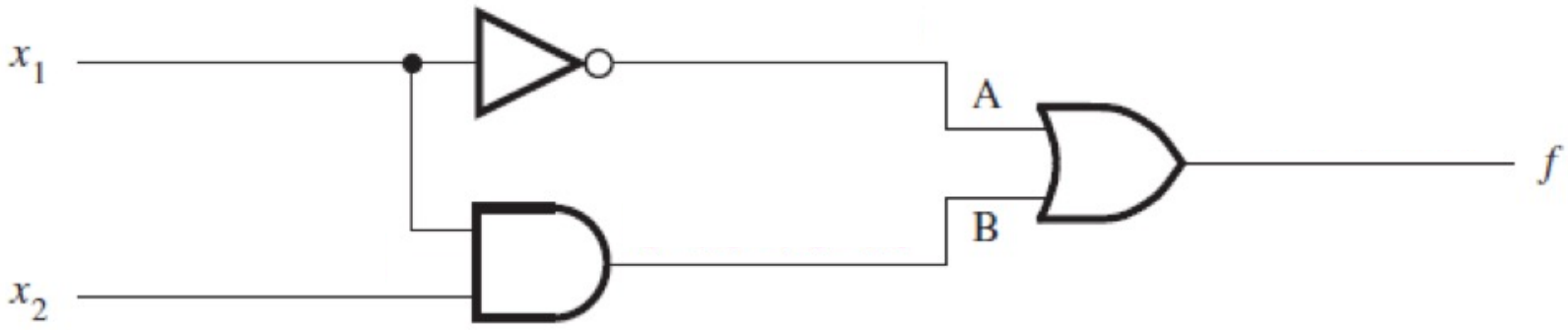
Example of a Logic Circuit Implemented with Logic Gates





[Figure 2.8 from the textbook]

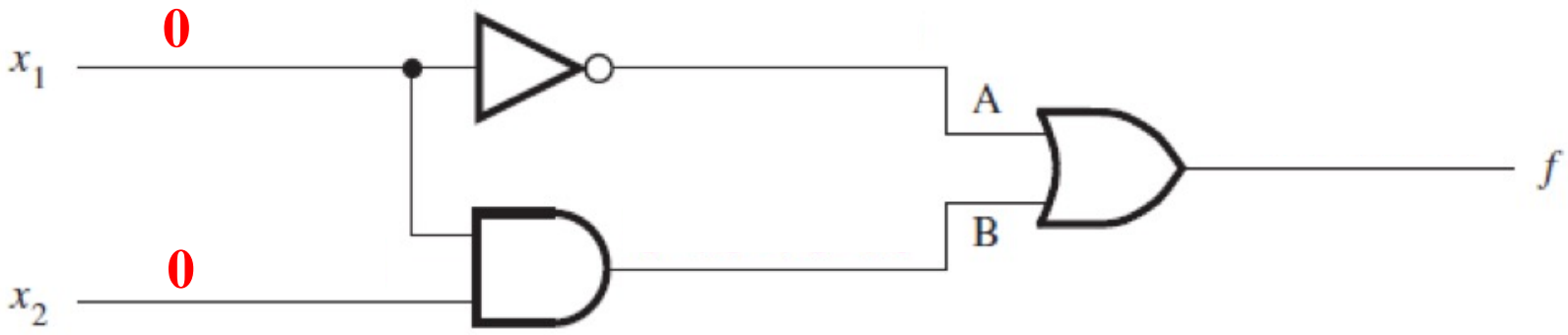
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

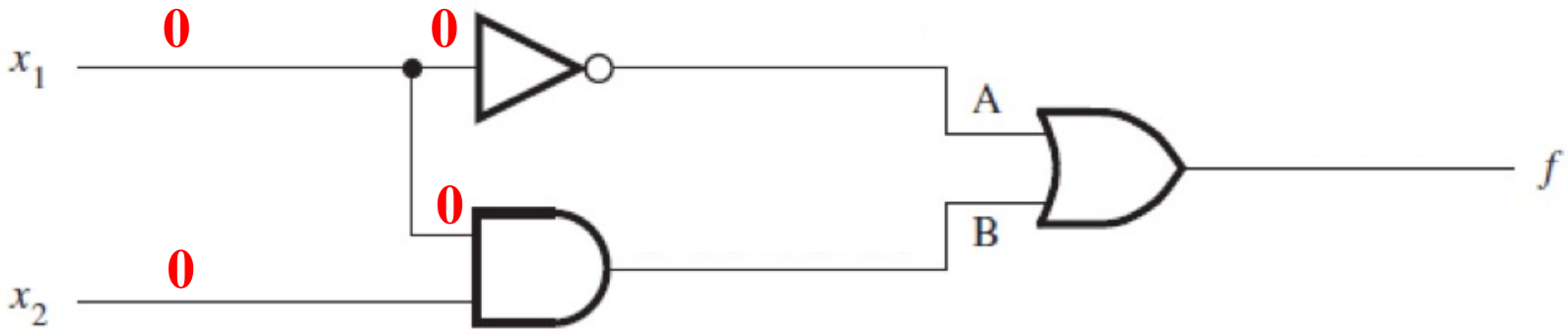
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

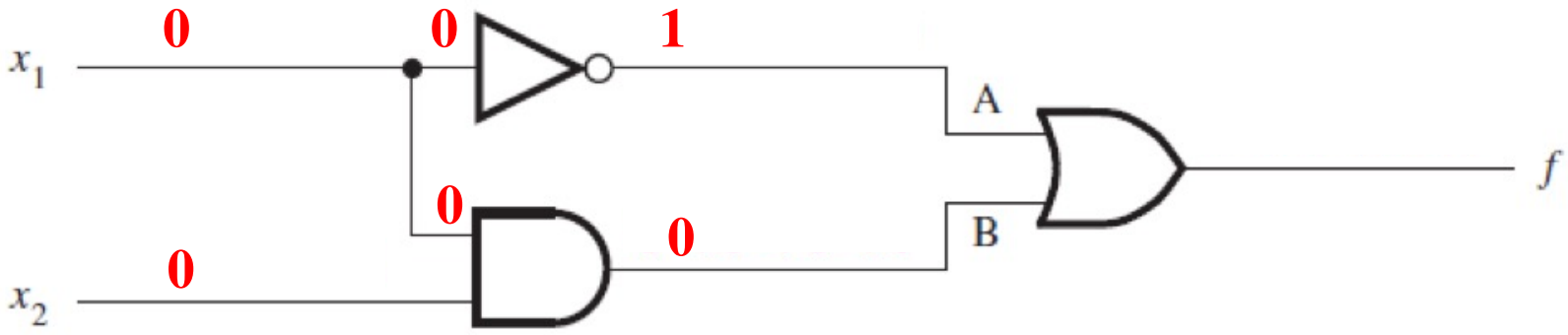
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

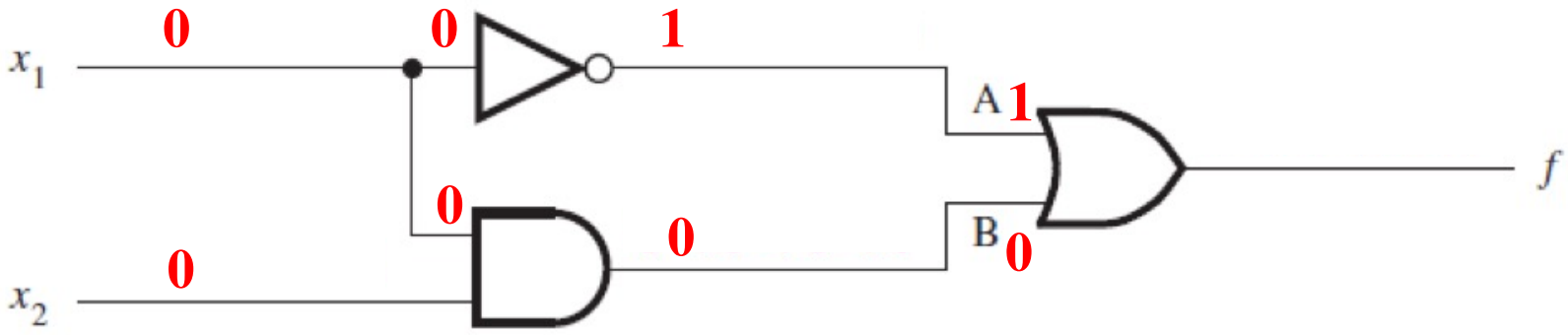
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

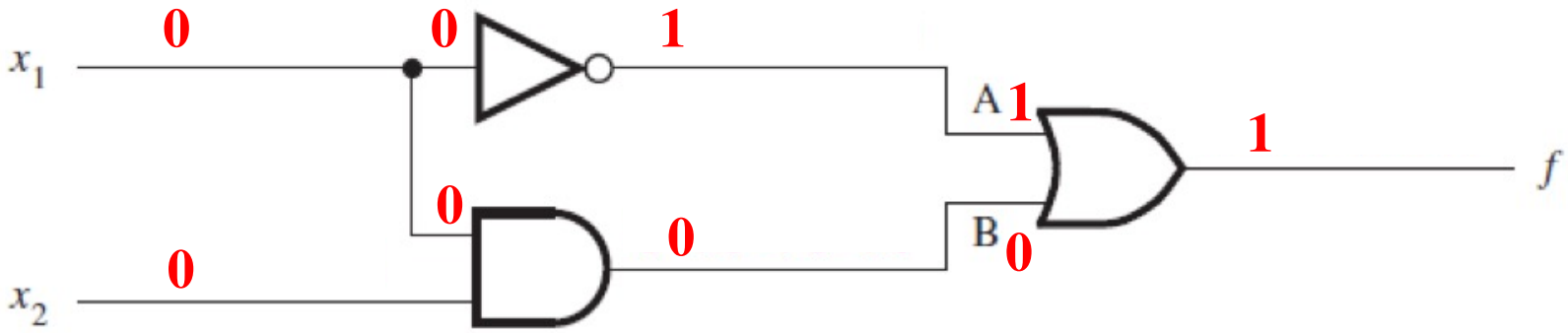
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

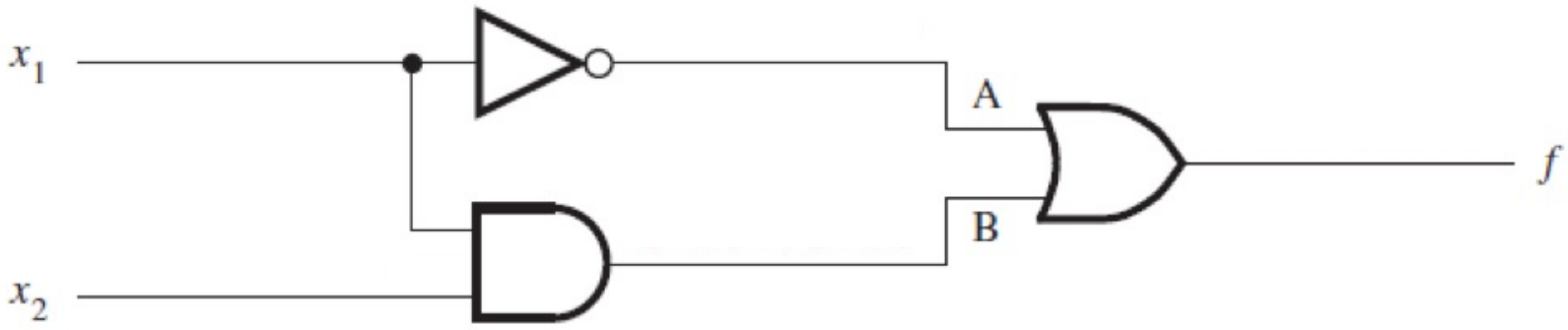
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

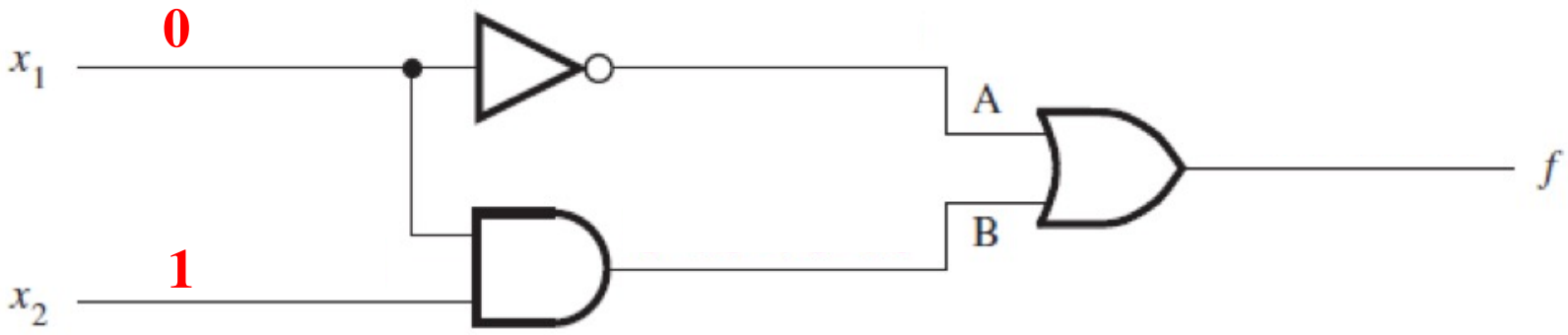
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

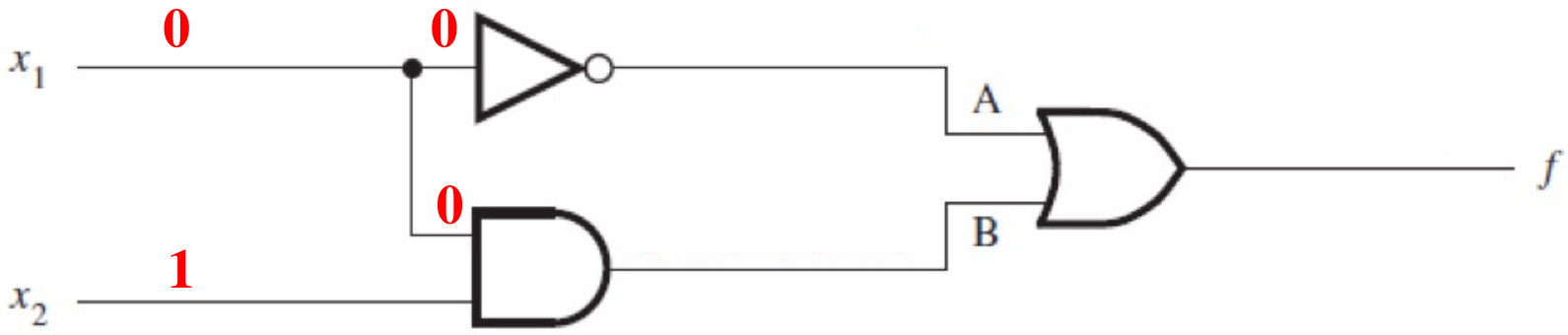
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

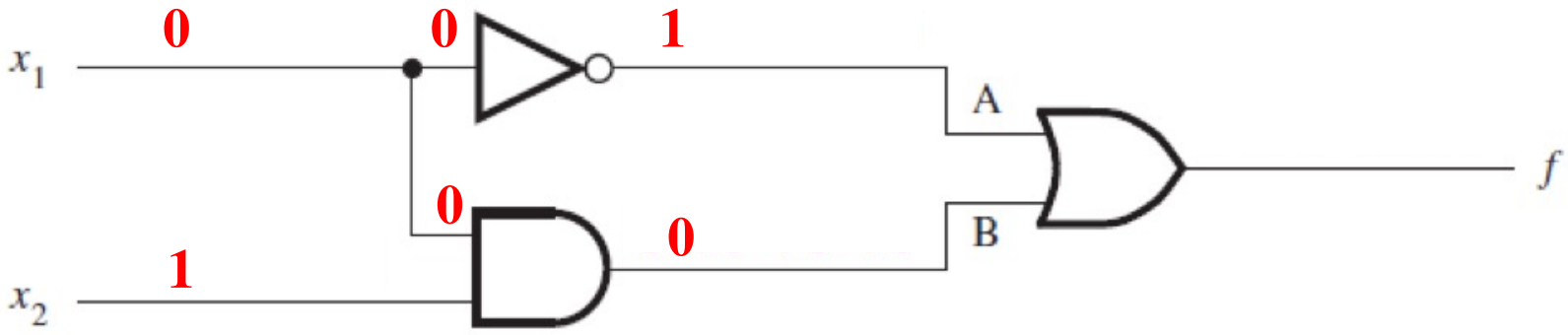
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

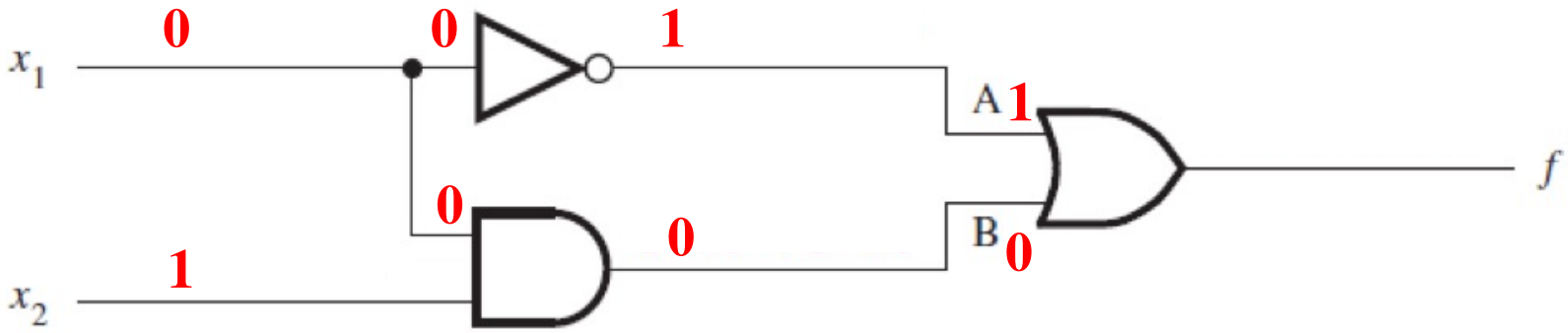
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

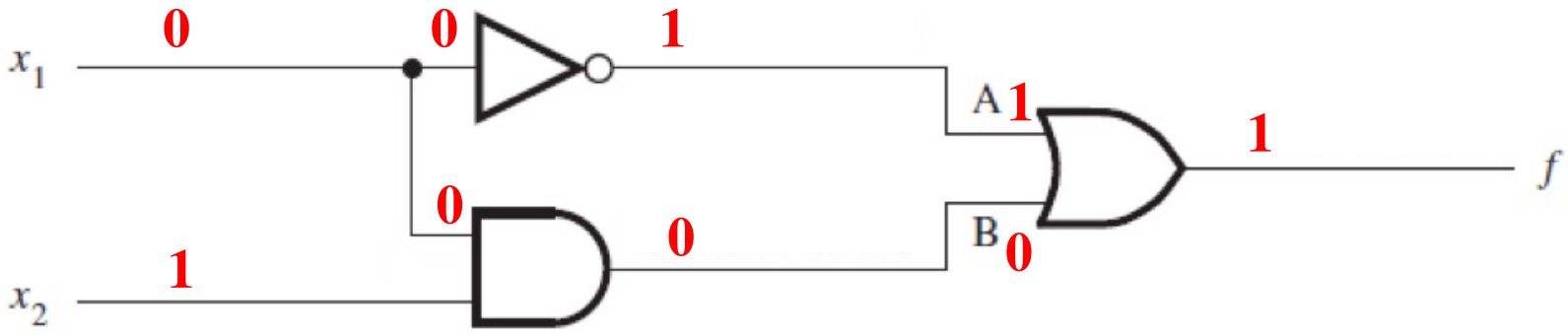
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

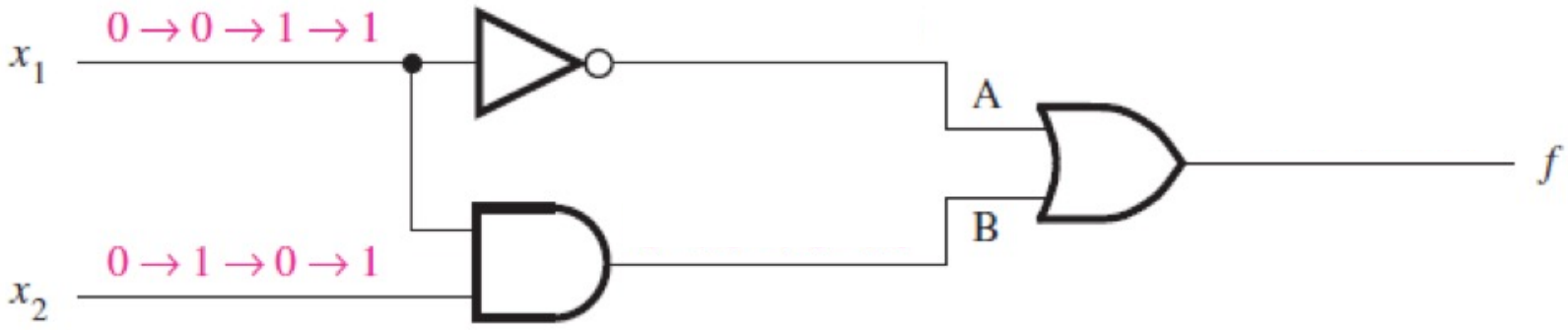
Circuit Analysis



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

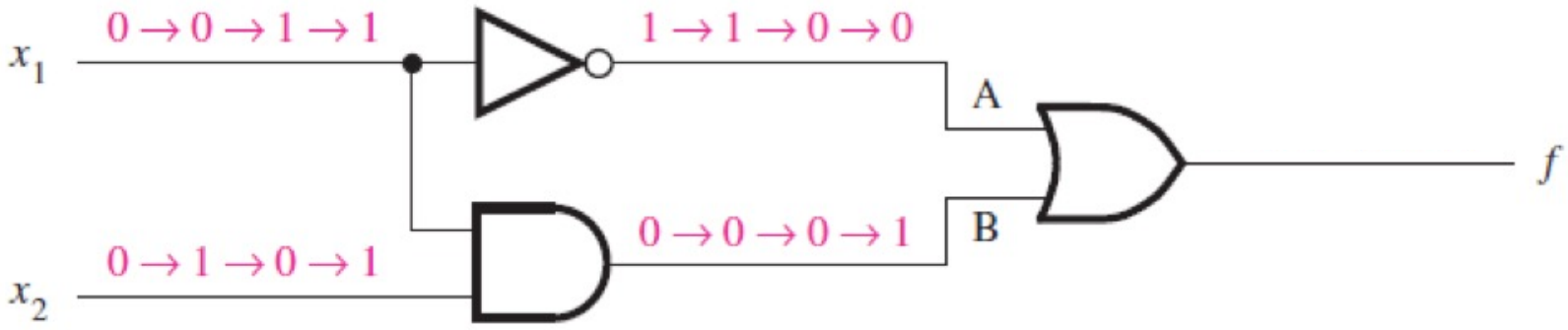
Circuit Analysis with Sequential Inputs



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs



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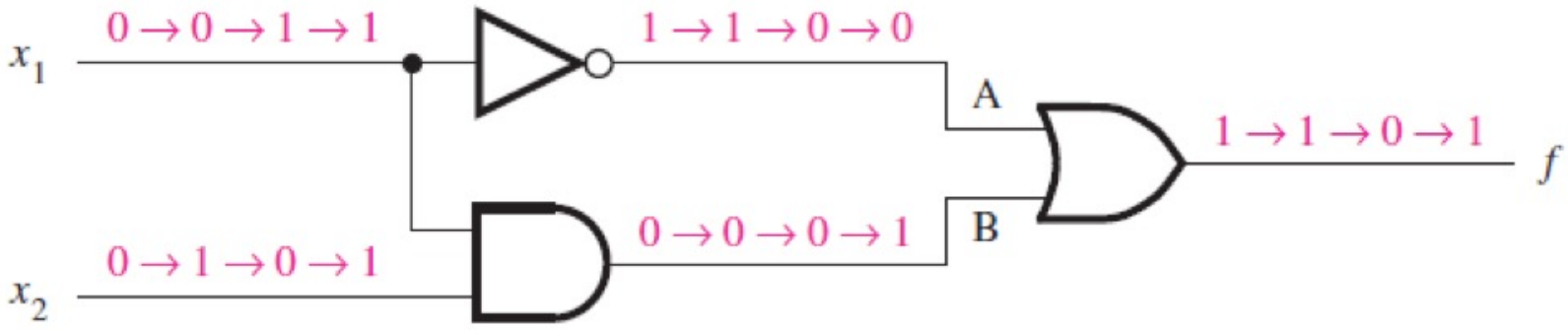
[Figure 2.10 from the textbook]

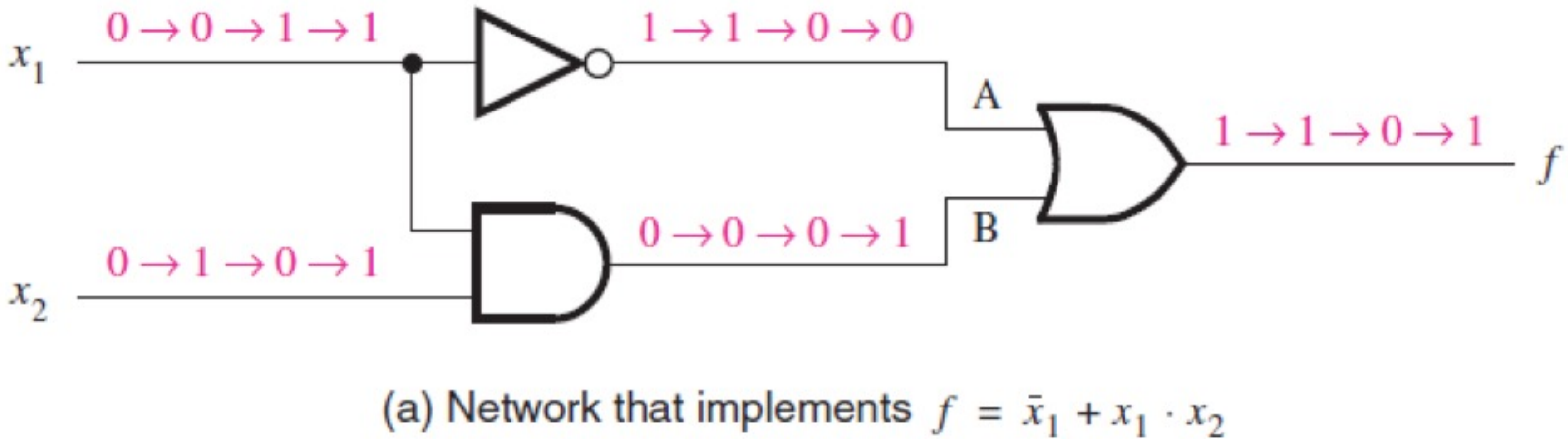
Circuit Analysis with Sequential Inputs



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs



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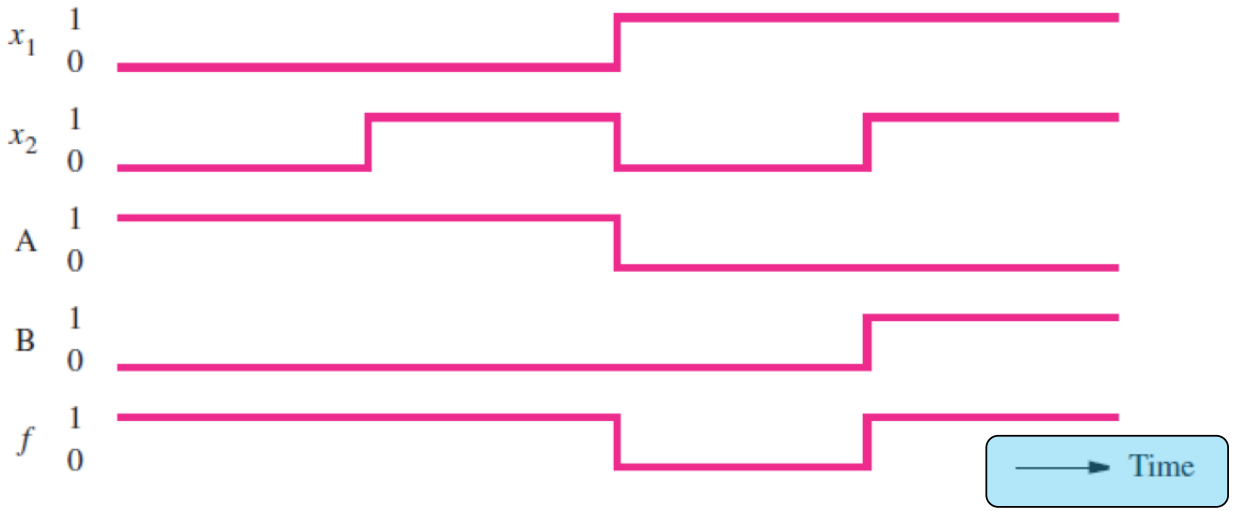
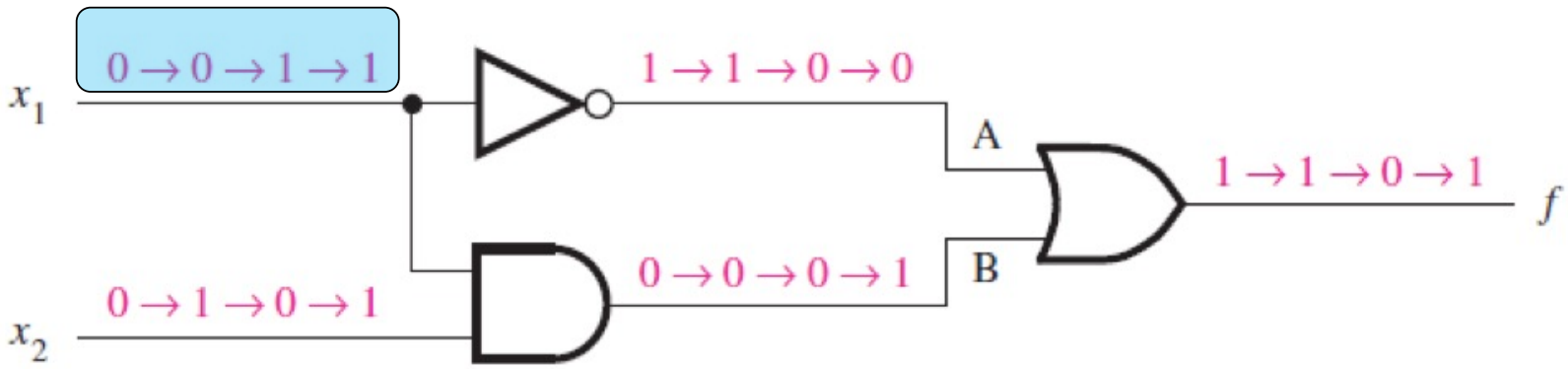
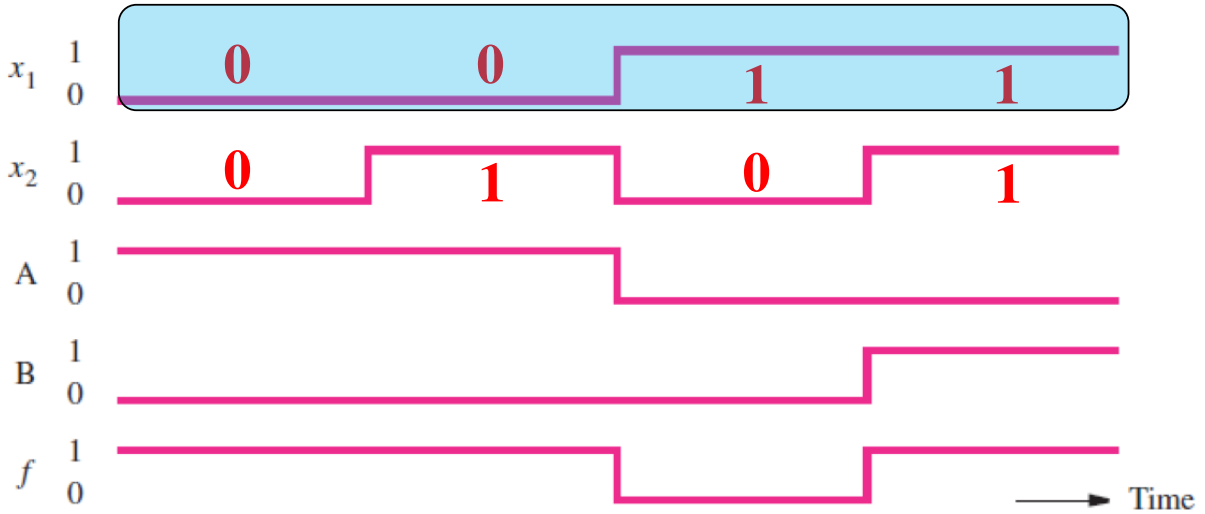


[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs

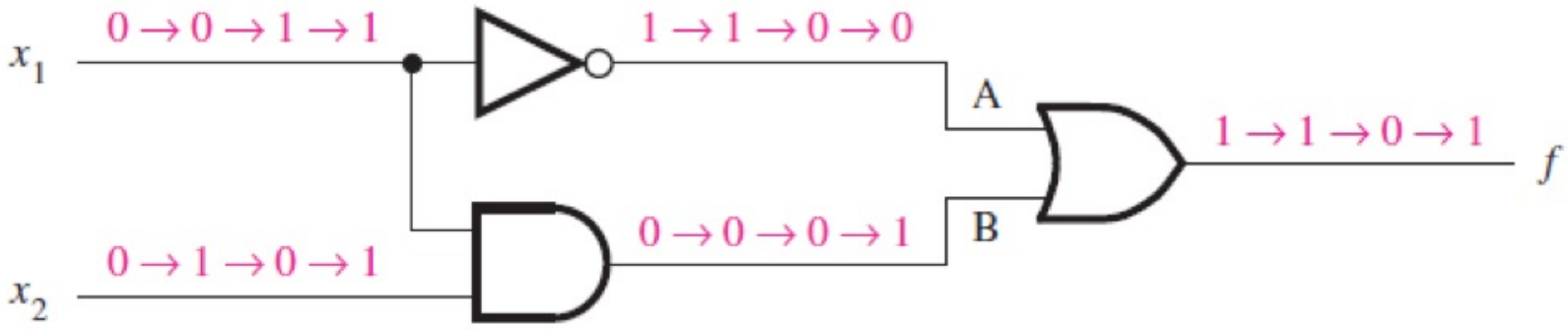


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs



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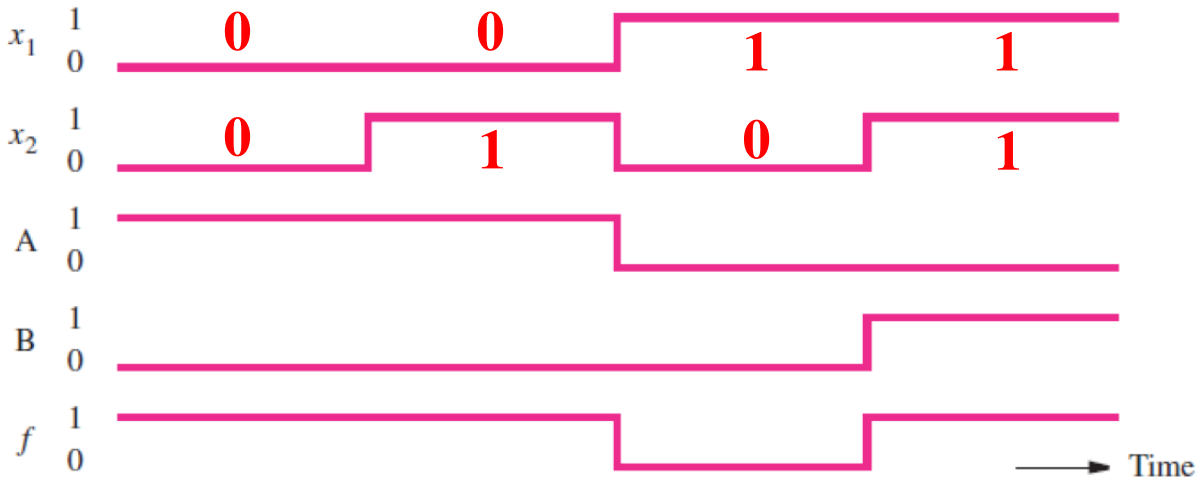
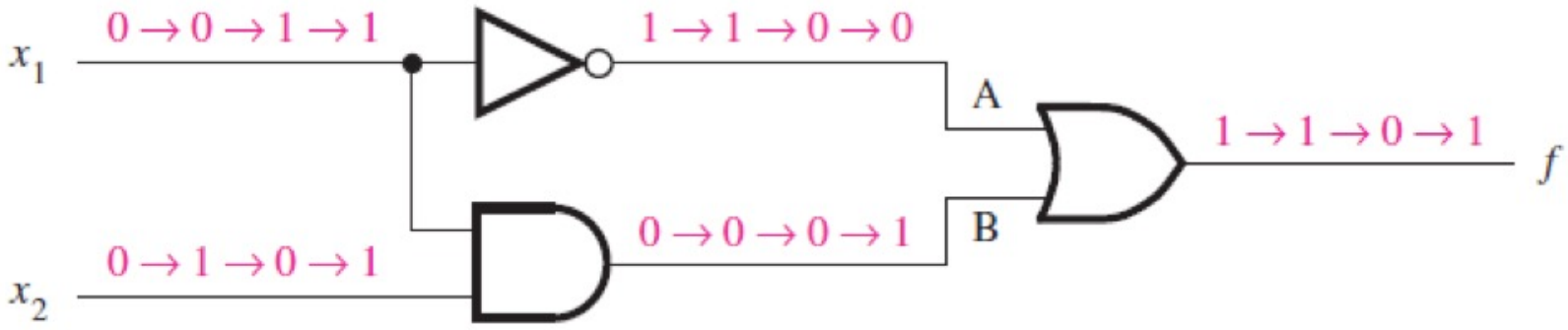


[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs



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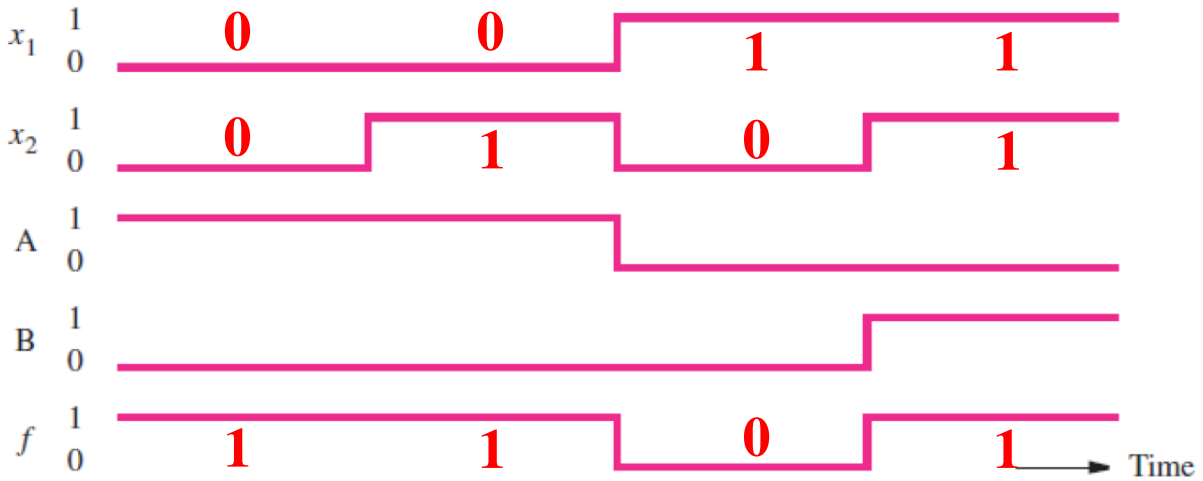
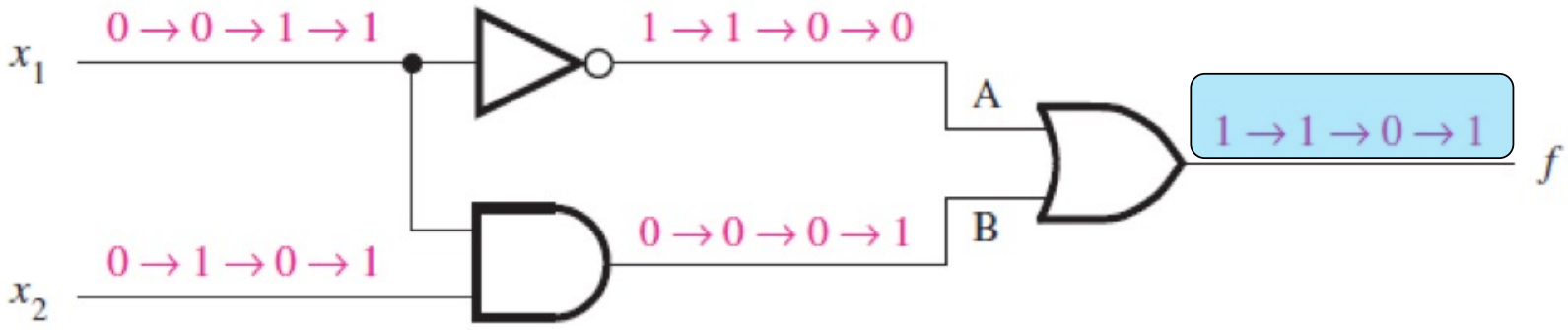
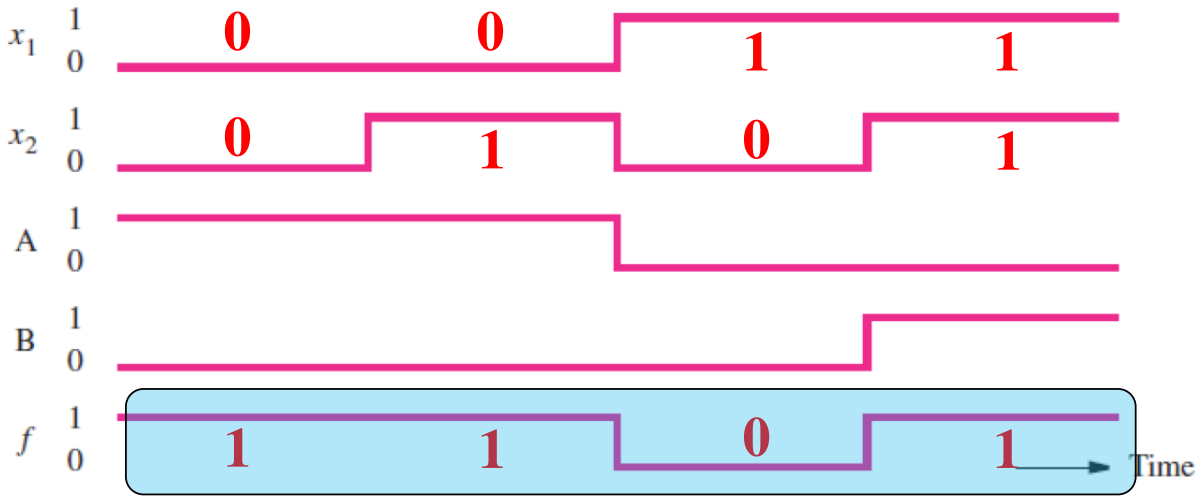


[Figure 2.10 from the textbook]

Circuit Analysis with Sequential Inputs

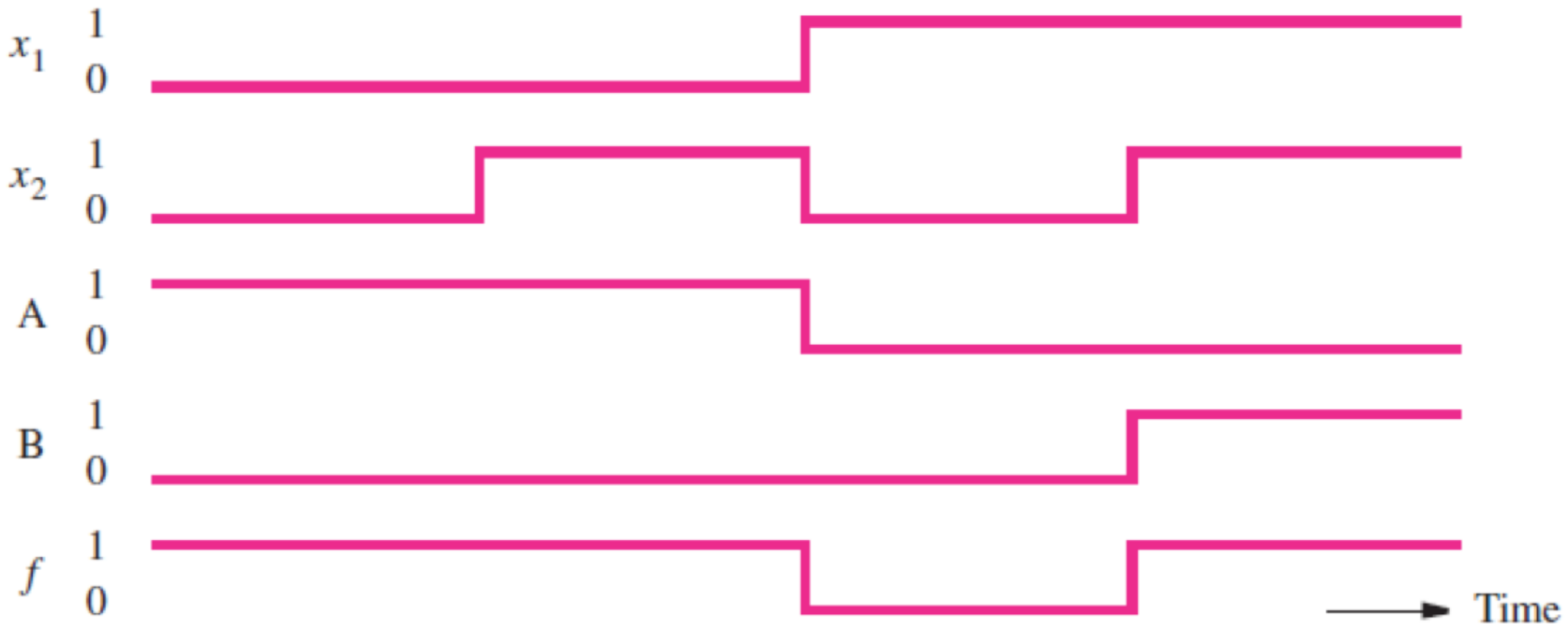


(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$



[Figure 2.10 from the textbook]

Timing Diagram



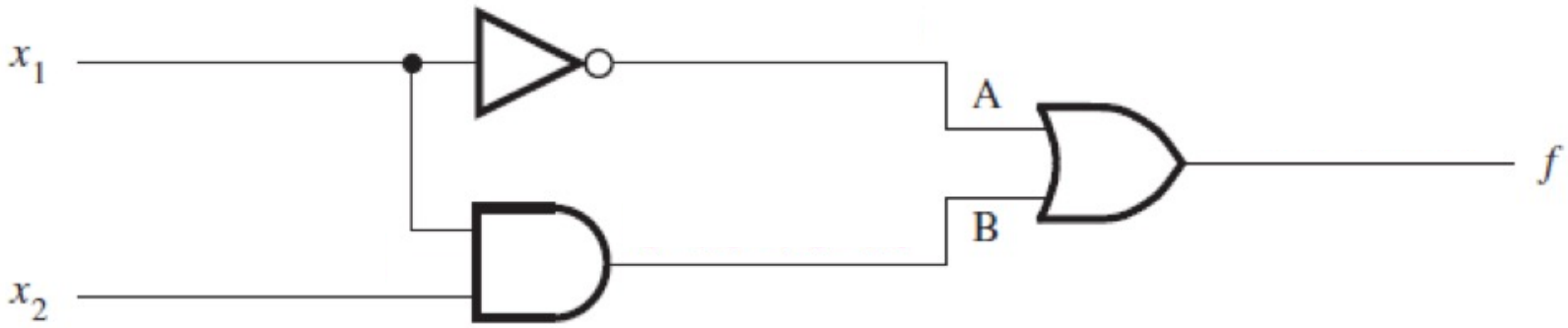
[Figure 2.10 from the textbook]

Truth Table for this Logic Circuit

x_1	x_2	$f(x_1, x_2)$
0	0	1
0	1	1
1	0	0
1	1	1

[Figure 2.10 from the textbook]

Truth Table for $f = \overline{x_1} + x_1 x_2$



x_1	x_2	$f(x_1, x_2)$
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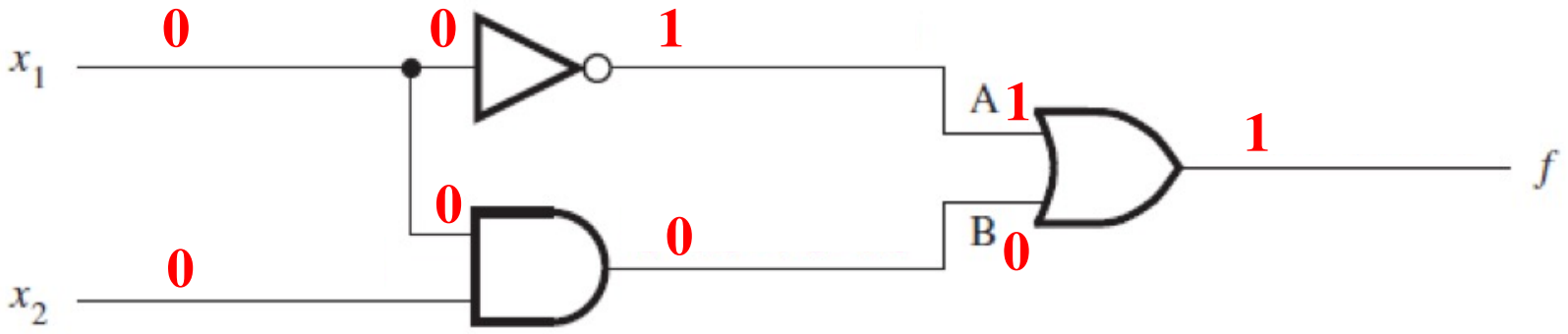
0	1	1
1	0	0
1	1	1

Truth Table for $f = \overline{x_1} + x_1 x_2$



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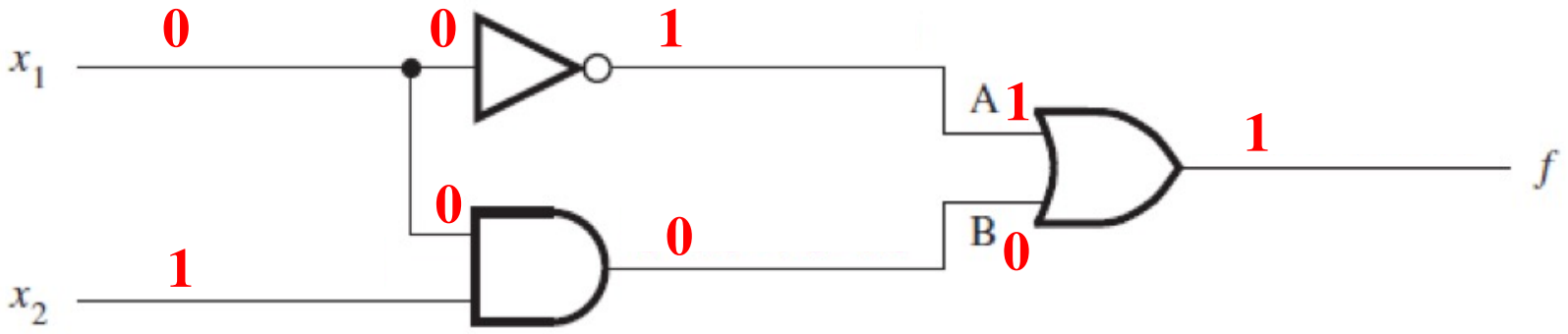
Truth Table for $f = \overline{x_1} + x_1 x_2$



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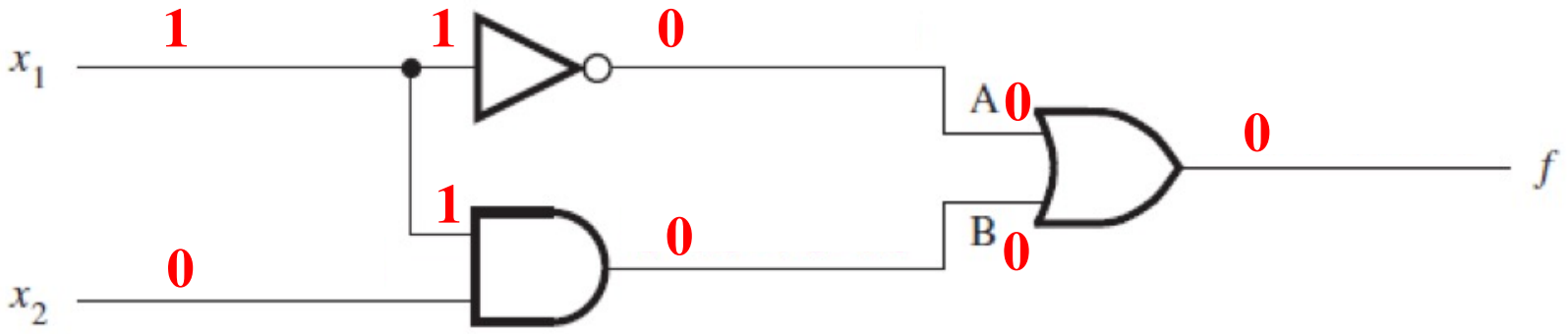

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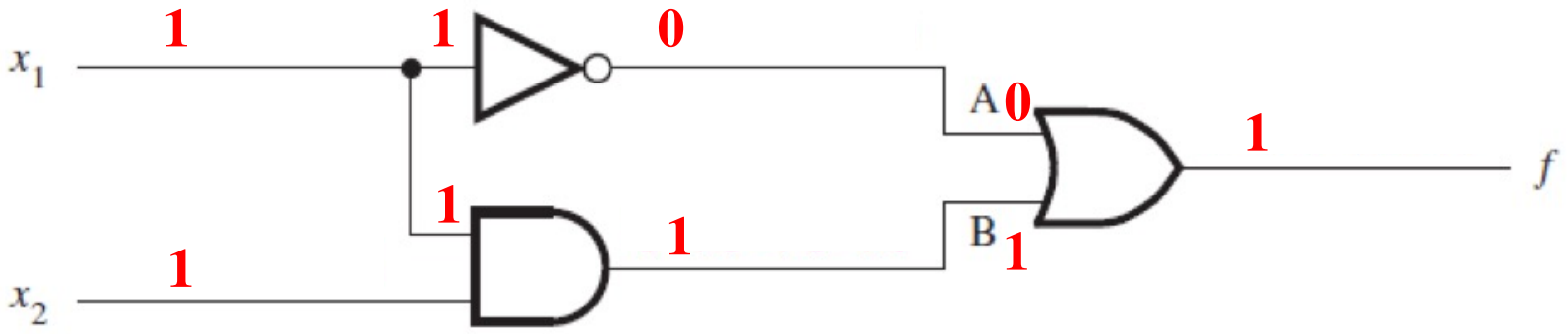
Truth Table for $f = \overline{x_1} + x_1 x_2$



x_1	x_2	$f(x_1, x_2)$
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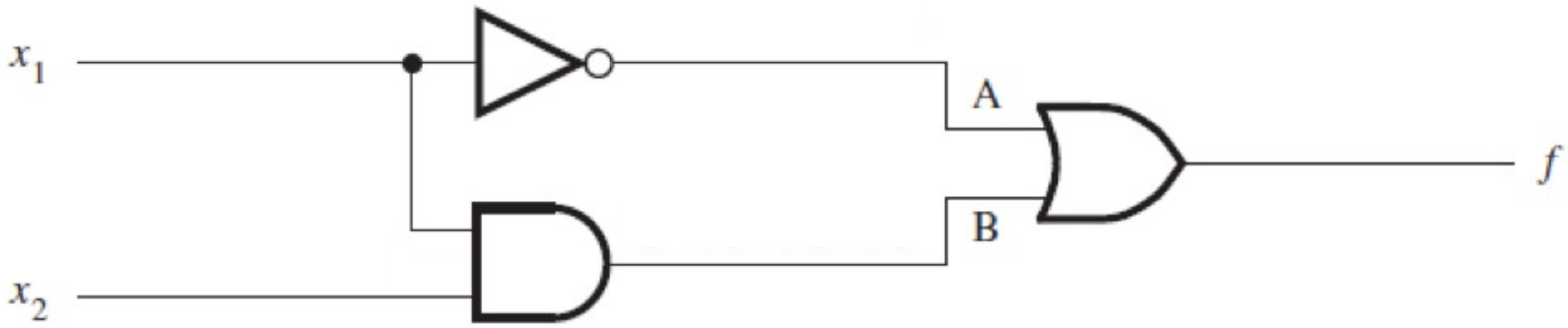
1	0	0
1	1	1

Truth Table for $f = \overline{x_1} + x_1 x_2$



x_1	x_2	$f(x_1, x_2)$
0	0	1
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1	0	0
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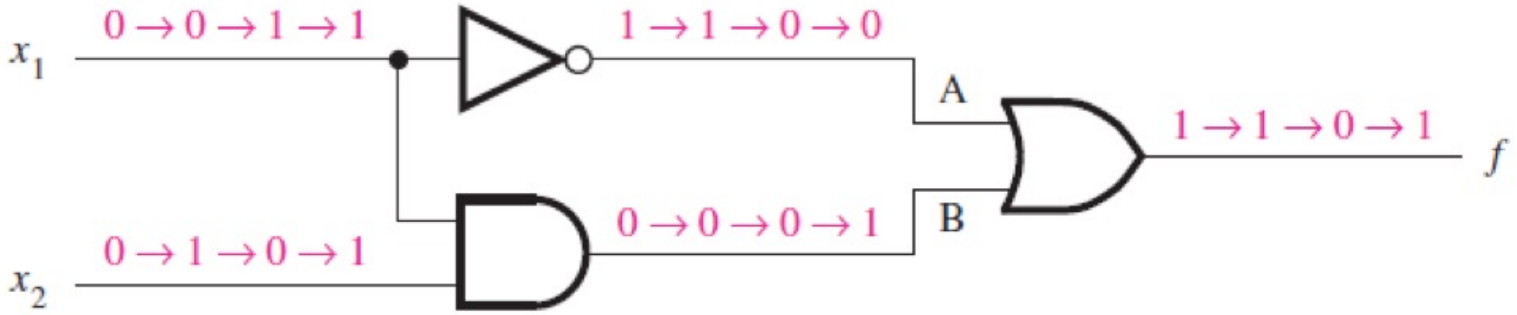
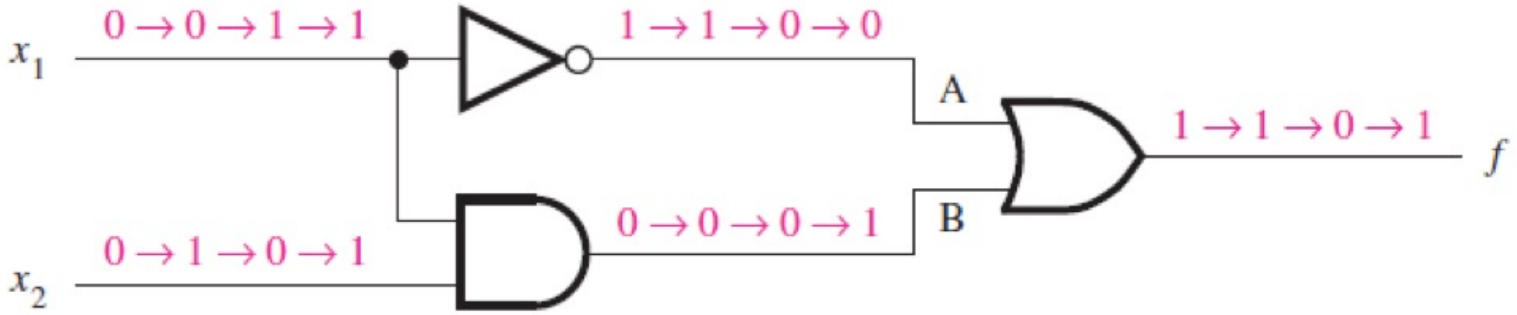
Functionally Equivalent Circuits



(a) Network that implements $f = \bar{x}_1 + x_1 \cdot x_2$

[Figure 2.10 from the textbook]

Functionally Equivalent Circuits



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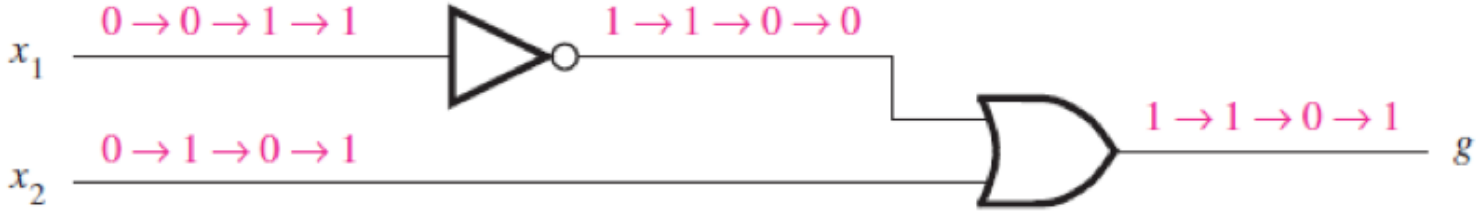
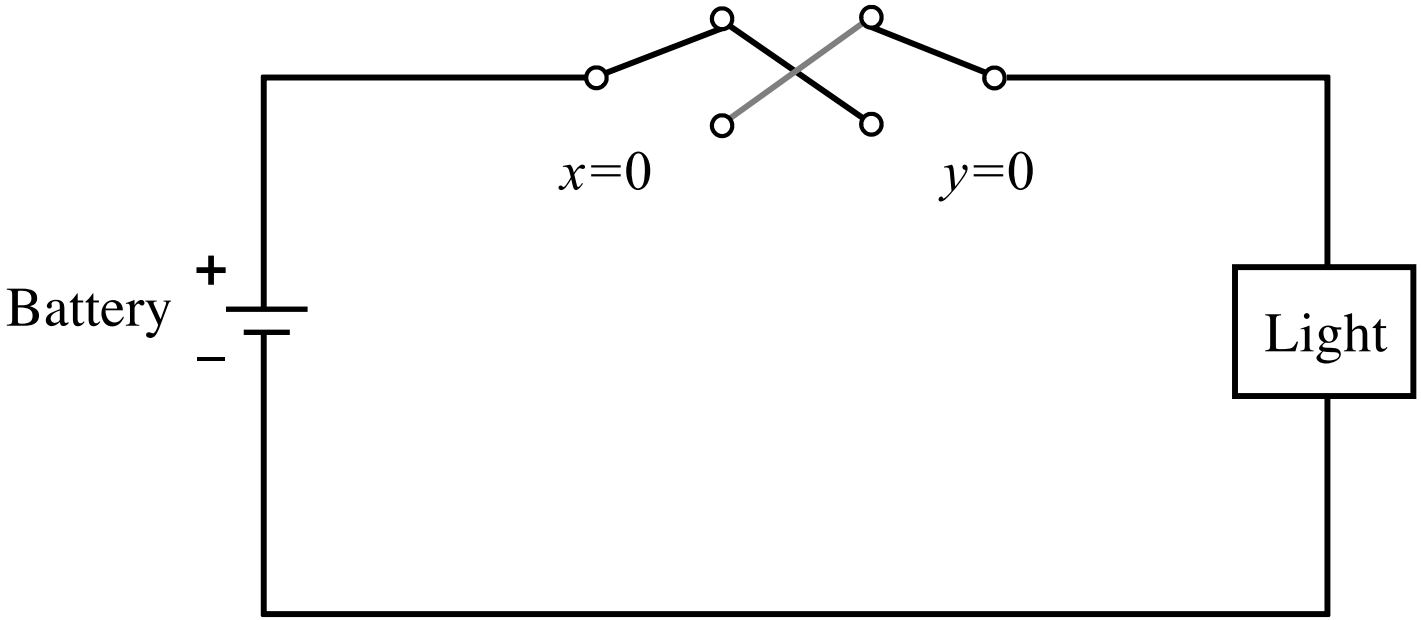


(d) Network that implements $g = \bar{x}_1 + x_2$

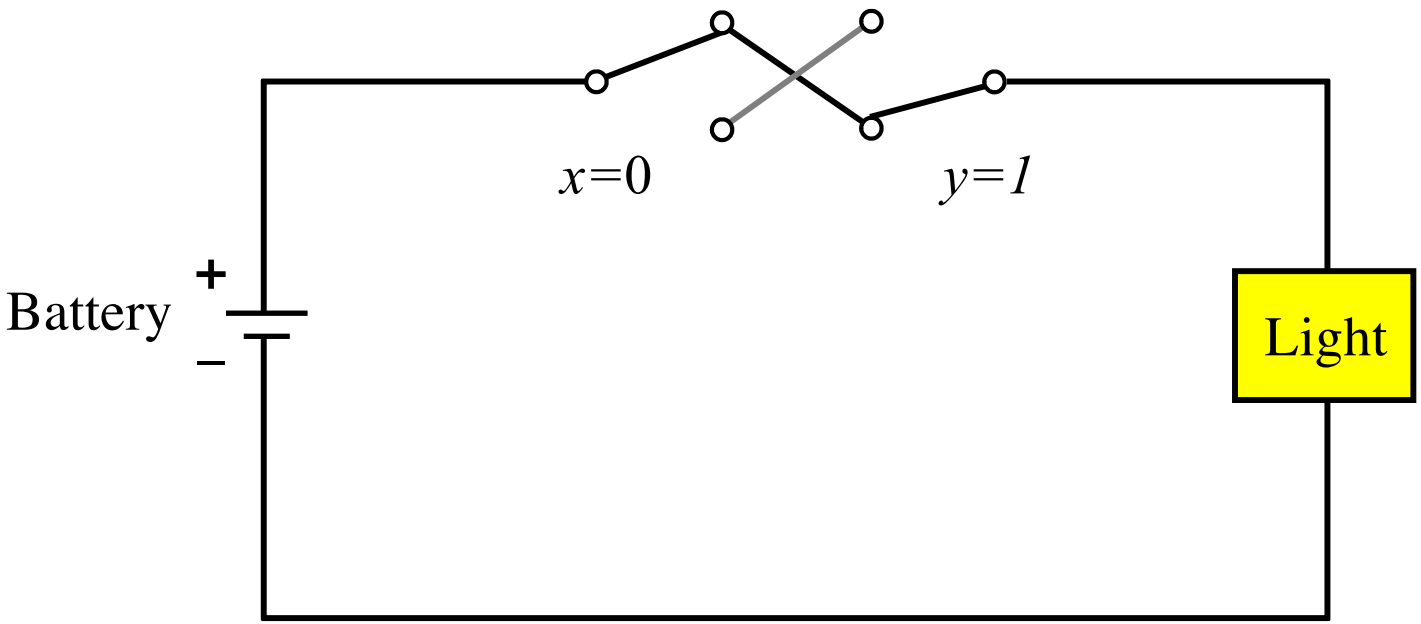
[Figure 2.10 from the textbook]

Logic XOR with Switches

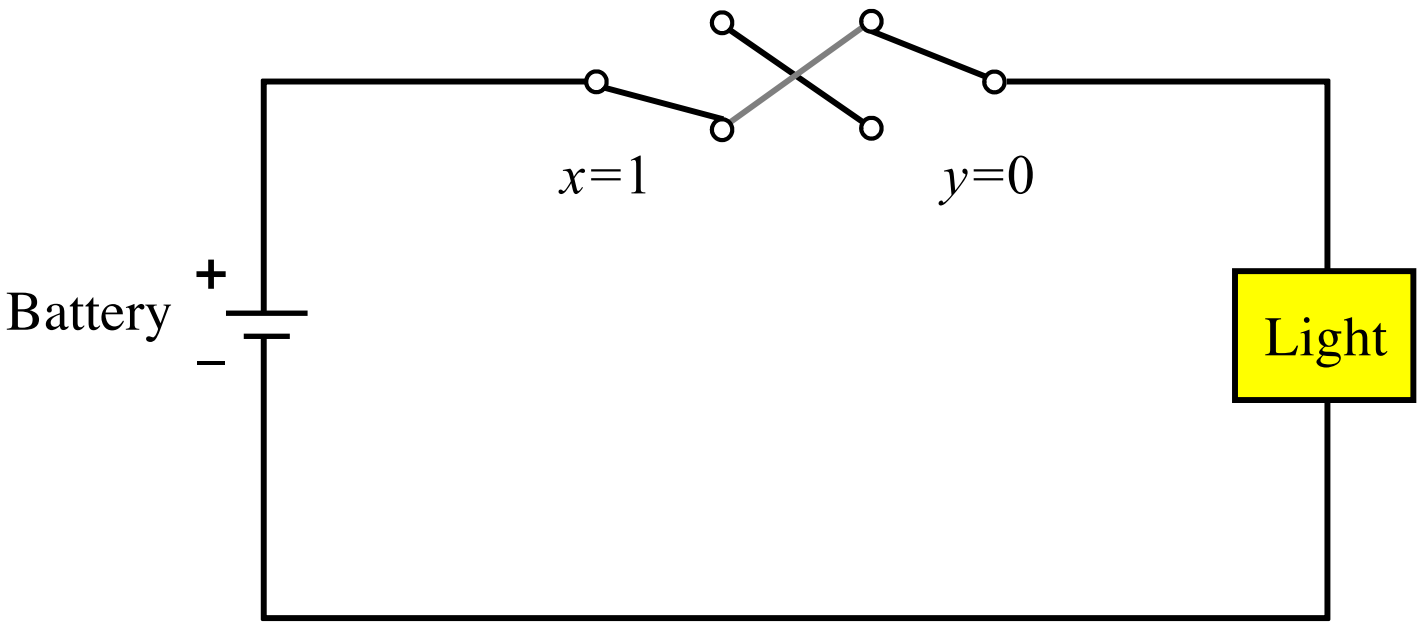
XOR Circuit



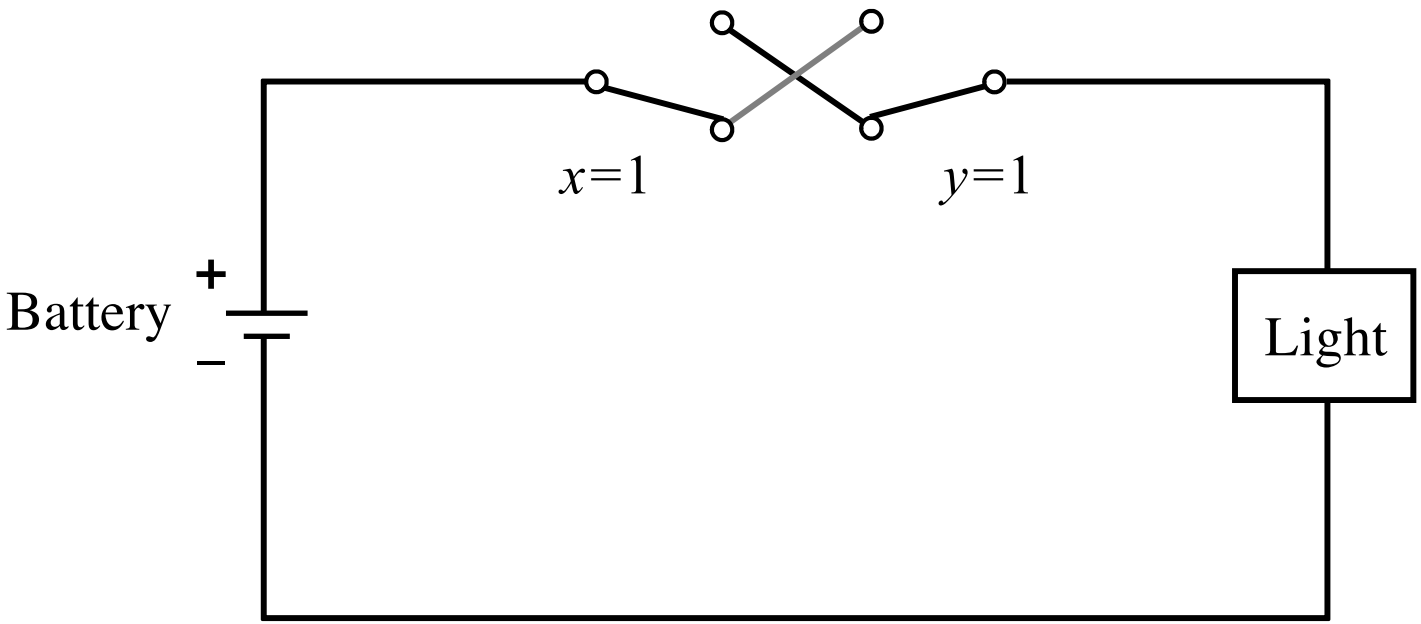
XOR Circuit



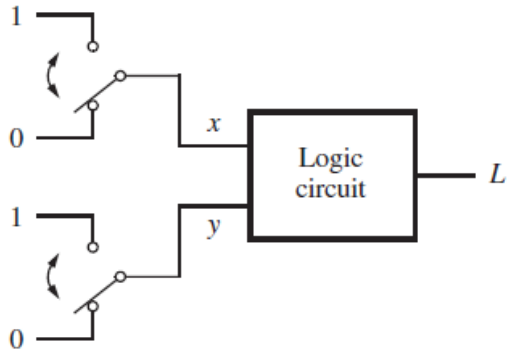
XOR Circuit



XOR Circuit



The XOR Logic Gate



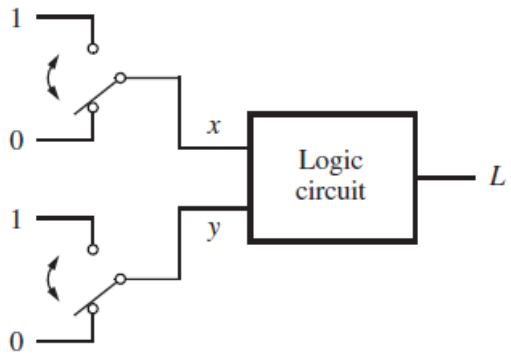
(a) Two switches that control a light

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

(b) Truth table

[Figure 2.11 from the textbook]

The XOR Logic Gate



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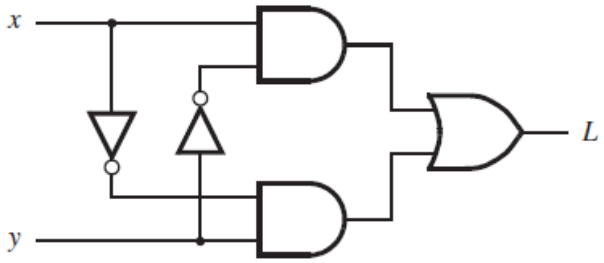
(b) Truth table

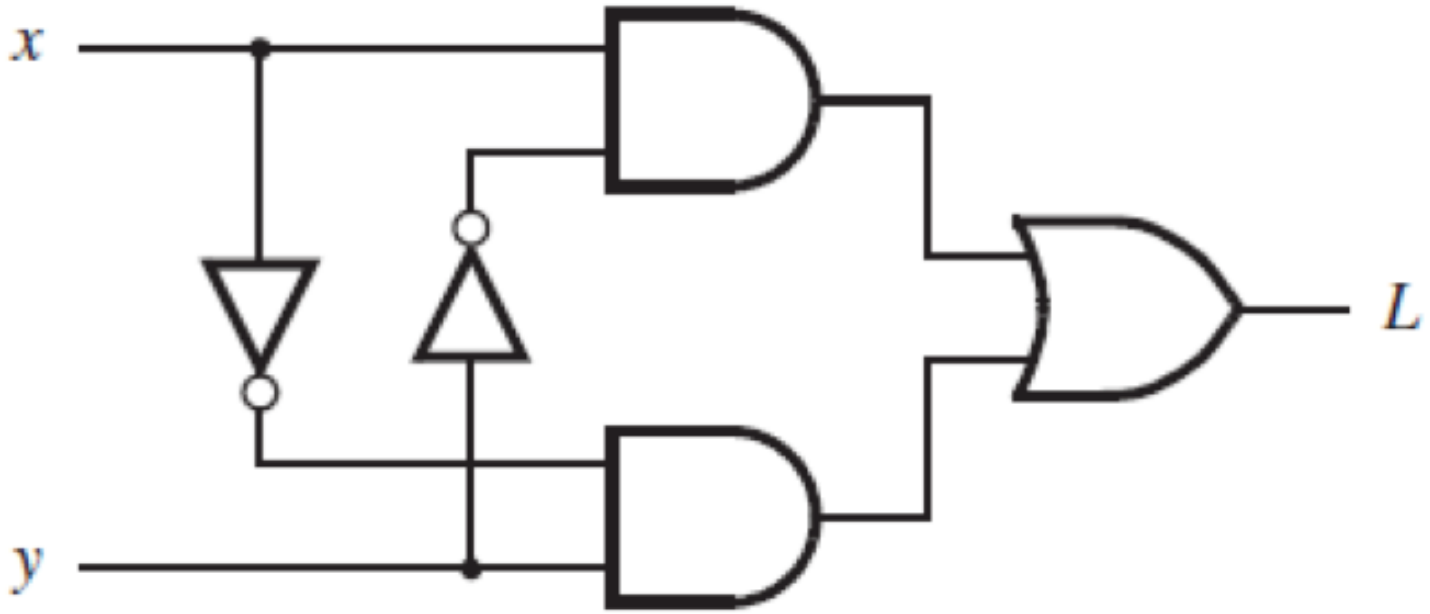


(c) Logic network

(d) XOR gate symbol

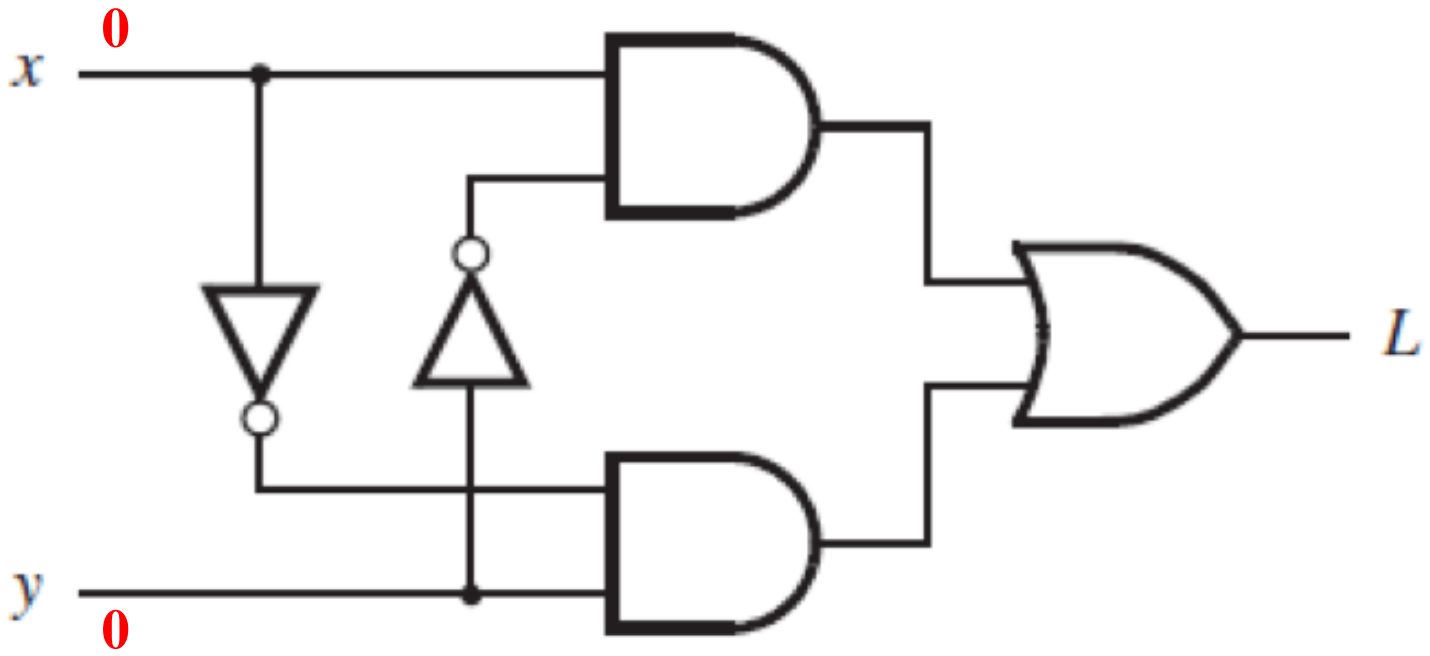
[Figure 2.11 from the textbook]

XOR Analysis

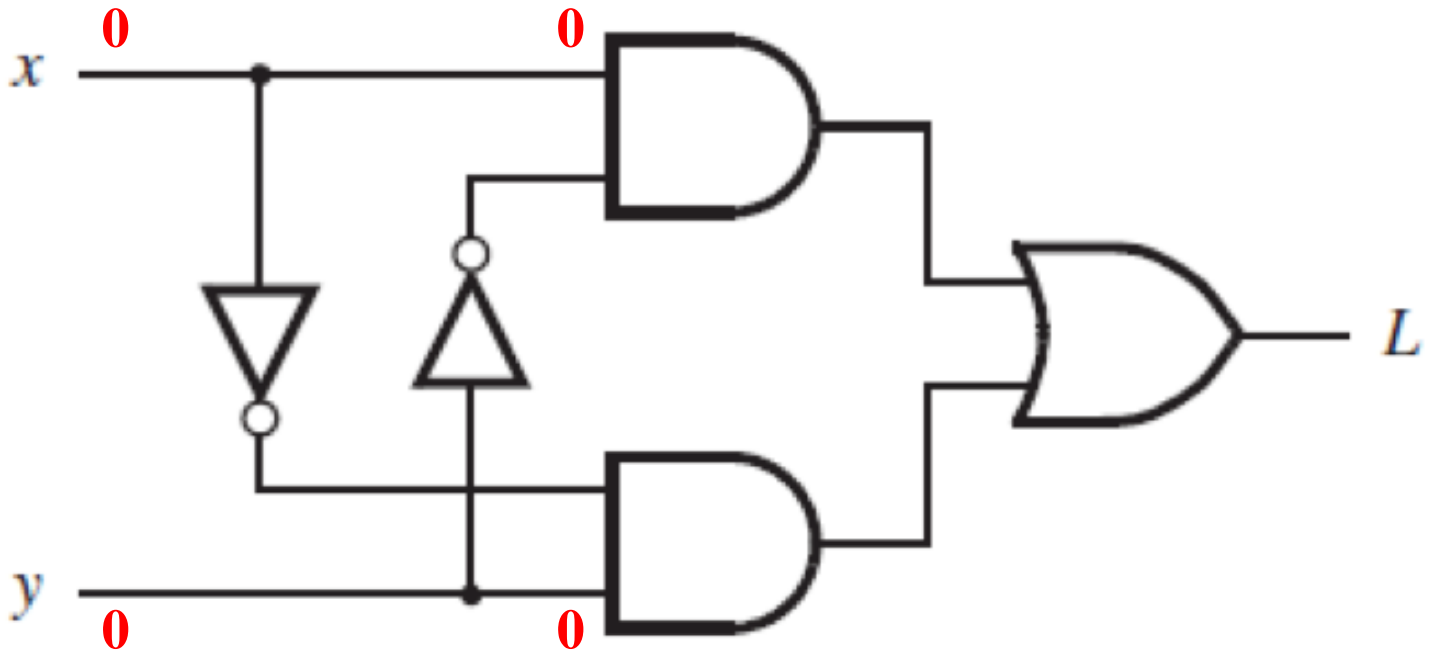


[Figure 2.11c from the textbook]

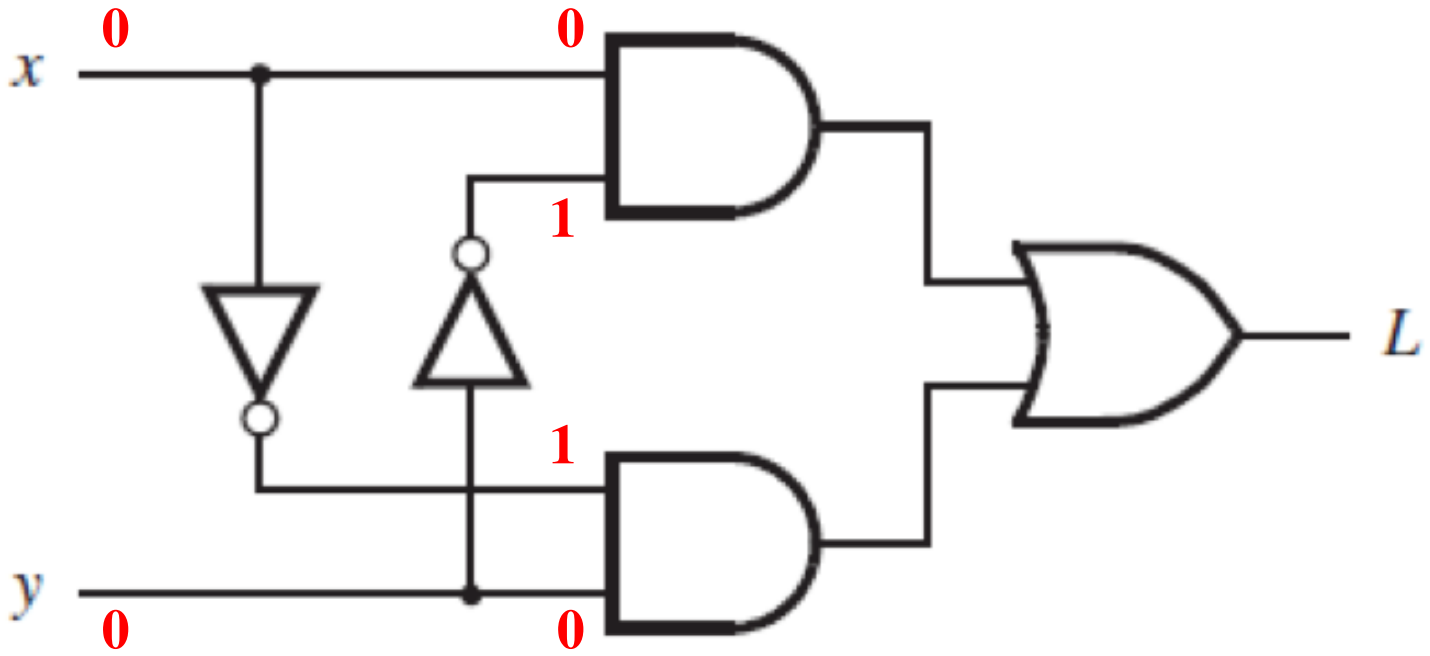
XOR Analysis (x=0, y=0)



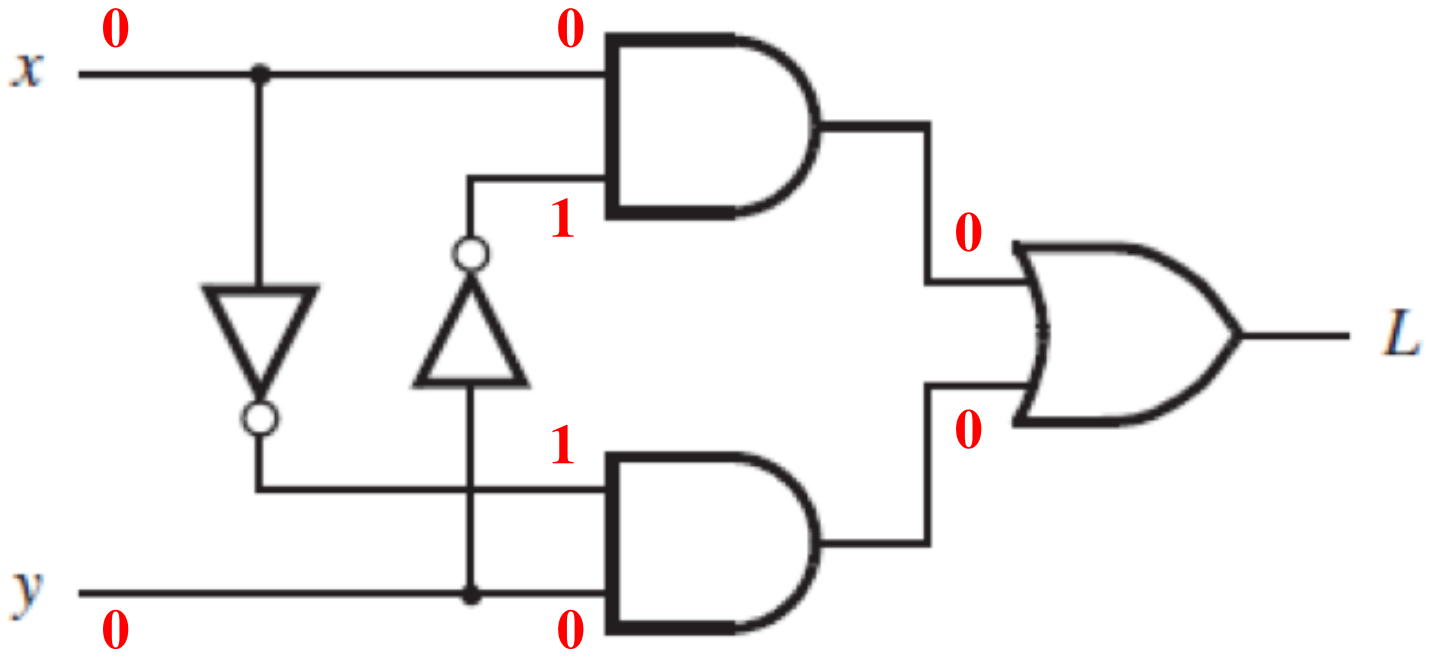
XOR Analysis (x=0, y=0)



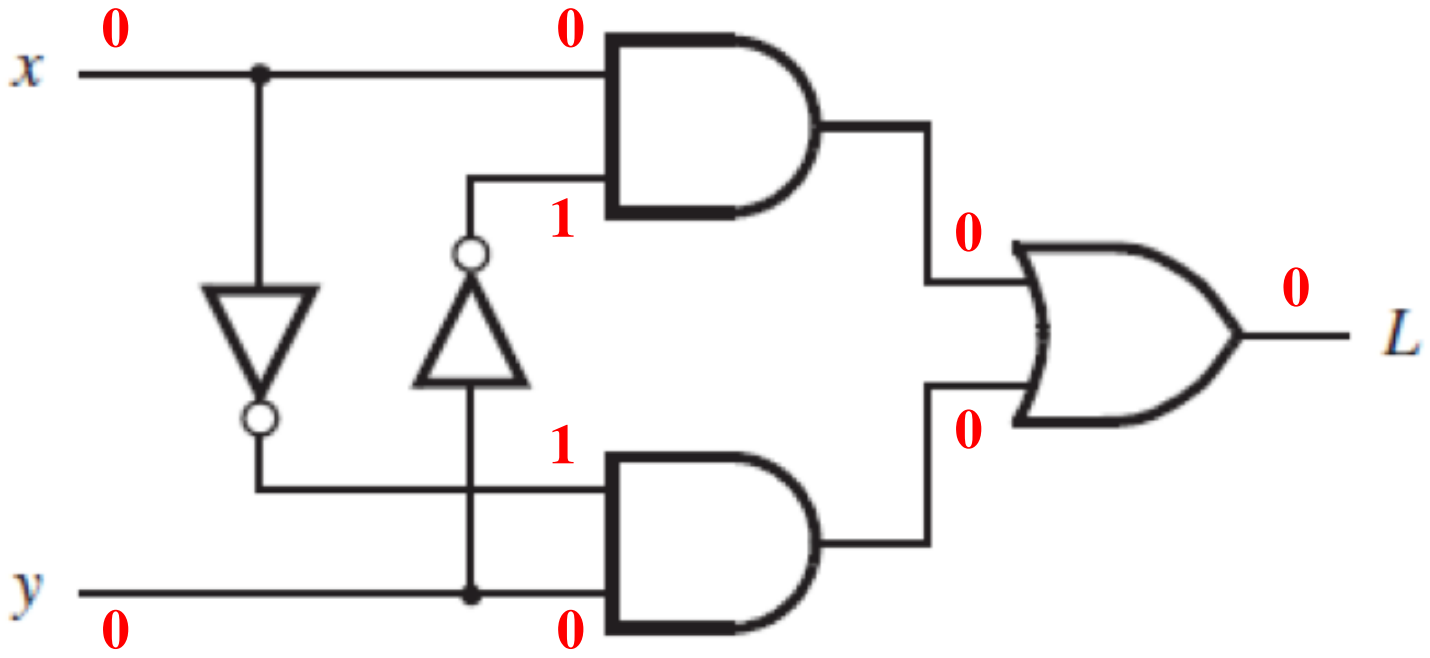
XOR Analysis (x=0, y=0)



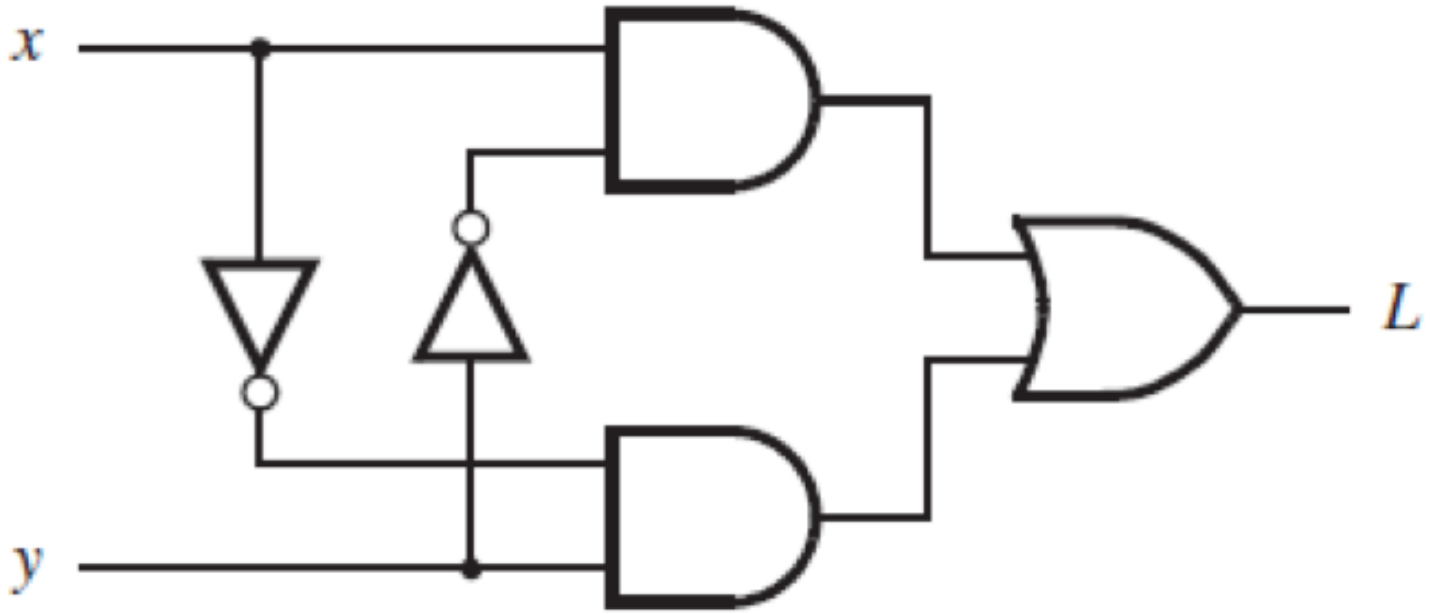
XOR Analysis (x=0, y=0)



XOR Analysis (x=0, y=0)

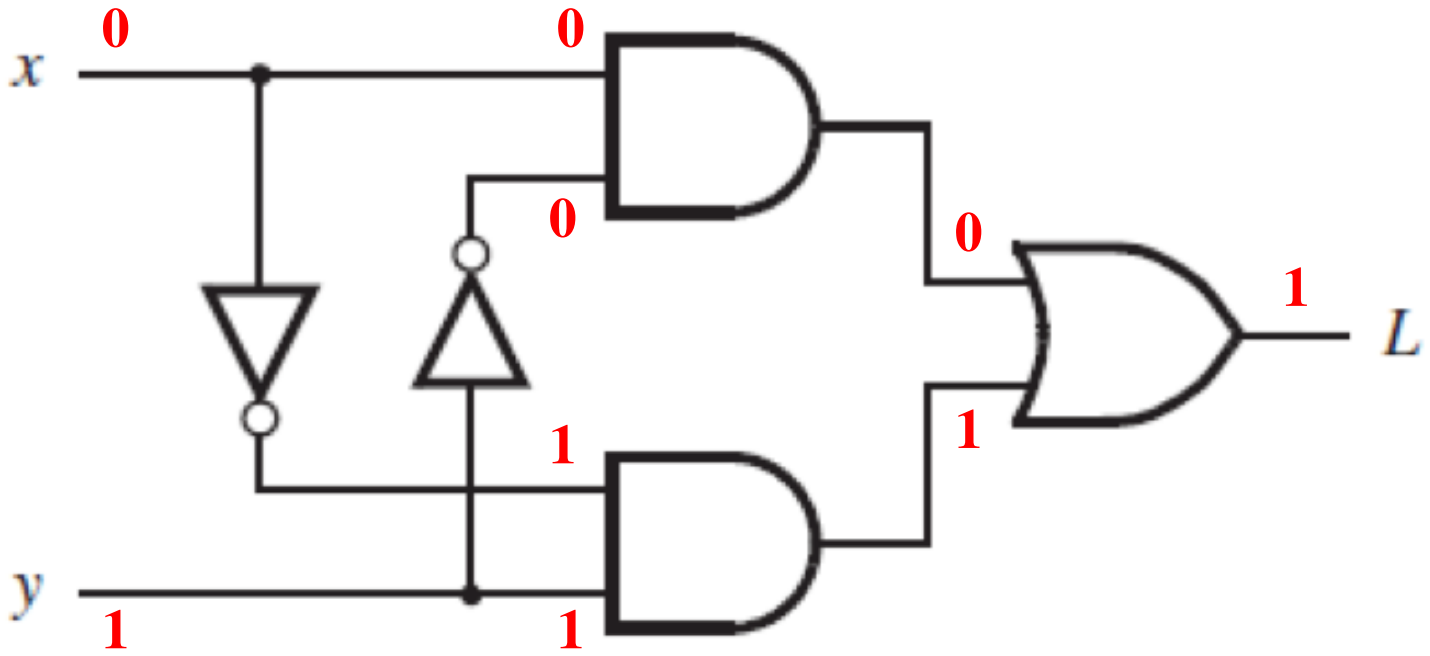


XOR Analysis

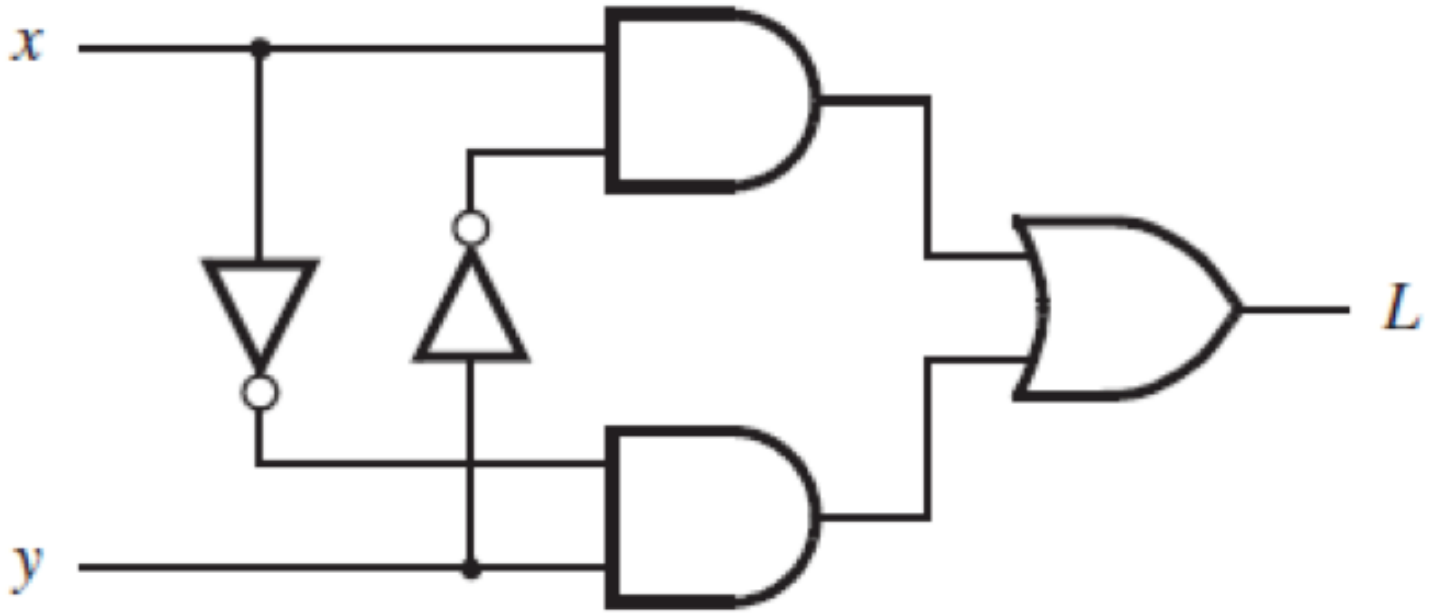


[Figure 2.11c from the textbook]

XOR Analysis (x=0, y=1)

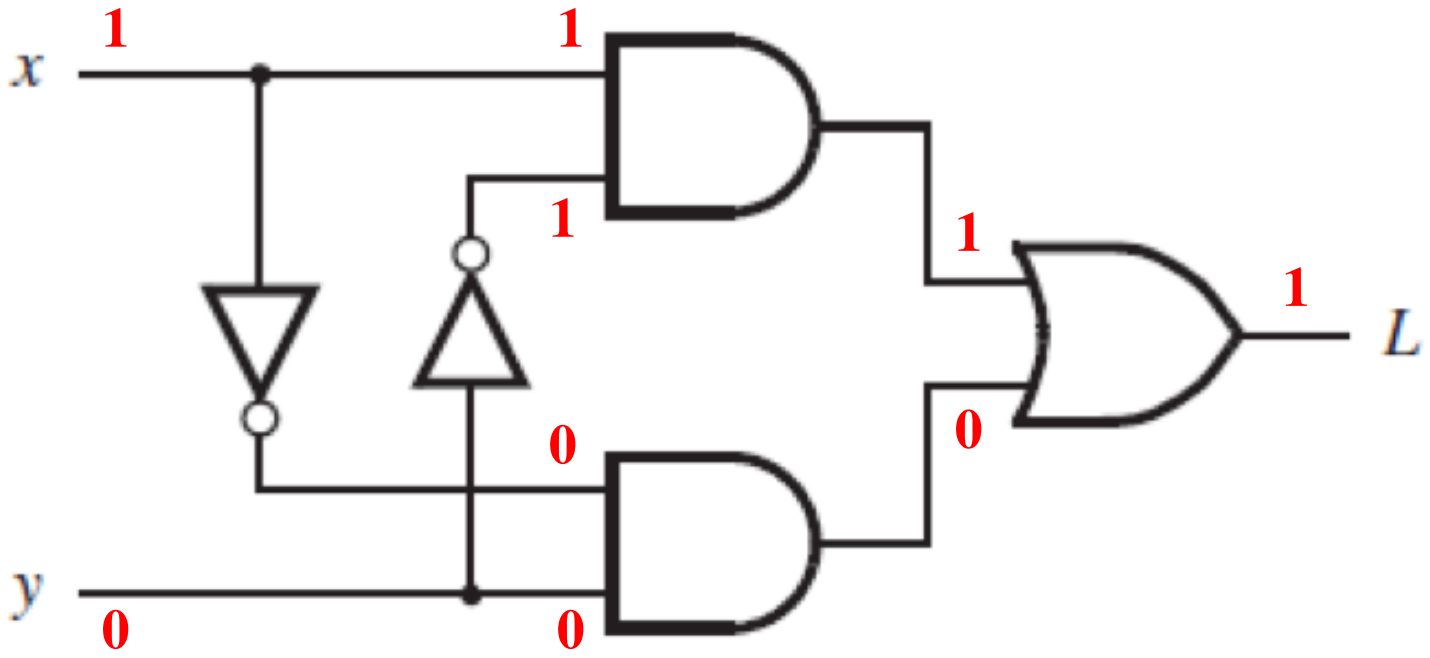


XOR Analysis

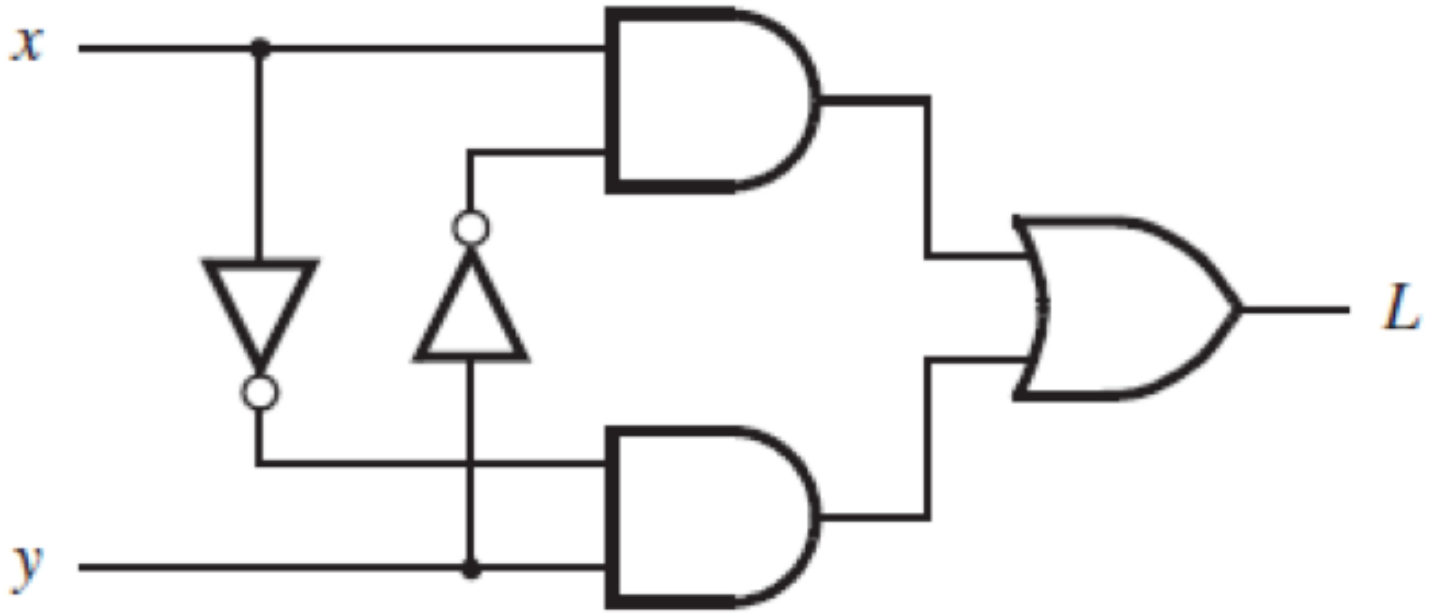


[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=0)

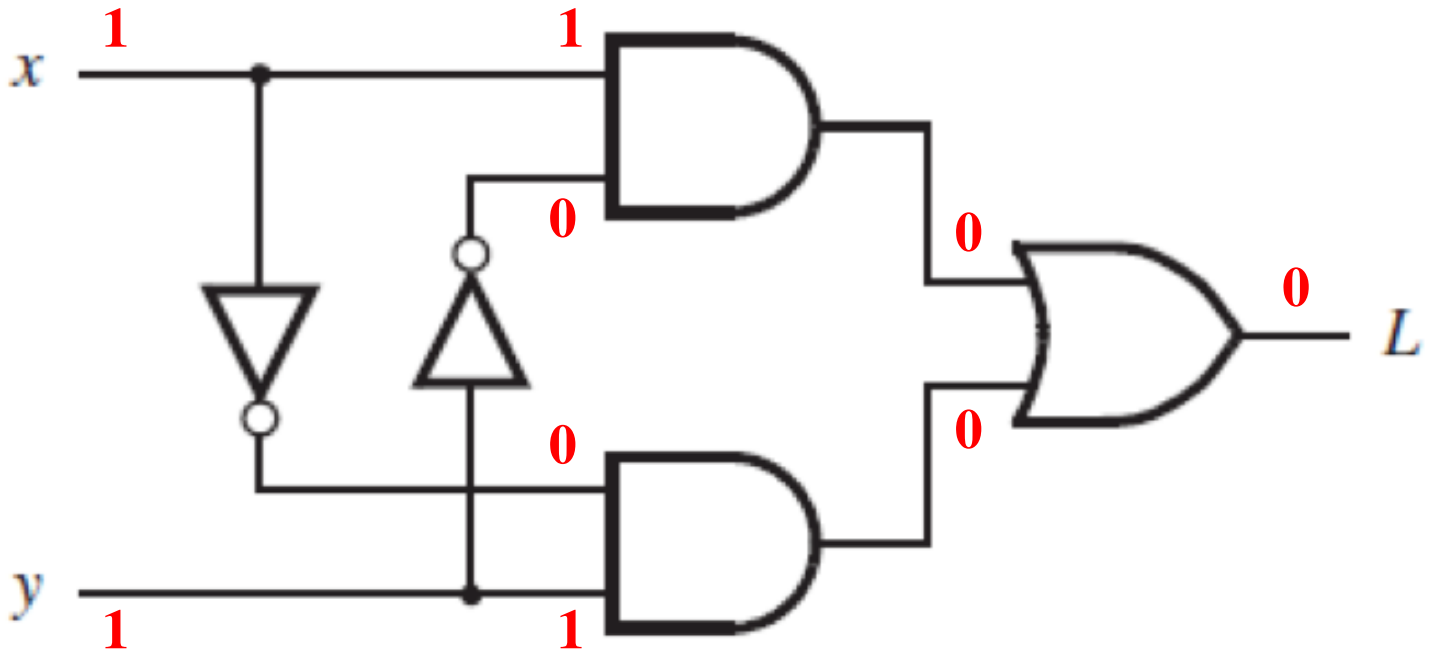


XOR Analysis



[Figure 2.11c from the textbook]

XOR Analysis (x=1, y=1)



Truth Table for XOR

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table for XOR

x	y	L
0	0	0
0	1	1
1	0	1
1	1	0

The output is 1 only if the two inputs are different.

Addition of Binary Numbers

a	0	0	1	1
$+\ b$	$+\ 0$	$+\ 1$	$+\ 0$	$+\ 1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

[Figure 2.12 from the textbook]

Addition of Binary Numbers

a	0	0	1	1
$+\ b$	$+\ 0$	$+\ 1$	$+\ 0$	$+\ 1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

[Figure 2.12 from the textbook]

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\ b$	$+\ 0$	$+\ 1$	$+\ 0$	$+\ 1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\ b$	$+\ 0$	$+\ 1$	$+\ 0$	$+\ 1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\ b$	$+\ 0$	$+\ 1$	$+\ 0$	$+\ 1$
$s_1\ s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$
\begin{array}{r}
a \\
+\,b \\
\hline
s_1\,s_0
\end{array}
\qquad
\begin{array}{r}
0 \\
+\,0 \\
\hline
0\,0
\end{array}
\qquad
\begin{array}{r}
0 \\
+\,1 \\
\hline
0\,1
\end{array}
\qquad
\begin{array}{r}
1 \\
+\,0 \\
\hline
0\,1
\end{array}
\qquad
\begin{array}{r}
1 \\
+\,1 \\
\hline
1\,0
\end{array}
$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

$$\begin{array}{r} a \\ +\,b \\ \hline s_1\,s_0 \end{array} \qquad \begin{array}{r} 0 \\ +\,0 \\ \hline 0\,0 \end{array} \qquad \begin{array}{r} 0 \\ +\,1 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,0 \\ \hline 0\,1 \end{array} \qquad \begin{array}{r} 1 \\ +\,1 \\ \hline 1\,0 \end{array}$$

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	0	0	1	1
$+\,b$	$+\,0$	$+\,1$	$+\,0$	$+\,1$
$s_1\,s_0$	0 0	0 1	0 1	1 0

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

?

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

AND

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

?

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

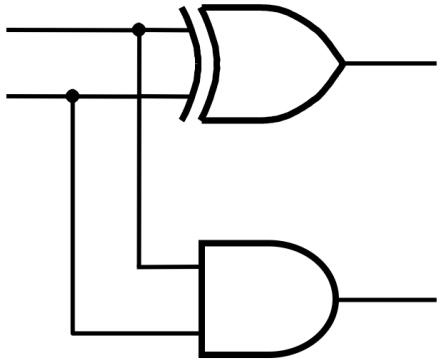
XOR

a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers

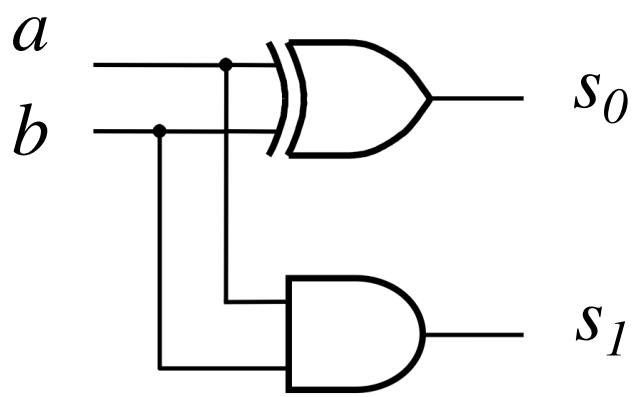
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Addition of Binary Numbers



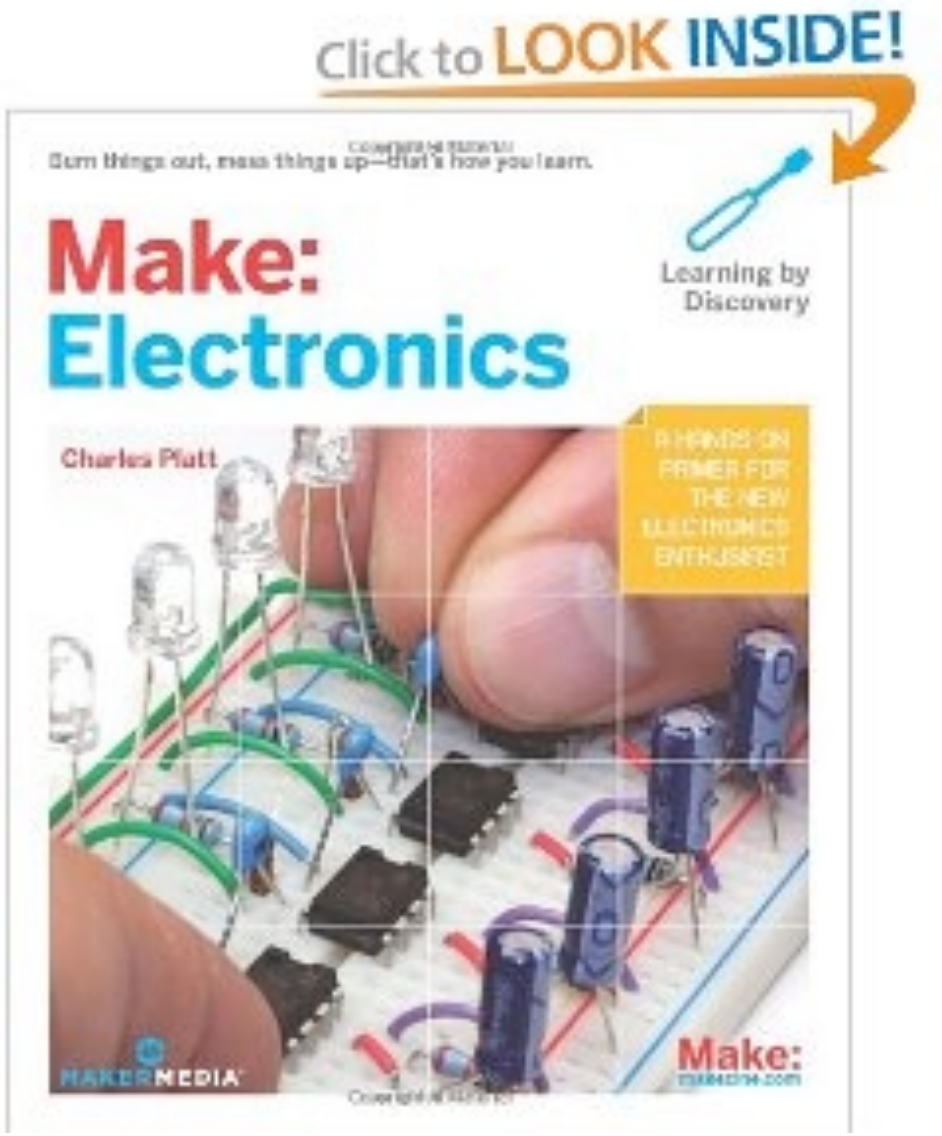
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

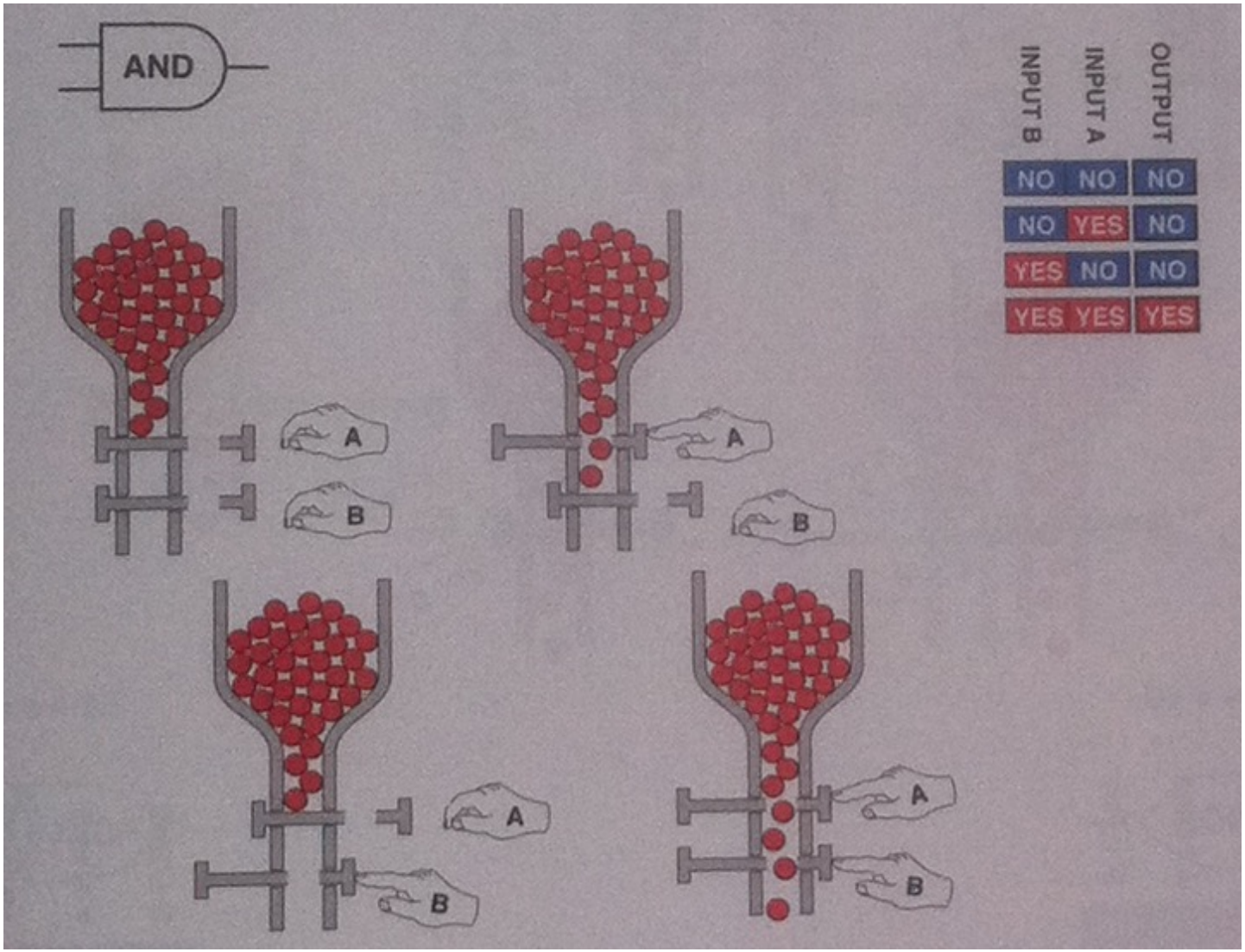
Addition of Binary Numbers



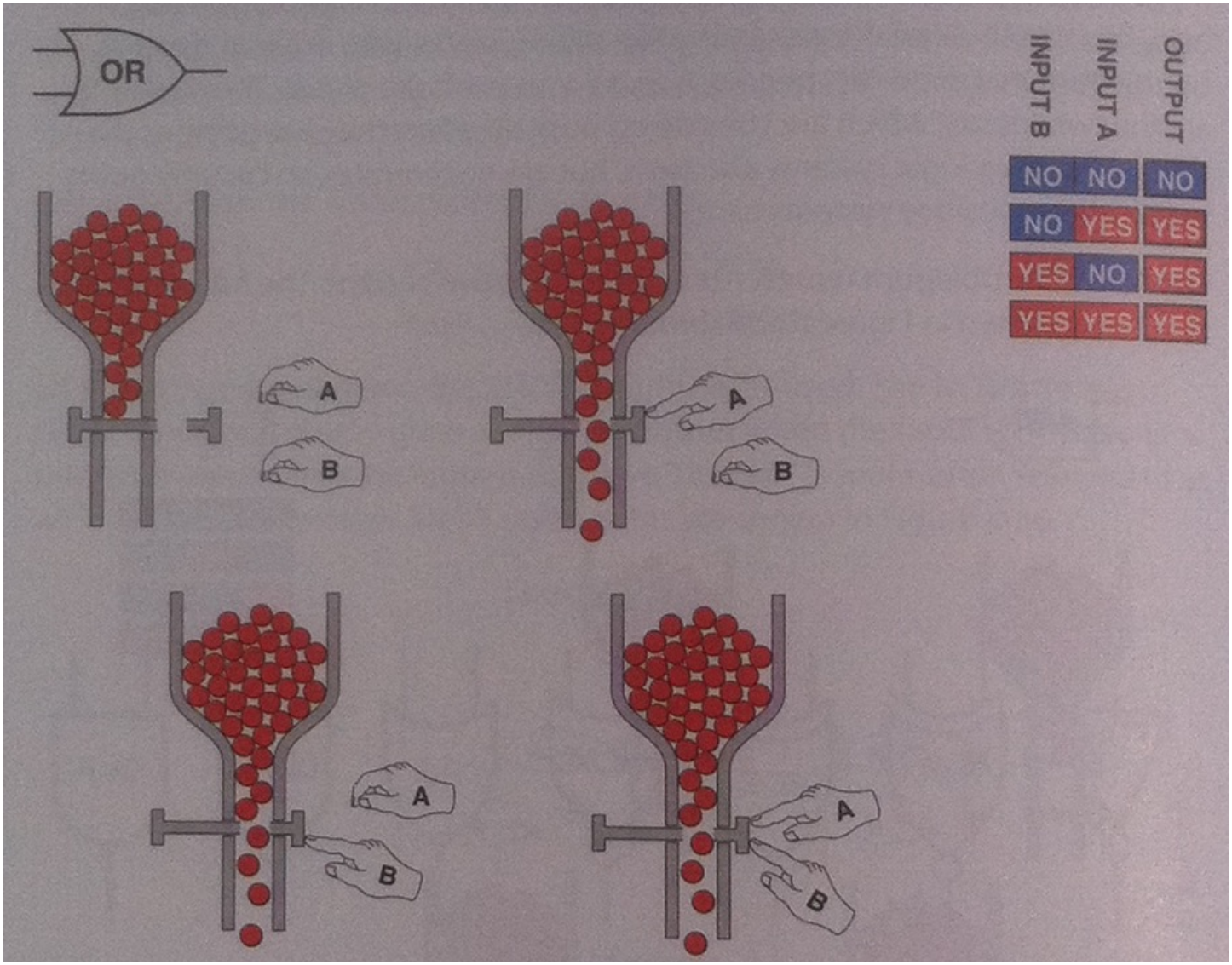
a	b	s_1	s_0
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The following examples came from this book

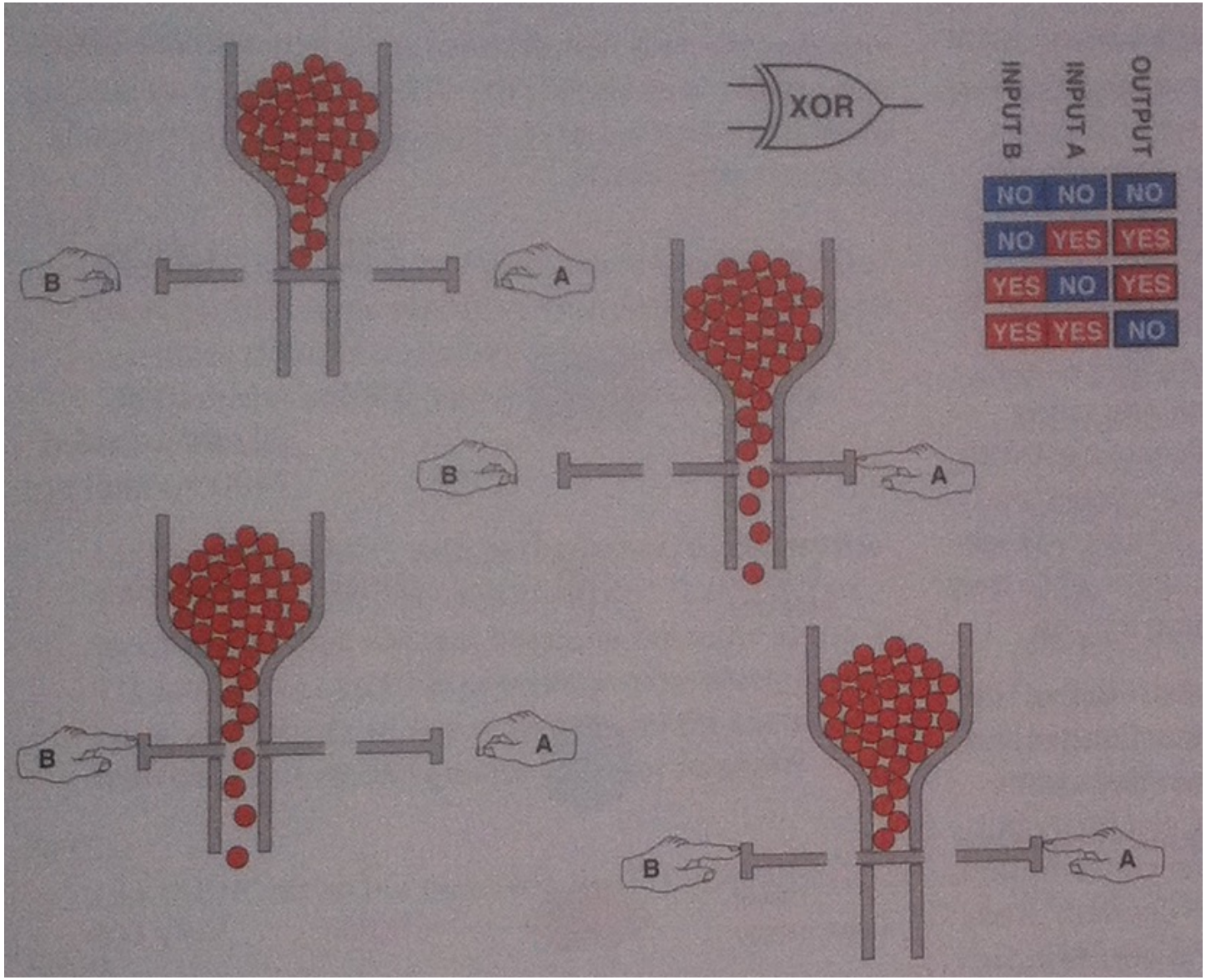



AND
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES NO
YES NO NO
YES YES YES
A
B
A
B
A
B
A
B

[Platt 2009]


OR
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES YES
YES NO YES
YES YES YES
A
B
A
B
A
B
A
B

[Platt 2009]


XOR
INPUT B
INPUT A
OUTPUT
NO NO NO
NO YES YES
YES NO YES
YES YES NO
B
A
B
A
B
A
B
A

[Platt 2009]

Questions?

THE END