

**P1 (15 points)** Draw the complete circuit diagram for each of these components using logic gates (no black boxes please):

- a) Basic Latch (with NOR Gates)
- b) Gated SR Latch (with NAND Gates)
- c) Gated D Latch

**P2 (10 points)** Draw the circuit diagram for a Positive-edge-triggered JK Flip-Flop. You are not allowed to use any high-level abstractions (e.g., latches) in this problem. You must use only logic gates.

**P3 (10 points)** Design a JK Flip-Flop (**JKFF**) using a T Flip-Flop (**TFF**). Draw the schematic diagram. The circuit designed must fully support all the functionalities of the JKFF (PRESET and CLEAR implementations are not necessary and can be skipped), but the circuit must use only one TFF.

**P4 (10 points)** Design a D Flip-Flop (**DFF**) using a T Flip-Flop (**TFF**). Draw the schematic diagram. The circuit designed must fully support all the functionalities provided by the DFF (PRESET and CLEAR implementations are not necessary and can be skipped).

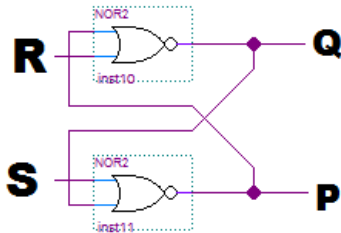
**P5 (10 points)** Explain the difference between a **positive-edge-triggered flip-flop** and a **negative-edge-triggered flip-flop**. Under what conditions will each update its state? Why might a designer choose one over the other?

**P6 (10 points)** Explain the purpose **and** difference between **synchronous control inputs** (Enable and data inputs) and **asynchronous control inputs** (Preset and Clear). How does each type interact with the clock? Under what conditions does each override the stored value?

**P7 (15 points)** Use an SR latch and some additional logic gates to implement an LM-latch, which is defined with this characteristic table:

L	M	Q	P
0	0	No change	No change
0	1	0	1
1	0	1	0
1	1	No change	No change

- a) (5 points) Complete the characteristic table for the SR Latch shown below



S	R	Q	P
0	0		
0	1		
1	0		
1	1		

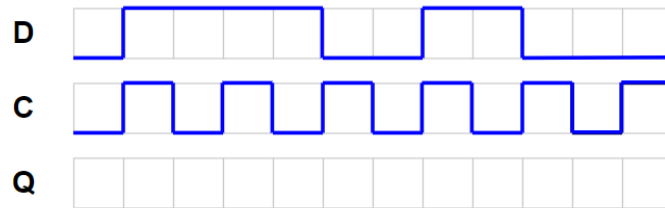
- b) (5 points) Write the values of **S** and **R** that produce the output combinations for each input combination to the LM-latch described by characteristic table shown above.

L	M	S	R	Q	P
0	0			No change	No change
0	1			0	1
1	0			1	0
1	1			No change	No change

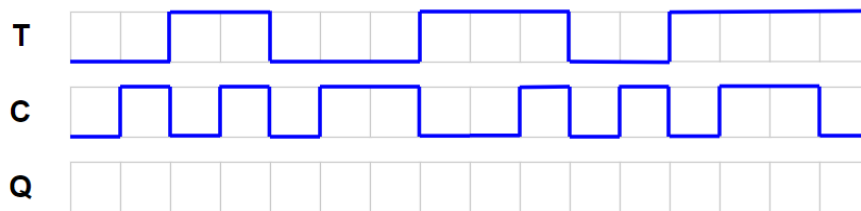
- c) (5 points) Use the table from part b) to derive Boolean expressions for **S** and **R** in terms of **L** and **M**. Then, draw the circuit for the LM-latch using logic gates.

**P8 (20 points)** Complete the timing diagrams for the specified flip-flops. In all cases the Clock signal is labeled C. You may assume that Q is initially at 0 unless specified otherwise (as in part c).

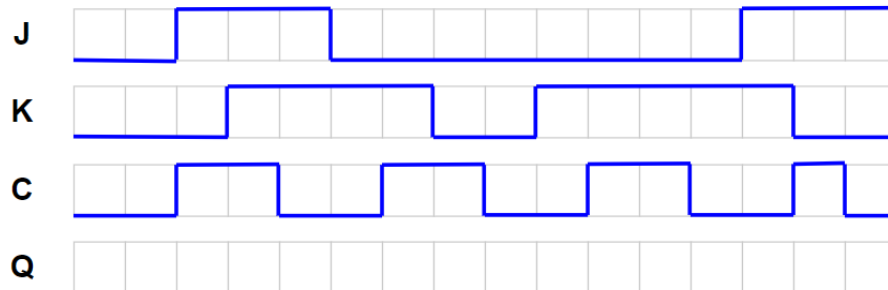
a) A negative-edge-triggered D Flip-Flop (DFF).



b) A positive-edge-triggered T Flip-Flop (TFF).



c) A negative-edge-triggered JK Flip-Flop (JKFF).



d) A positive-edge-triggered DFF with active-high Clear (CL). Note that clear occurs when CL=1.

