Cpr E 281 HW 10

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Synchronous Sequential Circuits
Assigned Date: Thirteenth Week
Due Date: Nov. 13, 2017

P1. (24 points) Design a modulo-6 counter that counts in the sequence 0, 1, 2, 3, 4, 5, 0, 1,… Also, this counter counts the clock pulses if its enable input w is equal to 1, otherwise it does not increment its count.

a) Use D flip-flops and include the state diagram, state-assigned table, next-state expressions and output expressions all clearly labeled. Let y_2, y_1, and y_0 be the current state values.
b) Repeat Problem 1 using JK flip-flops. Work through the entire design process rather than simply converting the D flip-flops to JK flip-flops. Use the same state diagram.
c) Repeat Problem 1 using T flip-flops. Work through the entire design process rather than simply converting the D flip-flops to T flip-flops. Use the same state diagram.

P2. (10 points) Derive the circuits that implement the state tables shown below. Compare the costs of these circuits.

Present state	Next state				Output
	$DN = 00$	01	10	11	z
S1	S1	S3	S2	–	0
S2	S2	S4	S5	–	0
S3	S3	S6	S7	–	0
S4	S1	–	–	–	1
S5	S3	–	–	–	1
S6	S6	S8	S9	–	0
S7	S1	–	–	–	1
S8	S1	–	–	–	1
S9	S3	–	–	–	1

Present state	Next state				Output
	$DN = 00$	01	10	11	z
S1	S1	S3	S2	–	0
S2	S2	S4	S5	–	0
S3	S3	S2	S4	–	0
S4	S1	–	–	–	1
S5	S3	–	–	–	1

P3. (16 points) Consider the state machine specified by the following state transition table.

Current		Input	Next	
x	y	I	X	Y
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

(a) Draw the state transition diagram of the machine.
(b) Write two next-state expressions for X and Y that will implement the transitions of the state machine. Make your expressions as simple as possible, and use XOR gates and NOT gates only.
(c) Implement the state machine using D flip-flops, XOR gates, and NOT gates.
(d) Suppose the machine is initially in 00 (i.e., x=0 and y=0). Indicate for each input sequence below, the state the machine is in after the last digit read in. Assume the digits are read from left to right.

I. 11111 II. 1001110000101100 III. 436 1s followed by 325 0s

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P4. (15 points) Deduce the purpose of a state machine with the next state logic and output logic given below. Let X, Y, and Z be the values of the three D flip-flops, X_{next}, Y_{next}, and Z_{next} be the next state expressions, and ABC be the three-bit output of the circuit.

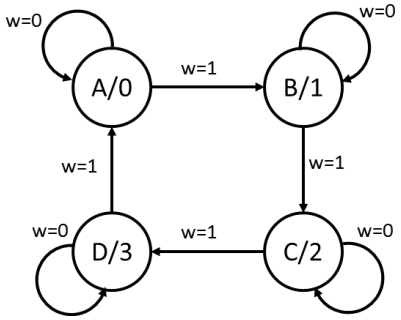
(a) Construct the state assigned table from the expression.
(b) Draw the state diagram from the table.
(c) Explain in one sentence the functionality of the circuit.

$X_{next} = X'YZ + XY' + XZ'$	$Y_{next} = Y'Z + YZ'$	$Z_{next} = Z'$
$A = X'$	$B = Y$	$C = Y + Z$

P5. (10 points) A state machine has one input P in addition to the clock input and one output Q. The value of Q is 1 if the total number of 1's in the sequence of input P is either a multiple of 2 or a multiple of 3. Otherwise, the output value Q is 0. Draw a state transition diagram for the state machine using as few states as possible.

P6. (10 points) Derive a minimal state table for an FSM that acts as a three-bit parity generator. For every three bits that are observed on the input w during three consecutive clock cycles, the FSM generates the parity bit p = 1 if and only if the number of 1s in the three-bit sequence is odd.

P7. (15 points) Consider a FSM with the following state diagram:



a) (5 points) Complete the following state table based on the state diagram:
b) (5 points) Encode each state and outputs in (a) with binary numbers to build the following state-assigned table:
c) (5 points) Derive the minimal logic expressions for Y_1, Y_0, z_1, and z_0.
d) (5 points) Draw the complete circuit diagram using D flip-flops and any additional logic gates that are required.
e) (5 points) What does this FSM do? What happens when w=0 and w=1?

Present State	Next State		Output
	w=0	w=1	
A	A	B	0
B			
C			
D			

Present State Y_1Y_0	Next State		Output z_1z_0
	w=0 Y_1Y_0	w=1 Y_1Y_0	