Abstract

Spectral testing is mainly used to test dynamic performance of Analog-to-Digital Converters (ADC) and waveform generators. Dynamic specifications for ADCs are very important in high speed applications such as digital communications, ultrasound imaging and instrumentation. With improvement in the performance of ADCs, it is becoming an expensive and challenging task to perform spectral testing using standard method, due to the requirement to satisfy several stringent conditions by the test setup instrumentation. In order to address these challenges and to decrease the test cost, in this dissertation, three new algorithms are proposed to perform accurate spectral testing of ADCs by relaxing three necessary conditions required for standard spectral testing.

The first method introduces a new fundamental identification and replacement (FIRE) method, which eliminates the requirement of coherent sampling in ADC testing. The robustness and accuracy of the proposed FIRE method is verified using simulation and measurement results on non-coherently sampled data.

The second method, namely, Fundamental Estimation, Removal and Residue Interpolation (FERARI) method, is proposed to eliminate the requirement of precise control over amplitude and frequency of the input signal to the ADC. This method can be used when the ADC output is both non-coherently sampled and clipped. Simulation and measurement results using FERARI method on non-coherently sampled and clipped ADC output are shown to validate this approach.

A third spectral test method is proposed that simultaneously relaxes the conditions to use a pure input source and to achieve coherent sampling. Using this method, a high resolution ADC can be accurately tested for spectral characteristics using a non-coherently sampled, non-linear (or impure) input signal. Simulation results are presented that show the accuracy and robustness of the proposed

method. The validation studies clearly demonstrate the cost effectiveness of the proposed three methods when compared to current testing approach.

Finally, the issue of metastability in comparators and Successive Approximation Register (SAR) ADCs is analyzed. The analysis of probability of metastability in SAR ADCs with and without using metastable detection circuits is provided. Using analysis, it is shown that as frequency of sampling clock increases, using a metastable detection circuit decreases the probability of metastability in SAR ADCs.