

Techniques for Design of Robust and Reliable Analog Circuits

Abstract

Recent decades have seen an influx of electronics into high volume safety-critical applications such as automotive. These applications differ from the conventional safety-critical applications like aircrafts in that they operate in a price sensitive market and are available to mass consumers. This makes it difficult to use traditional robustness and reliability mechanisms like redundancy and exhaustive testing. Techniques that can help improve the robustness and reliability of integrated circuits (ICs) to be used in these high-volume safety critical applications is at the forefront of industrial and academic discussions.

Unlike digital designs which have managed to achieve very low defects per million, required for the automotive sector, analog designs lag far behind. In fact, analog designs are responsible for the majority of in-field failures of any mixed signal system on chip (SoC). Building in, design margins to account for the robustness and reliability is running out of steam. Techniques such as on-chip functional testing, on-chip transistor degradation monitoring, lowering AMS test costs in general or through the use of already available on-chip resources is the way forward to deal with these robustness and reliability issues. In this dissertation these techniques have been touched upon.

Spectral testing and linearity testing are two primary test categories performed on data converters. On-chip testing of these specifications can help reduce test costs and improve functional safety. A low-cost sine wave generator for on-chip spectral testing has been designed and measurement results obtained in the 40nm bulk CMOS technology.

Taking advantage of the fact that modern SoCs have both ADCs and DACs, an algorithm that can enable co-linearity testing of these data converters without the need for any external equipment has also been developed. Using the test data, a methodology to calibrate these data converters has also been discussed.

A monolithic, fast, large dynamic range time dependent dielectric breakdown (TDDB) monitor has also been developed to enable on-chip ageing monitoring. The developed sensor is sensitive to currents as low as 200pA and directly measures the degrading parameters, that is the gate leakage current unlike previously proposed designs.

An algorithm to enable low-cost jitter segregation in pulse amplitude modulation 4(PAM4) links is also discussed.

A new FoM for level shifters to be used in charge constraint applications has also been proposed and new level shifter circuits that improve this FoM have been developed as well.

This dissertation touches upon varied aspects of improving the robustness and the reliability of ICs embedded in safety critical systems in general and analog/mixed signal circuits used therein in particular.