**Title:**

Cost-efficient solutions to detect and mitigate site-to-site variation in massive multisite (parallel) testing

**Abstract:**

The rising analog content in systems on chip (SoCs) and the stringent customer requirements are driving an increased need for accurate and robust measurement of analog parametric specifications during manufacturing tests, thereby significantly increasing overall chip cost. Multi-site (parallel) testing alleviates this issue by testing multiple chips at the same time, thus massively increasing throughput and reducing the testing time per chip. For successful multi-site testing, engineers have to design multi-site boards that can ensure robust measurement and test quality for every site. However, as the number of sites increases, the inevitable variations in site-to-site behavior become pronounced and do not correspond to actual problems in the devices under test (DUT). These variations result from various artifacts such as non-homogenous layout and routing, and compromises in component placement.

Significant variations in the measurements from site to site may result in potential yield loss and possible test escapes. Incorrect trim codes based on such measurements may also lead to further worsening of the DUT performance. However, since site-to-site variation is a recent concern, very little work has been done on investigating and mitigating this concern. The challenges in identifying and correcting sites with excessive variations will quickly become an important task in the near future, as the number of test sites in multi-site analog testing rapidly increases.

The goal of this research is to develop systematic strategies to detect and mitigate site-to-site variations in massive multi-site testing. To achieve this goal, advanced statistical learning and signal processing techniques like polynomial transform, method of least-squares, quantile-quantile plots, and cross-correlation, amongst many other tools, are employed. New algorithms are proposed and applied to test data.  The robustness and accuracy of each proposed method are confirmed after application to real-world industrial and simulated measurement data. Further validation is also provided by comparing the results of the proposed methods to a more accurate reference.

Proposed algorithms will further improve test quality and reduce possible test hardware influences. The proposed issue site detection algorithms will assist the test engineer in quickly detecting test sites with pronounced variations, including those that are difficult to identify visually. Traditional mechanical methods to troubleshoot test board and site anomalies are often ad hoc, leading to a time-consuming, expensive, labor-intensive, and expensive diagnosis cycle. Proposed polynomial transformation methods to correct the measurements at issue test sites offer a cost-effective, fast, and robust alternative. It presents a software solution to a hardware problem.