Title:

Cost-efficient solutions for Analog and Mixed-signal test and calibration challenges

Abstract:

The cost of test and calibration for Analog and mixed-signal ICs has been steadily rising to the point where it is a significant contributor to the overall cost of build. Increasing design complexity, new process nodes and defect models, etc. are pushing cost of test to the forefront of chip development cost. These are propelled by the increasing levels of integration to drive the system BOM (bill of materials) low, and the increasing quality needs from customers especially in automotive and other low dppm (defective parts per million) markets.

Data converters (ADCs and DACs) in particular are critical components of integrated circuits used in control/actuation and sensing applications. 5G communication, Internet of Things also drive a growing demand for chips containing data converters. As more analog circuitry is integrated in high-volume systems-on-a-chip (SoCs) applications, most of today’s data converters are deeply embedded in large system design, which adds significant extra difficulty in testing.

Built-in self-test (BIST), self-calibration and self-diagnosis is the most promising solution to these challenges. There is thus an urgent need to develop fast and low-cost methods to enable BIST and calibration of DACs on-chip. The major focus of this dissertation is on optimizing DAC linearity test time and cost.