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3D Global Router: a Study to Optimize Congestion, Wirelength and Via for Circuit Layout

Abstract
The increasing size of integrated circuits and aggressive shrinking process feature size for IC manufacturing process poses significant challenges on traditional physical design problems. Various design rules significantly complicate the physical design problems and large problem size abides nothing but extremely efficient techniques. Leading physical design tools have to be powerful enough to handle complex design demands and be nimble enough to waste no runtime. This thesis studies the challenges faced by global routing problem, one of the traditional physical design problems that needs to be pushed to its new limit. This work proposes three effective tools to tackle congestion, wire and via optimization in global routing process, from three different aspects.

The number of vias generated during the global routing stage is a critical factor for the yield of integrated circuits. However, most global routers only approach the problem by charging a cost for vias in the maze routing cost function. The first work of this thesis, FastRoute 4.0 presents a global router that addresses the via number optimization problem throughout the entire global routing ow. It introduces the via aware Steiner tree generation, 3-bend routing and layer assignment with careful ordering to reduce via count. The integration of these three techniques with existing academic global routers achieves significant reduction in via count without any sacrifice in runtime.

Despite of the recent development for popular rip-up and reroute framework, the congestion elimination process remains arbitrary and requires significant tuning. Global routing has congestion elimination as the first and foremost priority and congestion issue becomes increasingly severe due to timing requirements, design for manufacturability. The second work of this thesis, an auction algorithm based pre-processing framework (APF) for global routing focuses on how to eliminate congestion effectively. In order to achieve more consistent congestion elimination, the framework uses auction based detour techniques to alleviate the impacts of greedy sequential manner of maze routing, which remains as a major drawback in the most popular global routing framework. In the framework, APF first identifies the most congested global routing locations by an interval over ow lower bound technique. Then APF uses auction based detour algorithm to compute which nets to detour and where to detour. The framework can be applied to any global routers and would help them to achieve significant improvement in both solution quality and runtime.

The third work in this thesis combines the advantage of the two frameworks used to minimize via usage in global routing: 3D routers with good solution quality and efficient 2D routers with layer assignment process. It results in a new multi-level 3D global router called MGR (multi-level global router) that combines the advantage of both kinds. MGR resorts to an efficient multi-level framework to reroute nets in the congested region on the 3D grid graph. Routing on the coarsened grid graph speeds up the global router, while 3D routing introduces less vias. The powerful multi-level rerouting framework wraps three innovative routing techniques together: an adaptive resource reservation technique in coarsening process, a new 3-terminal maze routing algorithm and a network flow based solution propagation method in uncoarsening process. As a result, MGR can achieve the solution quality close to 3D routers with comparable runtime of 2D routers.