**Application aware performance, power consumption, and reliability tradeoff**

There is an unprecedented rise in the demand for microprocessor performance. Advance in fabrication technology enables the scaling of transistor counts to satisfy this demand. However, this leads to a variety of power supply and hardware reliability issues. Given the conflicting trends in Performance, Power consumption, and chip Reliability (PPR), it is imperative to balance them in a fine-grained fashion to meet system level goals and expectations.

This research focuses on providing solutions that cater to variant PPR demands. Two techniques that are very relevant in this area, namely dynamic voltage and frequency scaling (DVFS) and microarchitectural adaptation, are leveraged to produce expected PPR characteristics from hardware when executing a wide variety of tasks. To meet these demands efficiently, the solutions developed are tailored to observed hardware-software interactions.

In this dissertation, we demonstrate how the expected chip lifetime can be augmented using DVFS while paying heed to performance constraints. Individual tasks in a considered task queue are assigned specific voltage and frequency pairs to utilize for their execution. This assignment is empowered by knowledge of the individual task’s expected execution time and temperature profiles. Our observations indicate a 2 to 12 fold improvement in expected chip lifetime (studied under different failure mechanisms) when performance is sacrificed by 10%. Capitalizing on the power of microarchitectural adaptation, we further push the reliability boundaries 1.2-3 fold.

We also provide mechanisms to utilize microarchitectural adaptation to co-manage system performance and power consumption as per set constraints. Comprehensive microarchitectural adaptation space is huge and its usage thus leads to significant runtime overhead. To tackle this, we devote a fair bit of attention to its pruning so as to narrow down on and utilize only the most effective adaptations. A two stage adaptation scheme is developed to a) provide good performance for the power consumed, and b) to keep the runtime overhead in check. We also develop two alternate lightweight mechanisms to reduce profiling overhead associated with the aforementioned scheme. We observe that our schemes provide 20% higher normalized energy efficiency compared to the state of the art techniques proposed, while using just a very small fraction of the configuration space. We also find that our schemes effectively cater to a wide variety of demands on performance and power consumption, providing the necessary hardware characteristics within 10% bound.

We believe that application tailored schemes for PPR management are important to extract every possible ounce of performance while confirming to power consumption or reliability constraints. Given the effectiveness of our schemes, we are confident that they are applicable in different computing markets. Insights drawn from our research can also guide chip designers in the provision of effective adaptive controls to combat increasing demands on PPR characteristics.