ABSTRACT

The field of modern control theory and the systems used to implement these controllers have developed rapidly and mostly exclusive of each other over the last 50 years. Digital control systems are traditionally designed assuming constant sensor sampling-rates and consistent processor response-times, with their implementation platform unaccounted for. Concurrently, embedded systems engineers focus on maximizing resource utilization by sharing processors amongst control and non-control tasks, causing unintended interactions. The result of this isolation between the two fields is that computing mechanisms meant to improve average CPU throughput, such as cache, interrupts, and task scheduling by operating systems, are contributing to this non-deterministic and unaccounted delays in the control loop. These deviations from design specifications degrade performance and sometimes completely destabilize the control-loop. This issue is being addressed by both the controls and the computer engineering communities and now more often in collaboration. This dissertation addresses this challenge by adding application specific hardware accelerators to computer architecture while maintaining ease of implementation. The proposed solution is an on-chip co-processor implemented on a Field Programmable Gate Array (FPGA) to support the servicing of many simple plants or a single plant of many states, while maintaining microsecond level response times, tight deterministic control loop execution while allowing the main processor to service non-control tasks. We also study the effect of variations in digital control-loop delay on a plant's stability using an actual embedded platform consisting of a hardware-based plant emulator, as opposed to software-based simulations. Our experiments show that our test environment gives a significantly more accurate representation of the real system. The computation core of the co-processor is then redesigned to be scalable so that we can analyze the time-space complexity of the architecture.