Curriculum Vitae

JOSEPH ZAMBRENO

Department of Electrical and Computer Engineering
Iowa State University
Ames, IA 50011-3060

Email: zambreno@iastate.edu
Phone: (515) 294-3312
Fax: (515) 294-1152

APPOINTMENTS

2017–present	Professor of Electrical and Computer Engineering, Iowa State University
2012–2017	Associate Professor of Electrical and Computer Engineering, Iowa State University
2006–2012	Assistant Professor of Electrical and Computer Engineering, Iowa State University
2001–2006	Graduate Research Assistant, Northwestern University

PROFESSIONAL PREPARATION

Northwestern University	Evanston, IL	Electrical and Computer Engineering	Ph.D.	2006
Northwestern University	Evanston, IL	Electrical and Computer Engineering	M.S.	2002
Northwestern University	Evanston, IL	Computer Engineering	B.S.	2001

RESEARCH INTERESTS

- Computer architecture and compilers
- Reconfigurable computing and FPGAs
- Computer security, cryptography, and software protection
- Embedded systems and high-level design methodologies
- Low-power and power-aware computing

HONORS AND AWARDS

October 2016	Warren B. Boast Undergraduate Teaching Award, Iowa State University
November 2014	Research feature in NSF's "Perspectives on Broader Impacts" publication
August 2012	IEEE Senior Membership
June 2012	ACM SIGDA Distinguished Service Award
May 2012	ISU Award for Early Achievement in Teaching
April 2012	ISU College of Engineering Faculty Member of the Year
2012–2016	National Science Foundation CAREER Award
May 2011	Warren B. Boast Undergraduate Teaching Award, Iowa State University
September 2010	Article featured in IEEE's "Computing Now" research highlights
March 2010	Article featured in IEEE's "Computing Now" research highlights
May 2009	Warren B. Boast Undergraduate Teaching Award, Iowa State University
June 2006	EECS Department Best Dissertation Award, Northwestern University
2005–2006	Northwestern University Graduate Research Fellowship
2002–2005	National Science Foundation Graduate Research Fellowship
2001–2002	Walter P. Murphy Fellowship
June 2001	Graduation with distinction *summa cum laude*, Northwestern University

2000–2001	Motorola Undergraduate Research Award
2000–present	Tau Beta Pi Engineering Honors Society
2000–present	Eta Kappa Nu Electrical and Computer Engineering Honors Society

TEACHING EXPERIENCE

1. EE+SE 491 - *Senior Design Project I and Professionalism*, Iowa State University. Semesters taught: F17, S18.
2. CprE 488 - *Embedded Systems Design*, Iowa State University. Semesters taught: S14 (with P. Jones), F14, F15, S17.
3. CprE 480 - *Graphics Processing and Architecture*, Iowa State University. Semesters taught: S11, S12, S13.
4. CprE 185 - *Introduction to Computer Engineering and Problem Solving I*, Iowa State University. Semesters taught: S10.
5. CprE 594 - *Embedded Systems Research Skills*, Iowa State University. Semesters taught: S09 (with P. Jones).
6. CprE 381 - *Computer Organization and Assembly Level Programming*, Iowa State University. Semesters taught: F08, F09, F10, F11, S12, F16.
7. CprE 588 - *Embedded Computer Systems*, Iowa State University. Semesters taught: S07 (with D. Rover), S08, S09, S10.
8. CprE 583 - *Reconfigurable Computing*, Iowa State University. Semesters taught: F06, F07, F12, F13, F14, F15.
9. ECE 510 - *Computer Security and Information Assurance*, Northwestern University. Quarters taught: S05 (with A. Choudhary), S04 (with A. Choudhary).
10. ECE 362 - *Computer Architecture Projects*, Northwestern University. Quarters taught: W05 (with A. Choudhary), W04 (with A. Choudhary).

PROFESSIONAL ACTIVITY

Technical and Organizing Committees

- Technical Program Committee, Great Lakes Symposium on VLSI (GLSVLSI), 2015–2017
- Technical Program Committee, IEEE/ACM International Workshop on System-Level Interconnect Prediction (SLIP), 2016
- Technical Program Committee, IEEE International Symposium on Hardware-Oriented Security and Trust (HOST), 2011–2016
- Publications Chair, IEEE/ACM International Workshop on System-Level Interconnect Prediction (SLIP), 2015
- Technical Program Committee, IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2015

- Technical Program Committee, IEEE International Conference on Computer Design (ICCD), 2013, 2017
- Technical Program Committee, IEEE International Conference on Networking, Architecture, and Storage (NAS), 2013
- Technical Program Committee, International Conference on High Performance Computing (HiPC), Student Research Symposium, 2009–2013
- Technical Program Committee, International Conference on Contemporary Computing (IC3), 2011
- Technical Program Committee, IEEE International Conference on Microelectronic Systems Education (MSE), 2009
- Technical Program Committee, ACM SIGDA Student Research Competition at the Design Automation Conference (SRC@DAC), 2012
- Technical Program Committee, ACM SIGDA Student Research Competition at the International Conference on Computer Aided Design (SRC@ICCAD), 2013
- SIGDA University Booth Organizer, Design Automation Conference (DAC), 2008–2013
- Publicity Chair + Technical Program Committee, IEEE International Conference on Electro/Information Technology (EIT), 2008
- Student Advocate, International Symposium on Microarchitecture (MICRO), 2007
- Technical Program Committee, International Workshop on High Performance Data Mining (HPDM), 2007

Proposal Reviewing

- NSF Panelist, Graduate Research Fellowship Program (GRFP), 2017
- NSF Panelist, Small Business Innovation Research (SBIR) Program, Image and Video, 2016
- NSF Panelist, Small Business Innovation Research (SBIR) Program, Advanced Data Analytics, 2016
- NSF Panelist, Cyber-Physical Systems (CPS) Program, 2015
- NSF Panelist, Computer Systems Research (CSR) Program, 2015
- NSF Panelist, Secure, Trustworthy, Assured and Resilient Semiconductors and Systems (STARSS) Program, 2015
- NSF Panelist, Trustworthy Computing (TC) Program, 2009

Other Reviewing Activities

- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Transactions on Reconfigurable Technology and Systems (TRETS)
- IEEE/ACM Transsactions on Networking (TNET)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on Circuits and Systems I (TCAS-I)
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Dependable and Secure Computing (TDSC)
- IEEE Transactions on Parallel and Distributed Systems (TPDS)
- IEEE Transactions on Information Forensics and Security (TIFS)

- IEEE Design & Test of Computers (DT)
- IEEE Embedded Systems Letters
- IEEE Computer
- IEEE Micro
- EURASIP Journal on Advances in Signal Processing
- IEE Proceedings on Information Security
- International Journal of Computers and Applications (IJCA)
- International Journal of Computers and Electrical Engineering
- Journal of Systems and Software (JSS)
- The Journal of Supercomputing (TJS)
- Journal of Microprocessors and Microsystems
- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
- International Symposium on Microarchitecture (MICRO)
- International Symposium on High-Performance Computer Architecture (HPCA)
- International Conference for High Performance Computing, Neteworking, Storage, and Analysis (SC)
- Design Automation Conference (DAC)
- International Conference on VLSI Design (VLSID)
- International Conference on Computer Design (ICCD)
- Asia and South Pacific Design Automation Conference (ASP-DAC)
- IEEE International Symposium on Network Computing and Applications (NCA)
- International Symposium on Information Processing in Sensor Networks (IPSN)

Professional Memberships

- IEEE (M'02, SM'12)
- IEEE Computer Society (2004–present)
- ACM (2011–present)
- ACM SIGDA (2011–present)
- ASEE (2014–present)

PUBLICATIONS

Books and Book Chapters

1. A. Pande and **J. Zambreno**. *Embedded Multimedia Security Systems*, Springer-Verlag, London, 146 pages, 2013.

Journal Papers

2. P. Zhang, A. Mills, **J. Zambreno** and P. Jones, "The Design and Integration of a Software Configurable and Parallelized Coprocessor Architecture for LQR Control", *Journal of Parallel and Distributed Computing (JPDC)*, vol. 106, pp. 121-131, 2017.

3. C. Nelson, K. Townsend, O. Attia, P. Jones and **J. Zambreno**, "RAMPS: A Reconfigurable Architecture for Minimal Perfect Sequencing", *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 27, no. 10, 2016.

4. X. Wang, P. Jones and **J. Zambreno**, "A Configurable Architecture for Sparse LU Decomposition on Matrices with Arbitrary Patterns", *ACM Computer Architecture News (CAN)*, vol. 43, no. 4, 2015.

5. T. Johnson, D. Roggow, P. Jones and **J. Zambreno**, "An FPGA Architecture for the Recovery of WPA/WPA2 Keys", *Journal of Circuits, Systems, and Computers (JCSC)*, vol. 24, no. 7, 2015.

6. M. Monga, D. Roggow, M. Karkee, S. Sun, L. K. Tondehal, B. Steward, A. Kelkar and **J. Zambreno**, "Real-time Simulation of Dynamic Vehicle Models using a High-performance Reconfigurable Platform", *Microprocessors and Microsystems*, vol. 39, no. 8, pp. 720-740, 2015.

7. O. Attia, K. Townsend, P. Jones and **J. Zambreno**, "A Reconfigurable Architecture for the Detection of Strongly Connected Components", *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, vol. 9, no. 2, 2015.

8. K. Townsend, O. Attia, P. Jones and **J. Zambreno**, "A Scalable Unsegmented Multi-port Memory for FPGA-based Systems", *International Journal of Reconfigurable Computing (IJRC)*, vol. 2015, December, 2015.

9. C. Kumar, S. Vyas, R. Cytron, C. Gill, **J. Zambreno** and P. Jones. "Hardware-Software Architecture for Priority Queue Management in Real-time and Embedded Systems", *International Journal of Embedded Systems (IJES)*, vol. 6, no. 4, pp. 319-334, 2014.

10. S. Vyas, C. Kumar, **J. Zambreno**, C. Gill, R. Cytron and P. Jones. "An FPGA-based Plant-on-Chip Platform for Cyber-Physical System Analysis", *IEEE Embedded Systems Letters (ESL)*, vol. 6, no. 1, pp. 4-7, 2014.

11. A. Pande, S. Chen, P. Mohapatra and **J. Zambreno**. "Hardware Architecture for Video Authentication using Sensor Pattern Noise", *IEEE Transactions on Circuits and Systems for Video Technology (TCSVT)*, vol. 24, no. 1, pp. 157-167, 2014.

12. S. Vyas, A. Gupte, C. Gill, R. Cytron, **J. Zambreno**, and P. Jones. "Hardware Architectural Support for Control Systems and Sensor Processing", *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 13, no. 2, 2013.

13. A. Pande, P. Mohapatra, and **J. Zambreno**. "Securing Multimedia Content using Joint Compression and Encryption", *IEEE MultiMedia (MM)*, vol. 20, no. 4, pp. 50-61, 2013.

14. A. Pande and **J. Zambreno**. "A Chaotic Encryption Scheme for Real-time Embedded Systems: Design and Implementation", *Telecommunication Systems*, vol. 52, no. 2, pp. 551-561, 2013.

15. A. Pande, **J. Zambreno**, and P. Mohapatra. "Comments on 'Arithmetic Coding as a Non-Linear Dynamical System"', *Communications in Nonlinear Science and Numerical Simulation (CNSNS)*, vol. 17, no. 12, pp. 4536-4543, 2012.

16. A. Pande and **J. Zambreno**. "Poly-DWT: Polymorphic Wavelet Hardware Support For Dynamic Image Compression", *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 11, no. 1, 2012.

17. S. Sun, M. Monga, P. Jones, and **J. Zambreno**. "An I/O Bandwidth-Sensitive Sparse Matrix-Vector Multiplication Engine on FPGAs", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, vol. 59, no. 1, pp. 113-123, 2012.

18. S. Sun and **J. Zambreno**. "Design and Analysis of a Reconfigurable Platform for Frequent Pattern Mining", *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 22, no. 9, pp. 1497-1505, 2011.

19. A. Pande and **J. Zambreno**. "Efficient Mapping and Acceleration of AES on Custom Multi-Core Architectures", *Concurrency and Computation: Practice and Experience*, vol. 23, no. 4, pp. 372-389, 2011.

20. A. Baumgarten, M. Steffen, M. Clausman, and **J. Zambreno**. "A Case Study in Hardware Trojan Design and Implementation", *International Journal of Information Security (IJIS)*, vol. 10, no. 1, pp. 1-14, 2011.

21. A. Pande and **J. Zambreno**. "Reconfigurable Hardware Implementation of a Modified Chaotic Filter Bank Scheme", *International Journal of Embedded Systems (IJES)*, vol. 4, no. 3, pp. 248-258, 2010.

22. A. Pande and **J. Zambreno**. "The Secure Wavelet Transform", *Springer Journal of Real-Time Image Processing (RTIP)*, 2010.

23. A. Baumgarten, A. Tyagi, and **J. Zambreno**. "Preventing Integrated Circuit Piracy using Reconfigurable Logic Barriers", *IEEE Design and Test of Computers*, vol. 27, no. 1, pp. 66-75, January 2010.

24. G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. "Protecting Secure Execution Environments with a Last Line of Defense Against Trojan Circuit Attacks", *Computers and Security*, vol. 28, no. 7, pp. 660-669, October 2009.

25. S. Sun, Z. Yan, and **J. Zambreno**. "Demonstrable Differential Power Analysis Attacks on Real-World FPGA-Based Embedded Systems", *Integrated Computer-Aided Engineering*, vol. 16, no. 2, pp. 119-130, April 2009.

26. J. Sathre and **J. Zambreno**. "Automated Software Attack Recovery using Rollback and Huddle", *Springer Journal of Design Automation for Embedded Systems (DAES)*, vol. 12, no. 3, pp. 243-260, September 2008.

27. D. Nguyen, A. Das, **J. Zambreno**, G. Memik, and A. Choudhary. "An FPGA-Based Network Intrusion Detection Architecture", *IEEE Transactions on Information Forensics and Security (TIFS)*, vol. 3, no. 1, pp. 118-132, March 2008.

28. A. Das, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. "Microarchitectures for Managing Chip Revenues under Process Variations", *IEEE Computer Architecture Letters*, vol. 6, no. 2, pp. 29–32, July 2007.

29. **J. Zambreno**, D. Honbo, A. Choudhary, R. Simha, and B. Narahari. "High-Performance Software Protection using Reconfigurable Architectures", *Proceedings of the IEEE*, vol. 94, no. 2, pp. 1–13, February 2006.

30. **J. Zambreno**, A. Choudhary, R. Simha, B. Narahari, and N. Memon. "SAFE-OPS: An Approach to Embedded Software Security", *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 4, no. 1, pp. 189–210, February 2005.

Conference and Workshop Papers

31. P. Zhang, **J. Zambreno** and P. Jones, "An Embedded Scalable Linear Model Predictive Hardware-based Controller using ADMM", *Proceedings of the International Conference on Application-specific Systems, Architectures and Processors (ASAP)*, July, 2017.

32. D. Rover, **J. Zambreno**, M. Mina, P. Jones, D. Jacobson, S. McKilligan and A. Khokhar, "Riding the Wave of Change in Electrical and Computer Engineering", *Proceedings of the Annual Conference of the American Society for Engineering Education (ASEE)*, June 2017.

33. M. Qasaimeh, P. Jones and **J. Zambreno**, "A Modified Sliding Window Architecture for Efficient BRAM Resource Utilization", *Proceedings of the Reconfigurable Architectures Workshop (RAW)*, May, 2017

34. C. Young, **J. Zambreno**, and G. Bloom, "Towards a Fail-Operational Intrusion Detection System for In-Vehicle Networks", *Proceedings of the Workshop on Security and Dependability of Critical Embedded Real-Time Systems (CERTS)*, November, 2016.

35. X. Zhu, M. Awatramani, D. Rover, and **J. Zambreno**, "ONAC: Optimal Number of Active Cores Detector for Energy Efficient GPU Computing", *Proceedings of the International Conference on Computer Design (ICCD)*, October, 2016.

36. X. Wang and **J. Zambreno**, "Parallelizing Latent Semantic Indexing Using an FPGA-based Architecture", *Proceedings of the International Conference on Computer Design (ICCD)*, October, 2016.

37. D. Rover, **J. Zambreno**, M. Mina, P. Jones, and L. Chrystal, "Evidence-Based Planning to Broaden the Participation of Women in Electrical and Computer Engineering", *Proceedings of the Frontiers in Education Conference (FIE)*, October, 2016.

38. A. Mills, P. Jones, and **J. Zambreno**, "Parameterizable FPGA-based Kalman Filter Coprocessor using Piecewise Affine Modeling", *Proceedings of the Reconfigurable Architectures Workshop (RAW)*, May, 2016.

39. O. Attia, A. Grieve, K. Townsend, P. Jones and **J. Zambreno**, "Accelerating All-Pairs Shortest Path Using A Message-Passing Reconfigurable Architecture", *Proceedings of the International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, December, 2015.

40. P. Zhang, A. Mills, **J. Zambreno** and P. Jones, "A Software Configurable and Parallelized Coprocessor Architecture for LQR Control", *Proceedings of the International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, December, 2015.

41. A. Mills, P. Zhang, S. Vyas, **J. Zambreno** and P. Jones, "A Software Configurable Coprocessor-Based State-Space Controller", *Proceedings of the International Symposium on Field-Programmable Logic and Applications (FPL)*, September, 2015.

42. M. Awatramani, X. Zhu, **J. Zambreno** and D. Rover, "Phase Aware Warp Scheduling: Mitigating Effects of Phase Behavior in GPGPU Applications", *Proceedings of the International Conference on Parallel Architectures and Compilation Techniques (PACT)*, October, 2015.

43. X. Wang, P. Jones and **J. Zambreno**, "A Configurable Architecture for Sparse LU Decomposition on Matrices with Arbitrary Patterns", *Proceedings of the International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART)*, June, 2015.

44. D. Roggow, P. Uhing, P. Jones and **J. Zambreno**, "A Project-Based Embedded Systems Design Course Using a Reconfigurable SoC Platform", *Proceedings of the International Conference on Microelectronic Systems Education (MSE)*, May, 2015.

45. K. Townsend, S. Sun, T. Johnson, O. Attia, P. Jones and **J. Zambreno**, "k-NN Text Classification using an FPGA-Based Sparse Matrix Vector Multiplication Accelerator", *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May, 2015.

46. K. Townsend and **J. Zambreno**, "A Multi-Phase Approach to Floating-Point Compression", *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May, 2015.

47. A. Mills and **J. Zambreno**, "Estimating State of Charge and State of Health of Rechargable Batteries on a Per-Cell Basis", *Proceedings of the Workshop on Modeling and Simulation of Cyber-Physical Energy Systems (MSCPES)*, April, 2015.

48. K. Townsend, P. Jones and **J. Zambreno**. "A High Performance Systolic Architecture for k-NN Classification", *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, October 2014.

49. C. Kumar, S. Vyas, R. Cytron, C. Gill, **J. Zambreno**, and P. Jones. "Cache Design for Mixed Critical Real-Time Systems", *Proceedings of the International Conference on Computer Design (ICCD)*, October 2014.

50. M. Awatramani, D. Rover and **J. Zambreno**. "Perf-Sat: Runtime Detection of Performance Saturation for GPGPU Applications", *Proceedings of the International Workshop on Scheduling and Resource Management for Parallel and Distributed Systems (SRMPDS)*, September 2014.

51. X. Wang, P. Jones and **J. Zambreno**. "A Recongurable Architecture for QR Decomposition Using A Hybrid Approach", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2014.

52. A. Mills and **J. Zambreno**. "Towards Scalable Monitoring and Maintenance of Rechargeable Batteries", *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, June 2014.

53. X. Wang and **J. Zambreno**, "An FPGA Implementation of the Hestenes-Jacobi Algorithm for Singular Value Decomposition", *Proceedings of the Reconfigurable Architectures Workshop (RAW)*, May 2014.

54. O. Attia, T. Johnson, K. Townsend, P. Jones and **J. Zambreno**. "CyGraph: A Reconfigurable Architecture for Parallel Breadth-First Search", *Proceedings of the Reconfigurable Architectures Workshop (RAW)*, May 2014.

55. X. Wang and **J. Zambreno**. "An Efficient Architecture for Floating-Point Eigenvalue Decomposition", *Proceedings of the International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 2014.

56. A. Krishna, **J. Zambreno**, and S. Krishnan. "Polarity Trend Analysis of Public Sentiment on YouTube", *Proceedings of the International Conference on Management of Data (COMAD)*, December 2013.

57. M. Awatramani, **J. Zambreno**, and D. Rover. "Increasing GPU Throughput using Kernel Interleaved Thread Block Scheduling", *Proceedings of the International Conference on Computer Design (ICCD)*, October 2013.

58. K. Townsend and **J. Zambreno**. "Reduce, Reuse, Recycle (R^3): a Design Methodology for Sparse Matrix Vector Multiplication on Reconfigurable Platforms", *Proceedings of the International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, June 2013.

59. C. Kumar, S. Vyas, R. Cytron, C. Gill, **J. Zambreno**, and P. Jones. "Scheduling Challenges in Mixed Critical Real-time Heterogeneous Computing Platforms", *Proceedings of Dynamic Data Driven Application Systems (DDDAS)*, June 2013.

60. M. Patterson, A. Mills, R. Scheel, J. Tillman, E. Dye, and **J. Zambreno**. "A Multi-Faceted Approach to FPGA-Based Trojan Circuit Detection", *Proceedings of the IEEE VLSI Test Symposium (VTS)*, April 2013.

61. A. Mills, S. Vyas, M. Patterson, C. Sabotta, P. Jones, and **J. Zambreno**. "Design and Evaluation of a Delay-Based FPGA Physically Unclonable Function", *Proceedings of the International Conference on Computer Design (ICCD)*, September 2012.

62. C. Nelson, K. Townsend, B. S. Rao, P. Jones, and **J. Zambreno**. "Shepard: A Fast Exact Match Short Read Aligner", *Proceedings of the International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, July 2012.

63. M. Steffen and **J. Zambreno**. "Exposing High School Students to Concurrent Programming Principles using Video Game Scripting Engines", *Proceedings of the Annual Conference of the American Society for Engineering Education (ASEE)*, June 2012.

64. M. Steffen, P. Jones and **J. Zambreno**. "Introducing Graphics Processing from a Systems Perspective: A Hardware / Software Approach", *Proceedings of the Annual Conference of the American Society for Engineering Education (ASEE)*, June 2012.

65. C. Kumar, S. Vyas, J. Shidal, R. Cytron, C. Gill, **J. Zambreno**, and P. Jones. "Improving System Predictability and Performance via Hardware Accelerated Data Structures", *Proceedings of Dynamic Data Driven Application Systems (DDDAS)*, June 2012.

66. M. Monga, M. Karkee, L. K. Tondehal, B. Steward, A. Kelkar and **J. Zambreno**. "Real-Time Simulation of Dynamic Vehicle Models using a High-performance Reconfigurable Platform", *Proceedings of the International Conference on Computational Science (ICCS)*, June 2012.

67. A. Pande, P. Mohapatra, and **J. Zambreno**. "Using Chaotic Maps for Encrypting Image and Video Content", *Proceedings of the International Symposium on Multimedia (ISM)*, December 2011.

68. J. Rilling, D. Graziano, J. Hitchcock, T. Meyer, X. Wang, P. Jones, and **J. Zambreno**. "Circumventing a Ring Oscillator Approach to FPGA-Based Hardware Trojan Detection", *Proceedings of the International Conference on Computer Design (ICCD)*, October 2011.

69. A. Pande, **J. Zambreno**, and P. Mohapatra. "Hardware Architecture for Simultaneous Arithmetic Coding and Encryption", *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, July 2011.

70. A. Pande, **J. Zambreno**, and P. Mohapatra. "Architectures for Simultaneous Coding and Encryption using Chaotic Maps", *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2011.

71. M. Steffen, P. Jones, and **J. Zambreno**. "Teaching Graphics Processing and Architecture using a Hardware Prototyping Approach", *Proceedings of the International Conference on Microelectronic Systems Education (MSE)*, June 2011.

72. M. Steffen and **J. Zambreno**. "Improving SIMT Efficiency of Global Rendering Algorithms with Architectural Support for Dynamic Micro-Kernels", *Proceedings of the International Symposium on Microarchitecture (MICRO)*, pp. 237-248, December 2010.

73. A. Pande, **J. Zambreno**, and P. Mohapatra. "Joint Video Compression and Encryption using Arithmetic Coding and Chaos", *Proceedings of the IEEE International Conference on Internet Multimedia Systems Architecture and Applications (IMSAA)*, December 2010.

74. A. Pande and **J. Zambreno**. "Design and Hardware Implementation of a Chaotic Encryption Scheme for Real-Time Embedded Systems", *Proceedings of the IEEE Signal Processing and Communications Conference (SPCOM)*, July 2010.

75. M. Steffen and **J. Zambreno**. "A Hardware Pipeline for Accelerating Ray Traversal Algorithms on Streaming Processors", *Proceedings of the IEEE Symposium on Application Specific Processors (SASP)*, June 2010.

76. M. Karkee, M. Monga, B. Steward, **J. Zambreno**, and A. Kelkar. "Real-Time Simulation and Visualization Architecture with Field Programmable Gate Array (FPGA) Simulator", *Proceedings of the ASME World Conference on Innovative Virtual Reality (WINVR)*, May 2010.

77. A. Das, G. Memik, **J. Zambreno**, and A. Choudhary. "Detecting/Preventing Information Leakage on the Memory Bus due to Malicious Hardware", *Proceedings of Design, Automation, and Test in Europe (DATE)*, March 2010.

78. H. Chen, S. Sun, D. Aliprantis, and **J. Zambreno**. "Dynamic Simulation of DFIG Wind Turbines on FPGA Boards", *Proceedings of the Power and Energy Conference at Illinois (PECI)*, pp. 39-44, February 2010.

79. A. Pande and **J. Zambreno**. "A Reconfigurable Architecture for Secure Multimedia Delivery", *Proceedings of the International Conference on VLSI Design (VLSID)*, pp. 258-263, January 2010.

80. S. Sun and **J. Zambreno**. "A Floating-point Accumulator for FPGA-based High Performance Computing Applications", *Proceedings of the International Conference on Field-Programmable Technology (FPT)*, December 2009.

81. E. Leontie, G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. "Hardware-enforced Fine-grained Isolation of Untrusted Code", *Proceedings of the Workshop on Secure Execution of Untrusted Code (SecuCode)*, November 2009.

82. J. Sathre, A. Baumgarten, and **J. Zambreno**. "Architectural Support for Automated Software Attack Detection, Recovery, and Prevention", *Proceedings of the International Conference on Embedded and Ubiquitous Computing (EUC)*, August 2009.

83. A. Pande and **J. Zambreno**. "Efficient Translation of Algorithmic Kernels on Large-Scale Multi-Cores", *Proceedings of the International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES)*, August 2009.

84. E. Leontie, G. Bloom, B. Narahari, R. Simha, and **J. Zambreno**. "Hardware Containers for Software Components: A Trusted Platform for COTS-Based Systems", *Proceedings of the International Symposium on Trusted Computing and Communications (TrustCom)*, August 2009.

85. M. Steffen and **J. Zambreno**. "Design and Evaluation of a Hardware Accelerated Ray Tracing Data Structure", *Proceedings of Theory and Practice of Computer Graphics (TPCG)*, June 2009.

86. A. Pande and **J. Zambreno**. "An Efficient Hardware Architecture for Multimedia Encryption and Authentication using the Discrete Wavelet Transform", *Proceedings of the IEEE International Symposium on VLSI (ISVLSI)*, pp. 85-90, May 2009.

87. H. Chen, S. Sun, D. Aliprantis, and **J. Zambreno**. "Dynamic Simulation of Electric Machines on FPGA Boards", *Proceedings of the IEEE International Electric Machines and Drives Conference (IEMDC)*, May 2009.

88. S. Sun, M. Steffen, and **J. Zambreno**. "A Reconfigurable Platform for Frequent Pattern Mining", *Proceedings of the International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, December 2008.

89. A. Das, B. Ozisikyilmaz, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. "Evaluating the Effects of Cache Redundancy on Profit", *Proceedings of the International Symposium on Microarchitecture (MICRO)*, November 2008.

90. S. Sun and **J. Zambreno**. "Mining Association Rules with Systolic Trees", *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, September 2008.

91. A. Pande and **J. Zambreno**. "Polymorhpic Wavelet Architectures using Reconfigurable Hardware", *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, September 2008.

92. A. Pande and **J. Zambreno**. "Design and Analysis of Efficient Reconfigurable Wavelet Filters", *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May 2008.

93. S. Sun, Z. Yan, and **J. Zambreno**. "Experiments in Attacking FPGA-Based Embedded Systems using Differential Power Analysis", *Proceedings of the IEEE International Conference on Electro/Information Technology (EIT)*, May 2008.

94. A. Das, S. Misra, **J. Zambreno**, G. Memik, and A. Choudhary. "An Efficient FPGA Implementation of Principal Component Analysis-based Network Intrusion Detection System", *Proceedings of Design, Automation, and Test in Europe (DATE)*, March 2008.

95. S. Pati, R. Narayanan, G. Memik, A. Choudhary, and **J. Zambreno**. "Design and Implementation of an FPGA Architecture for High-Speed Network Feature Extraction", *Proceedings of the International Conference on Field-Programmable Technology (ICFPT)*, pp. 49–56, December 2007.

96. J. Sathre and **J. Zambreno**. "Rollback and Huddle: Architectural Support for Trustworthy Application Replay", *Proceedings of the Workshop on Embedded Software Security (WESS)*, October 2007.

97. A. Das, S. Ozdemir, G. Memik, **J. Zambreno**, and A. Choudhary. "Mitigating the Effects of Process Variation: Architectural Approaches for Improving Batch Performance", *Proceedings of the Workshop on Architectural Support for Gigascale Integration (ASGI)*, June 2007.

98. R. Narayanan, B. Ozisikyilmaz, G. Memik, A. Choudhary, and **J. Zambreno**. "Quantization Error and Accuracy-Performance Tradeoffs for Embedded Data Mining Workloads", *Proceedings of the International Workshop on High Performance Data Mining (HPDM)*, pp. 734–741, May 2007.

99. R. Narayanan, D. Honbo, G. Memik, A. Choudhary, and **J. Zambreno**. "An FPGA Implementation of Decision Tree Classification", *Proceedings of Design, Automation, and Test in Europe (DATE)*, pp. 189–194, April 2007.

100. A. Choudhary, R. Narayanan, B. Ozisikyilmaz, G. Memik, **J. Zambreno**, and J. Pisharath. "Optimizing Data Mining Workloads using Hardware Accelerators", *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, February 2007.

101. B. Ozisikyilmaz, R. Narayanan, **J. Zambreno**, G. Memik, and A. Choudhary. "An Architectural Characterization Study of Data Mining and Bioinformatics Workloads", *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, pp. 61–70, October 2006.

102. R. Narayanan, B. Ozisikyilmaz, **J. Zambreno**, G. Memik, and A. Choudhary. "MineBench: A Benchmark Suite for Data Mining Workloads", *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC)*, pp. 182–188, October 2006.

103. R. Simha, B. Narahari, **J. Zambreno**, and A. Choudhary. "Secure Execution with Components from Untrusted Foundries", *Proceedings of the Advanced Networking and Communications Hardware Workshop (ANCHOR)*, June 2006.

104. J. Pisharath, **J. Zambreno**, B. Ozisikyilmaz, and A. Choudhary. "Accelerating Data Mining Workloads: Current Approaches and Future Challenges in System Architecture Design", *Proceedings of the International Workshop on High Performance Data Mining (HPDM)*, April 2006.

105. **J. Zambreno**, B. Ozisikyilmaz, J. Pisharath, G. Memik, and A. Choudhary. "Performance Characterization of Data Mining Applications using MineBench", *Proceedings of the Workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW)*, February 2006.

106. **J. Zambreno**, T. Anish, and A. Choudhary. "A Run-Time Reconfigurable Architecture for Embedded Program Flow Verification", *Proceedings of the NATO Advanced Research Workshop (ARW) on Security and Embedded Systems*, August 2005.

107. O. Gelbart, P. Ott, B. Narahari, R. Simha, A. Choudhary, and **J. Zambreno**. "CODESSEAL: A Compiler/FPGA Approach to Secure Applications", *Proceedings of the IEEE International Conference on Intelligence and Security Informatics (ISI)*, pp. 530–535, May 2005.

108. K. Mohan, B. Narahari, R. Simha, P. Ott, A. Choudhary, and **J. Zambreno**. "Performance Study of a Compiler/Hardware Approach to Embedded Systems Security", *Proceedings of the IEEE International Conference on Intelligence and Security Informatics (ISI)*, pp. 543–548, May 2005.

109. **J. Zambreno**, D. Honbo, and A. Choudhary. "Exploiting Multi-Grained Parallelism in Reconfigurable SBC Architectures", *Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, pp. 333–334, April 2005.

110. R. Simha, A. Choudhary, B. Narahari, and **J. Zambreno**. "An Overview of Security-Driven Compilation", *Proceedings of the Workshop on New Horizons in Compiler Analysis and Optimizations*, December 2004.

111. D. Nguyen, **J. Zambreno**, and G. Memik. "Flow Monitoring in High-Speed Networks with 2D Hash Tables", *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, pp. 1093–1097, August 2004.

112. **J. Zambreno**, D. Nguyen and A. Choudhary, "Exploring Area/Delay Tradeoffs in an AES FPGA Implementation". *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, pp. 575–585, August 2004.

113. **J. Zambreno**. "Design and Evaluation of an FPGA Architecture for Software Protection", *Proceedings of the International Conference on Field-Programmable Logic and its Applications (FPL)*, p. 1180, August 2004. (poster paper)

114. **J. Zambreno**, R. Simha, and A. Choudhary. "Addressing Application Integrity Attacks using a Reconfigurable Architecture", *Proceedings of the ACM International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 2004. (poster paper)

115. **J. Zambreno**, A. Choudhary, R. Simha, and B. Narahari. "Flexible Software Protection using Hardware/Software Codesign Techniques", *Proceedings of Design, Automation, and Test in Europe (DATE)*, pp. 636–641, February 2004.

116. M. Kandemir, I. Kadayif, A. Choudhary, and **J. Zambreno**. "Optimizing Inter-nest Data Locality", *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, pp. 127–135, October 2002.

117. **J. Zambreno**, M. Kandemir, and A. Choudhary. "Enhancing Compiler Techniques for Memory Energy Optimizations", *Proceedings of the International Conference on Embedded Software (EMSOFT)*, pp. 364–381, October 2002.

Other Papers

118. **J. Zambreno**. *Compiler and Architectural Approaches to Software Protection and Security*. Ph.D. Thesis, Northwestern University, June 2006.

119. **J. Zambreno**. *Enhancing Compiler Techniques for Memory Energy Optimizations*. M.S. Thesis, Northwestern University, June 2001.

SELECTED TALKS

- **J. Zambreno**. "An FPGA-based Embedded Vision System for Real Time Motor-Grader Blade Tracking", John Deere ISG, May 2016.
- **J. Zambreno**, "Reconfigurable Computing at Iowa State: Research and Educational Activities", John Deere ISG (April 2015), Vermeer Corporation (May 2015).
- **J. Zambreno**. "How to use NVIDIA's GPUs on the CyEnce Cluster", HPC Training Workshop Series, Iowa State University, February 2016, October 2015.

- **J. Zambreno**. "The Security and Software Engineering Research Center (S2ERC) at Iowa State", Workiva (May 2014), John Deere ISG (September 2014), Sandia National Labs (January 2015), Resilient (January 2015), InfraGuard Iowa (August 2015).
- **J. Zambreno**, panelist. "Opportunities and Challenges of Research Collaboration between Industry and IS Academia", Big XII+ MIS Research Symposium, April 2015.
- **J. Zambreno**. "The Promise and Practice of Reconfigurable Application Acceleration", ECpE Faculty Seminar Series, Iowa State University, March 2015.
- **J. Zambreno**. "Engaging Students through Innovative Course Design", CELT Award-Winning Faculty Series, Iowa State University, January 2014.
- **J. Zambreno**. "Architectural Approaches to Embedded Program Flow Protection", Motorola Workshop on Security (held at Northwestern University), October 2006.
- **J. Zambreno** and B. Narahari. "Protecting Critical Computing Systems: A Hardware/Software Codesign Approach", Institute for Defense Analyses, March 2006.
- **J. Zambreno**. "Protecting Critical Computing Systems: A Hardware/Software Codesign Approach", University of Pittsburgh (April 2006), Texas A&M University (March 2006), Virginia Tech University (March 2006), Colorado State University (February 2006), Clemson University (February 2006), Iowa State University (February 2006).
- **J. Zambreno** and A. Choudhary. "Hardware/Software Co-Design for System Security", Institute for Defense Analyses (DARPA Workshop on Research Opportunities for Trusted ICs), August 2005.

SPONSORED RESEARCH FUNDING

External Funding

- "IUSE/PFE:RED: Reinventing the Instructional and Departmental Enterprise (RIDE) to Advance the Professional Formation of Electrical and Computer Engineers" (Co-PI with D. Jiles, S. Rajala, D. Rover, and D. Jacobson). *National Science Foundation (NSF), Revolutionizing Engineering Departments (RED) Program*. Total funding - $1,999,869, 2016–2021.
- "Collaborative Research: WI-ECSEL Scholarship Program (Women in Electrical, Computer, and Software Engineering as Leaders)" (PI with D. Jacobson, S. Rajala, D. Rover, M. Shelley, U. Tobey, J. Emmerson, K. Hensen, C. Sheller, M. Bausman, and H. Conley). *National Science Foundation (NSF), Scholarships in Science, Technology, Engineering, and Mathematics (S-STEM) Program*. Total funding - $4,999,954 (ISU share, $4,054,476), 2016–2021.
- "CPS: Breakthrough: Collaborative Research: Track and Fallback: Intrusion Detection to Counteract Carjack Hacks with Fail-Operational Feedback" (PI with G. Bloom). *National Science Foundation (NSF), Cyber Physical Systems (CPS) Program*. Total funding - $425,000 (ISU share, $190,449 + $16,000 REU supplement), 2016–2018.
- "CAREER:Architectural Support for CPU/GPU Hybridization" (PI). *National Science Foundation (NSF), CAREER Program*. Total funding - $466,310, 2012–2018.

External Funding (Completed)

- "An FPGA-Based Embedded Vision System for Real Time Motor-Grader Blade Tracking" (PI with co-PI P. Jones). *Deere and Company*. Total funding - $88,128, 2016.

- "CSR:Small:Hardware Architectures for Data Mining at the Exascale" (PI). *National Science Foundation (NSF), Computer Systems Research Program*. Total funding - $449,998 + $16,000 REU supplement, 2011–2016.
- "Industry Support for the Security and Software Engineering Research Center (S2ERC)" (PI). Various companies. Total funding - $120,000, 2014–2016.
- "An Adaptive Property-Aware HW/SW Framework for DDDAS" (Co-PI with P. Jones, N. Elia, R. Cytron, and C. Gill). *Air Force Office of Scientific Research (AFOSR), Dynamic Data Driven Application Systems Program*. Total funding - $299,987 (ISU share, $168,656), 2011–2013.
- "EAGER:Collaborative Research:Seamless Integration of Conjoined Cyber-Physical System Properties" (Co-PI with P. Jones, R. Cytron, and C. Gill). *National Science Foundation (NSF), Cyber-Physical Systems Program*. Total funding - $299,917 (ISU share, $149,928), 2010–2013.
- "CT-M: Hardware Containers for Software Components - Detection and Recovery at the Hardware/Software Interface" (Co-PI with R. Simha, B. Narahari, and A. Choudhary). *National Science Foundation (NSF), CyberTrust Program*. Total funding - $980,000 (ISU share - $200,000 + $16,000 REU supplement), 2009–2012.
- "Architectural Support for Detection and Recovery using Hardware Wrappers" (Co-PI with B. Narahari and R. Simha). *Air Force Office of Scientific Research (AFOSR)*. Total funding - $479,390 (ISU share - $172,083), 2009–2012.

Equipment and Software

- Donation of an NVIDIA GeForce GTX TITAN X GPU. *NVIDIA Hardware Grant Program*. Total commercial value - $999, 2015.
- Donation of Alpha-Data high performance reconfigurable computing platform and SDAccel software. *Xilinx University Program*. Total commercial value - $1,750, 2015.
- Donation of 10 Virtex 5 and 5 Virtex 6 FPGAs for use in high performance reconfigurable computing platform. *Xilinx University Program*. Total commercial value - $64,410, 2014.
- Donation of 4 Digilent Zedboards. *Xilinx University Program*. Total commercial value - $1,580, 2013.
- Donation of 5 DIGILAB-Atlys and 5 DIGILAB-Nexys3 boards. *Xilinx University Program*. Total commercial value - $2,740, 2012.
- Donation of 14 DIGILAB-XUP-V5 boards. *Xilinx University Program*. Total commercial value - $27,986, 2010.
- Donation of 15 Virtex 5 FPGAs for use in high performance reconfigurable computing platform. *Xilinx University Program*. Total commercial value - $57,268, 2010.
- Donation of 2 XUPV5-LX110T boards. *Xilinx University Program*. Total commercial value - $3,998, 2009.
- "A Strategic Vision for Autonomous Vehicle Research at Iowa State University" (PI with A. Stoytchev and A. Tyagi). *ECpE Strategic Planning and Execution Committee, Iowa State University*. Total funding - $25,000, 2008.
- "Comparative Studies on Using Multi-Core Processors in High-Performance Computing and Emerging Applications" (Co-PI with M. Chang, M. Sosonkina, and Z. Zhang). *ECpE Strategic Planning and Execution Committee, Iowa State University*. Total funding - $30,500, 2008.

- Donation of 16 Virtex 4 FPGAs for use in logic emulation platform. *Xilinx University Program*. Total commercial value - $75,000, 2007.
- "Laboratory for Trusted Embedded Systems" (Co-PI with T. Daniels, A. Tyagi, and Z. Zhang). *ECpE Strategic Planning Committee, Iowa State University*. Total funding - $50,000, 2007.

Internal Funding

- "Addressing Increasing Undergraduate Enrollment in ECpE with High-Capacity and High-Throughput Labs" (PI with D. Jacobson, S. Kovarik, M. Govindarasu, and D. Jiles). *Dean's Educational Initiatives, Iowa State University*. Total funding - $89,500 + $89,500 departmental match, 2012.
- "Enabling Real-time Vehicle Simulation with VR Interface using HW/SW Accelerators" (PI with B. Steward and A. Kelkar). *Information Infrastructure Institute (ICube), Iowa State University*. Total funding - $5,000, 2010.
- "Real-Time Management of Integrated Information, Physical, and Human Networks" (Co-PI with P. Jones). *Information Infrastructure Institute (ICube), Iowa State University*. Total funding - $5,000, 2009.
- "Enhancing Realism and Flexibilty of VR-Based Real-Time Dynamic Simulation Framework with Operator and Hardware-in-the-loop Interface" (Collaborator with A. Kelkar and B. Steward). *Virtual Reality Applications Center (VRAC), Iowa State University*. Personal share of funding - $50,000, 2008–2010.
- "Acceleration and Efficiency Exploration of Cryptographic Kernels on Multi-Core Processing Platforms" (PI). *Center for Information Protection (CIP), Iowa State University*. Total funding - $25,000, 2007–2008.
- "CODELESS: COnfigurable DEvices for Large-scale Energy System Simulation" (Co-PI with D. Aliprantis). *Information Infrastructure Institute (ICube)* and *Electric Power Research Center (EPRC), Iowa State University*. Total funding - $29,000, 2008–2009.
- "Architectural Approaches to Embedded Program Flow Protection" (PI). *Center for Information Protection (CIP), Iowa State University*. Total funding - $25,000, 2006–2007.

STUDENT SUPERVISION

Current Students

- Osama Attia, Ph.D. student
- Xian Zhu, Ph.D. student
- Clinton Young, Ph.D. student
- Quinn Murphy, M.S. student
- Joseph Avey, M.S. student

Previous Students

- Mihir Awatramani, Ph.D. 2017 (with D. Rover), *Workload-aware Scheduling Techniques for General Purpose Applications on Graphics Processing Units*. Currently at NVIDIA.
- Xinying Wang, Ph.D. 2016, *Using Reconfigurable Computing Technology to Accelerate Matrix Decomposition and its Applications*. Currently at Intel.

- Jeremy Bennett, Ph.D. 2016 (with J. Oliver), *Massive Model Visualization: A Practical Solution*. Currently at Siemens PLM Software.
- Dossay Oryspayev, Ph.D. 2016 (with P. Maris), *Performance Analysis and Acceleration of Nuclear Physics Application on High-Performance Computing Platforms using GPGPUs and Topology-Aware Mapping Techniques*. Currently at Iowa State University.
- Aaron Mills, Ph.D. 2016, *Design and Implementation of an FPGA-based Piecewise Affine Kalman Filter for Cyber-Physical Systems*. Currently at MIT Lincoln Laboratory.
- Kevin Townsend, Ph.D. 2016, *Sparse Matrix Vector Multiplication on FPGA-based Platforms*. Currently at Google.
- Sudhanshu Vyas, Ph.D. 2015 (with P. Jones), *Design Exploration of Hardware Accelerators for Mitigating the Effects of Computational Delay on Digital Control Loops*. Currently at Northrop Grumman.
- Michael Steffen, Ph.D. 2012, *A Hardware-Software Integrated Solution for Improved Single-Instruction Multi-Thread Processor Efficiency*. Currently at NVIDIA.
- Song Sun, Ph.D. 2011, *Analysis and Acceleration of Data Mining Algorithms on High Performance Reconfigurable Computing Platforms*. Currently at Symantec.
- Amit Pande, Ph.D. 2010, *Algorithms and Architectures for Secure Embedded Multimedia Systems*. Currently at University of California, Davis.
- Ben Williams, M.S. 2017, *Evaluation of a SoC for Real-time 3D SLAM*. Currently at Microsoft.
- Daniel Roggow, M.S. 2017, *Real-time Ellipse Detection on an Embedded Reconfigurable SoC*. Currently at Rockwell-Collins.
- Alex Grieve, M.S. 2016, *A Recompilation and Instrumentation-Free Monitoring Architecture for Detecting Heap Memory Errors and Exploits*. Currently at John Deere.
- Piriya Hall, M.S. 2016, *Adaptation of a GPU Simulator for Modern Architectures*. Currently at IBM.
- Matt Hinrichsen, M.S. 2014, *Reliable Authentication Using the Anderson PUF*. Currently at Workiva.
- Blake Vermeer, M.S. 2014 (with D. Jacobson), *Creating a Releasable Version of ISERink*. Currently at Keysight.
- Amar Krishna, M.S. 2014 (with L. Miller), *Polarity Trend Analysis of Public Sentiment on YouTube*. Currently at Chefling.
- Tyler Johnson, M.S. 2014, *An FPGA Architecture for the Recovery of WPA/WPA2 Keys*. Currently at Cerner.
- Zhong Hu, M.S. 2013 (with T. Bigelow), *Comparison of Gilmore-Akulichev Equation and Rayleigh-Plesset Equation on Therapeutic Ultrasound Bubble Cavitation*. Currently at TILE.
- Lakshmi Kiran Tondehal, M.S. 2013, *Optimization of Sparse-Matrix Vector Multiplication on Convey HC-1*. Currently at Micron.
- Michael Patterson, M.S. 2013, *Vulnerability Analysis of GPU Computing*. Currently at Pillar Technology.
- Aaron Mills, M.S. 2012, *Design and Evaluation of a Delay-Based FPGA Physically Unclonable Function*. Currently at MIT Lincoln Laboratory.
- Chad Nelson, M.S. 2012, *RAMPS: Reconfigurable Architecture for Minimal Perfect Sequencing using the Convey Hybrid Core Computer*. Currently at Talen-X.
- Justin Rilling, M.S. 2011, *Persistent Monitoring of Digital ICs to Verify Hardware Trust*.

Currently at Rockwell-Collins.
- Madhu Monga, M.S. 2010, *Real-Time Simulation of Dynamic Vehicle Models using High Performance Reconfigurable Computing Platforms*. Currently at Intel.
- Joel Millage, M.S. 2010, *GPU Integration into a Software Defined Radio Framework*. Currently at Integrity Applications.
- Dustin Counsell, M.S. 2010, *Evaluation of High-Level Hardware/Software Embedded System Design Flows*. Currently at MITRE.
- Jacob Braegelmann, M.S. 2009, *An Independent Analysis of High-Level System Modeling and Design Languages*. Currently at New Wave Design and Verification.
- Alex Baumgarten, M.S. 2009, *Preventing Integrated Circuit Piracy using Reconfigurable Logic Barriers*. Currently at Uber.
- Jesse Sathre, M.S. 2008, *Architectural Support for Secure and Survivable Software*. Currently at Iowa State.

Service on Ph.D. Graduate Student Committees

- Parijat Shukla (advisor - A. Somani), Ph.D., 2017, committee member
- Teng Wang (advisor - A. Somani), Ph.D., 2016, committee member
- Dan Gieseman (advisor - T. Daniels), Ph.D., 2015, committee member
- Yanan Cao (advisor - Z. Zhang), Ph.D., 2015, committee member
- Zhiming Zhang (advisor - M. Chang), Ph.D., 2015, committee member
- Chetan Kumar (advisor - P. Jones), Ph.D., 2015, committee member
- Pavan Kumar (advisor - A. Somani), Ph.D., 2014, committee member
- Long Chen (advisor - Z. Zhang), Ph.D., 2014, committee member
- Sparsh Mittal (advisor - Z. Zhang), Ph.D., 2013, committee member
- Meng Li (advisor - R. Kumar), Ph.D., 2013, committee member
- Sharhabeel Al Nabelsi (advisor - A. Kamal), Ph.D., 2012, committee member
- Hao Chen (advisor - D. Aliprantis), Ph.D., 2012, committee member
- Prasad Avirneni (advisor - A. Somani), Ph.D., 2012, committee member
- Tyler Sondag (advisor - H. Rajan), Ph.D., 2011, committee member
- Ramon Mercado (advisor - D. Rover), Ph.D., 2011, committee member
- Prem Ramesh (advisor - A. Somani), Ph.D., 2011, committee member
- Zijun Yan (advisor - C. Chu), Ph.D., 2011, committee member
- Abhinav Sarje (advisor - S. Aluru), Ph.D., 2010, committee member
- Abhishek Das (Northwestern University, advisor - A. Choudhary), Ph.D., 2010, committee member
- Benjamin Jackson (advisor - S. Aluru), Ph.D., 2009, committee member
- Viswanathan Subramanian (advisor - A. Somani), Ph.D., 2009, committee member
- Michael Frederick (advisor - A. Somani), Ph.D., 2008, committee member
- Pubali Banerjee (advisor - D. Jacobson), Ph.D., 2007, committee member
- Zhongbo Cao (advisor - D. Rover), Ph.D., TBD, committee member
- Bashar Gharaibeh (advisor - M. Chang), Ph.D., TBD, committee member
- Hao Ren (advisor - R. Kumar), Ph.D., TBD, committee member
- Piyush Lakhawat (advisor - A. Somani), Ph.D., TBD, committee member
- Pei Zhang (advisor - P. Jones), Ph.D., TBD, committee member

- Murad Qasaimeh (advisor - P. Jones), Ph.D., TBD, committee member
- Augusto Souza (advisor - S. Birrell), Ph.D., TBD, committee member
- Michael Williams (advisor - D. Rover), Ph.D., TBD, committee member

Service on M.S. Graduate Student Committees

- Jeramie Vens (advisor - D. Qiao), M.S., 2015, committee member
- Eric Rodine (advisor - D. Jacobson), M.S., 2015, committee member
- Christopher Farrington (advisor - D. Jacobson), M.S., 2015, committee member
- Arielle Czalbowski (advisor - D. Jacobson), M.S., 2015, committee member
- Yang Yang (advisor - T. Daniels), M.S., 2013, committee member
- Pooja Mhapsekar (advisor - P. Jones), M.S., 2013, committee member
- Matthew Sullivan (advisor - D. Jacobson), M.S., 2013, committee member
- Zhang Zhang (advisor - A. Tyagi), M.S., 2013, committee member
- Christian Fredrickson (advisor - D. Jacobson), M.S., 2013, committee member
- Moin Sayed (advisor - P. Jones), M.S., 2012, committee member
- J. Chargo (advisor - S. Kothari), M.S., 2012, committee member
- T. Meyer (advisor - Y. Guan), M.S., 2011, committee member
- D. Graziano (advisor - T. Daniels), M.S., 2011, committee member
- Preethika Kalyanasundaram (advisor - G. Manimaran), M.S., 2011, committee member
- Adwait Gupte (advisor - P. Jones), M.S., 2011, committee member
- Wade Paustian (advisor - T. Daniels), M.S., 2010, committee member
- Jeffrey Schmidt (advisor - Z. Zhang), M.S., 2009, committee member
- Andrew Riha (advisor - D. Rover), M.S., 2008, committee member
- Kenneth McVicker (advisor - D. Jacobson), M.S., 2007, committee member
- Eric Middleton (advisor - P. Jones), M.S., TBD, committee member
- Paul Baldwin (advisor - G. Manimaran), M.S., TBD, committee member

Undergraduate Student Supervision

- Michael Davies, 2017
- Victory Omole, 2017
- Bijan Choobineh, 2017 (REU)
- Zachary Glanz, 2016 (REU)
- Eric Middleton, 2016–2017 (REU)
- Dane Larson, 2016 (REU)
- Yazan Okasha, 2016–2017
- Nathan Kent, 2016
- Kevin Angeliu, 2016 (Freshman Honors program)
- Noah Ertz, 2016 (Freshman Honors program)
- Joshua Steffensmeier, 2016
- Michael Sgroi, 2015 (REU)
- Seth Rickard, 2015
- Alberto Di Martino, 2015
- Diva Agarwal, 2015

- Daniel Keith, 2015
- Quinn Murphy, 2015 (REU)
- Joseph Avey, 2015–2016 (REU)
- Bryce Wilson, 2014
- Joseph Meis, 2014
- Rohit Zambre, 2014
- Lamin Ceesay, 2014 (HHMI summer research program)
- Darren Hushak, 2014
- David Callen, 2014
- Grant Kamin, 2014 (Freshman Honors program)
- Jonathan Schmidt, 2014 (Freshman Honors program)
- Garret Meier, 2014 (Freshman Honors program)
- Kevin Engel, 2013 (REU)
- Mason Berhenke, 2013 (Freshman Honors program)
- Chris Rogers, 2013 (Freshman Honors program)
- Tanner Borglum, 2012–2013 (REU)
- Ryan Scheel, 2012 (REU)
- Robert Ray, 2012
- Matthew Rench, 2012
- Christopher Sabotta, 2011
- Kyle Peterson, 2011
- Max Mayfield, 2011–2012 (REU)
- Kevin Pope, 2011 (REU)
- Taehyun Park, 2010
- Jamin Hitchcock, 2010
- Mikhail Drob, 2010 (REU)
- Michael Patterson, 2010 (REU)
- Stephen LeBlanc, 2010 (Freshman Honors program)
- Abhishek Vemuri, 2010 (Freshman Honors program)
- Michael Carter, 2010 (Freshman Honors program)
- Bailey Steinfadt, 2010
- Greg Hogan, 2010
- Christopher Morgan, 2009 (Freshman Honors program)
- Gregory Gholson, 2009 (Freshman Honors program)
- Michael Svendsen, 2008 (Freshman Honors program)
- Dave Peters, 2008 (Freshman Honors program)
- Tim Meyer, 2007–2008 (Freshman Honors program)
- Cole Anagnost, 2007 (Freshman Honors program)

Senior Design Supervision

- Souparni Agnihotri, Fahmida Joyti, Eric Himmelbau, Ashley Dvorsky, and Bowen Zhang, "Use of Imaging Devices and Machine Learning Software to Assist in Autonomous Vehicle Path Planning", 2017-2018
- Alexander Orman, Chris Kelley, Lixing Liu, Evan Lambert, Sean Jellison, and Lucas Ince, "Autonomous Vehicle Processor", 2017

- Darren Davis, Bijan Choobineh, Tracy La Van, Jesse Luedtke, David Schott, and Robert Stemig, “Autonomous Learning Vehicle Integrating Neural Networks”, 2017
- Joseph Randazzo, Caleb Redman, Kit Kohl, Anthony Khounlo, Theim Nguyen, and Christopher Smit, “Arial Land Inspection System (ALIS), v2”, 2016-2017
- Matt Lee, Mike Croskey, Keane OKelley, Jordan Kauffman, and Samuel Oswalt, “Automotive Intrusion Detection System”, 2016-2017
- Katherine Gresback-Brock, David Orona, Jonathan Yeoh, Eric Riedl,“Binary LMS File Interpretation”, 2016
- Quinn Murphy, Brian Gillenwater, Bryce Poellet, Jonathan Schlueter, Nathan Kent, “Arial Land Inspection System (ALIS)”, 2015–2016
- Trevor Goodpasture, Kai Xiang Ching, Yufeng Jaing, Jongik Lee, “FPGA Signal Processing over Ethernet”, 2015–2016
- Alex Lende, Benjamin Williams, Joshua Steffensmeier, Nicholas Montelibano, Zachary Shaver, Ethan Brady, “Garmin Backboard: Computer Vision and Tracking Algorithm”, 2015–2016
- Caleb Van Dyke, Arlen Burroughs, Aaron Schafbuch, Mitch Meiss, Andrew Jiles, “SIDS Alert Device”, 2015
- Andy Heintz, Altay Ozen, Abe Devine, “Network Forensics User Interface”, 2014–2015
- Jake Bertram, Dan Smith, Kyle Tietz, Jacob Wallraff, Erich Kuerschner, Bryan Passini, “CoderLab: A Broswer-based Sandbox for Real-Time Code Collaboration”, 2014–2015
- Dustin Amesbury, Brittany Oswald, Wallace Davis, Darren Hushak, John Tuohy, “Chiptune Synthesizer”, 2013
- Allison Thongvanh, Matt Dresser, Riley Swindell, Blake Vermeer, Jordan Jacobson, “Automated Chess System”, 2013
- Taylor Anderson, Patrick Clark, Austin Laugen, Andrew Montag, Alison Spiess, “Project Hestia: Embedded Cloud Control and Automation”, 2012–2013
- Kevin Pope, Steven Bruening, MatthewDavid Grove, Max Mayfield, Michael Yeager, “Virtual Pinball Experience”, 2011–2012
- Brandon Otto, Jonathan Henze, Kevin Moore, Marvin Toeung, Richard Rojas, “Multi-Arcade Emulation System”, 2011–2012
- David Gartner, John Alexander, Danny Funk, Tony Milosch, Cory Mohling. “FPGA-based Arcade Emulation System”, 2010–2011
- Ashley Good, David Graziano, Tim Meyer, Matt Saladin. “FPGA-based Emulation of the Nintendo Entertainment System”, 2009–2010
- Adam Ahrens, Amelia Gee, Joshua Mensah, Jonathan Salvador, Bailey Steinfadt. “College of Engineering iPhone Application”, 2009–2010
- Derek Baldus, Greg Hogan, David Kaiser, Scott Penick. “Web-based Thermostat Control System”, 2008–2009
- Alex Burds, Jin-Ning Tioh, Tony Ross, Dave Zajicek. “Logic Design Training Tool”, 2007–2008
- Brendan Campbell, Sean Godinez, Daniel Risse, Aaron Westphal. “CyRay: An Interactive Ray Tracer for the PlayStation 3”, 2007–2008

Other Student Project Mentoring

- Jeramie Vens, Sebastian Roe, Kristopher Burney, Justin Wheeler, Andrew Snawerdt. “uCube”, Texas Instruments Innovation Challenge, 2015

Supervised Student Awards

- Quinn Murphy, Brian Gillenwater, Bryce Poellet, Jonathan Schlueter, Nathan Kent, *ECpE Best Senior Design Project Award*, 2nd place, 2016
- Daniel Roggow, *ASEE Science, Mathematics, and Research for Transformation (SMART) Scholarship* (declined), 2015
- Matt Hinrichsen, Aaron Mills, *CSI CyberSEED Hardware Challenge*, 1st place entry, 2014
- Kevin Townsend, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 1st place entry, 2014
- Daniel Roggow, *ISU Presidential Scholarship*, 2014
- Dustin Amesbury, Brittany Oswald, Wallace Davis, Darren Hushak, John Tuohy, *ECpE Best Senior Design Project Award*, 2013
- Amar Krishna, *International Conference on Management of Data (COMAD), Best Student Presentation Award*, 2013
- Chris Rogers, *University Honors Summer Research Grant*, 2013
- Taylor Anderson, Patrick Clark, Austin Laugen, Andrew Montag, Alison Spiess, *ECpE Best Senior Design Project Award*, 2013
- Chad Nelson and Kevin Townsend, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 1st place entry, 2012
- Michael Patterson, Christopher Sabotta, Sudhanshu Vyas, and Aaron Mills, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2011
- Amit Pande, *Zaffarano Prize for Graduate Research Research* (honorable mention), 2011
- Amit Pande, *Iowa State University Research Excellence Award (REA)*, 2010
- Amit Pande, *CRA/CCC Computing Innovation Fellow* (post-doctoral fellowship sponsored by NSF), 2010
- Michael Steffen and Veerendra Allada, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 5th place entry, 2010
- David Graziano, Tim Meyer, Jamin Hitchcock, Xinying Wang, and Justin Rilling, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2010
- Michael Steffen and Justin Rilling, *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE) Design Contest*, 2nd place entry (performance category), 2009
- Amit Pande, *International Conference on VLSI Design (VLSID) Design Contest*, 3rd place entry, 2009
- Alex Baumgarten and Michael Steffen, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 1st place entry, 2008
- Michael Steffen, *National Science Foundation (NSF) Graduate Research Fellowship*, 2008–2011
- Michael Steffen, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 3rd place entry, 2007
- Jesse Sathre, *Computer Security Awareness Week (CSAW) Embedded Systems Challenge*, 2nd place entry, 2007

- Tim Meyer, *University Honors Summer Research Grant*, 2007

UNIVERSITY SERVICE

2015–present	Member, Certificate in Computing Applications Committee
2014–present	Adviser, ISU chapter of Eta Kappa Nu (HKN)
2017–2018	Member, ECpE Promotion and Tenure Committee
2015–2017	Member, College Undergraduate Scholarships and Awards Committee
2016–2017	Chair, ECpE Search Committee, Computer / Software Engineering area
2012–2017	Member, ECpE Administrative Committee
2012–2017	ECpE Director of Undergraduate Education (DoUGE)
2012–2017	Chair, ECpE Curriculum Committee
2011–2017	Member, ECpE Student Professional Development Committee
2010–2017	Director of Certificate Studies (DOCS), Certificate in Embedded Systems
2010–2017	Director of Certificate Studies (DOCS), Certificate in Computer Networking
2014–2016	Site Director, Security and Software Engineering Research Center (S2ERC)
2014–2015	Member, ECpE Search Committee, "Emerging Needs" area
2014–2015	Member, ECpE Higher Learning Commission (HLC) Committee
2009–2015	Volunteer, IT Olympics Competition
2013–2014	Member, Iowa State University Emerging Leaders Academy (ELA)
2012–2013	Member, Student Innovation Center Communications Committee
2011–2012	Member, ECpE Curriculum Committee
2010–2011	Member, ECpE Promotion and Tenure Committee
2009–2010	Member, ECpE Senior Design Committee
2009–2011	Member, ECpE Graduate Committee
2009–2011	Chair, ECpE Computing and Networking Systems Group
2009–2011	Mentor, Engineering Leadership Program
2008–2010	Member, ECpE Chair Search Committee
2008–2010	Member, ECpE Elections and Oversight Committee
2008–2009	Member, ECpE Undergraduate Recruiting Committee
2007–2009	Member, ECpE Strategic Planning and Execution Committee
2007–2009	Member, ECpE Curriculum Committee
2006–2008	Member, ECpE Graduate Admissions Committee
Spring 2007	Judge, ECpE EAB poster competition
2014–present	Presenter, Computer Engineering students in EE/CprE 166
2011–2012	Presenter, ECpE Friday Activites at Noon (FAN) event
2008–present	Presenter, Undeclared Engineering students in ENGR 101
2006–present	Participant, Take Your Professor To Lunch (TYPTL) program
Spring 2008	Judge, Iowa State Science and Technology Fair
Spring 2007	Judge, Iowa State Science and Technology Fair