CprE 588
Embedded Computer Systems

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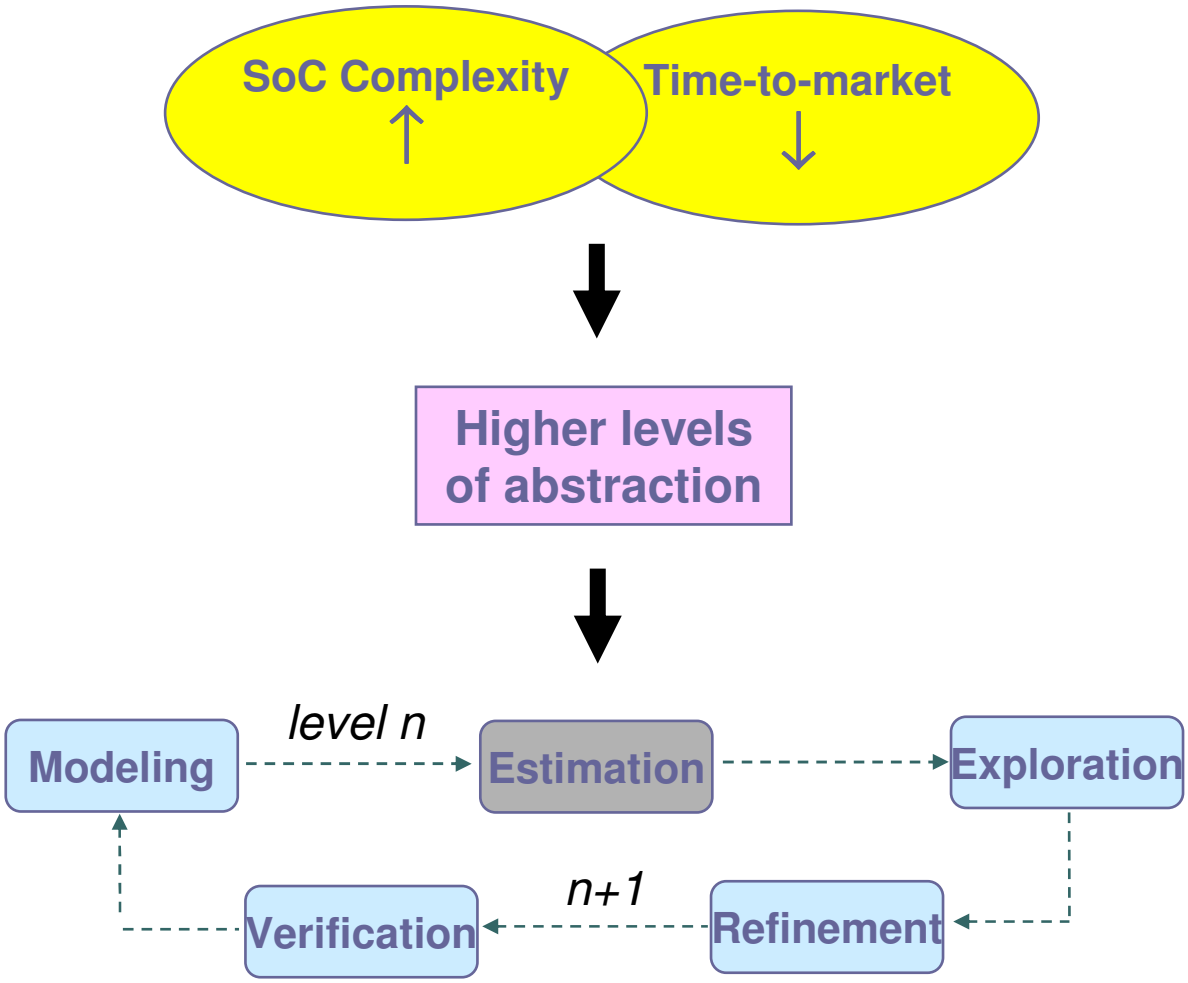
Lecture #8 – Architectural Specialization

Outline

- Motivation
- Related Work
- Design Flow
- Basic Concepts
- Multi-Metrics
- Experimental Results
- Conclusion

L. Cai, A. Gerstlauer, and D. Gajski, “Retargetable Profiling for Rapid, Early System-Level Design Space Exploration”, In *Proceedings of the Design Automation Conference (DAC*), 2004.

Motivation


SoC Complexity
Time-to-market
Higher levels of abstraction
level n
Modeling
Estimation
Exploration
n+1
Verification
Refinement

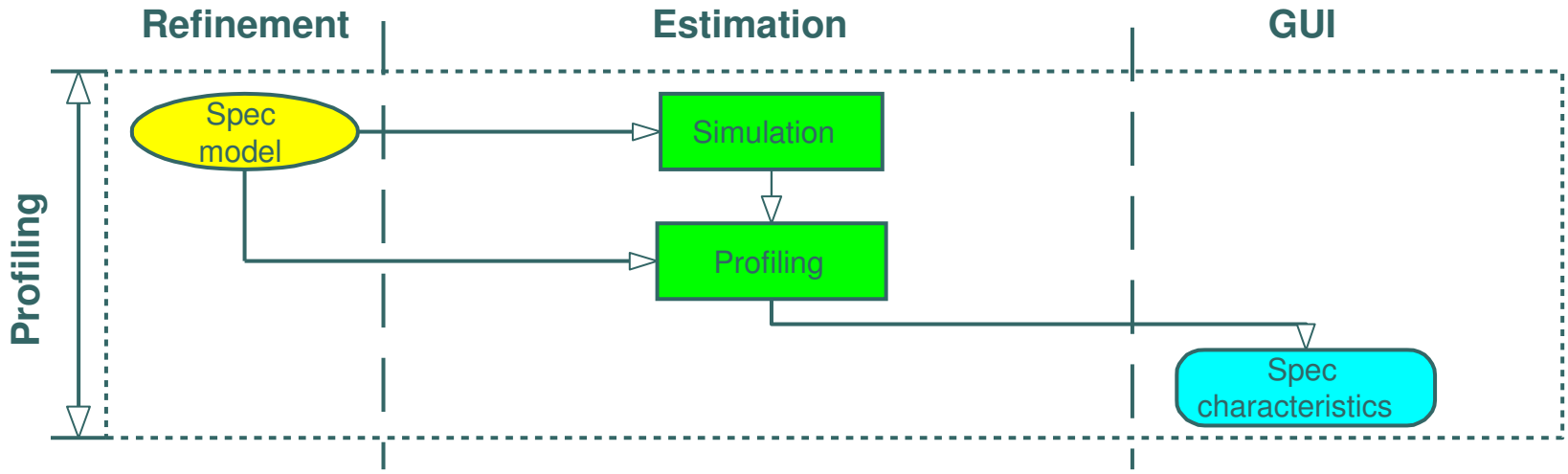
System Level Estimation

- Fast
- Accurate ➔ Fidelity
- Different abstraction levels
- Wide range of metrics
- Wide variety of target implementation

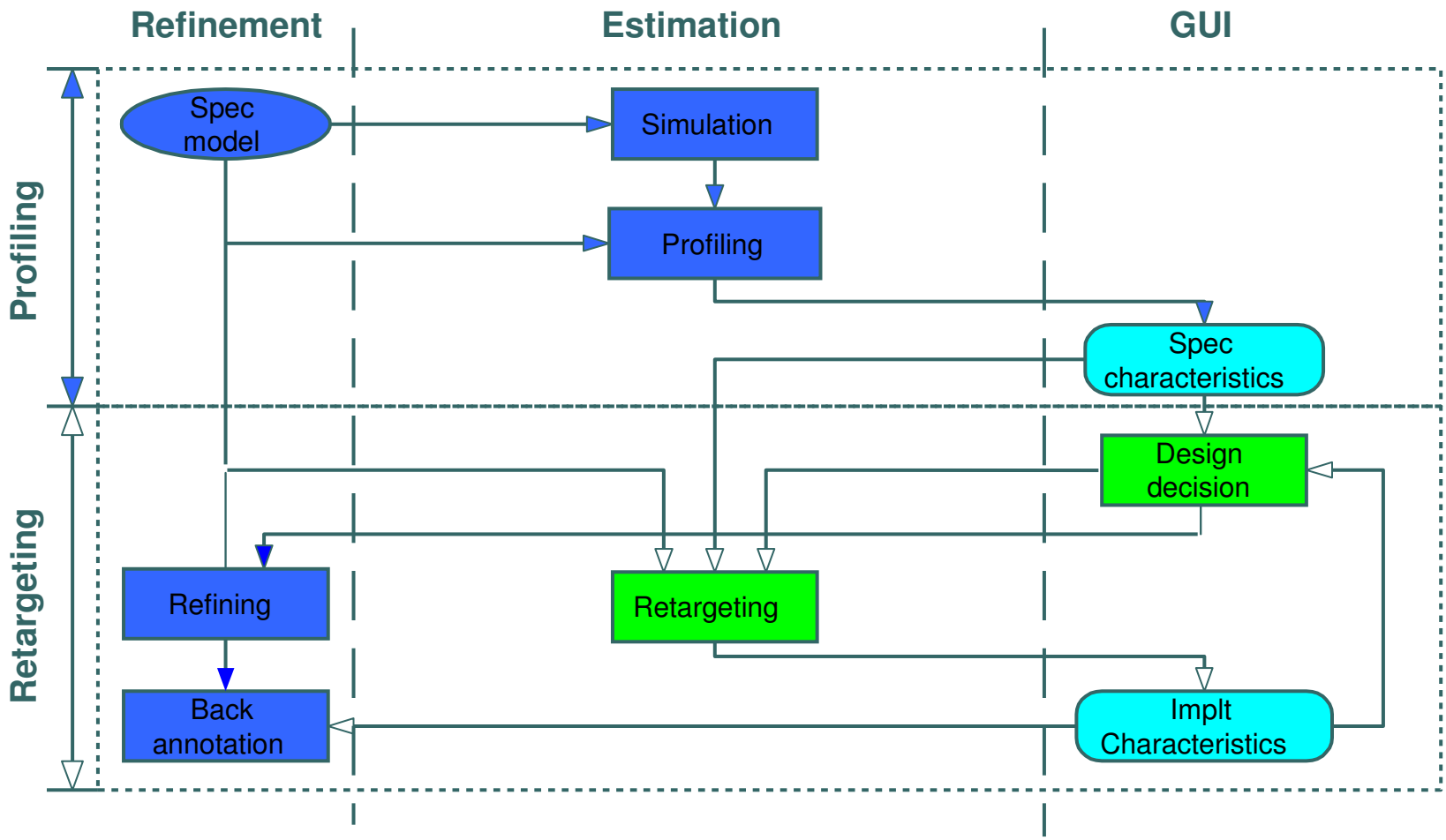
Related Work

- Static analysis-based approaches
  - **Examples**
    - WCET (Y. Li), scheduling analysis (G. Buttazzo)
    - Memory size estimation (Y. Zhao)
  - **Limitations**
    - Time-consuming, manual interference
- Dynamic simulation-based approaches
  - **Examples**
    - Profiling tools (GNU profiler)
    - Instruction-set simulators
    - Multi-processor, multi-level co-simulation (P. Gerin)
    - Trace-based simulation (K. Lahir, P. Lieverse)
  - **Limitations**
    - A simulation is required for each design alternative
    - Target/host machine-dependent characteristics
    - Operation-related data

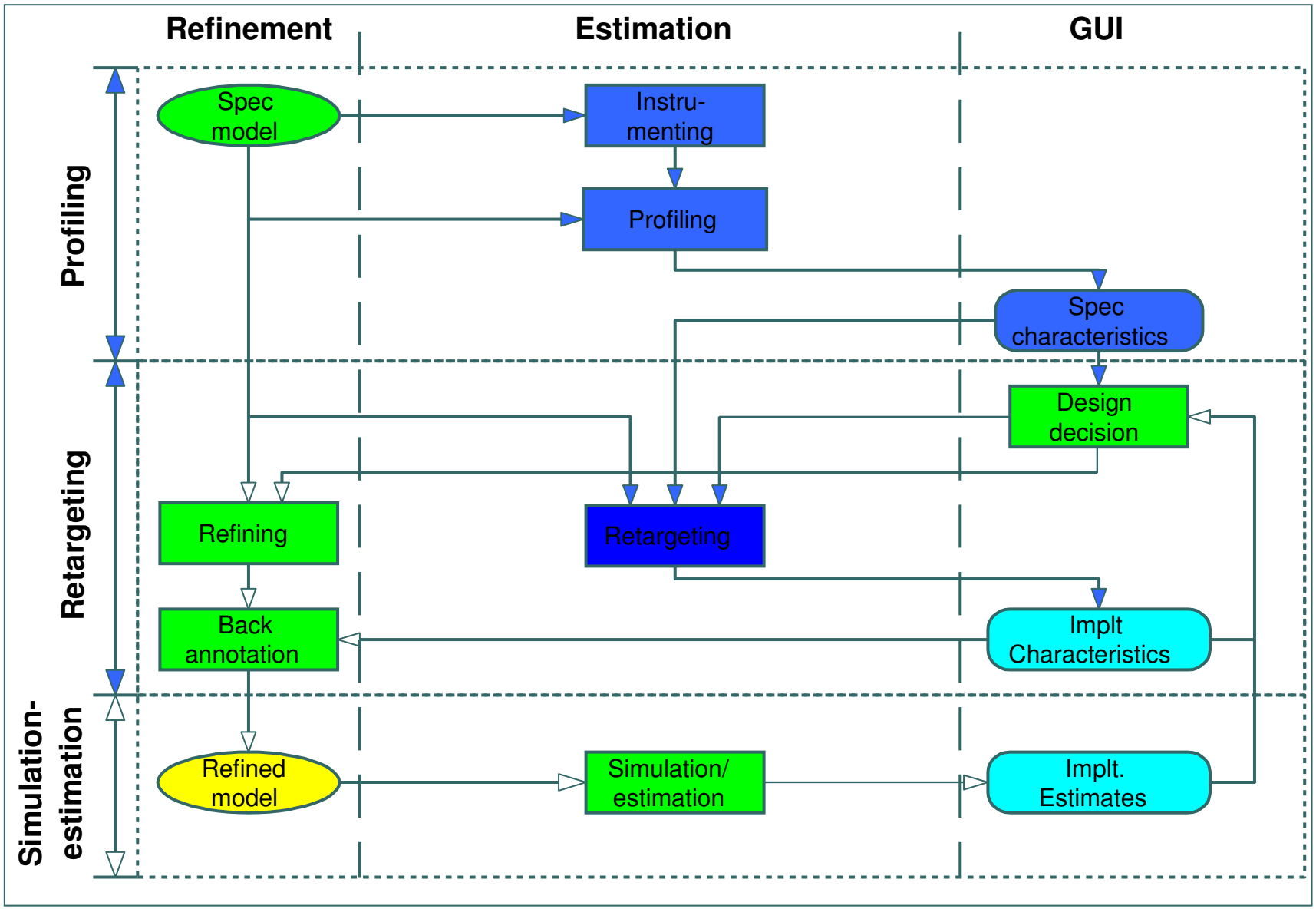
Design Flow


Refinement
Estimation
GUI
Profiling
Spec model
Simulation
Profiling
Spec characteristics

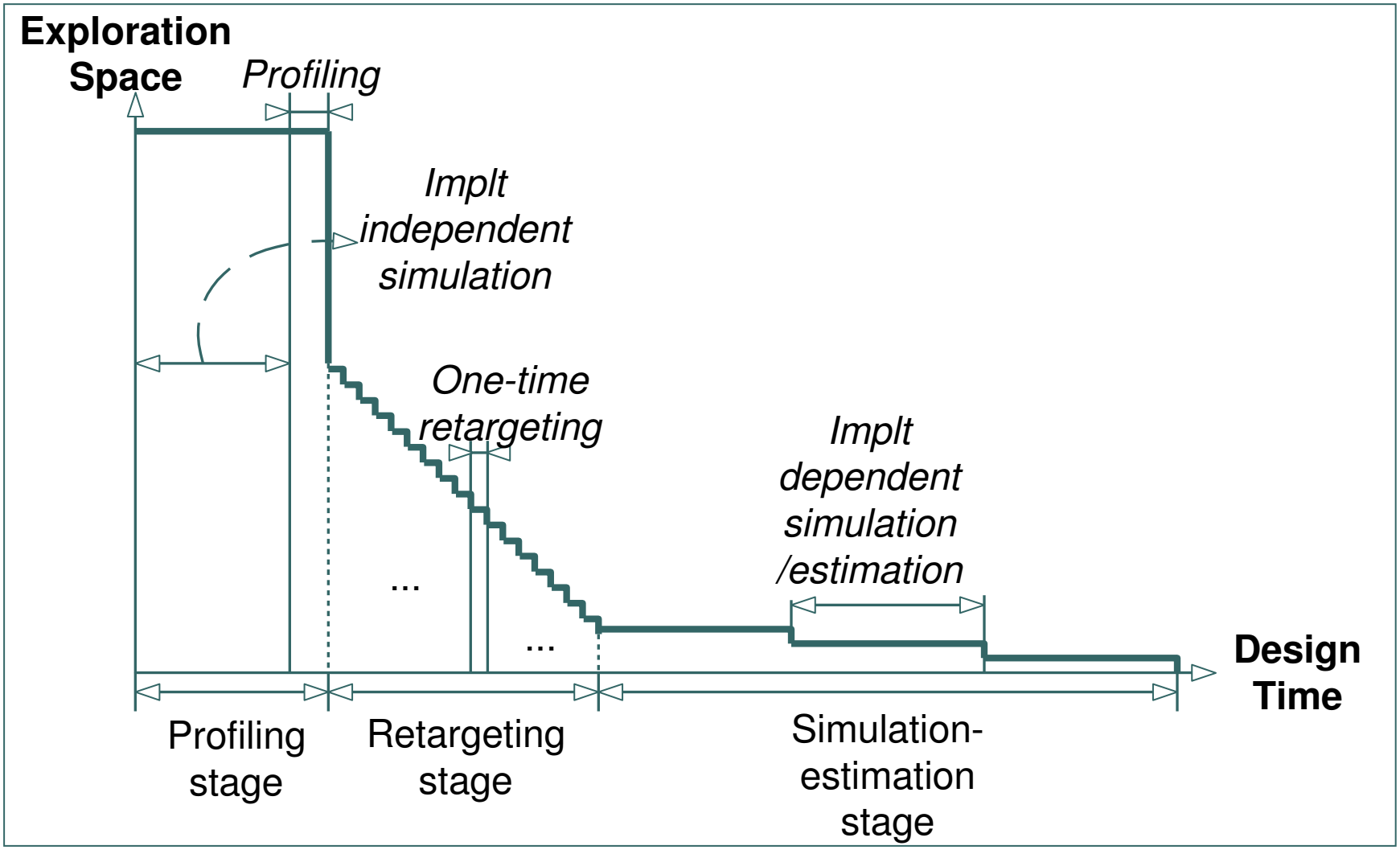
Design Flow (cont.)



Design Flow (cont.)



Explore and Trim



Profiling

- Instrumentation-based profiling
  - B_b: The execution counts of basic block b
  - $C_{b,i,d}$: No. of computed characteristics for item type i and data type d in the block b
  - Data type i: float, int, ..
  - Item type d: metric dependant

```
int b,c;
if( a = 0){
   b++;
}
else{
   b++;
   c++;
}
```

$B_1 = 1$, $C_{1,++,int} = 1$

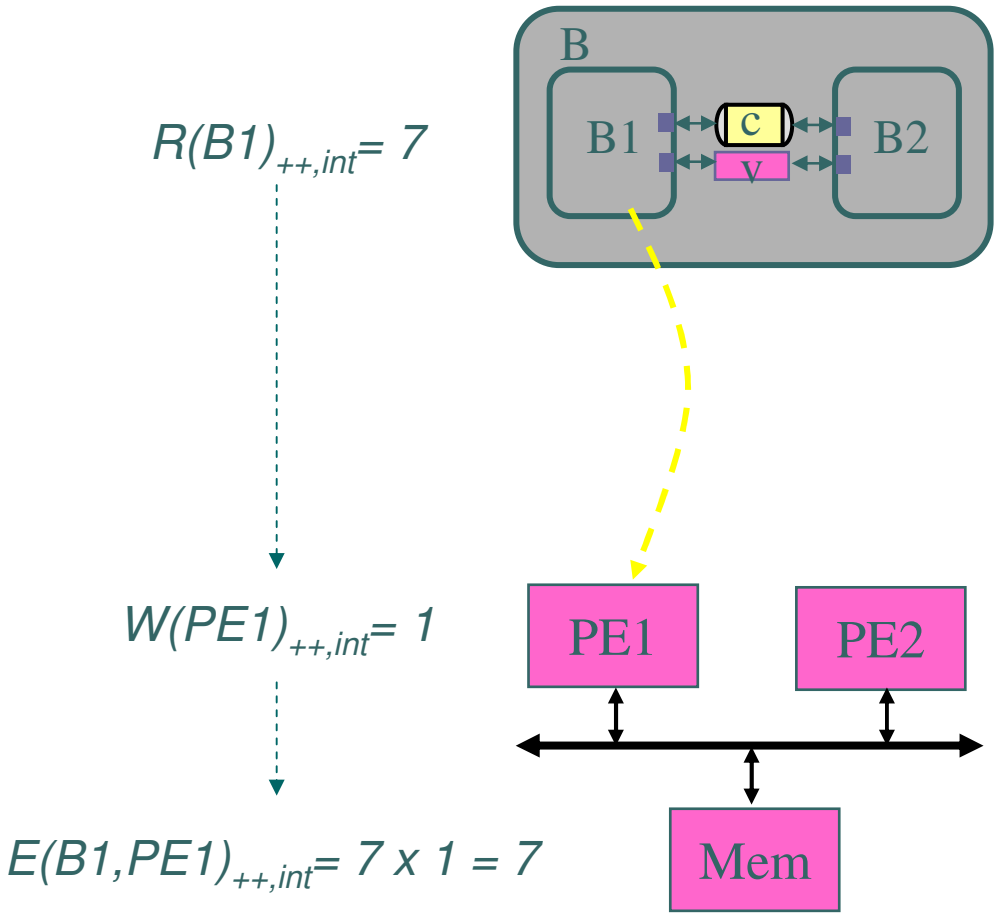
$B_3 = 3$, $C_{3,++,int} = 2$

- $R_{i,d} = \Sigma_b C_{b,i,d} B_b$
- $R = \Sigma_i \Sigma_d R_{i,d}$

$$R_{++,int} = \Sigma_i [B_i * C_{i,++,int}]$$
$$= 1 \times 1 + 3 \times 2$$
$$= 7$$

Retargeting

- Impl. characteristics
  - $R_{i,d}$: Spec. characteristics
  - $W_{i,d}$: weights of components which the entity mapped to
    - Manual
    - Simulation
  - $E = \Sigma_i \Sigma_d (R_{i,d} \; X \; W_{i,d})$
  - Time complexity: O(n)

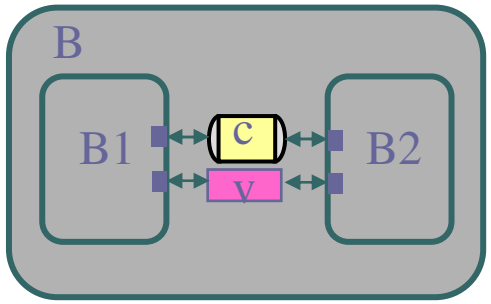


Challenges

- Separating dynamic and static analysis

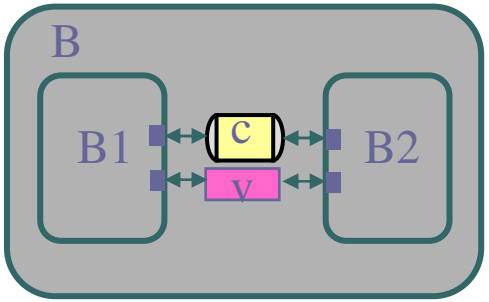
Challenges (cont.)

- Separating dynamic and static analysis
- Supporting complex models
  - Hierarchy
  - Recursion



Challenges (cont.)

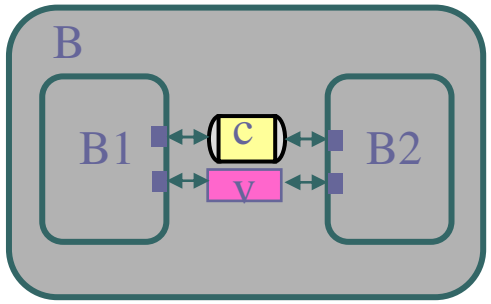
- Separating dynamic and static analysis
- Supporting complex models
  - Hierarchy
  - Recursion
- Multi-dimensional analysis

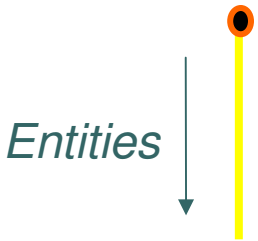


Traditional approach

Challenges (cont.)

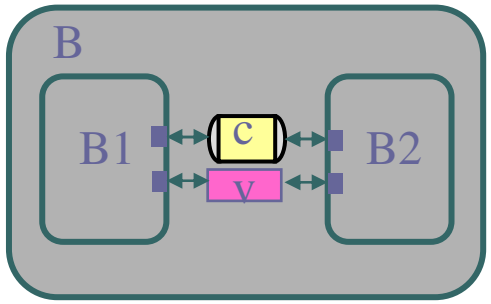
- Separating dynamic and static analysis
- Supporting complex models
  - Hierarchy
  - Recursion
- Multi-dimensional analysis
  - Multi-entities
    - Behavior, channel, port, variable

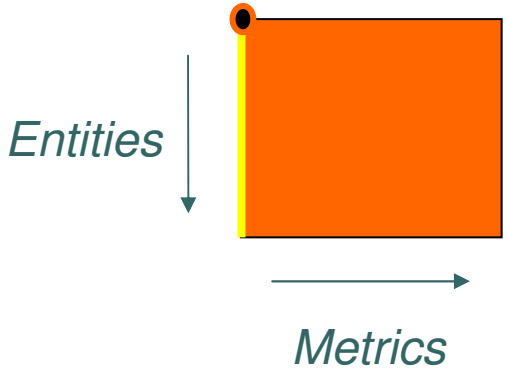




Challenges (cont.)

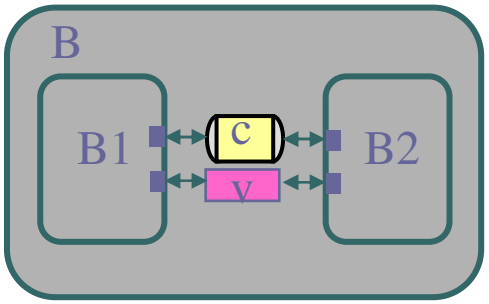
- Separating dynamic and static analysis
- Supporting complex models
  - Hierarchy
  - Recursion
- Multi-dimensional analysis
  - Multi-entities
    - Behavior, channel, port, variable
  - Multi-metrics
    - Operation, traffic, storage
    - Static, dynamic

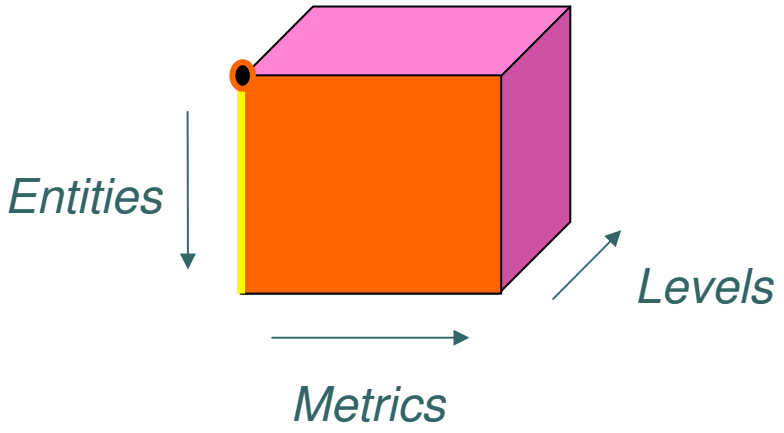




Challenges (cont.)

- Separating dynamic and static analysis
- Supporting complex models
  - Hierarchy
  - Recursion
- Multi-dimensional analysis
  - Multi-entities
    - Behavior, channel, port, variable
  - Multi-metrics
    - Operation, traffic, storage
    - Static, dynamic
  - Multi-levels
    - Application, transaction, bus-functional





Operation Metrics

- Entities: behavior
- Item types
  - 84 basic types: '+'.., '='.., 'if'..
  - Special operation types: global function
- Specification characteristics

	Static	Dynamic
Def.	No. of operations in spec	No. of executed Oper. during simulation
Rep.	Code complexity	Computational complexity

- Mapping: behavior → PE
- Implementation characteristics

	Static	Dynamic
Rep.	Code Size: Program memory size(SW) Custom hardware controller(HW)	No. of executed clock cycles: Execution time; power consumption

Traffic Metrics

- Entities: port, variable, channel, behavior
- Item types: in, out
- Specification characteristics

	Static	Dynamic
Def.	No. of connected ports	No. of P/V/C accessed during simulation
Rep.	Connectivity complexity.	Access complexity.

- Mapping:
  - Port → PE
  - Variable/channel → bus
- Implementation characteristics

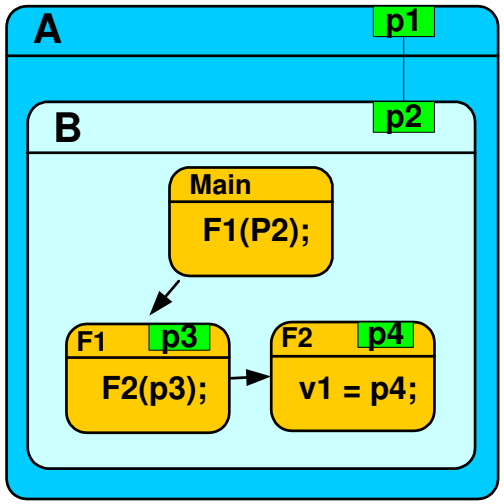
Bus	Communication delay
PE	Data preparation time

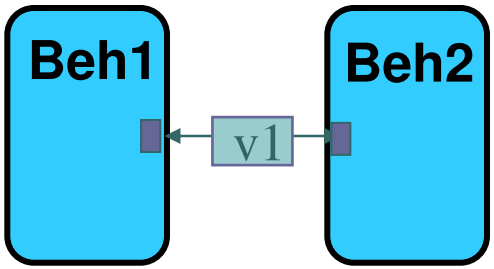
Static	Sequential behaviors
Dyn.	Parallel behaviors

Application level	Traffic between behaviors.
Bus functional level	Fan-in/fan-out, bus capacity, traffic over pin

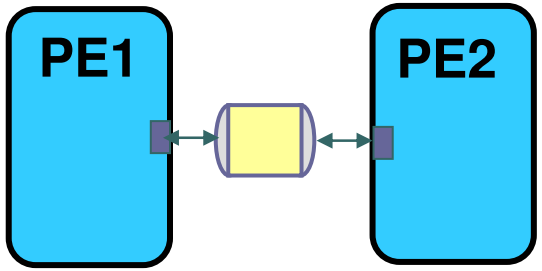
Deriving Traffic Metrics

- Profiling for the hierarchically instantiated behaviors and recursively called functions
  - A.p1 ➔ B.p2 ➔ B.F1.p3 ➔ B.F2.P4
- Different abstraction levels

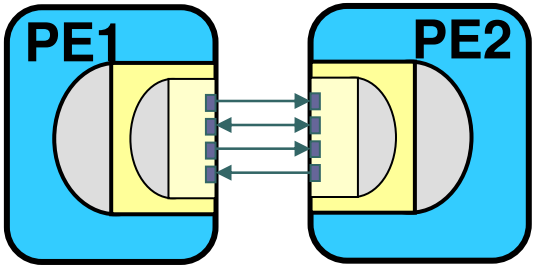




- Beh.port → Var



- Beh.port → Chan
- Chan in Chan



- Beh.port → Pin
- Chan.port ←→ Chan

Storage Metrics

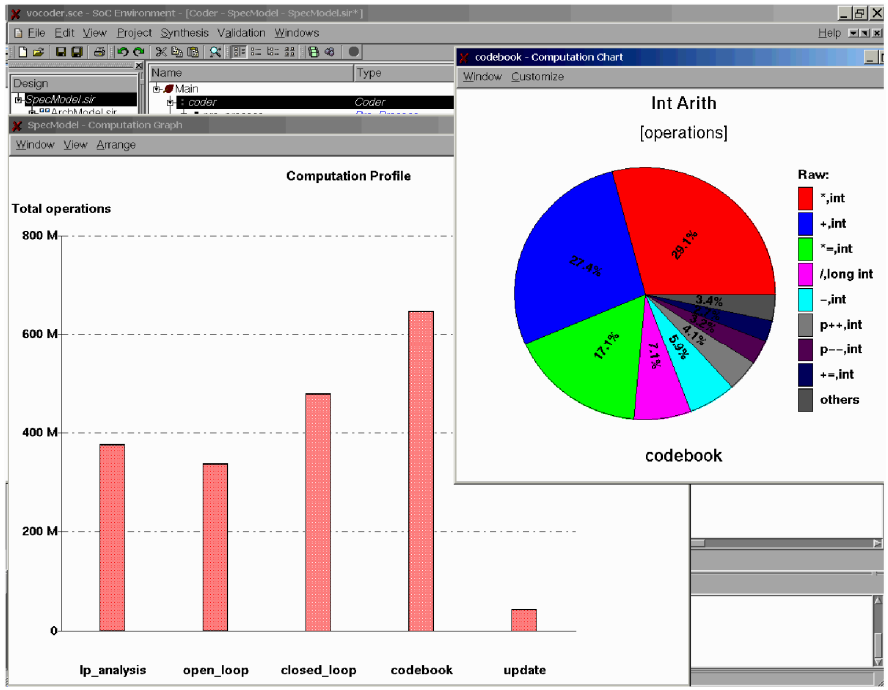
- Entity: variable, behavior
- Item types: local, global
- Specification characteristics

	Static	Dynamic
Def.	No. of static variables	No. of dynamic allocated memory
Rep.	Static memory requirement	Stack requirement (local) Heap requirement (global)

- Mapping:
  - Variable ➔ local/global memory
- Implementation characteristics

	Static	Dynamic
Rep.	Static memory size	Stack/heap size

Exp. Result: Vocoder Profiling



Floating –point not required

Dedicated hardware multipliers

HW acceleration

Table 1: Computational complexity of top-level Vocoder behaviors

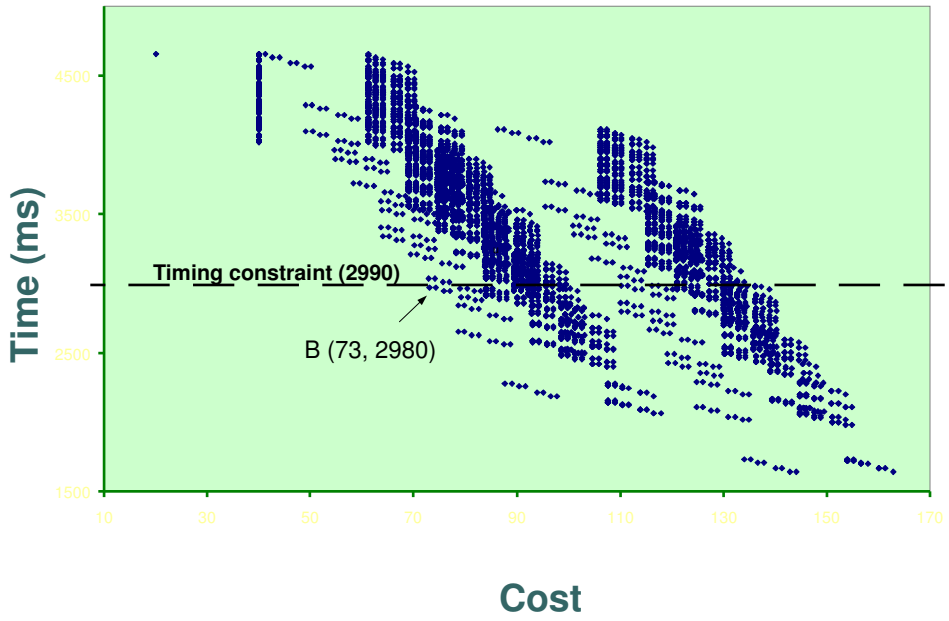
LP_Analysis	Open_Loop	Closed_Loop	Codebook	Update
377.0 MOp	337.1MOp	478.7 Mop	646.4 Mop	43.6 Mop

Table 2: Codebook operation mix

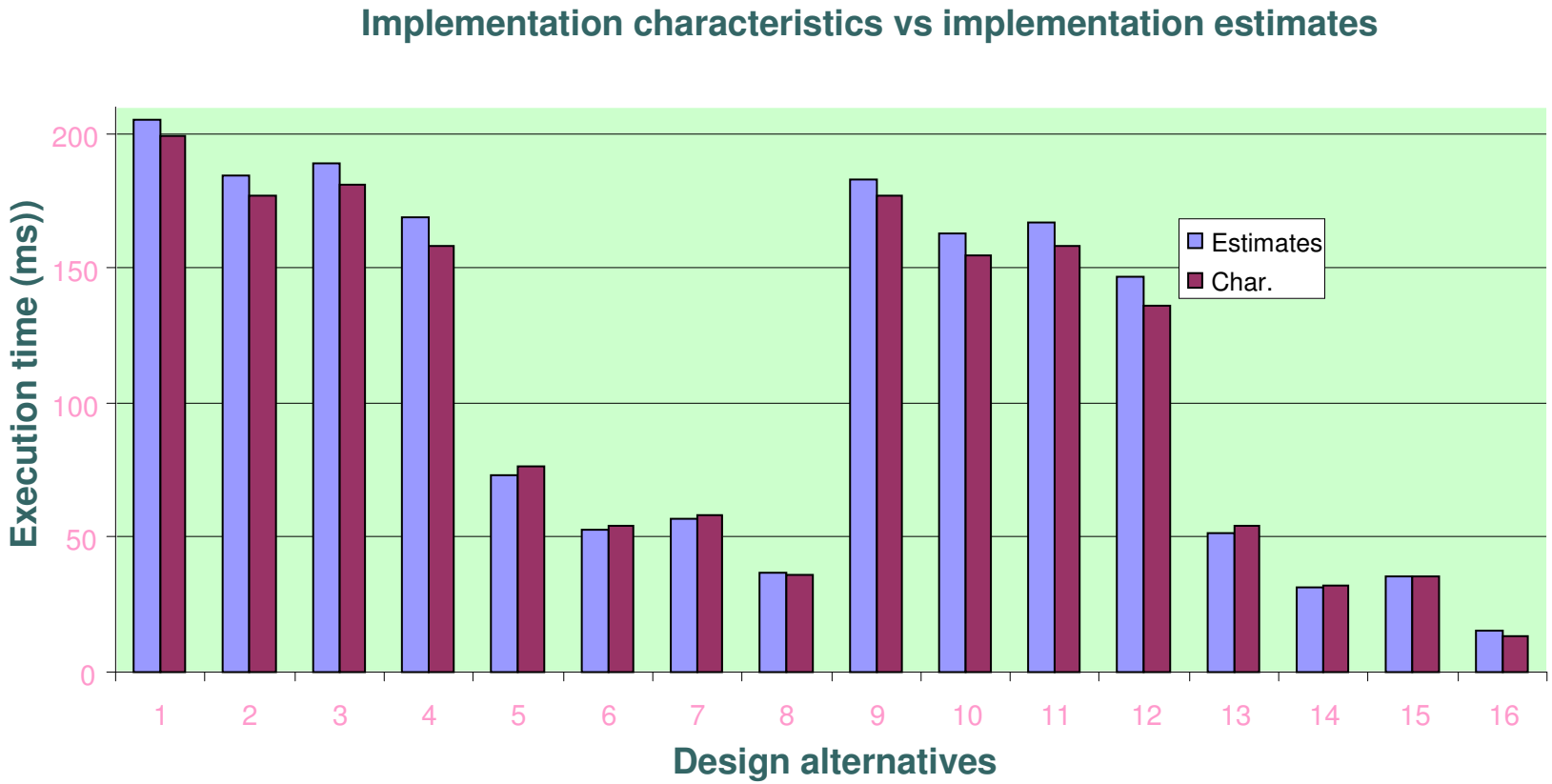
(x, int)	(+, int)	(-, int)	(/,int)	(others,int)
46.2%	33.5%	9.1%	7.1%	4.1%

Exp. Result: Vocoder Profiling (cont.)

- 8 behaviors ➔ 3 PEs
- Total 3^8 =6561 design alternatives
- Evaluation time: 3:15 hour
  - 1 simulation (2.23s)
  - 1 profiling (8.41s)
  - 6561 retargeting (0.8s)
  - 6561mapping (0.97s)



Exp. Result: JPEG Encoder



- Map 4 behaviors ➔ 2 PEs: 2^4 design alternatives
- Accuracy: 12.5%, fidelity = 100%

Conclusion

- Dynamic profiling + static retargeting
  - Profiling: helps completely comprehend the specification
  - Retargeting: ultra-fast (linear time), enables initial, exhaustive exploration of design space.
- Multi-dimensional analysis
  - Multi-entities
    - Behavior, channel, variable, port
  - Multi-abstraction levels
    - Application level, transaction level, bus-functional level
  - Multi-metrics
    - Operation, traffic, storage
    - Static, dynamic