Stretch®

S5530

Data Sheet

Version 1.2

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Changes from Previous Release

Release	Chapter	Change
1.2	Chapter 3, “Electrical Characteristics”	Updated V_{OH}, V_{OL} conditions

5530 at a Glance

This document highlights the features and peripheral devices that constitute the S5530 processor. For full details on each peripheral device refer to the *S5000 Peripheral Reference*. Figure 1 on the following page is a block diagram of the S5530 processor.

Processor Features

- 300 MHz, 32-bit Xtensa® core processor
  - 16- and 24-bit instructions
  - MMU with TLB
  - Single-precision floating point operations
- Instruction Set Extension Fabric (ISEF)
  - 32 x 128-bit wide register file
  - Aligned load and store
    - 8, 16, 32, 64, and 128 bit
  - Unaligned load and store
    - Up to 16 bytes variable byte streaming I/O
    - Up to 32 bits variable bit streaming I/O
  - User-defined extensions to the Xtensa ISA
    - Defined in C/C++
    - Fully pipelined and interlocked
- Support for various operating systems

Memory

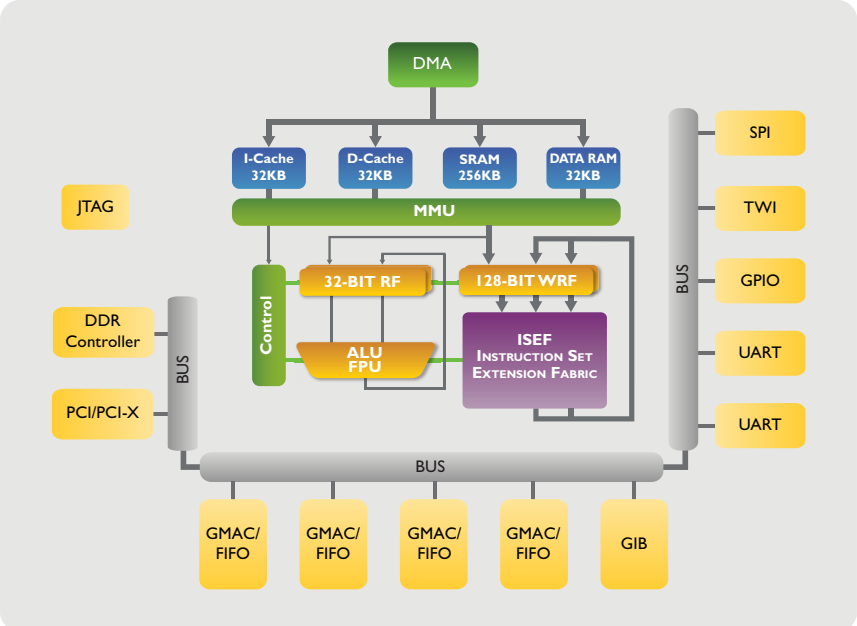
- 256 KBytes on-chip single-port SRAM
- 32 KBytes instruction cache
- 32 KBytes data cache
- 32 KBytes dual port data SRAM
- Up to 2 GBytes external DDR SDRAM (no ECC)
- DMA controller

Peripherals

- One PCI/PCI-X port
- Up to four 10/100/1000 Media Access Controllers with bypass to FIFO
- One Serial Peripheral Interface (SPI)
- One Generic Interface Bus (GIB)

- One two-wire interface (TWI)
- Eight General Purpose I/O and interrupt pins (GPIO)
- Two UARTs with IrDA support
- One Standard test port supporting JTAG IEEE 1149.1
- One 64-bit DDR400 SDRAM port

Figure 1 S5530 Block Diagram



Chapter 1 S5530 Features

Stretch's S5530 software-configurable processors combine the best of two previously divergent semiconductor worlds—the ease of software development associated with general-purpose processors (GPPs) and DSPs, with the parallelism and flexibility of FPGAs. Stretch achieves this by embedding programmable logic entirely inside the processor architecture.

The S5530 processor chip is powered by the Stretch® S5 Engine, which incorporates the widely accepted Tensilica® Xtensa® RISC processor core and the powerful Stretch Instruction Set Extension Fabric (ISEF). The ISEF is a software-configurable data path based on proprietary programmable logic. Using the ISEF, system designers extend the processor instruction set and define the new instructions using only their C/C++ code. As a result, developers get the performance of logic with C/C++ development simplicity—achieving unprecedented performance, easy and rapid development, and significant cost savings.

By integrating a rich set of system and memory peripherals with Stretch's S5 Engine, the S5530 delivers significant cost–performance improvements to a wide range of applications, including:

- Networking
- Telecommunications
- Military
- Security
- Image processing

1.1 The S5530 Processor

At the heart of the S5 Engine are a fixed Tensilica Xtensa ISA and Stretch additions to that ISA that allow end-users to add application-specific instructions (Extension Instructions). Tensilica's Xtensa ISA is a RISC architecture designed for embedded applications with industry-leading code density and many modern RISC architectural features. Stretch additions provide a frame-

work within which Extension Instructions can be specified and implemented to provide significant processing power without requiring the programmer to write in assembly language.

1.1.1 Xtensa ISA

The Xtensa Instruction Set Architecture is a modern RISC ISA targeted at embedded applications. It offers industry-leading code density, and enables high performance and low-power. The Xtensa ISA consists of a rich set of 16- and 24-bit instructions.

Programmers are spared the need to know the details of the Xtensa core architecture, however, because compute-intensive code is optimized using Extension Instructions specified in the C programming language, not in assembly language—a modest familiarity with the Xtensa ISA is all that is really needed.

1.1.2 Stretch Additions

Stretch additions comprise two major components:

- *Stretch load–store architecture*: This includes a 128-bit wide register file, and a fixed set of instructions supporting a variety of ways to move data efficiently between memory, the Xtensa core register file, and the wide register file.
- *Extension Unit*: This is a configurable unit for executing Extension Instructions.

Extension Instructions performing complex computations offer several advantages over existing technologies:

- Compared with fixed instruction set architectures, a single Extension Instruction can, in many cases, replace tens or hundreds of simple instructions.
- Compared with SIMD, VLIW, and Vector architectures, Extension Instructions can accommodate specialized application data sizes as well as specialized computations—providing flexibility previously only available to hardware designs.
- Compared with ASIC and FPGA designs, the Extension Instruction mechanism offers similar flexibility in defining computations without the need to write Verilog or to design complex control logic using finite-state machines. The complex computations are invoked as intrinsics in application software.
- Compared with other products that combine processors with field programmable logic, the S5 architecture enables a completely software-based development methodology using a common set of software development tools.

1.2 S5530 Peripherals

The S5530 contains a rich set of peripherals categorized as follows:

- Low-speed peripherals
  - Two UART with IrDA ports
  - One Serial Peripheral Interface (SPI)
  - One two-wire interface (TWI)
  - Eight General Purpose I/O and external interrupt pins (GPIO)
- Mid-speed peripherals
  - One parallel Generic Interface Bus (GIB) connecting to Flash, SRAM, and Intel- or Motorola-type devices
  - Four Programmable Parallel Ports
    - FIFO (up to four)
- High-speed peripherals
  - One 64-bit PCI/PCI-X port (32-bit capable)
  - One 64-bit DDR400 SDRAM port with optional 32-bit mode

1.2.1 UART Ports

The S5530 contains two UART ports that support full duplex, asynchronous, non-DMA transfer of serial data. Each UART supports the following features:

- Completely compatible with the 16550 standard
- Programmable auto flow control mode (for compatibility with the 16750 standard) (UART 0 only)
- 16-byte transmit and receive FIFO depths
- Continuous transmission with low CPU overhead
- IrDA 1.0 SIR (Serial Infrared) mode (115.2 KBaud)
- Fully programmable serial interface
- External 1.8423 MHz clock signal

1.2.2 Serial Peripheral Interface Port

The Serial Peripheral Interface (SPI) port lets you connect up to eight SPI-compatible slave devices to the S5530. The SPI port supports the following features:

- SPI master operations

- Communication with up to eight devices
- Full duplex synchronous serial data transfer
- Optimized for up to 128-bit transfers (supports longer transfers)
- MSB or LSB data transfer
- Receive and Transfer on rising or falling edge of serial clock (independently)

The SPI device uses three pins for transferring data: two data pins (spi_si, spi_so), and a clock pin (spi_sck). Eight SPI chip select output pins (spi_cs[7:0]#) lets the S5530 choose up to eight other SPI devices. Using these pins, the SPI port provides a full-duplex, synchronous, master-only serial interface.

1.2.3 TWI Interface

The TWI interface lets the S5530 communicate with I2C compatible devices. The TWI is a simple, bi-directional, two-wire, serial data, and serial clock bus for inter-IC control. The interface's features support:

- Both master and slave modes
- Multi-master configurations
- 7-bit addressing
- Both standard and fast modes

Each connected device is recognized by a unique address, and can operate as either a receiver-only device, or as a transmitter with the capability to both receive and send information. Transmitters or receivers can operate in either master or slave mode. The TWI can also be controlled by more than one device connected to it.

The TWI also supports both standard (up to 100 Kb per second) and fast (up to 400 Kb per second) data flow rates.

1.2.4 General Purpose I/O Lines

The GPIO supports eight general purpose input–output–interrupt lines.

Software can configure each bit of the GPIO to be either input or output. Each bit may also be controlled individually through addressing registers without affecting adjacent bits. When in input mode, the GPIO can be configured as an interrupt input.

GPIO interrupt capabilities include the ability to:

- Generate an interrupt on any input

- Program inputs independently for level sensitivity (positive or negative) or for edge sensitivity (positive, negative, or both)
- Mask each interrupt individually
- Read the state of an interrupt
- Clear an interrupt
- Generate up to four interrupt outputs from the internal interrupt controller to an external processor

1.2.5 Generic Interface Bus

The S5530 contains a Generic Interface Bus (GIB) designed to support a wide assortment of parallel slave devices. You specify the handshake signals and the timing by writing a short sequence of instructions (typically 3 or fewer), with each instruction specifying the control signals to be activated, and their duration.

The GIB supports the following features:

- Big or little endian devices
- Booting from 16-bit asynchronous Flash memory (28F128J3 or equivalent)
- Most asynchronous 8- or 16-bit Flash memory devices
- Most asynchronous 8- or 16-bit static RAM
- Adjustable timing and programmable handshaking for a wide range of devices
- An external ready signal
- Up to 256 Mbit Flash memories (32 MBytes)
- Support for 32-bit devices
- Support for devices that use multiplexed address–data bus

1.2.6 Programmable Parallel Ports

The four independent 8-bit parallel ports are each capable of supporting ethernet traffic or a simple FIFO mode.

- All ports support an IEEE 802.3 compliant GMII and MII interface for 10/100/1000Mbps operation (both full and half-duplex modes)
  - Ports 0 and 1 have deeper FIFOs and will therefore provide higher performance than ports 2 and 3 in some applications
- MDIO management interface
- Simple 8-bit FIFO mode for raw data on all ports
- Pairs of ports may be combined to produce a 16-bit FIFO mode for raw data

1.2.7 PCI-X Interface

The PCI-X core module provides access to the S5530 from any PCI or PCI-X bus initiator or target. It can also be configured as a host bridge. The PCI-X controller supports the following features:

- Compliance with PCI Bus Revision 2.3, and with PCI-X Addendum Revision 1.0a
- 32-or 64-bit PCI or PCI-X interface
- Synchronous 22.22–133 MHz PCI-X-to-application clock frequencies
- Support for
  - PCI-X Timing A Decode and PCI Medium Decode
  - Master Deferred (up to 2) and Target Delayed (up to 8) Read transactions
  - Master (up to 8) and Target (up to 16) Split Read-Write transactions
  - PCI Target Fast Back-to-Back Cycle
  - Memory word address for Control Register access
  - PCI-X Bus Message Signaled Interrupt
  - Various clock and data width configurations
- Application or Configuration Register-requested Target
  - Abort-Retry cycles, Deferred Read transactions, and Split Read–Write transactions
- PCI Target Burst size of up to 2 MBytes, aligned
- PCI-X Target Burst size of up to 256 KBytes
- PCI and PCI-X Master Burst size of up to 256 bytes per access
- Application Interface Configuration Register access port

1.2.8 DDR Controller

The S5530 DDR SDRAM controller interfaces to the various available SDRAM DDR400 and lower devices. It supports the following features:

- Fully pipelined command, read, and write data interface
- Advanced bank lookahead for high memory throughput
- Programmable register interface to control memory device parameters and protocols such as auto-precharge
- Built-in adjustable Delay Compensation Circuitry for reliable data transmit and receive timing
- Clock frequencies from 100 MHz to 200 MHz

1.2.9 JTAG

S5530 processor chips contain one JTAG test access port. This port is used as a portal into the chip for booting, on-chip debugging (OCD), testing, and boundary scanning functions.

1.2.9.1 On Chip Debugging

OCD allows access to the processor subsystem through the JTAG port. This permits a debug probe to be plugged into the JTAG port to single-step, modify memory and registers, and to provide hardware breakpoints and watchpoints.

Setting the debug pin determines whether JTAG or OCD mode is selected; when set to 0, JTAG is selected; when set to 1, OCD is selected. Refer to “GIB Bootstrapping Options” on page 3-11 for more information on bootstrapping options.

1.3 Clocks

The S5530 contains five phase locked loops (PLLs). PLL1 generates the DDR clock and, optionally, the PCI and Programmable Parallel port clocks. PLL2 generates the clocks for the core logic, including the processor. The remaining three PLLs are used for clock de-skew for the PCI DDR interfaces.

Clock pins are provided for PLL1 and PLL2, and for the various interfaces.

1.4 Reset

The S5530 contains numerous internal resets, mostly derived from one master reset supplied externally. All global resets are generated in a single reset block. All generated resets are synchronous to a specific block, depending on the reset destination.

The three modes recognized by the reset block are: power-on, hard reset, and soft reset.

- *Power-on Reset*: This mode is active while the chip is powering up, and is equivalent to a hard reset. Reset is released to the PLLs after power-up, based on board-level power-up reset circuitry.
- *Hard Reset*: This mode resets everything on the chip, and is a result of asserting the global reset.

- *Soft Reset*: This reset is initiated by a software action, PCI reset (when in PCI slave mode), or by a watchdog reset non-maskable interrupt. The processor, bus, all peripherals, and most of the system registers blocks are reset by a soft reset, except for the PLLs.

1.5 Interrupt Controller

Each I/O device on the S5530 can generate a set of interrupts to the Xtensa core. The interrupt controller allows each interrupt source to be mapped to any of the Xtensa core's 20 interrupt inputs. This permits flexible software-controlled mapping of interrupts into distinct priority groups.

A total of 20 interrupts, one of which is an NMI, are provided. Of these 20 interrupts, four can be output through the GPIO to an external processor. An additional interrupt output is provided to the PCI block to allow generation of a PCI interrupt.

The interrupt controller supports the following features:

- Interrupts can be enabled or disabled
- Any interrupt source (input) can activate any single interrupt output, including NMI, and each source controls its own cause and clear mechanism
- Any interrupt output can be activated by any number of interrupt inputs
- A status register shows which interrupt inputs are active *and* unmasked
- An aggregation register shows status based upon blocks of interrupts
- Synchronizers are present on all interrupt inputs
- Up to four external interrupts can originate through the GPIO
- The edge trigger programming for the external interrupts is done in the GPIO controller

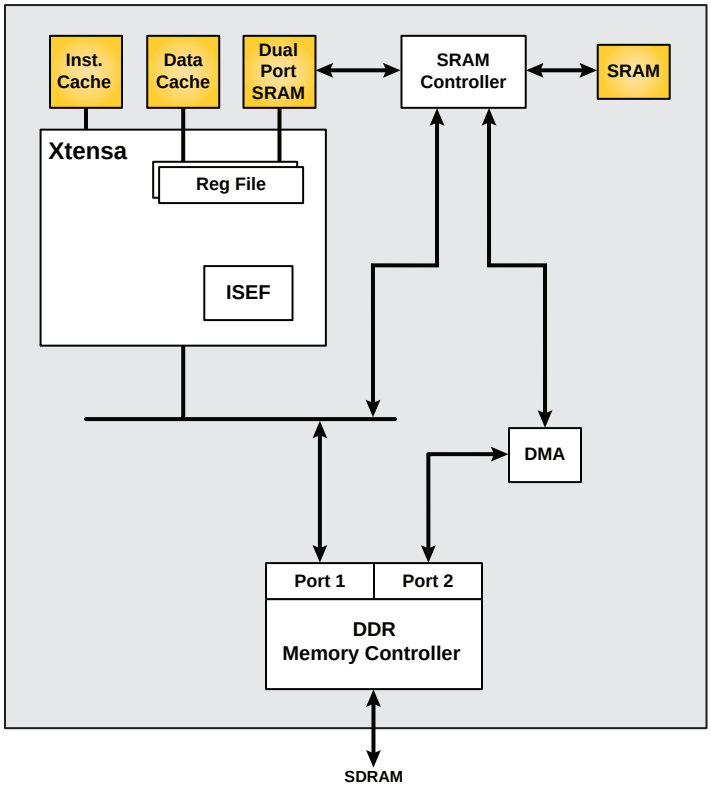
1.6 Memory Architecture

Stretch's memory architecture supports the following features:

- 32 KB instruction cache (4-way associative, with parity)
- 32 KB data cache (2-way associative, with parity)
- Support for write-back cache and write-through cache
- 32 KB dual-port local data memory, with parity

- 256 KB on-chip SRAM, with parity
- Up to 2 GB of 64-bit wide DDR400 (up to 1 GB of 32-bit)
- Operation from internal SRAM without DDR

Figure 1-1 5530 memory block diagram



1.7 DMA Controller

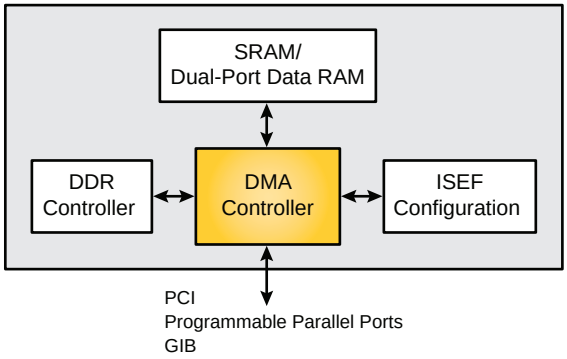
The DMA Controller (DMAC) provides four master interfaces for implementing DMA transfers between system memory (SRAM and DRAM) and various peripherals. A slave interface is also provided for configuring and monitoring DMA operations.

The DMA Controller supports 24 unidirectional DMA channels, where each channel has a programmable priority (0-3) and a dedicated peripheral interface. An internal transfer buffer and logic support both single- and dual-master transfers that utilize the full bus bandwidth. Per-channel scatter–gather operations are also supported.

Software overhead to manage network peripherals is minimized through the following features:

- A descriptor-based control scheme to queue, process, and monitor transfers.
- Pre- or post-fix operations per transfer that allow the DMAC to interact autonomously with peripherals without per-packet software intervention.
- Programmable interrupts.

Figure 1-2 DMA controller block diagram



Chapter 2 The S5530 Package

The S5530 package is a 27 mm x 27 mm Flip-Chip BGA with a heat spreader (HFCBGA). Table 2-1 lists signal-to-pin mappings as well as a short description for all signals except those for the Programmable Parallel Interface (PPI, refer to Section 2.1, “Programmable Port Interface”).

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
DDR	sdram_addr[0]	A13	O	Address to DDR memories
	sdram_addr[1]	E12	O	Address to DDR memories
	sdram_addr[2]	B11	O	Address to DDR memories
	sdram_addr[3]	A11	O	Address to DDR memories
	sdram_addr[4]	F11	O	Address to DDR memories
	sdram_addr[5]	E9	O	Address to DDR memories
	sdram_addr[6]	A9	O	Address to DDR memories
	sdram_addr[7]	B8	O	Address to DDR memories
	sdram_addr[8]	A8	O	Address to DDR memories
	sdram_addr[9]	A7	O	Address to DDR memories
	sdram_addr[10]	A14	O	Address to DDR memories
	sdram_addr[11]	E7	O	Address to DDR memories
	sdram_addr[12]	B6	O	Address to DDR memories
	sdram_addr[13]	B2	O	Address to DDR memories
	sdram_bank[0]	A17	O	Bank address to memory
	sdram_bank[1]	A15	O	Bank address to memory
	sdram_cas#	A19	O	Column address strobe
	sdram_ck[0]	A23	O	Clock to DDR memories
	sdram_ck[0]#	B23	O	Clock to DDR memories
	sdram_ck[1]	C13	O	Clock to DDR memories
	sdram_ck[1]#	B13	O	Clock to DDR memories, inverted
	sdram_ck[2]	B4	O	Clock to DDR memories, inverted
	sdram_ck[2]#	C4	O	Clock to DDR memories, inverted
	sdram_cke0	C5	O	Clock enable

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
DDR (cont.)	sdram_cke1	D6	O	Clock enable
	sdram_clk_fb	F22	I	Feedback clock for the SDRAM PLL
	sdram_cs[0]#	B19	O	Chip select
	sdram_cs[1]#	C19	O	Chip select
	sdram_cs[2]#	D19	O	Chip select
	sdram_cs[3]#	E19	O	Chip select
	sdram_dm[0]	B1	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[1]	A4	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[2]	C7	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[3]	A10	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[4]	D16	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[5]	B20	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[6]	C22	O	Data mask. When active, inhibits writing the selected byte
	sdram_dm[7]	B25	O	Data mask. When active, inhibits writing the selected byte
	sdram_dq[0]	D2	I/O	Data. Output during writes; input during reads
	sdram_dq[1]	C1	I/O	Data. Output during writes; input during reads
	sdram_dq[2]	E4	I/O	Data. Output during writes; input during reads
	sdram_dq[3]	E5	I/O	Data. Output during writes; input during reads
	sdram_dq[4]	F4	I/O	Data. Output during writes; input during reads
	sdram_dq[5]	E3	I/O	Data. Output during writes; input during reads
	sdram_dq[6]	F5	I/O	Data. Output during writes; input during reads
	sdram_dq[7]	D3	I/O	Data. Output during writes; input during reads
	sdram_dq[8]	D4	I/O	Data. Output during writes; input during reads
	sdram_dq[9]	A2	I/O	Data. Output during writes; input during reads
	sdram_dq[10]	A5	I/O	Data. Output during writes; input during reads
	sdram_dq[11]	E6	I/O	Data. Output during writes; input during reads
	sdram_dq[12]	F6	I/O	Data. Output during writes; input during reads
	sdram_dq[13]	A3	I/O	Data. Output during writes; input during reads
	sdram_dq[14]	D5	I/O	Data. Output during writes; input during reads
	sdram_dq[15]	B5	I/O	Data. Output during writes; input during reads
	sdram_dq[16]	A6	I/O	Data. Output during writes; input during reads
	sdram_dq[17]	D7	I/O	Data. Output during writes; input during reads
	sdram_dq[18]	F8	I/O	Data. Output during writes; input during reads
	sdram_dq[19]	E8	I/O	Data. Output during writes; input during reads

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
DDR (cont.)	sdram_dq[20]	C6	I/O	Data. Output during writes; input during reads
	sdram_dq[21]	B7	I/O	Data. Output during writes; input during reads
	sdram_dq[22]	C8	I/O	Data. Output during writes; input during reads
	sdram_dq[23]	D8	I/O	Data. Output during writes; input during reads
	sdram_dq[24]	B9	I/O	Data. Output during writes; input during reads
	sdram_dq[25]	E10	I/O	Data. Output during writes; input during reads
	sdram_dq[26]	C11	I/O	Data. Output during writes; input during reads
	sdram_dq[27]	E11	I/O	Data. Output during writes; input during reads
	sdram_dq[28]	C9	I/O	Data. Output during writes; input during reads
	sdram_dq[29]	B10	I/O	Data. Output during writes; input during reads
	sdram_dq[30]	D11	I/O	Data. Output during writes; input during reads
	sdram_dq[31]	D12	I/O	Data. Output during writes; input during reads
	sdram_dq[32]	C15	I/O	Data. Output during writes; input during reads
	sdram_dq[33]	E15	I/O	Data. Output during writes; input during reads
	sdram_dq[34]	C16	I/O	Data. Output during writes; input during reads
	sdram_dq[35]	D17	I/O	Data. Output during writes; input during reads
	sdram_dq[36]	D15	I/O	Data. Output during writes; input during reads
	sdram_dq[37]	A16	I/O	Data. Output during writes; input during reads
	sdram_dq[38]	E16	I/O	Data. Output during writes; input during reads
	sdram_dq[39]	B17	I/O	Data. Output during writes; input during reads
	sdram_dq[40]	E17	I/O	Data. Output during writes; input during reads
	sdram_dq[41]	E18	I/O	Data. Output during writes; input during reads
	sdram_dq[42]	C20	I/O	Data. Output during writes; input during reads
	sdram_dq[43]	D20	I/O	Data. Output during writes; input during reads
	sdram_dq[44]	A18	I/O	Data. Output during writes; input during reads
	sdram_dq[45]	C18	I/O	Data. Output during writes; input during reads
	sdram_dq[46]	E20	I/O	Data. Output during writes; input during reads
	sdram_dq[47]	A21	I/O	Data. Output during writes; input during reads
	sdram_dq[48]	D21	I/O	Data. Output during writes; input during reads
	sdram_dq[49]	B21	I/O	Data. Output during writes; input during reads
	sdram_dq[50]	D22	I/O	Data. Output during writes; input during reads
	sdram_dq[51]	B24	I/O	Data. Output during writes; input during reads
	sdram_dq[52]	C21	I/O	Data. Output during writes; input during reads
	sdram_dq[53]	B22	I/O	Data. Output during writes; input during reads

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
DDR (cont.)	sdram_dq[54]	A24	I/O	Data. Output during writes; input during reads
	sdram_dq[55]	C23	I/O	Data. Output during writes; input during reads
	sdram_dq[56]	D23	I/O	Data. Output during writes; input during reads
	sdram_dq[57]	E22	I/O	Data. Output during writes; input during reads
	sdram_dq[58]	D25	I/O	Data. Output during writes; input during reads
	sdram_dq[59]	E23	I/O	Data. Output during writes; input during reads
	sdram_dq[60]	F20	I/O	Data. Output during writes; input during reads
	sdram_dq[61]	A25	I/O	Data. Output during writes; input during reads
	sdram_dq[62]	B26	I/O	Data. Output during writes; input during reads
	sdram_dq[63]	C26	I/O	Data. Output during writes; input during reads
	sdram_dqs[0]	C2	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[1]	B3	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[2]	F7	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[3]	D10	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[4]	B16	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[5]	A20	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[6]	E21	I/O	Data strobe. Output during writes; input during reads
	sdram_dqs[7]	C25	I/O	Data strobe. Output during writes; input during reads
	sdram_ras#	B18	O	Row address strobe
	sdram_sel_ddr32	D24	I	Selects memory width. Set high it selects 32-bit. Set low it selects 64-bit.
	sdram_we#	D18	O	Write enable
	sstl_ref1	A22	I	Reference voltage for the SDRAM interface
	sstl_ref2	D9	I	Reference voltage for the SDRAM interface
GIB	gib[0]	AC10	I/O	General purpose address and data
	gib[1]	AB10	I/O	General purpose address and data
	gib[2]	AA10	I/O	General purpose address and data
	gib[3]	AA7	I/O	General purpose address and data
	gib[4]	AA6	I/O	General purpose address and data
	gib[5]	AF11	I/O	General purpose address and data
	gib[6]	Y6	I/O	General purpose address and data
	gib[7]	AA8	I/O	General purpose address and data
	gib[8]	AE11	I/O	General purpose address and data
	gib[9]	AC11	I/O	General purpose address and data

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
GIB (cont.)	gib[10]	AB9	I/O	General purpose address and data
	gib[11]	AA9	I/O	General purpose address and data
	gib[12]	AD11	I/O	General purpose address and data
	gib[13]	AC9	I/O	General purpose address and data
	gib[14]	AB8	I/O	General purpose address and data
	gib[15]	AB11	I/O	General purpose address and data
	gib[16]	AE12	I/O	General purpose address and data
	gib[17]	AC8	I/O	General purpose address and data
	gib[18]	AB7	I/O	General purpose address and data
	gib[19]	AF12	I/O	General purpose address and data
	gib[20]	AC12	I/O	General purpose address and data
	gib[21]	AE10	I/O	General purpose address and data
	gib[22]	AD9	I/O	General purpose address and data
	gib[23]	AD12	I/O	General purpose address and data
	gib[24]	AF13	I/O	General purpose address and data
	gib[25]	AF10	I/O	General purpose address and data
	gib[26]	W6	I/O	General purpose address and data
	gib[27]	AB12	I/O	General purpose address and data
	gib[28]	AD13	I/O	General purpose address and data
	gib[29]	AB6	I/O	General purpose address and data
	gib[30]	AE9	I/O	General purpose address and data
	gib[31]	AE13	I/O	General purpose address and data
	gib[32]	AD8	I/O	General purpose control or address out. During reset, this pin is hclk_sel[0] input, controlling pll2 operation. Refer to Section 3.6.10, "PLL and Clock Timing" and Table 3-26 for the relationship between this pin and the PLL operation.
	gib[33]	AC7	I/O	General purpose control or address out. During reset, this pin is hclk_sel[1] input, controlling pll2 operation. Refer to Section 3.6.10, "PLL and Clock Timing" and Table 3-26 for the relationship between this pin and the PLL operation.
	gib[34]	AC13	I/O	General purpose control or address out. During reset, this pin is hclk_sel[2] input, controlling pll2 operation. Refer to Section 3.6.10, "PLL and Clock Timing" and Table 3-26 for the relationship between this pin and the PLL operation.
	gib[35]	AA13	I/O	General purpose control or address out. During reset, this pin is pci_host_mode in.
	gib[36]	AE8	I/O	General purpose control or address out, or ready in

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
GIB (cont.)	gib[37]	AF9	I/O	General purpose control or address out. During reset, this is flash_enable#.
	gib[38]	AB13	O	General purpose control or address out
	gib[39]	AE14	O	General purpose control or address out
	gib[40]	V6	O	General purpose control out
	gib[41]	U7	O	General purpose control out
	gib_ce[0]#	AF14	O	Active low chip enables to external devices
	gib_ce[1]#	AC14	O	Active low chip enables to external devices
	gib_ce[2]#	AD7	O	Active low chip enables to external devices
	gib_ce[3]#	W5	O	Active low chip enables to external devices
GPIO	gpio[0]	AB16	I/O	General purpose I/O signals mapped to register space
	gpio[1]	AE25	I/O	General purpose I/O signals mapped to register space
	gpio[2]	AC23	I/O	General purpose I/O signals mapped to register space
	gpio[3]	AC16	I/O	General purpose I/O signals mapped to register space
	gpio[4]	AD16	I/O	General purpose I/O signals mapped to register space
	gpio[5]	AF25	I/O	General purpose I/O signals mapped to register space
	gpio[6]	AB22	I/O	General purpose I/O signals mapped to register space
	gpio[7]	AE16	I/O	General purpose I/O signals mapped to register space
JTAG	tck	AE18	I	JTAG (IEEE 1149.1) clock input
	tdi	AC21	I	JTAG (IEEE 1149.1) serial data in
	tdo	AE22	O	JTAG (IEEE 1149.1) serial data out
	tms	AB21	I	JTAG (IEEE 1149.1) tap mode select in
	trst#	AF22	I	JTAG (IEEE 1149.1) reset in
PCI	pci_ack64#	N26	I/O	Accept 64-bit transfer
	pci_ad[0]	N22	I/O	Address–data
	pci_ad[1]	N25	I/O	Address–data
	pci_ad[2]	N21	I/O	Address–data
	pci_ad[3]	P26	I/O	Address–data
	pci_ad[4]	P22	I/O	Address–data
	pci_ad[5]	P25	I/O	Address–data
	pci_ad[6]	P20	I/O	Address–data
	pci_ad[7]	P23	I/O	Address–data
	pci_ad[8]	R26	I/O	Address–data
	pci_ad[9]	R23	I/O	Address–data

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
PCI (cont.)	pci_ad[10]	R25	I/O	Address–data
	pci_ad[11]	R21	I/O	Address–data
	pci_ad[12]	R24	I/O	Address–data
	pci_ad[13]	R22	I/O	Address–data
	pci_ad[14]	T25	I/O	Address–data
	pci_ad[15]	T22	I/O	Address–data
	pci_ad[16]	V21	I/O	Address–data
	pci_ad[17]	V26	I/O	Address–data
	pci_ad[18]	V22	I/O	Address–data
	pci_ad[19]	V24	I/O	Address–data
	pci_ad[20]	V23	I/O	Address–data
	pci_ad[21]	W26	I/O	Address–data
	pci_ad[22]	W21	I/O	Address–data
	pci_ad[23]	W25	I/O	Address–data
	pci_ad[24]	W23	I/O	Address–data
	pci_ad[25]	Y25	I/O	Address–data
	pci_ad[26]	Y21	I/O	Address–data
	pci_ad[27]	Y26	I/O	Address–data
	pci_ad[28]	Y22	I/O	Address–data
	pci_ad[29]	Y24	I/O	Address–data
	pci_ad[30]	Y23	I/O	Address–data
	pci_ad[31]	AA25	I/O	Address–data
	pci_ad[32]	F24	I/O	Address–data
	pci_ad[33]	F26	I/O	Address–data
	pci_ad[34]	G24	I/O	Address–data
	pci_ad[35]	G22	I/O	Address–data
	pci_ad[36]	G25	I/O	Address–data
	pci_ad[37]	G23	I/O	Address–data
	pci_ad[38]	G26	I/O	Address–data
	pci_ad[39]	H26	I/O	Address–data
	pci_ad[40]	H24	I/O	Address–data
	pci_ad[41]	H25	I/O	Address–data
	pci_ad[42]	H23	I/O	Address–data
	pci_ad[43]	H22	I/O	Address–data

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
PCI (cont.)	pci_ad[44]	J23	I/O	Address–data
	pci_ad[45]	J25	I/O	Address–data
	pci_ad[46]	J22	I/O	Address–data
	pci_ad[47]	J26	I/O	Address–data
	pci_ad[48]	J24	I/O	Address–data
	pci_ad[49]	J21	I/O	Address–data
	pci_ad[50]	K23	I/O	Address–data
	pci_ad[51]	K20	I/O	Address–data
	pci_ad[52]	K25	I/O	Address–data
	pci_ad[53]	K21	I/O	Address–data
	pci_ad[54]	K26	I/O	Address–data
	pci_ad[55]	K22	I/O	Address–data
	pci_ad[56]	L22	I/O	Address–data
	pci_ad[57]	L26	I/O	Address–data
	pci_ad[58]	L23	I/O	Address–data
	pci_ad[59]	L25	I/O	Address–data
	pci_ad[60]	L21	I/O	Address–data
	pci_ad[61]	L24	I/O	Address–data
	pci_ad[62]	M23	I/O	Address–data
	pci_ad[63]	M25	I/O	Address–data
	pci_cbe[0]#	P24	I/O	Command and byte enable
	pci_cbe[1]#	T23	I/O	Command and byte enable
	pci_cbe[2]#	V25	I/O	Command and byte enable
	pci_cbe[3]#	W24	I/O	Command and byte enable
	pci_clk	AA24	I	PCI input clock
	pci_cbe[4]#	M26	I/O	Command and byte enables
	pci_cbe[5]#	M20	I/O	Command and byte enables
	pci_cbe[6]#	M24	I/O	Command and byte enables
	pci_cbe[7]#	N24	I/O	Command and byte enables
	pci_clk_out	AB26	O	PCI output clock
	pci_devsel#	U25	I/O	Device select
	pci_frame#	U21	I/O	Frame number request
	pci_gnt#	AA21	I	Bus grant
	pci_idsel	W22	I	IDSEL signal

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
PCI (cont.)	pci_inta#	AB24	I/O	Interrupt A. Used to request an interrupt
	pci_intb#	AB25	I	Interrupt B. Used to request an interrupt in a multi-function device
	pci_intc#	AC26	I	Interrupt C. Used to request an interrupt in a multi-function device
	pci_intd#	AA22	I	Interrupt D. Used to request an interrupt in a multi-function device
	pci_irdy#	U23	I/O	Initiator ready
	pci_m66en	T26	I	Enable 66MHz. Indicates whether the bus segment is operating at 66MHz or 33MHz
	pci_par	T21	I/O	Parity
	pci_par64	M22	I/O	Parity on pci_ad[63:32]
	pci_pcix_133#	H21	I	Enable 133 MHz
	pci_pcix_mode#	F25	I	Indicates PCI-X mode
	pci_perr#	U26	I/O	Parity error
	pci_req#	AA26	O	Bus request
	pci_req64#	N23	I/O	Request 64-bit transfer
	pci_rst#	AA23	I/O	PCI reset. This pin must be pulled down to Vss with a 4.7K resistor when the PCI is configured as host. When the device is configured for standalone, non-PCI mode, it should be driven to logic 0 by external logic or pull-down.
	pci_sel_pci32	F23	I	Indicates 32-bit-only mode. Upper 32 bits and associated signals are disabled.
	pci_serr#	T24	I/O	System error
	pci_stop#	U22	I/O	PCI stop
	pci_trdy#	U20	I/O	Target ready
PLL	pll_refclk	E24	I	Clock for PLL1. Used internally to generate the SDRAM clock
	pll2_refclk	E25	I	Clock for PLL2. Used internally to generate the HP (processor) and LP clocks
SPI	spi_cs[0]#	AC22	O	Chip select
	spi_cs[1]#	AE17	O	Chip select
	spi_cs[2]#	AC17	O	Chip select
	spi_cs[3]#	AE23	O	Chip select
	spi_cs[4]#	AF23	O	Chip select
	spi_cs[5]#	AB17	O	Chip select
	spi_cs[6]#	AA17	O	Chip select
	spi_cs[7]#	AD22	O	Chip select
	spi_sck	AD23	O	SPI clock
	spi_si	AF16	I	Serial data in

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
SPI (cont.)	spi_so	AF17	O	Serial data out
TWI	twi_clk	AE24	I/O	TWI interface clock
	twi_data	AF24	I/O	Serial data
UART	uart_sclk	AC25	I	UART clock
	uart0_cts#	AF15	I	UART 0 clear to send
	uart0_dcd#	AD25	I	UART 0 data carrier detect
	uart0_dsr#	AC24	I	UART 0 data set ready
	uart0_dtr#	AB23	O	UART 0 data terminal ready.
	uart0_ri#	AE15	I	UART 0 ring indicator
	uart0_rts#	AE26	O	UART 0 request to send
	uart0_sin	AD15	I	UART 0 serial data in or infrared data in
	uart0_sout	AC15	O	UART 0 serial data out or active low infrared data out.
	uart1_sin	AD26	I	UART 1 serial data in or active low infrared data in
	uart1_sout	AB15	O	UART 1 serial data out or active low infrared data out
Misc. Signals	debug	AF18	I	Processor debug mode select. This signal has an internal pull-down resistor of nominally 10K ohms. This pin toggles the JTAG interface to OCD mode for on-chip debugging. If this feature is not being used, this pin can be left unconnected.
	lp_bpc	E26	I	For Stretch in-house testing only. Connect to GND in functional mode.
	pll_bypass	D26	I	For Stretch in-house testing only. Connect to GND in functional mode.
	pull-down	Each pull-down must be independently connected by a 4.7k resistor to Vss. A12, AB14, AC18, AD14, B12, B14, B15, C12, C14, D13, D14, E13, E14		
	pullup_ddr	Each pullup_ddr must be independently connected by a 4.7k resistor to Vdd_ddr AA16, Y14		
	reset#	AF21	I	Full chip reset. This is an asynchronous input
	se	AD18	I	For Stretch in-house testing only. This signal has an internal pull-down resistor of nominally 10K ohms. If this feature is not being used, this pin can be left unconnected.
	sm	AD21	I	For Stretch in-house testing only. This signal has an internal pull-down resistor of nominally 10K ohms. If this feature is not being used, this pin can be left unconnected.
IMPORTANT! *Every* power and ground ball listed in the following sections *must* be connected to its appropriate power or ground.				
Power/Gnd	AVdd			Quiet power for the PLL logic G19, G20, H20, J20

Table 2-1 S5530 Signal Description (alphabetic within ports)

Port	Signal Name	Pin #	Type	Description
	Vdd_core			Power for the core logic L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N11, N12, N15, N16, P11, P12, P15, P16, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V15
	Vdd_ddr			Power for the DDR interface G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, W14, W15
	Vdd_io			Power for the Programmable Parallel Port and GIB interface J8, K8, L8, M8, N8, P8, R8, T8, U8, V8, W8, W9, W10, W11, W12, W13, Y11, Y12, Y13
	Vdd_io2			Power for the SPI, TWI, UART, GPIO, JTAG, reset, and test pins W16, W17, W18, Y16, Y17, Y19
	Vdd_pci			Power for the PCI interface J19, K19, L19, M19, N19, P19, R19, T19, U19, V19, W19
	Vdd_pll			Power for the PLL interface pins (lp_bpc, pll2_refclk, pll_refclk, pll_bypass) G18, H18
	Vss			Ground AA11, AA12, AA14, AA15, AA18, AA19, AA20, AB18, AB19, AB20, AC19, AC20, AD3, AD5, AD10, AD17, AD19, AD20, AD24, AE7, AE19, AE20, AE21, AF19, AF20, C3, C10, C17, C24, D1, F9, F10, F12, F13, F14, F15, F16, F17, F18, F19, F21, G6, G7, G21, H7, H19, J7, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, K3, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K24, L7, L9, L10, L17, L18, L20, M7, M9, M10, M17, M18, M21, N6, N9, N10, N13, N14, N17, N18, N20, P4, P7, P9, P10, P13, P14, P17, P18, P21, R7, R9, R10, R17, R18, R20, T4, T7, T9, T10, T17, T18, T20, U3, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U24, V7, V9, V10, V11, V12, V13, V14, V16, V17, V18, V20, W20, W7, Y7, Y8, Y9, Y10, Y15, Y18, Y20
Open Pins	n/a			Leave pin open; do not connect to anything. AB2, AB4, AB5, AC2

2.1 Programmable Port Interface

The Programmable Port Interface (PPI) consists of four independent ports that can function in several different modes and combinations. In addition, each port may be independently unused. Table 2-2 lists one of the possible function and port combinations available for use by designers. Eight-bit and 16-bit functions are used in MAC bypass mode, and GMI and MII functions are used in MAC mode. Following sections describe each port's ball and signal assignments for each mode.

Table 2-2 Example of possible port combinations

Port #	Solo Functions					Paired Function
0	8-bit	MII	GMII	8-bit	GMII	16-bit Port 0
1	8-bit	MII	GMII	GMII	8-bit	
2	8-bit	MII	GMII	8-bit	MII	16-bit Port 2
3	8-bit	MII	GMII	MII	8-bit	

Each port can operate independently in 8-bit, GMII, or MII modes. When Port 0 is paired with Port 1, it can operate in 16-bit mode (16-bit Port 0), and when Port 2 is paired with Port 3, it can operate in 16-bit mode. (16-bit Port 2). Unused pins are specified as *Vss, Pull-up*, or *Do not connect* in the Unused column, and should be connected or not based on that classification.

2.1.1 MAC Mode Signal Descriptions

The following sections describe the pin and signal assignments for each MAC mode by port.

2.1.1.1 Port 0 Pin and Signal Assignments

Table 2-3 lists Port 0 pin and signal assignments for each MAC mode.

Table 2-3 S5530 PPI Port 0 Signal Descriptions

Ball	Type	GMII	MII	Description	Unused
E2	O	mac_mdc	mac_mdc	Management data clock. See also IEEE 802.3 22.2.2.11.	Do not connect
E1	I/O	mac_mdio	mac_mdio	Management data input/output. See also IEEE 802.3 22.2.2.12.	Pull-up
J6	I	mac0_rx_clk	mac0_rx_clk	Receive clock. See also IEEE 802.3 22.2.2.2.	Vss
J4	I	mac0_rx_dv	mac0_rx_dv	Receive data valid. See also IEEE 802.3 22.2.2.6.	Vss
J3	I	mac0_rx_er	mac0_rx_er	Receive error. See also IEEE 802.3 22.2.2.8.	Vss
J2	I	mac0_col	mac0_col	Collision detect. See also IEEE 802.3 22.2.2.10	Vss
J1	O	Do not connect	Do not connect	Do not connect	Do not connect
K1	I	mac0_rxd[0]	mac0_rxd[0]	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
K2	I	mac0_rxd[1]	mac0_rxd[1]	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
J5	I	mac0_rxd[2]	mac0_rxd[2]	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
M1	I	mac0_rxd[3]	mac0_rxd[3]	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
L2	I	mac0_rxd[4]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
N1	I	mac0_rxd[5]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
L1	I	mac0_rxd[6]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss

Table 2-3 S5530 PPI Port 0 Signal Descriptions

Ball	Type	GMII	MII	Description	Unused
M2	I	mac0_rxd[7]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss
H2	I	Vss	mac0_tx_clk	Transmit clock. See also IEEE 802.3 22.2.2.1	Vss
H3	O	mac0_gtx_clk	Do not connect	125MHz transmit clock output. See also IEEE 802.3 352.2.1	Do not connect
H6	O	mac0_tx_en	mac0_tx_en	Transmit enable. See also IEEE 802.3 35.2.2.3	Do not connect
H5	O	mac0_tx_er	mac0_tx_er	Transmit coding error. See also IEE 802.3 35.2.2.5	Do not connect
H4	O	Do not connect	Do not connect	Do not connect.	Do not connect
H1	I	mac0_crs	mac0_crs	Carrier sense. See also IEEE 802.3 22.2.2.9.	Vss
F2	O	mac0_txd[0]	mac0_txd[0]	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
F3	O	mac0_txd[1]	mac0_txd[1]	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
G5	O	mac0_txd[2]	mac0_txd[2]	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
F1	O	mac0_txd[3]	mac0_txd[3]	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
G3	O	mac0_txd[4]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
G2	O	mac0_txd[5]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
G1	O	mac0_txd[6]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect
G4	O	mac0_txd[7]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4	Do not connect

2.1.1.2 Port 1 pin and Signal Assignments

Table 2-4 lists Port 1 pin and signal assignments for each MAC mode.

Table 2-4 S5530 PPI Port 1 Signal Description

Pin	Type	GMII	MII	Description	Unused
E2	O	mac_mdc	mac_mdc	Management data clock. See also IEEE 802.3 22.2.2.11.	Do not connect
E1	I/O	mac_mdio	mac_mdio	Management data input–output. See also IEEE 802.3 22.2.2.12.	Pull-up
AE1	I	mac1_rx_clk	mac1_rx_clk	Receive clock. See also IEEE 802.3 35.2.2.2.	Vss
Y1	I	mac1_rx_dv	mac1_rx_dv	Receive data valid. See also IEEE 802.3 35.2.2.6.	Vss
AC1	I	mac1_rx_er	mac1_rx_er	Receive error. See also IEEE 802.30 35.2.2.8.	Vss
AB1	I	mac1_col	mac1_col	Collision detect. See also IEEE 802.3 35.2.2.20.	Vss
W1	O	Do not connect	Do not connect	Do not connect.	Do not connect
L5	I	mac1_rxd[0]	mac1_rxd[0]	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
L6	I	mac1_rxd[1]	mac1_rxd[1]	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
AD1	I	mac1_rxd[2]	mac1_rxd[2]	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
N3	I	mac1_rxd[3]	mac1_rxd[3]	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss

Table 2-4 S5530 PPI Port 1 Signal Description

Pin	Type	GMII	MII	Description	Unused
P2	I	mac1_rxd[4]	Vss	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
R2	I	mac1_rxd[5]	Vss	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
M4	I	mac1_rxd[6]	Vss	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
T2	I	mac1_rxd[7]	Vss	Receive data bit. See also IEEE 802.3 22.2.2.7.	Vss
N2	I	Vss	mac1_tx_clk	Transmit clock. See also IEEE 802.3 22.2.2.1.	Vss
K5	O	mac1_gtx_clk	Do not connect	125MHz transmit clock. See also IEEE 802.3 35.2.2.1.	Do not connect
V1	O	mac1_tx_en	mac1_tx_en	Transmit enable. See also IEEE 802.3 35.2.2.3.	Do not connect
M3	O	mac1_tx_er	mac1_tx_er	Transmit error coding. See also IEEE 802.3 35.2.2.5.	Do not connect
L4	O	Do not connect	Do not connect	Do not connect.	Do not connect
AA1	I	mac1_crs	mac1_crs	Carrier sense. See also IEEE 802.3 35.2.2.9.	Vss
L3	O	mac1_txd[0]	mac1_txd[0]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
K4	O	mac1_txd[1]	mac1_txd[1]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
P1	O	mac1_txd[2]	mac1_txd[2]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
T1	O	mac1_txd[3]	mac1_txd[3]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
U1	O	mac1_txd[4]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
K7	O	mac1_txd[5]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
R1	O	mac1_txd[6]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
K6	O	mac1_txd[7]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect

2.1.1.3 Port 2 Pin and Signal Assignments

Table 2-5 lists Port 2 pin and signal assignments for each MAC mode.

Table 2-5 S5530 PPI Port 2 Signal Description

Pin	Type	GMII	MII	Description	Unused
E2	O	mac_mdc	mac_mdc	Management data clock. See also IEEE 802.3 22.2.2.11.	Do not connect
E1	I/O	mac_mdio	mac_mdio	Management data input/output. See also IEEE 802.3 22.2.2.12.	Pull-up
N7	I	mac2_rx_clk	mac2_rx_clk	Receive clock. See also 802.3 35.2.2.2.	Vss
Y3	I	mac2_rx_dv	mac2_rx_dv	Receive data valid. See also IEEE 802.3 35.2.2.6.	Vss
W3	I	mac2_rx_er	mac2_rx_er	Receive error. See also IEEE 802.3 35.2.2.8.	Vss
V3	I	mac2_col	mac2_col	Collision detect. See also IEEE 802.3 35.2.2.10.	Vss

Table 2-5 S5530 PPI Port 2 Signal Description

Pin	Type	GMII	MII	Description	Unused
R3	O	Do not connect	Do not connect	Do not connect.	Do not connect
P5	I	mac2_rxd[0]	mac2_rxd[0]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
R4	I	mac2_rxd[1]	mac2_rxd[1]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AA3	I	mac2_rxd[2]	mac2_rxd[2]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AC3	I	mac2_rxd[3]	mac2_rxd[3]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AE3	I	mac2_rxd[4]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AF3	I	mac2_rxd[5]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AB3	I	mac2_rxd[6]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
R5	I	mac2_rxd[7]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AF2	I	Vss	mac2_tx_clk	Transmit clock. See also IEEE 802.3 22.2.2.1.	Vss
Y2	O	mac2_gtx_clk	Do not connect	125MHz transmit clock. See also IEEE 802.3 35.2.2.1.	Do not connect
AD2	O	mac2_tx_en	mac2_tx_en	Transmit enable. See also IEEE 802.3 35.2.2.3.	Do not connect
AE2	O	mac2_tx_er	mac2_tx_er	Transmit coding error See also IEEE 802.3 35.2.2.5.	Do not connect
N5	O	Do not connect	Do not connect	Do not connect.	Do not connect
T3	I	mac2_crs	mac2_crs	Carrier sense. See also IEEE 802.3 35.2.2.9.	Vss
U2	O	mac2_txd[0]	mac2_txd[0]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
V2	O	mac2_txd[1]	mac2_txd[1]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
M5	O	mac2_txd[2]	mac2_txd[2]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
N4	O	mac2_txd[3]	mac2_txd[3]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
P3	O	mac2_txd[4]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
W2	O	mac2_txd[5]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect

Table 2-5 S5530 PPI Port 2 Signal Description

Pin	Type	GMII	MII	Description	Unused
AA2	O	mac2_txd[6]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
M6	O	mac2_txd[7]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect

2.1.1.4 Port 3 Pin and Signal Assignments

Table 2-6 lists Port 3 pin and signal assignments for each MAC mode.

Table 2-6 S5530 PPI Port 3 Signal Description

Pin	Type	GMII	MII	Description	Unused
E2	O	mac_mdc	mac_mdc	Management data clock. See also IEEE 802.3 22.2.2.11.	Do not connect
E1	I/O	mac_mdio	mac_mdio	Management data input/output. See also IEEE 802.3 22.2.2.12.	Pull-up
AE6	I	mac3_rx_clk	mac3_rx_clk	Receive clock. See also IEEE 802.3 22.2.2.2.	Vss
AE5	I	mac3_rx_dv	mac3_rx_dv	Receive data valid. See also IEEE 802.3 22.2.2.6.	Vss
T6	I	mac3_rx_er	mac3_rx_er	Receive error. See also IEEE 802.3 22.2.2.8.	Vss
AC5	I	mac3_col	mac3_col	Collision detect. See also IEEE 802.3 35.2.2.10.	Vss
AA5	O	Do not connect	Do not connect	Do not connect.	Do not connect
AF5	I	mac3_rxd[0]	mac3_rxd[0]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AF6	I	mac3_rxd[1]	mac3_rxd[1]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AF7	I	mac3_rxd[2]	mac3_rxd[2]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AD6	I	mac3_rxd[3]	mac3_rxd[3]	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
V5	I	mac3_rxd[4]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
U6	I	mac3_rxd[5]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AC6	I	mac3_rxd[6]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7.	Vss
AF8	I	mac3_rxd[7]	Vss	Receive data bit. See also IEEE 802.3 35.2.2.7	Vss

Table 2-6 S5530 PPI Port 3 Signal Description

Pin	Type	GMII	MII	Description	Unused
Y5	I	Vss	mac3_tx_clk	Transmit clock. See also IEEE 802.3 22.2.2.1.	Vss
AE4	O	mac3_gtx_clk	Do not connect	125MHz transmit clock. See also IEEE 802.3 35.2.2.1.	Do not connect
T5	O	mac3_tx_en	mac3_tx_en	Transmit enable. See also IEEE 802.3 22.2.2.3.	Do not connect
R6	O	mac3_tx_er	mac3_tx_er	Transmit coding error. See also IEEE 802.3 22.2.2.5.	Do not connect
AF4	O	Do not connect	Do not connect	Do not connect.	Do not connect
U5	I	mac3_crs	mac3_crs	Carrier sense. See also IEEE 802.3 22.2.2.9.	Vss
V4	O	mac3_txd[0]	mac3_txd[0]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
P6	O	mac3_txd[1]	mac3_txd[1]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
Y4	O	mac3_txd[2]	mac3_txd[2]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
W4	O	mac3_txd[3]	mac3_txd[3]	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
U4	O	mac3_txd[4]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
AA4	O	mac3_txd[5]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
AD4	O	mac3_txd[6]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect
AC4	O	mac3_txd[7]	Do not connect	Transmit data bit. See also IEEE 802.3 35.2.2.4.	Do not connect

2.1.2 MAC Bypass Signal Descriptions

The following sections describe the pin and signal assignments for MAC bypass mode.

2.1.2.1 MAC Bypass Port 0 and Port 1 Pin and Signal Assignments

Table 2-7 lists MAC bypass Port 0 and Port 1 pin and signal assignments.

Table 2-7 S5530 MAC Bypass Port 0 and Port 1 Signal Description

Ball	Type	16-bit	8-Bit	Description	Unused
E2	O	Do not connect	Do not connect	Do not connect.	Do not connect
E1	I/O	Pull-up	Pull-up	Pull-up.	Pull-up
J6	I	mac0_rx_clk	mac0_rx_clk	Receive clock.	Vss
J4	I	mac0_rx_sidechan[0]	mac0_rx_sidechan[0]	Bit 0 of the receive side channel.	Vss
J3	I	mac0_rx_sidechan[1]	mac0_rx_sidechan[1]	Bit 1 of the receive side channel.	Vss
J2	I	mac0_rx_sidechan[2]	mac0_rx_sidechan[2]	Bit 2 of the receive side channel.	Vss
J1	O	mac0_rx_stall	mac0_rx_stall	Receiver stall. Indicates that the receiver cannot handle more data.	Do not connect
K1	I	mac0_rxd[0]	mac0_rxd[0]	Receive data bit.	Vss
K2	I	mac0_rxd[1]	mac0_rxd[1]	Receive data bit.	Vss
J5	I	mac0_rxd[2]	mac0_rxd[2]	Receive data bit.	Vss
M1	I	mac0_rxd[3]	mac0_rxd[3]	Receive data bit.	Vss
L2	I	mac0_rxd[4]	mac0_rxd[4]	Receive data bit.	Vss
N1	I	mac0_rxd[5]	mac0_rxd[5]	Receive data bit.	Vss
L1	I	mac0_rxd[6]	mac0_rxd[6]	Receive data bit.	Vss
M2	I	mac0_rxd[7]	mac0_rxd[7]	Receive data bit.	Vss
H2	I	mac0_tx_clk_in	mac0_tx_clk_in	Transmit clock in.	Vss
H3	O	mac0_tx_clk_out	mac0_tx_clk_out	Buffered version of mac0_tx_clk_in.	Do not connect
H6	O	mac0_tx_sidechan[0]	mac0_tx_sidechan[0]	Bit 0 of the transmit side channel.	Do not connect
H5	O	mac0_tx_sidechan[1]	mac0_tx_sidechan[1]	Bit 1 of the transmit side channel.	Do not connect
H4	O	mac0_tx_sidechan[2]	mac0_tx_sidechan[2]	Bit 2 of the transmit side channel.	Do not connect
H1	I	mac0_tx_stall	mac0_tx_stall	Transmit stall. Requests that the transmitter stall and drive the bus to idle.	Vss
F2	O	mac0_txd[0]	mac0_txd[0]	Transmit data bit.	Do not connect
F3	O	mac0_txd[1]	mac0_txd[1]	Transmit data bit.	Do not connect
G5	O	mac0_txd[2]	mac0_txd[2]	Transmit data bit.	Do not connect
F1	O	mac0_txd[3]	mac0_txd[3]	Transmit data bit.	Do not connect
G3	O	mac0_txd[4]	mac0_txd[4]	Transmit data bit.	Do not connect
G2	O	mac0_txd[5]	mac0_txd[5]	Transmit data bit.	Do not connect
G1	O	mac0_txd[6]	mac0_txd[6]	Transmit data bit.	Do not connect
G4	O	mac0_txd[7]	mac0_txd[7]	Transmit data bit.	Do not connect
AE1	I	Vss	mac1_rx_clk	Receive clock.	Vss
Y1	I	Vss	mac1_rx_sidechan[0]	Bit 0 of the receive side channel.	Vss
AC1	I	Vss	mac1_rx_sidechan[1]	Bit 1 of the receive side channel.	Vss

Table 2-7 S5530 MAC Bypass Port 0 and Port 1 Signal Description

Ball	Type	16-bit	8-Bit	Description	Unused
AB1	I	Vss	mac1_rx_sidechan[2]	Bit 2 of the receive side channel.	Vss
W1	O	Do not connect	mac1_rx_stall	Receive stall. Indicates that the receiver cannot handle more data.	Do not connect
L5	I	mac0_rxd[8]	mac1_rxd[0]	Receive data bit.	Vss
L6	I	mac0_rxd[9]	mac1_rxd[1]	Receive data bit.	Vss
AD1	I	mac0_rxd[10]	mac1_rxd[2]	Receive data bit.	Vss
N3	I	mac0_rxd[11]	mac1_rxd[3]	Receive data bit.	Vss
P2	I	mac0_rxd[12]	mac1_rxd[4]	Receive data bit.	Vss
R2	I	mac0_rxd[13]	mac1_rxd[5]	Receive data bit.	Vss
M4	I	mac0_rxd[14]	mac1_rxd[6]	Receive data bit.	Vss
T2	I	mac0_rxd[15]	mac1_rxd[7]	Receive data bit.	Vss
N2	I	tie to mac0_tx_clk_in	mac1_tx_clk_in	Transmit clock in.	Vss
K5	O	Do not connect	mac1_tx_clk_out	Buffered version of mac1_tx_clk_in.	Do not connect
V1	O	Do not connect	mac1_tx_sidechan[0]	Bit 0 of the transmit side channel.	Do not connect
M3	O	Do not connect	mac1_tx_sidechan[1]	Bit 1 of the transmit side channel.	Do not connect
L4	O	Do not connect	mac1_tx_sidechan[2]	Bit 2 of the transmit side channel.	Do not connect
AA1	I	Vss	mac1_tx_stall	Transmit stall. Requests that the transmitter stall and drive the bus to idle.	Vss
L3	O	mac0_txd[8]	mac1_txd[0]	Transmit data bit.	Do not connect
K4	O	mac0_txd[9]	mac1_txd[1]	Transmit data bit.	Do not connect
P1	O	mac0_txd[10]	mac1_txd[2]	Transmit data bit.	Do not connect
T1	O	mac0_txd[11]	mac1_txd[3]	Transmit data bit.	Do not connect
U1	O	mac0_txd[12]	mac1_txd[4]	Transmit data bit.	Do not connect
K7	O	mac0_txd[13]	mac1_txd[5]	Transmit data bit.	Do not connect
R1	O	mac0_txd[14]	mac1_txd[6]	Transmit data bit.	Do not connect
K6	O	mac0_txd[15]	mac1_txd[7]	Transmit data bit.	Do not connect

2.1.2.2 MAC Bypass Port 2 and Port 3 Pin and Signal Assignments

Table 2-8 lists MAC bypass Port 2 and Port 3 pin and signal assignments.

Table 2-8 S5530 MAC Bypass Port 2 and Port 3 Signal Descriptions

Pin	Type	16-Bit	8-Bit	Description	Unused
E2	O	Do not connect	Do not connect	Do not connect.	Do not connect
E1	I/O	Pull-up	Pull-up	Pull-up.	Pull-up
N7	I	mac2_rx_clk	mac2_rx_clk	Receive clock.	Vss
Y3	I	mac2_rx_sidechan[0]	mac2_rx_sidechan[0]	Bit 0 of the receive side channel.	Vss
W3	I	mac2_rx_sidechan[1]	mac2_rx_sidechan[1]	Bit 1 of the receive side channel.	Vss
V3	I	mac2_rx_sidechan[2]	mac2_rx_sidechan[2]	Bit 2 of the receive side channel.	Vss
R3	O	mac2_rx_stall	mac2_rx_stall	Receiver stall. Indicates that the receiver cannot handle more data.	Do not connect
P5	I	mac2_rxd[0]	mac2_rxd[0]	Receive data bit.	Vss
R4	I	mac2_rxd[1]	mac2_rxd[1]	Receive data bit.	Vss
AA3	I	mac2_rxd[2]	mac2_rxd[2]	Receive data bit.	Vss
AC3	I	mac2_rxd[3]	mac2_rxd[3]	Receive data bit.	Vss
AE3	I	mac2_rxd[4]	mac2_rxd[4]	Receive data bit.	Vss
AF3	I	mac2_rxd[5]	mac2_rxd[5]	Receive data bit.	Vss
AB3	I	mac2_rxd[6]	mac2_rxd[6]	Receive data bit.	Vss
R5	I	mac2_rxd[7]	mac2_rxd[7]	Receive data bit.	Vss
AF2	I	mac2_tx_clk_in	mac2_tx_clk_in	Transmit clock in.	Vss
Y2	O	mac2_tx_clk_out	mac2_tx_clk_out	Buffered version of mac2_tx_clk_in.	Do not connect
AD2	O	mac2_tx_sidechan[0]	mac2_tx_sidechan[0]	Bit 0 of the transmit side channel.	Do not connect
AE2	O	mac2_tx_sidechan[1]	mac2_tx_sidechan[1]	Bit 1 of the transmit side channel.	Do not connect
N5	O	mac2_tx_sidechan[2]	mac2_tx_sidechan[2]	Bit 2 of the transmit side channel.	Do not connect
T3	I	mac2_tx_stall	mac2_tx_stall	Transmit stall. Requests that the transmitter stall and drive the bus to idle.	Vss
U2	O	mac2_txd[0]	mac2_txd[0]	Transmit data bit.	Do not connect
V2	O	mac2_txd[1]	mac2_txd[1]	Transmit data bit.	Do not connect
M5	O	mac2_txd[2]	mac2_txd[2]	Transmit data bit.	Do not connect
N4	O	mac2_txd[3]	mac2_txd[3]	Transmit data bit.	Do not connect
P3	O	mac2_txd[4]	mac2_txd[4]	Transmit data bit.	Do not connect
W2	O	mac2_txd[5]	mac2_txd[5]	Transmit data bit.	Do not connect
AA2	O	mac2_txd[6]	mac2_txd[6]	Transmit data bit.	Do not connect
M6	O	mac2_txd[7]	mac2_txd[7]	Transmit data bit.	Do not connect
AE6	I	Vss	mac3_rx_clk	Receive clock.	Vss
AE5	I	Vss	mac3_rx_sidechan[0]	Bit 0 of the receive side channel.	Vss
T6	I	Vss	mac3_rx_sidechan[1]	Bit 1 of the receive side channel.	Vss

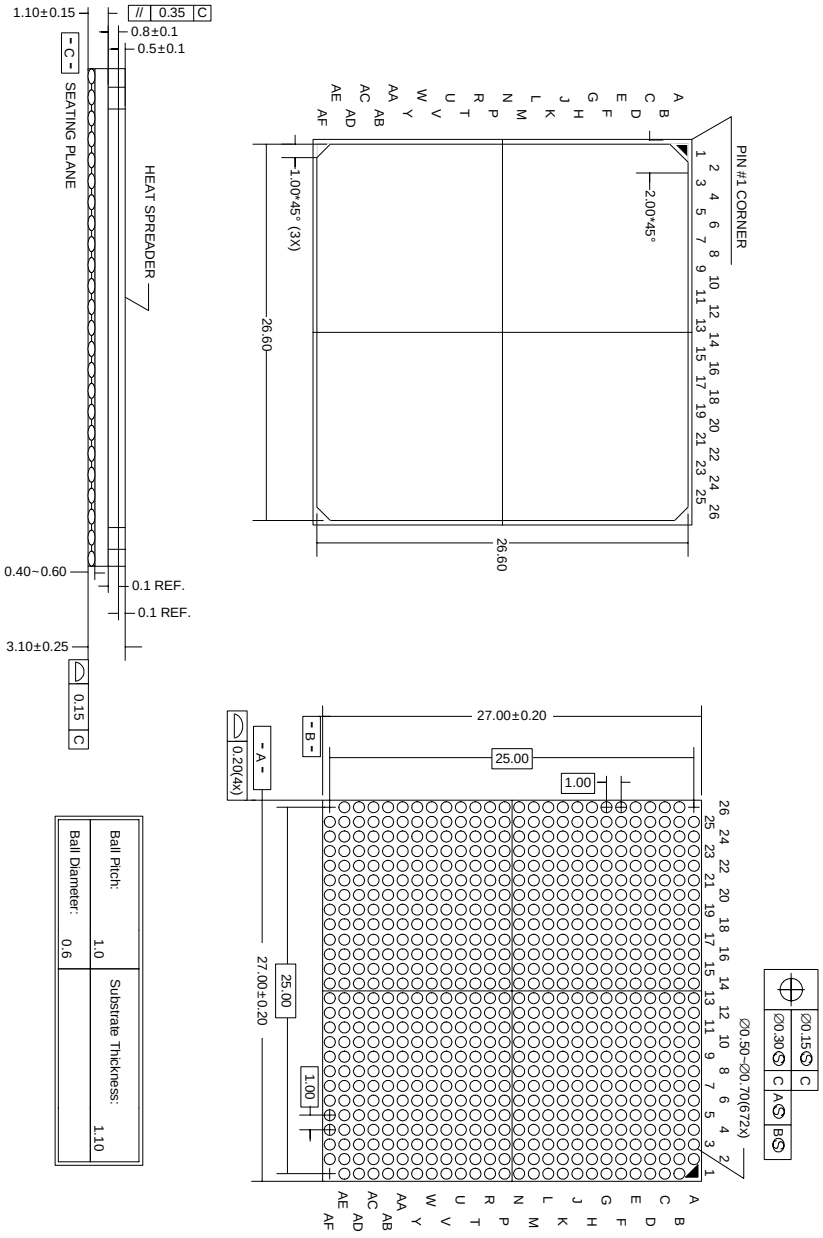
Table 2-8 S5530 MAC Bypass Port 2 and Port 3 Signal Descriptions

Pin	Type	16-Bit	8-Bit	Description	Unused
AC5	I	Vss	mac3_rx_sidechan[2]	Bit 2 of the receive side channel.	Vss
AA5	O	Do not connect	mac3_rx_stall	Receive stall. Request that the transmitter stall and drive the bus to idle.	Do not connect
AF5	I	mac2_rxd[8]	mac3_rxd[0]	Receive data bit.	Vss
AF6	I	mac2_rxd[9]	mac3_rxd[1]	Receive data bit.	Vss
AF7	I	mac2_rxd[10]	mac3_rxd[2]	Receive data bit.	Vss
AD6	I	mac2_rxd[11]	mac3_rxd[3]	Receive data bit.	Vss
V5	I	mac2_rxd[12]	mac3_rxd[4]	Receive data bit.	Vss
U6	I	mac2_rxd[13]	mac3_rxd[5]	Receive data bit.	Vss
AC6	I	mac2_rxd[14]	mac3_rxd[6]	Receive data bit.	Vss
AF8	I	mac2_rxd[15]	mac3_rxd[7]	Receive data bit.	Vss
Y5	I	tie to mac2_tx_clk_in	mac3_tx_clk_in	Transmit clock in.	Vss
AE4	O	Do not connect	mac3_tx_clk_out	Buffered version of mac3_tx_clk_in.	Do not connect
T5	O	Do not connect	mac3_tx_sidechan[0]	Bit 0 of the transmit side channel.	Do not connect
R6	O	Do not connect	mac3_tx_sidechan[1]	Bit 1 of the transmit side channel.	Do not connect
AF4	O	Do not connect	mac3_tx_sidechan[2]	Bit 2 of the transmit side channel.	Do not connect
U5	I	Vss	mac3_tx_stall	Transmit stall. Requests that the transmitter stall and drive the bus to idle.	Vss
V4	O	mac2_txd[8]	mac3_txd[0]	Transmit data bit.	Do not connect
P6	O	mac2_txd[9]	mac3_txd[1]	Transmit data bit.	Do not connect
Y4	O	mac2_txd[10]	mac3_txd[2]	Transmit data bit.	Do not connect
W4	O	mac2_txd[11]	mac3_txd[3]	Transmit data bit.	Do not connect
U4	O	mac2_txd[12]	mac3_txd[4]	Transmit data bit.	Do not connect
AA4	O	mac2_txd[13]	mac3_txd[5]	Transmit data bit.	Do not connect
AD4	O	mac2_txd[14]	mac3_txd[6]	Transmit data bit.	Do not connect
AC4	O	mac2_txd[15]	mac3_txd[7]	Transmit data bit.	Do not connect

2.2 Physical Characteristics

Figure 2-1 illustrates the S5530 's physical characteristics (measurements are in mm).

Figure 2-1 S5530 physical characteristics



Chapter 3 Electrical Characteristics

IMPORTANT! Some values are preliminary and as such cannot be used for final designs. Updated values will be incorporated as they become available. Contact your Stretch representative to ensure that you have the most up-to-date documentation before finalizing your design.

3.1 DC Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings for S5530. Operating the chip outside these maximum values may cause permanent damage to the chip and attached devices. Exposing the chip to these maximum ratings for extended periods may affect its reliability.

Table 3-1 DC absolute maximum ratings

Symbol	Parameter name	Min	Max	Units
VIN	Input Voltage – on any pin	VSS - 0.5	VDD + 0.5	V
TJ	Junction Temperature – power applied	-40	125	°C
TX	Storage Temperature – no power applied	-55	150	°C
VDD_CORE	Supply voltage	-0.3	1.55	V
AVDD	PLL supply voltage	-0.3	1.55	V
VDD_IO	Interface supply voltage (except DDR, PCI/PCI-X)	-0.3	3.45	V
VDD_PCI	PCI/PCI-X I/O supply voltage	-0.3	3.45	V
VDD_DDR	DDR SDRAM SSTL-2 supply voltage	-0.3	2.7	V

3.1.1 Power-on Sequence Requirements

To avoid the possibility of latch-up or large power supply current spikes during power-on, the following requirements must be met:

- All I/O power supplies must be turned on prior to VDD_CORE and AVDD
- I/O power supplies must be turned on such that there is never more than 2.8V difference between any two I/O power supplies
- VDD_CORE and AVDD must never be more than 0.5V greater than any I/O power supply.

These conditions can be easily met by first turning on I/O supplies in order from lowest to highest, followed by turning on Vdd_core and AVdd.

3.2 DC Recommended Operating Conditions

Table 3-2 lists the recommended operating conditions for S5530. Operating the chip within these ranges guarantees functional operation of the chip. ‘

Table 3-2 DC recommended operating conditions

Symbol	Parameter name			Min	Nom	Max	Units
TJ	Junction Temperature - Operating			0	-	100	°C
VSS	Ground			0	0	0	V
AVDD	PLL Supply Voltage	-3	300 MHz Max	1.3	1.35	1.4	V
VDD_CORE	Core Supply Voltage	-3	300 MHz Max	1.3	1.35	1.4	V
VDD_IO	Interface Supply Voltage (except DDR, PCI/PCI-X) **NOTE:** Value depends on chosen voltage.			2.37/3.15	2.5/3.3	2.63/3.45	V
VDD_PCI	PCI/PCI-X I/O Supply Voltage			3.15	3.3	3.45	V
VDD_DDR	DDR SDRAM SSTL-2 Supply Voltage			2.37	2.5/2.6	2.7	V
VTTS	SSTL-2 Termination Voltage			VREFS - .04	VREFS	VREFS + .04	V
VREFS	SSTL-2 Input Reference Levels			VDD_DDR/2 - 0.1	VDD_DDR/2	VDD_DDR/2 + 0.1	V
VIH	Input HIGH Voltage (except SSTL-2, PCI/PCI-X)			1.7	-	VDD_IO + 0.3	V
VIL	Input LOW Voltage (except SSTL-2, PCI/PCI-X)			-0.3	-	0.8	V
VIHP	Input HIGH Voltage (PCI/PCI-X)			.5 VDD_PCI	-	3.6	V
VILP	Input LOW Voltage (PCI/PCI-X)			-0.3	-	.35 VDD_PCI	V
VIHD	Input HIGH Voltage (SSTL-2)			VREF + 0.15	-	VDD_DDR + 0.3	V
VILD	Input LOW Voltage (SSTL-2)			-0.3	-	VREF - 0.15	V

3.3 Package Thermal Characteristics

Based on the following thermal characteristics, the power consumption specifications in Table 3-5, and the specific system operating and environment conditions, you must ensure that the S5530 junction temperature (T_J) does not exceed the maximum specified in Table 3-2.

Table 3-3 Package thermal characteristics

Symbol	Parameter name	Air Velocity (m/s)	Value	Units
Θ_{JC}	HFCBGA package, junction-to-case thermal resistance	-	0.42	°C/W
Θ_{JA}	HFCBGA package junction-to-ambient thermal resistance	0	13.9	°C/W
		1	11.0	°C/W
		2	10.0	°C/W
		3	9.3	°C/W

NOTE: The values in Table 3-4 are simulated under the following conditions (based on JEDEC JEDSD51-9). Values are provided as a general guideline. Actual thermal performance is system dependent.

PCB layers	PCB dimensions	PCB thickness
4 layers (2s2p)	101.5 x 114.5 mm	1.6 mm

3.4 DC Electrical Characteristics

Table 3-4 lists the DC characteristics that apply to the S5530 under the recommended operating condition listed in Table 3-2.

Table 3-4 DC electrical characteristics at recommended operating conditions

Symbol	Parameter name	Conditions	Min	Nom	Max	Units
$I_{LEAKAGE}$	Driver Pad Leakage [1]	V_I = 0 Volts V_I = V_{DD}	-	-	± 100	µA
V_{OH}	Output HIGH Voltage (except SSTL-2, PCI/PCI-X)	I_{OUT} = -4mA	V_{DD_IO} - 0.4	-	-	V
V_{OL}	Output LOW Voltage (except SSTL-2, PCI/PCI-X)	I_{OUT} = 4mA	-	-	0.4	V
V_{OHD}	Output HIGH Voltage (DDR, SSTL-2 Class 1)	I_{OUT} = -8.1mA	V_{TT} + 0.405	-	-	V

Table 3-4 DC electrical characteristics at recommended operating conditions

Symbol	Parameter name	Conditions	Min	Nom	Max	Units
VOLD	Output LOW Voltage (DDR, SSTL-2 Class 1)	IOUT = 8.1mA	-	-	VTT - 0.405	V
VOHP	Output HIGH Voltage (PCI/PCI-X)	IOUT = -500µA	.9 VDD_PCI	-	-	V
VOLP	Output LOW Voltage (PCI/PCI-X)	IOUT = 1500µA	-	-	.1 VDD_PCI	V
RUP	Pull-up Resistance [2]		-	10K	-	ohms
RDOWN	Pull-down Resistance [3]		-	10K	-	ohms
CIN	Input Pin Capacitance [4]		-	5	8	pf

[1] Internal weak hold circuits are present on the following pins: pci_ad[63:32], pci_cbe[7:4]#, and pci_par64. The hold pull-up and pull-down resistance is typically 6K ohms.

[2] Internal pull-up resistors are present on the following pins: tdi, tms, trst#, gib[36], and gib[31:0]

[3] Internal pull-down resistors are present on the following pins: se, sm, tck, and debug

[4] Value is guaranteed by design, and not tested.

3.5 Power Consumption

Table 3-5 lists power consumption values for S5 processors.

Table 3-5 Power Consumption

Power Supply [1]	VDD (Volts)	Clock	Clock Frequency (MHz)	Current (mA)	Power (Watts)
VDD_CORE	1.35	Processor Clock	300	2600	3.5
			250	2200	3.0
VDD_DDR	2.6	DDR Clock	200	300	0.8
VDD_IO	3.3			60	0.2
VDD_PCI	3.3	pci_clk	33	30	0.1
AVDD	1.35			45	0.1

[1] All values in the table are typical. Actual power consumption depends on the application and system conditions.

3.6 AC Electrical Characteristics

The following sections describe the AC specification and timing for peripheral devices on the S5530. All timing is specified over the DC recommended operating conditions.

Load capacitance is 10pf unless otherwise specified.

The term "PCLK" is the period of the internal LP clock

3.6.1 UART Timing

Table 3-6 UART interface AC specification

Symbol	Parameter	Min	Nominal	Max	Units
FCLK	UART clock frequency	-	1.8432	20.0	MHz
TH	UART clock high time	24.0	-	-	ns
TL	UART clock low time	24.0	-	-	ns

Figure 3-1 UART timing diagram

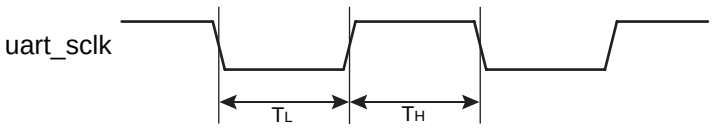
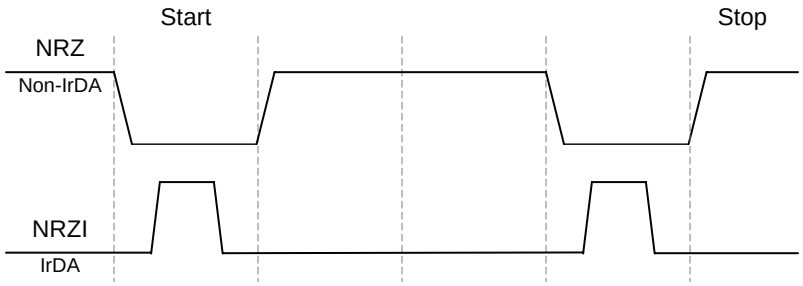


Figure 3-2 IrDA pulse



3.6.2 Serial Peripheral Interface Timing

The serial interface consists of slave select lines, serial clock lines, as well as input and output data lines. All transfers are full duplex transfers of a programmable number of bits per transfer (up to 64 bits).

Compared to the SPI/Microwire protocol, the SPI device has some additional functionality. It can drive data to the output data line with respect to the falling (SPI/Microwire compliant) or rising edge of the serial clock, and it can latch

data on an input data line on the rising (SPI/Microwire compliant) or falling edge of a serial clock line. It also can transmit (receive) the MSB first (SPI/Microwire compliant) or the LSB first.

The SPI clock rate is programmable. The polarity of the clock, and which clock edge transmits and receives data, and clock idle are also programmable. The nominal clock high or low time is the PCLK period times the programmed divider value plus 1, and is noted here as TCN.

It is important to know that the RxX and TxX registers share the same flip-flops, which means that what is received from the input data line in one transfer is transmitted on the output data line in the next transfer if no write access to the TxX register is executed between the transfers.

Table 3-7 Serial Peripheral interface (SPI) AC specification

Symbol	Parameter	Min	Max	Units
TCH	Clock high time	TCN – 3.0	TCN + 3.0	ns
TCL	Clock low time	TCN – 3.0	TCN + 3.0	ns
TCS	Chip select high time [1]	6 * PCLK	-	ns
TCSL	Chip select to first clock rising edge	TCN - 3.0	TCN + 3.0	ns
TCSH	Last falling clock edge to chip select inactive	TCN – 3.0	-	ns
TSU	Receive data setup	3.0	-	ns
TH	Receive data hold time	3.0	-	ns
TTCO	Clock falling to transmit data valid	TCN – 3.0	-	ns
TTHO	Transmit data hold time	TCN – 3.0	-	ns

[1] This parameter is dependent upon the software driver, and is normally much larger.

Figure 3-3 through Figure 3-8 illustrate the timing for the SPI, and for the various SPI configurations.

3.6.3 TWI Interface Timing

The S5 has software programmable clock low and clock high times on the TWI interface. Table 3-8 shows timing for 100Kbit/sec.

The maximum capacitance on `twi_clk` and `twi_data` is 400pf.

Figure 3-3 SPI timing diagram

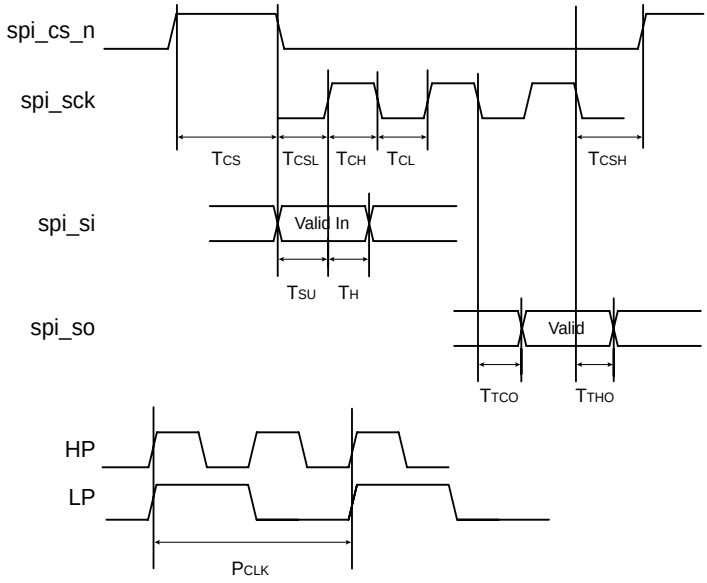


Figure 3-4 SPI timing 1

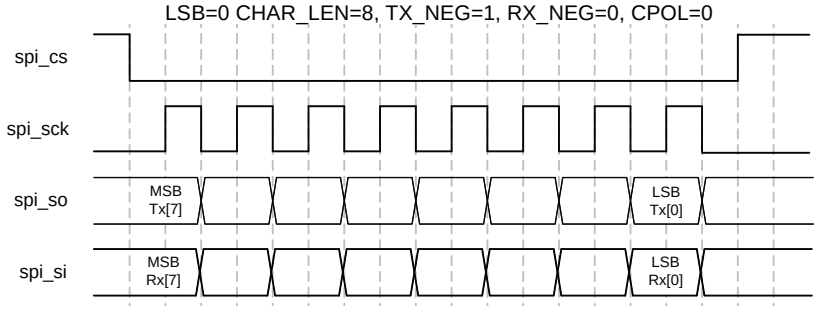
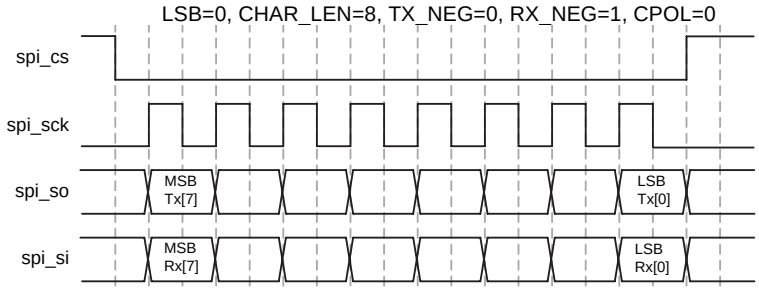


Figure 3-5 SPI timing 2



3.6.4 GIB Timing

The GIB provides programmable timing and handshake to support a variety of devices. The timing shown here is based upon the described programs. Wait states in the GIB programs are used to support a wide range of memory speeds. The programs can also specify the handshake.

Figure 3-6 SPI timing 3

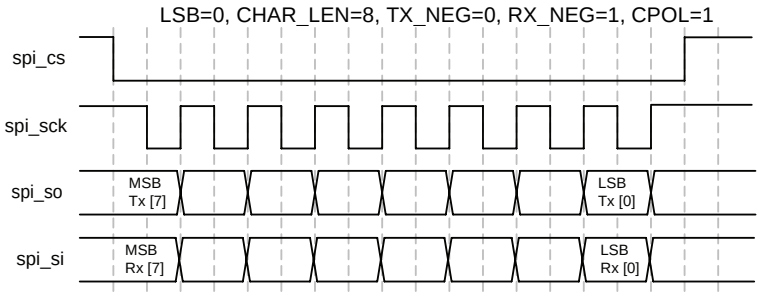


Figure 3-7 SPI timing 4

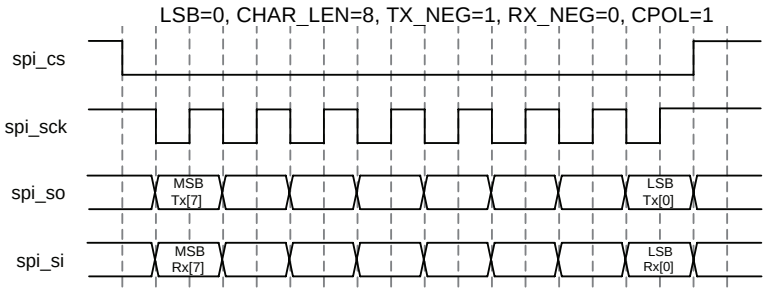


Figure 3-8 SPI timing 5

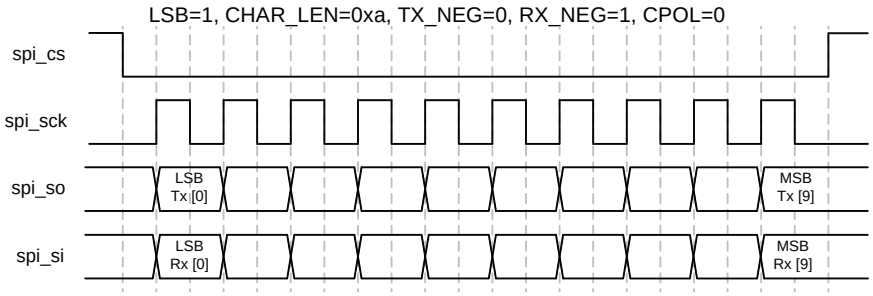


Table 3-8 TWI interface AC specification

Symbol	Parameter	Input	Output
tHD;STA	START condition hold time	-	> 4.0 µsec [1]
tLOW	twi_clk low time	-	> 4.7 µsec [1]
tHIGH	twi_clk high time	-	> 4.0 µsec [1]
tSU;STA	Repeated START set-up time	-	> 4.7 µsec [1]
tHD;DAT	Data hold time	>= 0 ns	> PCLK - tR [2]
tSU;DAT1	Data set-up time	>= 50 ns	> 4.0 µsec [1]
tSU:DAT2	Data set-up time before repeated START condition	-	> 4.0 µsec [1]
tSU;DAT3	twi_data set-up time before STOP condition	-	> 4.0 µsec [1]

Table 3-8 TWI interface AC specification

Symbol	Parameter	Input	Output
tR	twi_clk and twi_data rise time	<= 1 µsec	- [3]
tF	twi_clk and twi_data fall time	<= 0.3 µsec	< 0.3 µsec [4]
tSU;STO	Stop condition set-up time	-	> 4.0 µsec [1]
tBUF	Bus free time	-	> 4.7 µsec [1]
Cb	Capacitive load per bus line	-	<= 400 pF

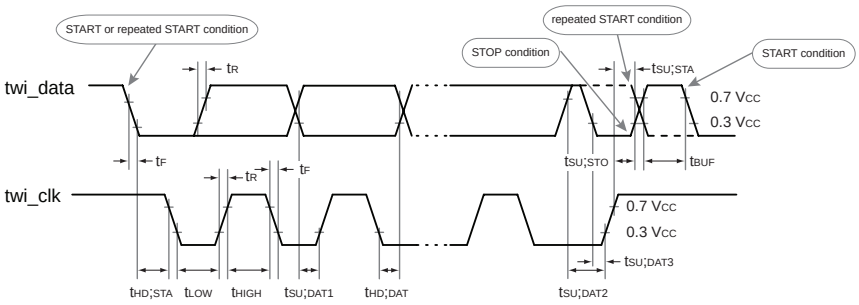
[1] At 100Kbit/second. At other bit rates this value is inversely proportional to the bit rate at 100kbit/sec.

[2] This hold time can be increased by adding a 50 ohm series resistance on the twi_data pin of the S5. This series resistance is needed to guarantee that the tf on twi_data is less than the tF on twi_clk—thereby guaranteeing at least 0 ns hold time at the TWI receiver

[3] The rise time of twi_clk and twi_data is determined by the external capacitance and pull-up resistance. The rise time must be less than 1 µsec.

[4] Glitches on the twi_data and twi_clk lines with a duration of less than 3 PCLK will be filtered out.

Figure 3-9 TWI timing diagram

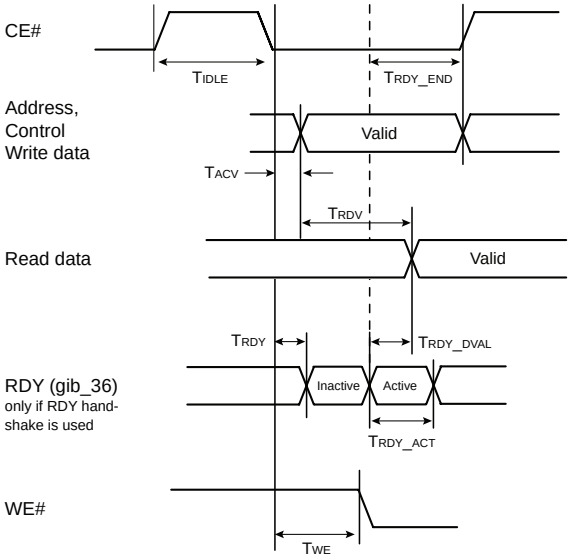


In the formulas, the following terms are used:

- PCLK is the period of the S5530LP [1] clock; normal frequency is 150 MHz.
- wait*n* is the number of wait states specified in the program

[1] One-half the processor clock rate (refer to "Clocks" on page 1-7).

Figure 3-10 GIB timing diagram



3.6.4.1 GIB Memory Read

Table 3-9 lists the AC characteristics for GIB memory reads.

Program 1 – for asynchronous memories

Configuration Register	`0x01070001`
Read Program	`0xa000 + wait1`

Program 2 – for devices with RDY handshake

Configuration Register	`0x01070001`
Read Program	`0x8a000 + wait2,` `0x4a000 + wait3`

Table 3-9 GIB memory read AC specification

Symbol	Parameter	Min	Max	Units
TIDLE	CEx inactive from previous cycle to CEx active	(PCLK * 2) – 5.0	-	ns
TACV	CEx active to address, control, and write data valid [1]	-0.5	2.0	ns
TRDV	Memory access time from CEx, control and address valid, given program 1	-	-11 + (PCLK * wait1)	ns
TRDY	CEx active until RDY valid, given program 2 [2]	-	-7.5 + (PCLK * wait2)	ns
TRDY_DVAL	RDY active until data valid, given Program 2	-	2.5 + (PCLK * (wait3 - 2))	ns
TRDY_ACT	RDY active time	PCLK+2	-	ns
TRDY_END	Refer to Table 3-10			

[1] This delay can be increased under program control

[2] RDY valid means active *or* inactive

3.6.4.2 GIB Memory Write

Table 3-10 lists the AC characteristics for GIB memory writes.

Program 3 – for asynchronous memories

Configuration Register	`0x01070001`
Write Program	`0xA9000 + wait4`
	`0x28000 + wait5`

Program 4 – for devices with RDY handshake

Configuration Register	`0x01070001`
Write Program	`0xA9000 + wait4`
	`0x68000 + wait5`

Table 3-10 GIB memory write AC specification

Symbol	Parameter	Min	Max	Units
TIDLE	Control signals inactive from previous cycle to CEx active [1]	(Pclk * 2) - 0.5	-	ns
TACV	CEx active to address, control, and write data valid [2]	-0.5	2.0	ns
TWE	Address and write data valid to WE# active [3]	-	-2 + (PCLK * (wait4 +1))	ns
TRDY	CEx active until RDY valid, given Program 4 [4]	-	-7.5 + (PCLK * wait4)	ns
TRDY_END	RDY active until address and write data invalid, CEx and control inactive	-	-12 + (PCLK * (wait5 + 3))	ns

[1] This configuration register can be used to increase this number.

[2] This delay can be increased under program control by multiples of PCLK.

[3] WE# is any GIB control output signal, gib[41:37,35,34]

[4] RDY valid means active *or* inactive

3.6.5 GIB Bootstrapping Options

In addition to supporting a variety of slave devices, GIB pins 32-35, and 37 are used on power-up to control bootstrapping options; refer to the pin descriptions beginning with “gib[32]” on page 2-5 for information on which pin controls which bootstrap option.

3.6.6 Programmable Parallel Interface Timing

The following sections describe the timing parameters for the various Programmable Parallel Interface (PPI) modes.

3.6.6.1 GMII Mode Timing

Table 3-11 PPI GMII mode AC specification

Symbol	Parameter	Min	Max	Units
T1	Clock period	8.0	8.0	ns
T2	Set-up time of transmit data to PHY	2.5	-	ns
T3	Transmit data clock → q	0.5	5.5	ns
T4	Input set-up on receive data (at receiver)	2.0	-	ns
T5	Input hold on receive data (at receiver)	0.0	-	ns
TJITTER	mac*_gtx_clk long-term jitter	-	±100	ppm

Figure 3-11 PPI GMII TX output timing diagram

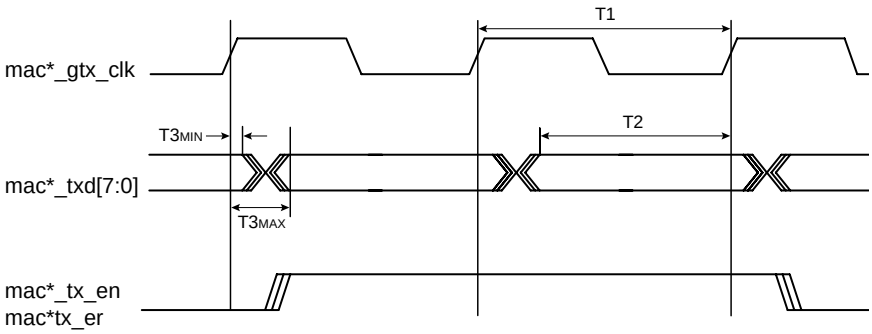
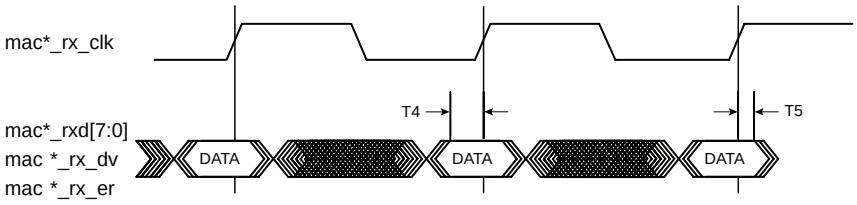


Figure 3-12 PPI GMII RX input timing diagram



3.6.6.2 MII Mode Timing

Table 3-12 lists MII mode timing.

Table 3-12 PPI MII mode AC specification

Symbol	Parameter	Min	Max	Units
T1	Clock period	40	400	ns
T2	Transmit clock → q	0	25	ns
T4	Receive data set-up (at receiver)	10	-	ns
T5	Receive data hold (at receiver)	0	-	ns
TJITTER	mac*_tx_clk long-term jitter	-	±100	ppm

Figure 3-13 PPI MII TX output timing diagram

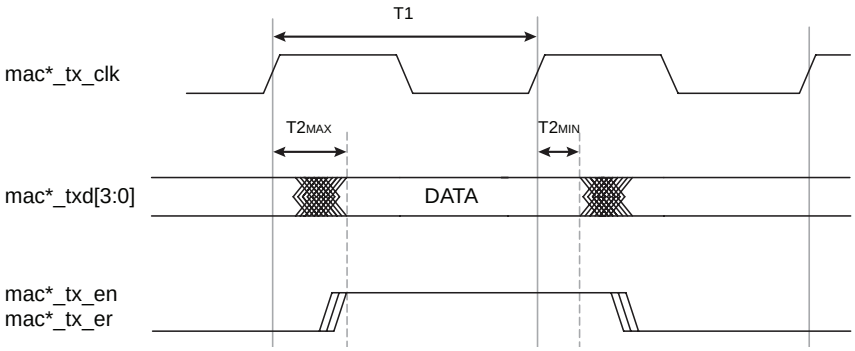
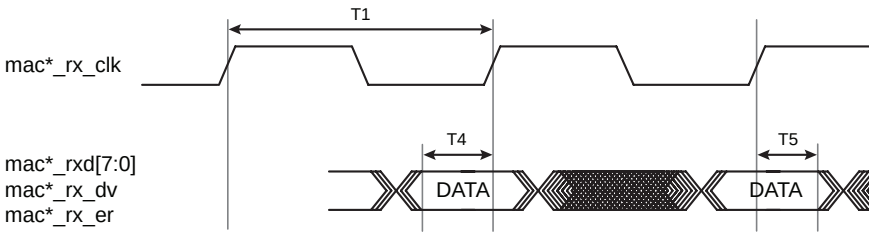


Figure 3-14 PPI MII RX input timing diagram



3.6.6.3 FIFO Mode Timing

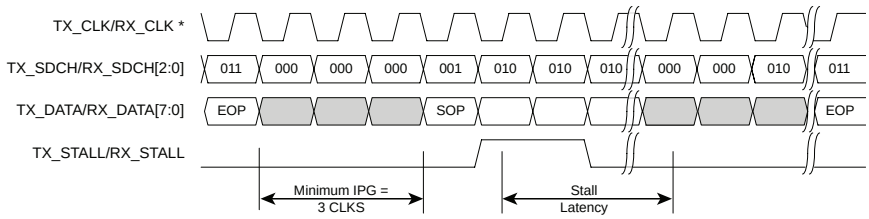
Table 3-13 lists FIFO mode timing.

Table 3-13 PPI FIFO mode AC specification

Symbol	Parameter	Min	Max	Units
T1	Clock period	10	-	ns
T2	Transmit data clock → q	0.50	2.5	ns
T4	Input set-up on mac*_tx_stall	2.10	-	ns
T5	Input hold on mac*_tx_stall	0.50	-	ns
T6	Input set-up on receive data	2.10	-	ns
T7	Input hold on receive data	0.50	-	ns
T8	Rx stall clk → q	2.50	7.50	ns

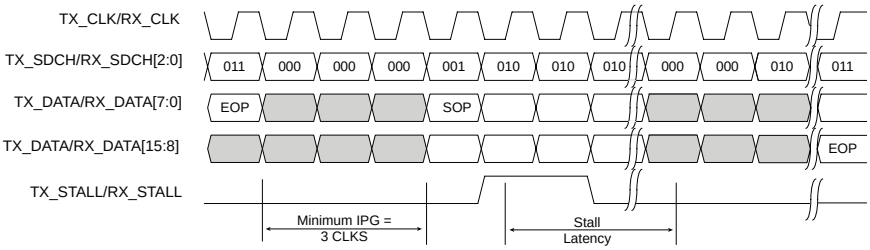
Figure 3-15 illustrates 8-bit MAC-bypass timing, and Figure 3-16 illustrates 16-bit MAC-bypass timing.

Figure 3-15 8-bit MAC-bypass timing



* TX_CLK/RX_CLK *must* be frequency-locked to each other.

Figure 3-16 16-bit MAC-bypass timing



*TX_CLK/RX_CLK *must* be frequency-locked to each other.

In both Tx and Rx directions, the MAC-bypass interface consists of either 8 or 16 bits of data, and 3 bits of side-channel. Table 3-14 lists the side-channel encoding for 8- and 16-bit modes. A stall signal is also available to apply back pressure as needed.

Data integrity checking using a trailing CRC-32 can be optionally enabled. In the transmit direction, if the CRC generation is enabled, an Ethernet Format CRC-32 is appended to each packet, increasing its length by 4 bytes. CRC gen-

Figure 3-17 PPI 8-bit FIFO TX timing diagram

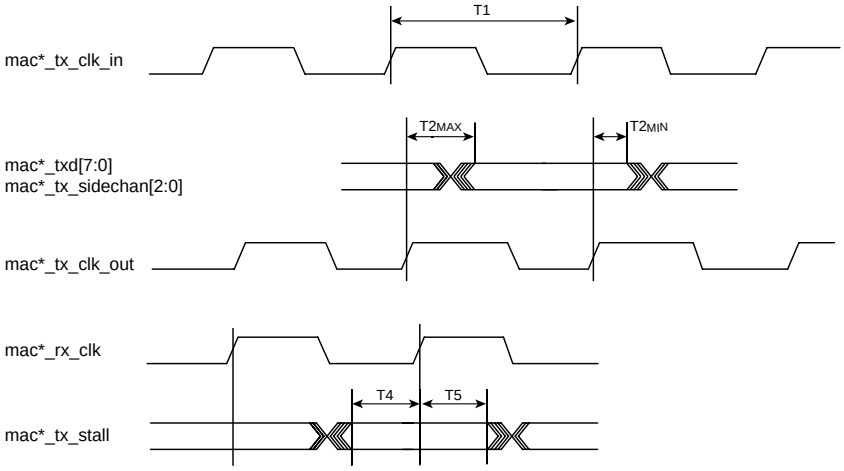


Figure 3-18 PPI 8-bit FIFO RX timing diagram

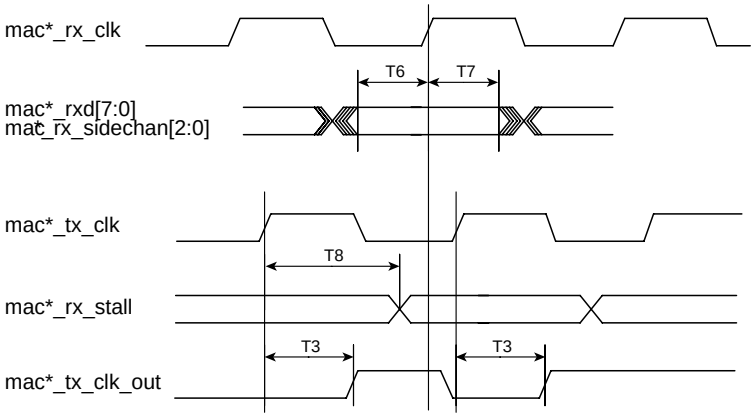


Table 3-14 8-bit and 16-bit MAC-bypass mode side-channel encoding

TX_SDCH RX_SDCH[2:0]	Meaning
000	Idle
001	Start-of-Packet (SOP): data lines contain the first valid data
010	Data Valid
011	End-of-Packet 1 byte valid: Tx and Rx data 7:0 are valid
100	End-of-Packet 2 bytes valid (16-bit mode only): Tx and Rx data 15:8 and 7:0 are valid
101	End-of-Packet Error: Used by the sender to abort a packet
110	Reserved
111	Reserved

eration can be enabled globally or on a per-packet basis. In the receive direction, if the FIFO block is configured to drop packets with an incorrect CRC-32, then MAC-bypass packets with incorrect CRC-32s are dropped.

Keys to Correct MAC-bypass Operation

Following are several key considerations for correct operation in MAC-bypass mode.

- Both the transmit and receive clocks must be frequency-locked to each other.
- The minimum inter-packet-gap (IPG) from the end-of-packet (EOP) to the start-of-packet (SOP) is three interface clock cycles.
- The transmit interface stalls within 3 to 4 clocks of seeing the TX_STALL input go high. The transmit interface treats the TX_STALL input as an asynchronous signal and double-registers it before use.
- The requirement for how fast the link partner must stall, once the RX_STALL output is asserted, is a function of how the receive FIFO watermark registers are set in the FIFO block.
- The minimum packet size is 2 bytes in 8-bit mode, and 3 bytes in 16-bit mode (that is packets must span at least two clock periods)

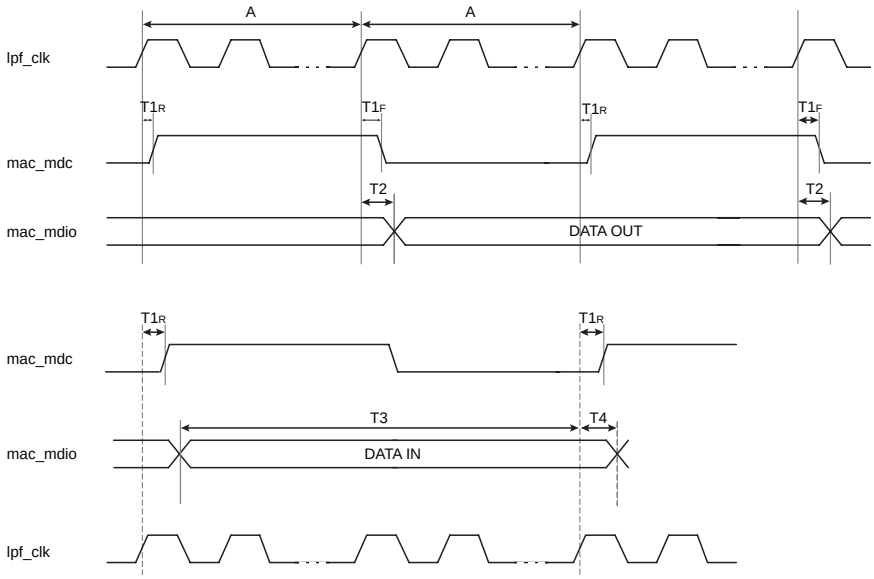
3.6.6.4 MDIO Timing

Table 3-15 lists MDIO timing.

Table 3-15 PPI MDIO AC specification

Symbol	Parameter	Min	Max	Units
T1F	MDC output delay	3.9	8.5	ns
T1R	MDC output delay	4.0	8.8	ns
T2	MDIO output delay	-	2.5	ns
T3	MDIO input set-up	2.7	-	ns
T4	MDIO input hold	2.1	-	ns
A	MDC divider	5	68	-

Figure 3-19 PPI MDIO timing diagram



3.6.7 PCI Interface Timing

Table 3-16 PCI interface timing specification [1]

		66 MHz		33 MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TVAL [2]	pci_clk to Signal Valid Delay	2	6	2	11	ns
TON [2 3]	Float to Active Delay	2	-	2	-	ns
TOFF [2 3]	Active to Float Delay	-	14	-	28	ns
TSU [4 5 6]	Input Setup Time to pci_clk-Bused signals	3	-	7	-	ns
TSU (ptp) [4 5]	Input Setup Time to pci_clk; point-to point signals	5	-	10	-	ns
TH [5]	Input Hold Time from pci_clk	0	-	0	-	ns
TRST [7]	Reset Active Time after power stable	1	-	1	-	ms
TRST-CLK [7]	Reset Active Time after pci_clk stable	100	-	100	-	µs
TRST-OFF [7 8 3]	Reset Active to output float delay	-	40	-	40	ns
TRRSU	pci_req# to pci_rst# setup time	10		10	-	clocks
TRRH	pci_req64# to pci_req# hold Time	0	50	0	50	ns
TRHFA	pci_req64# high to first configuration access	2^{25}	-	2^{25}	-	clocks
TRHFF	pci_rst# high to first pci_frame# assertion	5	-	5	-	clocks

1 All parameters are guaranteed by simulation or characterization.

2 See Figure 3-21. It is important that all driven signal transitions drive to their VOH or VOL level within one TCYC.

3 For purposes of active/float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4 pci_gnt# is a point-to-point signal and has a different input set-up time than do bused signals All other inputs are bused.

5 See Figure 3-20.

6 Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals at the same time. Refer to the *PCI Local Bus Specification* for more details.

7 If pci_m66en is asserted, pci_clk is stable when it meets the requirements in the *PCI Local Bus Specification, Revision 2.2*. pci_rst# is asserted and deasserted asynchronously with respect to pci_clk.

8 All output drivers are floated when pci_rst# is active.

Figure 3-20 PCI input timing diagram

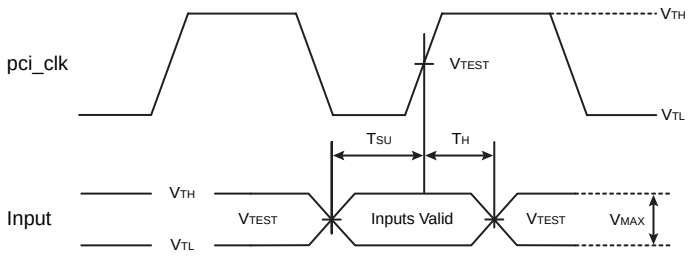
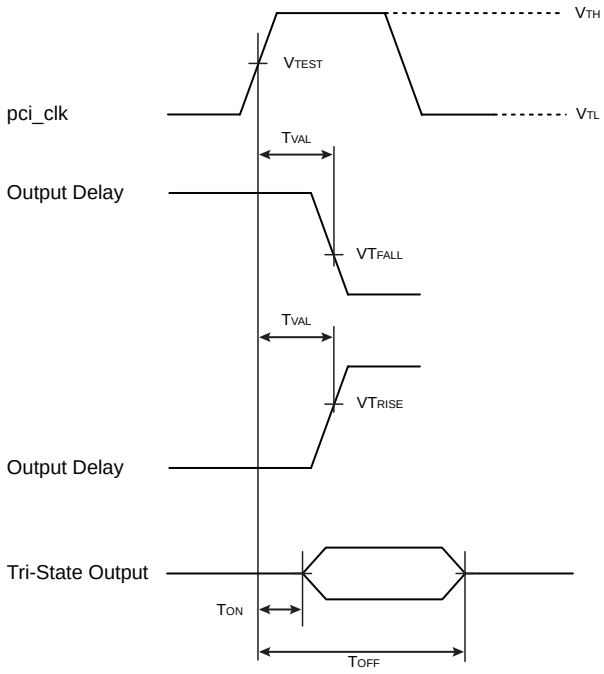


Figure 3-21 PCI output timing diagram



3.6.7.1 PCI Clock Characteristics

Table 3-17 PCI clock characteristics

		66 MHz		33 MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TCYC [1] [2]	pci_clk cycle time	15	30	30	45	ns
THIGH	pci_clk high time	6	-	11	-	ns
TLOW	pci_clk low time	6	-	11	-	ns
— [3]	pci_clk slew rate	1.5	4	1	4	V/ns

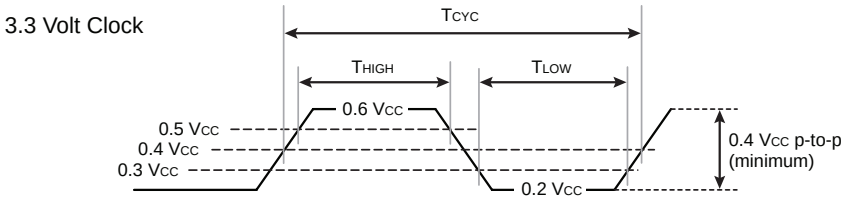
[1] Device operational parameters at frequencies at or under 33 MHz will conform to the *PCI Local Bus Specification, Revision 2.2* in Chapter 4, except the minimum clock frequency is 22.22 MHz.

For all clock frequencies, the frequency may not change except while pci_rst# is asserted or when spread spectrum clocking (SSC) is used to reduce EMI emissions

[2] The minimum clock period must not be violated for any single clock cycle (i.e., accounting for all system jitter).

[3] Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 3-22.

Figure 3-22 PCI clock waveform diagram



3.6.7.2 PCI Measurment Conditions

Table 3-18 PCI measurement parameters

Symbol	Value	Units
VTEST	0.4 * VDD_PCI	V
VTFALL	0.615 * VDD_PCI	V
VTRISE	0.285 * VDD_PCI	V
VTH	0.6 * VDD_PCI	V
VTL	0.2 * VDD_PCI	V

3.6.8 PCI-X Interface Timing

Table 3-19 PCI-X general timing parameters [1]

		PCI-X 133		PCI-X 66		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TVAL [2]	pci_clk to Signal Valid Delay	0.7	3.8	0.7	3.8	ns
TON [2 3]	Float to Active Delay	0	-	0	-	ns
TOFF [2 3]	Active to Float Delay	-	7	-	7	ns
TSU [4 5 6]	Input Setup Time to pci_clk-bused signals	1.2	-	1.7	-	ns
TSU (ptp) [4 5]	Input Setup Time to pci_clk-point to point signals	1.2	-	1.7	-	ns
TH [5]	Input Hold Time from pci_clk	0.5	-	0.5	-	ns
TRST [7]	Reset Active Time after power stable pci_clk	1	-	1	-	ms
TRST-CLK [7]	Reset Active Time after pci_clk stable	100	-	100	-	µs
TRST-OFF [7 8]	Reset Active to output float delay	-	40	-	40	ns
TRRSU	pci_req64# to pci_rst# setup time	10	-	10		clocks
TRRH	pci_rst# to pci_req64# hold Time	0	50	0	50	ns
TRHFA	pci_rst# high to first configuration access	2^{26}	-	2^{26}	-	clocks
TRHFF	pci_rst# high to first pci_frame# Assertion	5	-	5	-	clocks
TPVRH	Power valid to pci_rst# high	100	-	100	-	ms
TPRSU	PCI-X initialization pattern to pci_rst# setup time	10	-	10	-	clocks
TPRH [9]	pci_rst# to PCI-X initialization pattern hold time	0	50	0	50	ns
TRLCX	Delay from pci_rst# low to pci_clk frequency change	0	-	0	-	ns

1 All parameters are guaranteed by simulation or characterization.

2 Refer to Figure 3-24. For timing and measurement condition details, refer to the PCI-X Addendum to the PCI Local Bus Specification document.

3 For purposes of Active/Float timing measurements, the Hi-Z or "off" state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4 Setup time for point-to-point signals applies to pci_gnt# only. All other inputs are bused.

5 See the timing measurement conditions in Figure 3-23.

6 Setup time applies only when the device is not driving the pin. Devices cannot drive and receive signals and pci_frame# at the same time.

7 pci_rst# is asserted and deasserted asynchronously with respect to pci_clk.

8 All output drivers are floated when pci_rst# is active.

9 Maximum value is also limited by delay to the first transaction (TRHFF). The PCI-X initialization pattern control signals after the rising edge of pci_rst# must be deasserted no later than two clocks before the first pci_frame# and must be floated no later than one clock before pci_frame# is asserted.

Figure 3-23 PCI-X input timing diagram

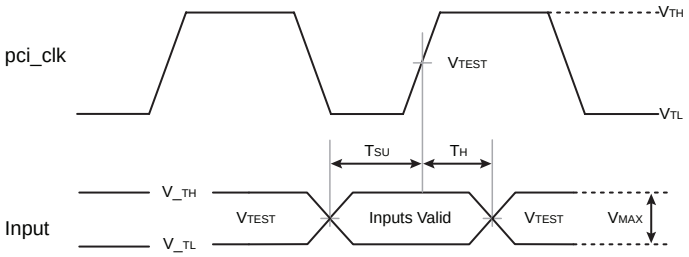
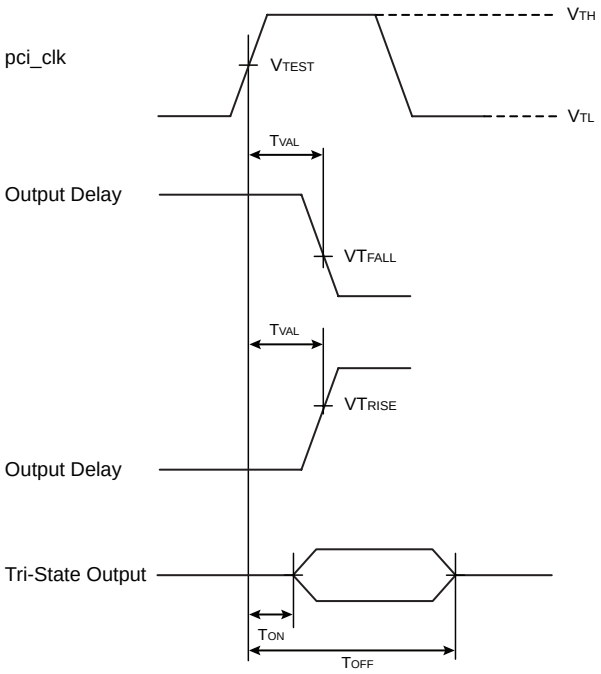


Figure 3-24 PCI-X output timing diagram



3.6.8.1 PCI-X Clock Characteristics

Table 3-20 PCI-X clock timing specification

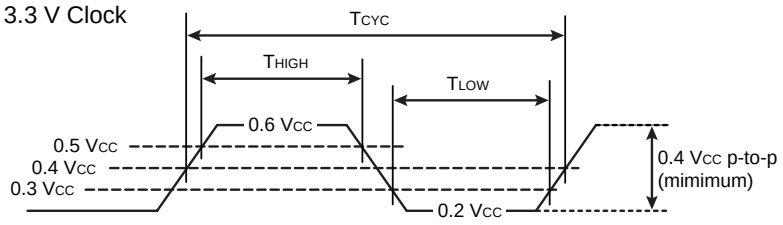
		PCI-X 133		PCI-X 66		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
TCYC [1,2]	pci_clk cycle time	7.5	20	15	20	ns
THIGH	pci_clk high time	3	-	6	-	ns
TLOW	pci_clk low time	3	-	6	-	ns
— [3]	pci_clk slew rate	1.5	4	1.5	4	V/ns

1 For clock frequencies above 33 MHz, the clock frequency may not change beyond the spread-spectrum limits except while pci_rst# is asserted.

2 The minimum clock period must not be violated for any single clock cycle (that is, accounting for all system jitter).

3 This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in Figure 3-25.

Figure 3-25 PCI-X 3.3V clock wave form diagram



3.6.8.2 PCI-X Measurment Conditions

Table 3-21 PCI-X measurement parameters

Symbol	Value	Units
VTEST	0.4 * VDD_PCI	V
VTFALL	0.615 * VDD_PCI	V
VTRISE	0.285 * VDD_PCI	V
VTH	0.6 * VDD_PCI	V
VTL	0.25 * VDD_PCI	V

3.6.9 DDR Timing

The DDR interface was designed for compatibility with JEDEC standard 79C (JESD79C) DDR400 (PC3200) memories. Contact your Stretch representative for a list of approved DDR400 vendors and part numbers.

Figure 3-26 PCI clock skew diagram

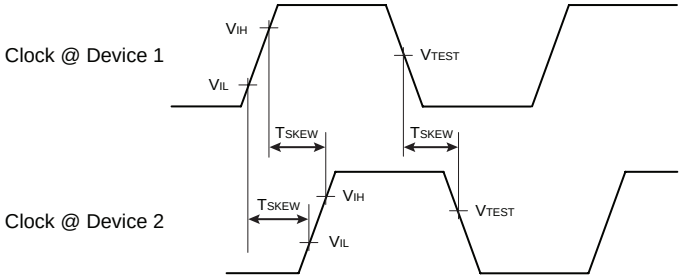


Table 3-22 DDR timing skew

Skew measurement	Skew	Units
Any sdram_ck clock pair to any other sdram_ck clock pair [1]	± 100	ps
Any sdram_dq to any sdram_dq [1 2]	± 275	ps
Any sdram_dqs to any sdram_dqs [1 2]	± 75	ps
Any sdram_addr/command to any sdram_addr/command [1]	± 250	ps

1 Parameter guaranteed by simulation or characterization.

2 Write cycle timing parameter

Table 3-23 DDR SDRAM timing specification

Symbol	Parameter		Min	Max	Units
tCK	sdram_ck cycle time [1]	-3 speed grade	5.0	10.0	ns
		-2 speed grade	6.0	10.0	ns
tCH	sdram_ck high pulse width [1 2]		0.50*tCK - 0.20	0.50*tCK + 0.20	ns
tCL	sdram_ck low pulse width [1 2]		0.50*tCK - 0.20	0.50*tCK + 0.20	ns
tCKS	sdram_ck output skew [1 2]		-100	100	ps
tDQSH	sdram_dqs high pulse width [1 3]		0.50*tCK - 0.20	0.50*tCK + 0.20	ns
tDQSL	sdram_dqs low pulse width [1 3]		0.50*tCK - 0.20	0.50*tCK + 0.20	ns
tDSS	sdram_dqs falling edge to sdram_ck rising edge [1 3 4 5]		0.45*tCK - 500	-	ps
tDSH	sdram_ck rising edge to sdram_dqs falling edge [1 3 4 5]		0.45*tCK - 500	-	ps
tDS	sdram_dq to sdram_dqs (when data becomes valid) [1 3 6 7]		0.25*tCK - 750	-	ps
tDH	sdram_dqs to sdram_dq (when data becomes invalid) [1 3 6 7]		0.25*tCK - 750	-	ps
tCA	sdram_ck to sdram_addr/command [1 8]		0.25*tCK	0.75*tCK	ns
tDVW	Data valid input window [1 9 10 11]		800	-	ps

1 Parameter guaranteed by simulation or characterization.

2 Refer to Figure 3-27 on page 3-25.

3 Write cycle timing parameter.

Figure 3-27 `sdram_ck` output skew

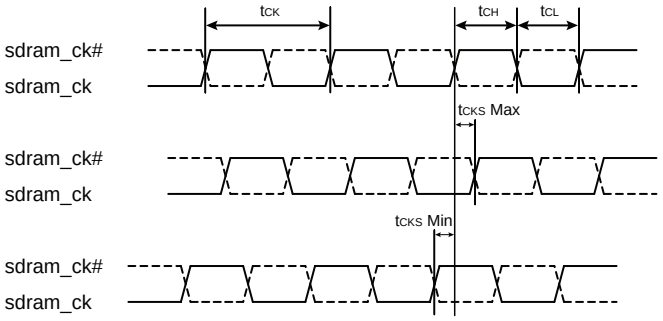


Figure 3-28 tDSS/tDSH timing parameters

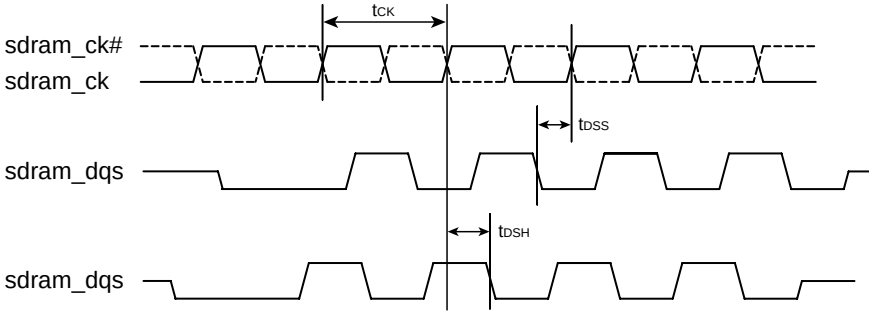


Figure 3-29 tDS/tDH timing parameters

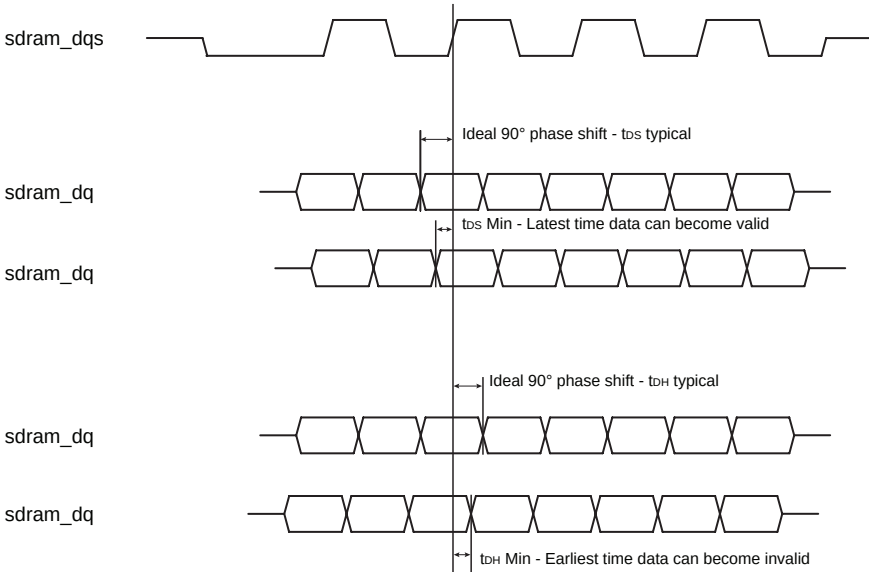


Figure 3-30 `sdram_ck` to `sdram_addr/command` timing parameter

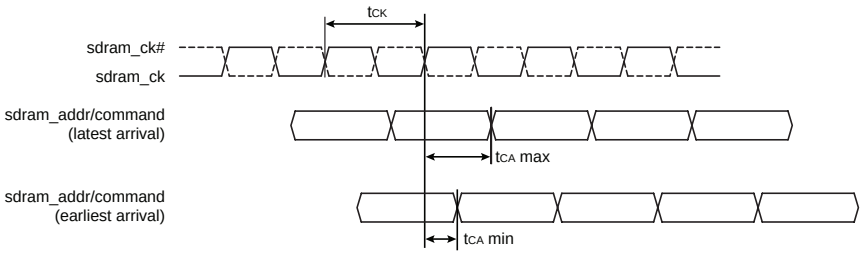
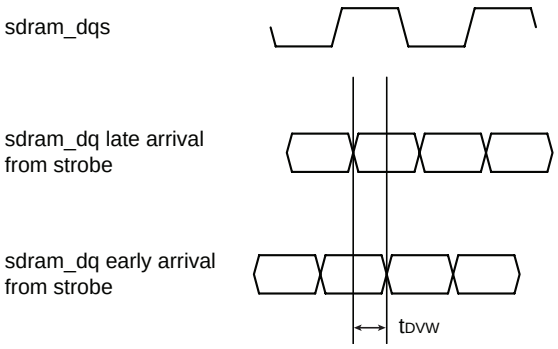


Figure 3-31 DDR read operation



3.6.10 PLL and Clock Timing

The `hclk_sel[2:0]` value is determined by pull-ups and pull-downs on the `gib[34:32]` pins. Table 3-24 and Table 3-25 determine the valid clock frequencies for the processor and LP clocks based on `hclk_sel[2:0]`. Additional values may be available in the future. Contact your Stretch representative if other values are needed.

Table 3-24 Processor and LP clock values based on hclk_sel[2:0]

hclk_sel[2:0]	Processor clock	LP clock
0	Do not use. For internal test only	
1	TREF2_FREQ *15/6	TREF2_FREQ * 15/12
2	TREF2_FREQ * 15/8	TREF2_FREQ * 15/16
3	TREF2_FREQ * 15/10	TREF2_FREQ * 15/20
4	Do not use. For internal test only.	
5	Do not use. For internal test only.	
6	Do not use. For internal test only.	
7	Do not use. For internal test only.	

The PLL timing specification applies to both `pll_refclk` and `pll2_refclk`. The required period for `pll_refclk` is 7.5 ns, which is a frequency of approximately 133.33 MHz.

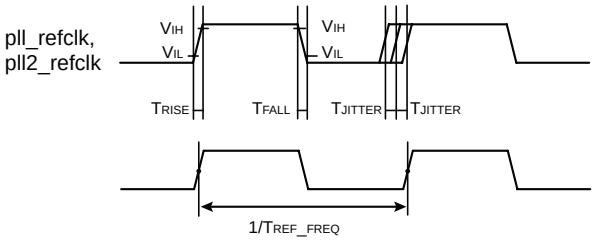
Table 3-25 Clock timing specification

Symbol	Parameter		Min	Max	Units
THP_FREQ	Processor clock frequency	-3 speed grade	200	300	MHz
		-2 speed grade	200	250	MHz
TLP_FREQ	LP clock frequency	-3 speed grade	100	150	MHz
		-2 speed grade	100	125	MHz

Table 3-26 PLL timing specification

Symbol	Parameter	Min	Max	Units
TREF_FREQ	pll_refclk a frequency	133.33	133.33	MHz
TREF2_FREQ	pll2_refclk frequency	120	133.33	MHz
TREF_DUTY	pll_refclk and pll2_refclk duty cycle measured at 50% of VDD_PLL	40	60	%
TREFJITTER	pll_refclk and pll2_refclk jitter	-	±50	ps
TREF_RISE	pll_refclk rise time	-	2	ns
TREF_FALL	pll_refclk fall time	-	2	ns

Figure 3-32 PLL timing diagram



3.6.11 JTAG Timing

The JTAG pins are referenced to VDD_IO.

Table 3-27 JTAG AC timing specification

Symbol	Parameter	Min	Max	Units
tck	Frequency of operation	-	25	MHz
tCYC	tck cycle time	40	-	ns
TL, TH	tck clock high or low time measured at VDD_IO/2	15	-	ns
TRISE, TFALL	tck rise and fall times [1]	-	2	ns
TRST_SU	trst# setup to tck rising edge [2]	10	-	ns
TRUST_HOLD	trst# hold from tck rising edge	10	-	ns
TSU	tms, sdi setup time	10	-	ns

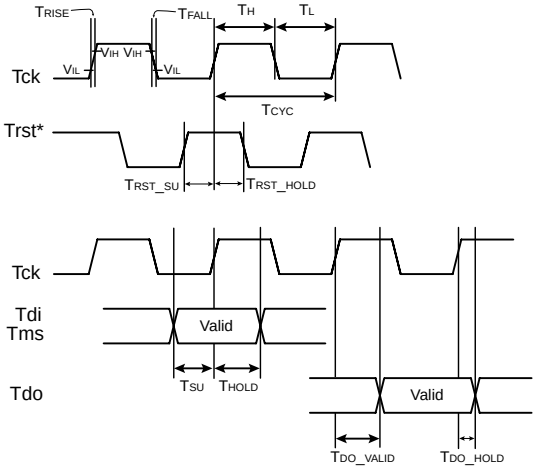
Table 3-27 JTAG AC timing specification

Symbol	Parameter	Min	Max	Units
THOLD	tms, tdi hold time	10	-	ns
TDO_VALID	tck to tdo valid	-	10	ns
TDO_HOLD	tck to tdo hold time	-	-	ns

[1] From VIL to VIH or from VIH to VIL

[2] trst# may be asserted asynchronously, but must be deasserted synchronous to tck.

Figure 3-33 JTAG timing diagram



Appendix A **Ordering Information**

Use the codes in the following diagram for ordering parts from Stretch. Contact your Stretch representative if you have any questions about how to place an order.

Figure A-1 Product ordering code

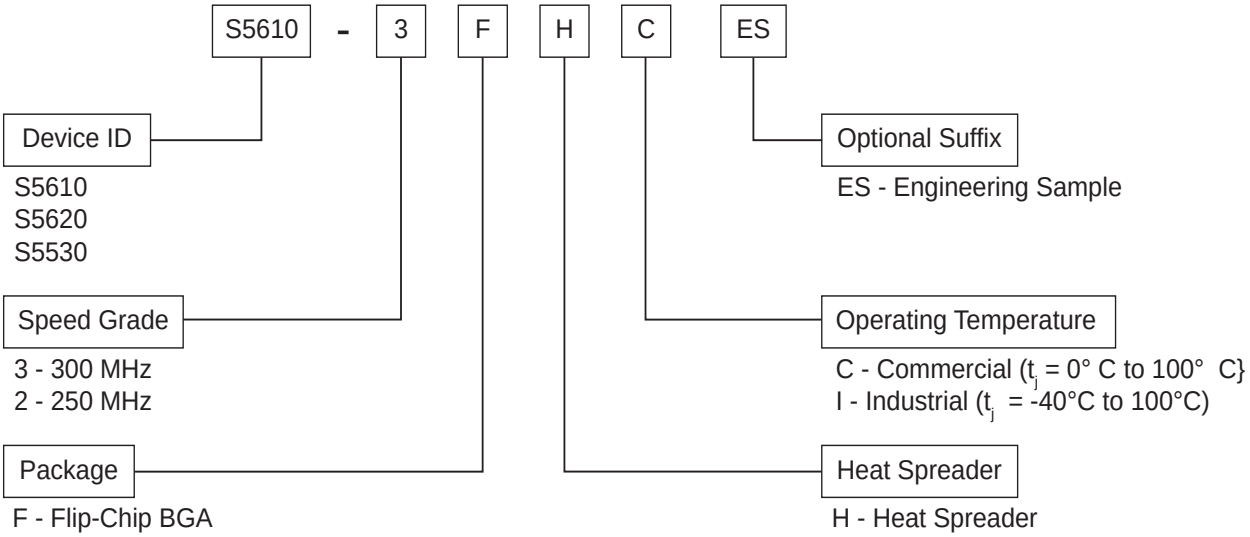


Figure A-2 Product marking