CprE 588 – Embedded Computer Systems

Homework #3

Assigned: April 7

Due: April 16

Directions:

- Please submit this assignment by the due date via WebCT.
- Submissions should be in the form of 1) a PDF file with the writeup and 2) a ZIP file containing any additional necessary material.
- You must submit individual work, although you may collaborate with classmates on the problems. Please acknowledge any such collaboration when submitting.
- Engineering Distance Education students are provided with an automatic one week extension to the due date.
- Some of these questions do not have a strictly correct answer. You will be graded based on how well-formed your arguments are.

1) Specification Modeling in SystemC

Review the "Getting Started with SystemC" course document (link) and make sure that you are able to access and compile specifications using the SystemC libraries. Please use WebCT as a resource if you are having problems.

For the purposes of this assignment we will be following the embedded system design flow as described in the following paper (link): L. Cai et al. "Comparison of SpecC and SystemC Languages for System Design", UC-Irvine Technical Report, May 2003.

Consider the SpecC specification model of the parity checker example that was provided with Homework #2 (link):

(a) Implement the specification (untimed functional) version of this model using SystemC. Submit your source files as a ZIP file to be attached to your writeup. Describe in detail how your SystemC model code differs from the equivalent SpecC version.

(b) Using the same "System-under-Test (SUT)" behavioral structure as was provided with the SpecC parity model, compile your SystemC model and simulate the parity calculation for a sample test input vector. Provide the results of your simulation.

(c) Draw the schematic of your SystemC specification model using a comparable drawing style that is depicted in the L. Cai UC-Irvine technical report linked above. Are there any differences between this schematic and the SCE schematic for the SpecC parity model in Homework #2?

2) Architecture Modeling in SystemC

(a) Refine your SystemC specification model to an IP-assembly (timed function / architectural) model by following the direct guidelines in Section 4 of the L. Cai et al. UC-Irvine technical report. Submit your source files as a ZIP file to be attached to your writeup. Describe the specific steps taken in order to convert your SystemC model.

(b) Compile your new SystemC model and simulate the parity calculation for the sample test input vector that you created in Question 1. Provide the results of your simulation.

(c) Draw the representative schematic for this IP-assembly model. How has it changed from the schematic in Question 1?

3) Communication Modeling in SystemC

(a) Refine your SystemC specification model to a bus-functional (behavior-level / communication) model by following the direct guidelines in Sections 5 and 6 of the L. Cai et al. UC-Irvine technical report. Submit your source files as a ZIP file to be attached to your writeup. Describe the specific steps taken in order to convert your SystemC model.

(b) Compile your new SystemC model and simulate the parity calculation for the sample test input vector that you created in Question 1. Provide the results of your simulation.

(c) Draw the representative schematic for this bus-functional model. How has it changed from the schematic in Question 2?