Consider the following circuit:

\[ z[n] = (x[n] \land y[n]) \lor z[n-1] \lor \overline{y[n]} \]

\[ = (x[n] \lor z[n-1]) \land y[n] \]

Thus, if \( z[n-1] = 0 \) \( \Rightarrow \ z[n] = x[n] \land y[n] \)

\[ z[n-1] = 1 \Rightarrow z[n] = y[n] \]

Now suppose circuit is asynchronous (inputs change randomly) and each gate has unit delay, then does this hold?

Suppose initially \( (x=1, y=0, z=0) \), then \( z \) becomes high within 3 units of \( y \) becoming high?
Hardware Verification

Spec:

Model of AND gate:

Model of NOT gate:

\[ \text{CKT} = \text{AND} \parallel \text{NOT} \parallel \text{NOR1} \parallel \text{NOR2} \]

\[ T_m(\text{CKT}) \leq T_m(\text{spec}) \]

- Typically spec is given as a real-time temporal logic formula.
- "Model checking" is used for verification. (Uses data structure called BDD)