Phillip H. Jones III

Contact Information:

Phillip H. Jones III
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Research Interests:

- Adaptive computing systems
- Reconfigurable hardware
- Embedded systems
- Real-time systems
- Fault tolerant systems
- Microprocessor off-load hardware for application acceleration
- Space-born applications

Education:

Ph.D in Computer Engineering at Washington University (St. Louis), May 2008
M.S in Electrical Engineering, University of Illinois (Urbana-Champaign), May 2002
B.S in Electrical Engineering, University of Illinois (Urbana-Champaign), May 1999

Published Papers:

First Authored Papers

- "Adaptive Thermoregulation for Applications on Reconfigurable Devices," Phillip H. Jones, James Moscola, Young H. Cho, and John W. Lockwood,
  IEEE International Conference on Field Programmable Logic and Applications (FPL)
  Amsterdam, Netherlands, Aug 27-29, 2007. (acceptance rate 21%)

- "Dynamically Optimizing FPGA Applications by Monitoring Temperature and Workloads," Phillip H. Jones, Young H. Cho, and John W. Lockwood,
  IEEE International Conference on VLSI Design (VLSI Design),
  Bangalore, India, Jan 6-10, 2007. (acceptance rate 32%)
  (Best Paper Award)

- "An Adaptive Frequency Control Method Using Thermal Feedback for Reconfigurable Hardware Applications,"
  Phillip H. Jones, Young H. Cho, and John W. Lockwood,

IEEE International Conference on Field Programmable Technology (FPT),
Bangkok, Thailand, Dec 13-15, 2006. (acceptance rate 20%)

- "A Thermal Management and Profiling Method for Reconfigurable Hardware Applications," Phillip H. Jones, John W. Lockwood, and Young H. Cho,
  IEEE International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, Aug 28-30, 2006. (acceptance rate 30%)

- "Liquid Architecture," Phillip Jones, Shobana Padmanabhan, Daniel Rymarz, John Maschmeyer David V. Schuehler, John W. Lockwood, and Ron K. Cytron,
  IEEE IPDPS NGS Workshop, Santa Fe, New Mexico, April 26.

Co-authored Journal Papers

- "Extracting and Improving Microarchitecture Performance on Reconfigurable Architectures," Shobana Padmanabhan, Phillip Jones, David V. Schuehler, Scott J. Friedman, Praveen Krishnamurthy, Huakai Zhang, Roger Chamberlain, Ron K. Cytron, Jason Fritts, and John W. Lockwood,
  International Journal of Parallel Programming,
  Volume 33, Issue 2 - 3, June 2005, Pages 115 - 136.

- "The effects of an ARMOR-based SIFT environment on the performance and dependability of user applications," K. Whisnant, R.K. Iyer, Z.T. Kalbarczyk, P.H. Jones III, D.A. Rennels, R. Some,
  IEEE Transactions on Software Engineering (TSE),
  Volume 30, Issue 4, April 2004, Page(s):257 – 277.

Co-authored Conference and Workshop Papers

- "Cycle-Accurate Microarchitecture Performance Evaluation,"
  Richard Hough, Phillip Jones, Scott Friedman, Roger Chamberlain, Jason Fritts, John Lockwood, Ron Cytron,
  IEEE Workshop on Introspective Architecture (WISA),
  Austin, TX, February 2006.

- "Use of a Soft-Core Processor in a Hardware/Software Codesign Laboratory,"
  Roger Chamberlain, John Lockwood, Saurabh Gayen, Richard Hough, and Phillip Jones, IEEE Intl. Conf. on Microelectronic Systems Education,
  June, 2005.

- "Extracting and Improving Microarchitecture Performance on Reconfigurable Architectures," Shobana Padmanabhan, Phillip Jones, David V. Schuehler, Scott J. Friedman, Praveen Krishnamurthy, Huakai Zhang, Roger Chamberlain, Ron K. Cytron, Jason Fritts, and John W. Lockwood,
  CASES CTCES Workshop,
  Washington DC, September 22, 2004.

Invited Talks:

- **"Adaptive Thermoregulation for Applications on Reconfigurable Devices,"** ECE Department Seminar Invited Talk, Boston University, Boston, MA, December 3, 2007

Research, Industry and Teaching Experience:

Research Experience

- **August 2008 – Present, Iowa State University (Ames, IA),**
  Assistant Professor
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- **January 2008 – August 2008, Washington University (St. Louis, MO),**
  Post-Doc (NIH-funded)
    - Develop and test hardware/software codesigns for a biosequence search application (BLAST)
    - Explore the use of hardware reconfiguration for increasing the performance of BLAST

- **September 2003 - Present, Washington University (St. Louis, MO)**,
  Ph.D research
    - Liquid Architecture (NSF-funded): Responsible for the design of hardware infrastructure necessary to integrate a soft-core SPARC-compatible processor (LEON) into a networked Field Programmable Gate Array (FPGA) based platform (FPX), for processor architecture/micro-architecture level research.
    - Digital Systems Laboratory: CSE465 (Spring 2005)
        - Responsible for hardware infrastructure support
        - Responsible for the design and implementation of most lab assignments
        - Provided general hardware design assistance to students
    - Adaptive computing using temperature feedback for applications implemented in reconfigurable hardware
    - Thermally constrained real-time embedded systems
    - Run-time dynamic reconfiguration on FPGAs

- **September 2000 - December 2001, University of Illinois (Urbana-Champaign, IL),**
  MS research
    - Developed fault injectors for a distributed network fault injection tool (NFTAPE), for use in performing fault tolerance evaluation experiments.

- Summer 2001, Jet Propulsion Laboratory (JPL-NASA)
  - Train JPL employees how to develop fault tolerance evaluation experiments using NFTAPE
  - Assist in the evaluation of several fault injection tools including NFTAPE

Teaching Experience

- Iowa State University (Ames, Iowa)
  - **Embedded Systems Research Skills: CPRE 594 (Spring 2009)**
  - **Reconfigurable Computing: CPRE 583 (Fall 2008)**
- Washington University (St. Louis, Missouri)
  - **Introduction to Computing Tools: CSE100 (G,W,X) (Fall 2007)**
    Note: Course Material developed by Dr. Ronald Loui

Industry Experience

- **June 2005 - August 2005, Intel Corporation (Hillsboro, OR), Summer Intern**
  Developed modifications/extensions to CLIPS (an open source expert systems development infrastructure), to build a proof of concept prototype for the management of system reliability at the firmware level.
- **June 2004 - August 2004, Intel Corporation (Hillsboro, OR), Summer Intern**
  Developed Linux device driver and made Linux kernel modifications to develop a proof of concept prototype to extend the functionality of IA-64 (Itanium-2) based firmware.
- **February 2002 - August 2003, Intel Corporation (Chandler, AZ), Intern**
  - Ran, debugged, and converted regression tests for the validation of a South Bridge I/O chip.
  - Performed initial work to interface two validation environments (C++ based and VHDL based)
- **June 2000 - August 2000, Intel Corporation (Hillsboro, OR), Summer Intern**
  Developed tests to fault grade several modules of the Pentium 4.
- **June 1999 - August 1999, Intel Corporation (Hillsboro, OR), Summer Intern**
  Wrote tests to validate the functionality of modules for a Next Generation I/O (NGIO) networking ASIC.

- **June 1998 - August 1998, Intel Corporation (Hillsboro, OR), Summer Intern**
  Ran regression tests, and helped analyze the results of regression test simulations for the functional validation of a networking ASIC.

- **June 1997 - August 1997, Intel Corporation (Hillsboro, OR), Summer Intern**
  Used VHDL to design a simple interface to allow a generic micro-controller to read/write status and control registers of a generic device

- **June 1996 - August 1996, Intel Corporation (Hillsboro, OR), Summer Intern**
  Initial design of a LED status display, for the front panel of a 10/100 Ethernet system

Students Advised:

- Ph.D. Students

- MS Students

  - Adwait Gupta (Spring 2009 – Present)

  - Ben Armfield (Fall 2008, Graduated, Distance Education, Rockwell Collins)

    - Advised for creative component only

Skill Set:

Programming Languages

- Proficient in VHDL, C++, C, 80x86 assembler, Perl.
- Some experience with ACE middleware, Spice, Verilog, AWK

System Level Development

- Experience with:
    - System on Chip Design (FPGA-based): Soft-core processor (LEON) centric, Network packet processing
    - Socket programming
    - Integration of special purpose hardware via the SPARC V8 coprocessor interface
    - Linux device driver development
    - SPARC and PowerPC instruction sets
- Some experience with: CMOS circuit design, Analog circuit design
- Background in:
    - Embedded real-time system design
    - Fault tolerant system design

Communication Protocols

Familiar with: TCP, UDP, IP, RTP, PCI, PCI-X, PCI-Express, USB, Ethernet, Pentium-4 front-side bus

General Tools

Familiar with: Oscilloscopes, Logic Analyzers, Network/Spectrum analyzers

Course Work:

Computer Systems Performance Analysis, Computer Architecture, Reliable Computer Systems, Digital Systems Design for Testability, CMOS Circuit Analysis and Design, Computer Algorithms, System on Chip Design, Operating Systems, Network Protocols, Data Security (e.g. cryptography algorithms), Multimedia Computing and Networking, Introduction to Languages and the Theory of Computation, Artificial Intelligence, Logic Design, Data Structures, Analog Circuit Analysis and Design, Linear Systems and Signals Analysis, IC Fabrication, Solid-State Electronics, Digital Signal Processing, Radio Frequency Circuit Design, Advanced Electromagnetics, Advanced calculus, Differential equations, Linear algebra, Quantum physics.

Honors:

- Best Paper Award, IEEE International Conference on VLSI Design (VLSI Design), 2007
- Graduate Engineering Minority (GEM) Fellowship (1999-2000, 2003-2004)
- Intel Minority Scholarship (1996-1999)
- High School Perfect Attendance (1992-1995)

Activities:

- IEEE Society Member
- Reviewer:
    - IEEE Transactions on Computers
- University of Illinois Gymnastics team member (1996-1999)
- Capoeira Brazil Martial Arts group member (2003-2005)
- St. Louis Ultimate Frisbee League Summer/Fall (2006, 2007, 2008)