EE 506X – CMOS PHASE LOCKED LOOPS

IOWA STATE UNIVERSITY DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING

Required Text: William F. Egan, Phase-Lock Basics

References: Floyd M. Gardner, Phaselock Techniques, 3rd Ed. and Roland E. Best, Phase-Locked Loops: Design, Simulation, and Applications 5th Ed.

Instructor:

Nathan M. Neihart
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Office: 2132 Coover Hall
Office Hours: **TBD**

Prerequisites: EE 435 or EE 501 (If you are unsure if you meet the prerequisite requirements or would like to take the course despite not meeting the requirements, please see the professor to discuss your situation.)

Course Description (Lecture): Phase-locked loops (PLL) are an integral part of many systems from television to high-speed wireless and wired communication systems. The lecture portion of this class will incorporate both the analysis and design of PLLs and upon completion of this course students will be able to:

1. Identify and analyze PLLs of different types and orders
2. Understand the design trade-offs between different performance metrics including settling time, tuning range, noise, etc.
3. Analyze and design the various PLL sub-components such as phase/frequency detectors, charge pumps, loop-filters, and voltage controlled oscillators
4. Understand the various integration issues and their impacts upon PLL performance

There is also a required laboratory associated with this class in which students will perform transistor-level design and simulation of a full PLL.

Laboratory Description: There is a required laboratory associated with this class. The laboratory sections will consist of weekly laboratory assignments in the beginning. These beginning assignments will focus on ideal modeling and simulation techniques for PLLs and will likely include learning to use VerilogA and/or Matlab Simulink to aid in PLL design. Later in the semester students will be assigned a term project which will consist of the transistor-level design and simulation of a 900 MHz PLL using a commercially available 130 nm CMOS technology. During this time, laboratory sessions will not meet formally, instead students will be allowed to complete the project milestones in a time and manner of their choosing. For this time period, however, the instructor will be available during regular laboratory meeting times to answer any questions and provide any needed assistance. Lab reports will be required for each lab assignment. In addition, a 5-10 minute oral presentation will be given at the end of the semester detailing your PLL design and simulation results.

Students will be using Cadence design tools, which are available on campus, for all circuit design and simulation. While the more specialized simulation tools will be explained, some familiarity with Cadence will be necessary. If you have never used Cadence before please see the instructor. Finally, while the laboratory projects are to be completed individually, students are encouraged to work together.

Homework: There will be approximately ten homework assignments throughout the semester. Homework will be assigned on Mondays and will be due the following Monday by 5:00 pm in my office, unless otherwise noted. While it is encouraged to collaborate with other students, direct copying is not permitted and each student must turn in his or her own complete assignment. All questions regarding homework grading should go to the grader.

Exams: There will be one in-class midterm exam and one final exam for this class. Students will be allowed to bring one page of notes to the midterm and two pages of notes to the final exam (one page is defined as one 8.5" x 11" (or A4) sheet of paper front and back). Otherwise, both exams will be closed book and closed note. The use of any wireless device is strictly prohibited during exams. Exam make-ups will only be considered in extreme circumstances and with prior notification.

Late Policy: No late homework assignments or lab reports will be accepted without prior approval from the instructor.

Grading:

- Homework Assignments: 10%
- Midterm Exam: 20%
- Final Exam: 30%
- Laboratory: 40%
    + Weekly Lab Assignments: 10%
    + Term Project: 25%
    + Final Presentation: 5%

Students with Disabilities: If you have a documented disability and anticipate needing accommodations in this course, please make arrangements to meet with me soon. Please request that a Disability Resources staff send a SAAR form verifying your disability and specifying the accommodation that you will need.