**Page Tables**

Virtual page number: Page offset

- Physical page number: Page offset

Typical values: 16-512 entries, miss-rate: 0.1% - 1%, miss-penalty: 10 - 100 cycles

- **Making Address Translation Fast**
  - A cache for address translations: translation lookaside buffer

  Typical values: 16-512 entries, miss-rate: 0.1% - 1%, miss-penalty: 10 - 100 cycles

- **TLBs and caches**
Modern Systems

- Things are getting complicated!

<table>
<thead>
<tr>
<th>Year</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
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<tr>
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<td>10,000</td>
</tr>
<tr>
<td>100,000</td>
<td>100,000</td>
</tr>
</tbody>
</table>

- Processor speeds continue to increase very fast — much faster than either DRAM or disk access times

Some Issues

- Design challenge: dealing with this growing disparity
  - Prefetching? 3rd level caches and more? Memory design?
Pages 9 to 12

Chapters 8 & 9

(partial coverage)

Interfacing Processors and Peripherals

- I/O Design affected by many factors (expandability, resilience)
- Performance:
  - access latency
  - throughput
  - connection between devices and the system
  - the memory hierarchy
  - the operating system
- A variety of different users (e.g., banks, supercomputers, engineers)

I/O

- Important but neglected
  - “The difficulties in assessing and designing I/O systems have often relegated I/O to second class status”
  - “courses in every aspect of computing, from programming to computer architecture often ignore I/O or give it scanty coverage”
  - “textbooks leave the subject to near the end, making it easier for students and instructors to skip it!”
- GUILTY!
  - we won’t be looking at I/O in much detail
  - be sure and read Chapter 8 in its entirety.
  - you should probably take a networking class!

I/O Devices

- Very diverse devices
  - behavior (i.e., input vs. output)
  - partner (who is at the other end?)
  - data rate
**I/O Example: Disk Drives**

- To access data:
  - seek: position head over the proper track (3 to 14 ms. avg.)
  - rotational latency: wait for desired sector (.5 / RPM)
  - transfer: grab the data (one or more sectors) 30 to 80 MB/sec

**I/O Example: Buses**

- Shared communication link (one or more wires)
- Difficult design:
  - may be bottleneck
  - length of the bus
  - number of devices
  - tradeoffs (buffers for higher bandwidth increases latency)
  - support for many different devices
  - cost
- Types of buses:
  - processor-memory (short high speed, custom design)
  - backplane (high speed, often standardized, e.g., PCI)
  - I/O (lengthy, different devices, e.g., USB, Firewire)
- Synchronous vs. Asynchronous
  - use a clock and a synchronous protocol, fast and small
  - don't use a clock and instead use handshaking

**I/O Bus Standards**

- Today we have two dominant bus standards:

**Other important issues**

- Bus Arbitration:
  - daisy chain arbitration (not very fair)
  - centralized arbitration (requires an arbiter), e.g., PCI
  - collision detection, e.g., Ethernet
- Operating system:
  - polling
  - interrupts
  - direct memory access (DMA)
- Performance Analysis techniques:
  - queuing theory
  - simulation
  - analysis, i.e., find the weakest link (see "I/O System Design")
- Many new developments
Pentium 4

- I/O Options