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HARC: A Heterogeneous Array of Redundant Persistent Clocks for Batteryless, Intermittently-Powered Systems

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Introduction

- Growing number of IoT devices
- Why consider Batteryless ?
- Expensive \implies Inexpensive capacitor
- Limited lifetime \implies Longer lifetime
- Need maintenance in Maintenance free
- Not environment friendly \implies Environment friendly

Batteryless devices have significant benefits for IoT

RF energy harvesting batteryless, intermittent devices

• We consider RF energy harvesting batteryless, intermittent devices



RF Transmitter



Intermittent Computing

- Why Intermittent?
 - Harvested power < Consumed power
- Little/No control when the device is
 on
- No power off-time (TOFF) info
- Need time information for
 - Communication, timestamping data, check for staleness etc.
- Demonstration use-case: Communication



Persistent Clock

- Known decay of charge on capacitance -> estimate power-off time
- MCU charges the capacitor(C) with a GPIO
- ADC reads capacitor voltage





Persistent clocks can be used for time keeping during power-off period

Observation #1



Off-time varies significantly with distance and relative reflection, diffraction, interference, and scattering

Observation #2



Observation #3a – Local Variations



Observation #3b – Systemic Variations



Goal of the work

- Increase the accuracy and reliability of persistent clocks over wide range of off-time
- Resilience to local and systemic variation
- Leverage the energy accuracy trade-off

Insights

- Insight #1: A persistent clock must be able to provide accurate timing information across a wide range of off-times.
- Insight #2: Multiple persistent clocks with heterogeneous decay rates must be used in parallel.
- Insight #3: Multiple redundant and heterogenous clocks need to be used.















HARC SOFTWARE – Estimate Fusion

- HARC-naïve
 - Takes average of time estimates
- HARC-reg



- Lasso regression technique
- HARC-lite
 - Selects a clock based on the slope

Evaluation

- Experimental Setup
- MSP430FR5994 MCU 16 MHz, 8KB SRAM, 256 KB FRAM, 12-bit ADC, 16-bit Timers

















HARC Overheads



HARC-reg 6% runtime overhead; ripe for optimization

HARC Overheads

• Charging Time and energy consumption

Capacitor	Charging Time	Charging Energy
$100 \ \mu F$	$4.5 \mathrm{ms}$	$1.60 \mathrm{~mJ}$
$47 \ \mu F$	$2.7 \mathrm{\ ms}$	$0.686 \mathrm{~mJ}$
$10 \ \mu F$	$1.1 \mathrm{ms}$	$86.078~\mu\mathrm{J}$
$1 \ \mu \mathrm{F}$	$125 \ \mu s$	$6.90 \ \mu J$
$0.1 \ \mu F$	$10.8 \ \mu s$	$0.884 \ \mu J$
$0.01 \ \mu F$	$10.4 \ \mu s$	$0.0972~\mu\mathrm{J}$
HARC Total	$4.5 \mathrm{\ ms}$	$2.38 \mathrm{~mJ}$

Energy vs. Accuracy Trade-offs

HARC can provide a timing mechanism with an energy vs accuracy setting that is dynamically adjustable after deployment.



LMP: Lifecycle Management Protocol

 Two nodes decides on a rendezvous and schedule their on-times



Lifecycle Management Protocol (LMP) Evaluation



HARC increases the probability of communication between intermittently-powered nodes

Conclusion

- HARC heterogeneous, redundant array of capacitor-based persistent clocks
 - Variation-resilient high accuracy over a wide range of power offtimes
 - Demonstrated the feasibility and effectiveness of HARC using experimental evaluations on a HARC prototype
 - HARC use case communication between two intermittentlypowered nodes