Revisiting Time Remanence Clocks for Energy Harvesting Wireless Sensor Nodes

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ABSTRACT

The intermittent operation of batteryless devices makes it difficult to have time information in order to synchronize and communicate between these devices. In this paper, we analyze time remanence clocks and compare them with real time clocks in keeping time when device looses power. We argue that the time remanence clocks can keep the time for longer period but there are several challenges the needs to be considered. In particular, high chip and board variation, coupled with a *fixed*, proportionally small window of time measurement inhibit the effectiveness of remanence clocks. This paper proposes the possibility of constructing small, customized SRAM-based time remanence clocks to provide an increased measurement window.

KEYWORDS

EHWSN, energy-harvesting, time-remanence clocks, SRAM retention, batteryless, intermittent-devices, RTC

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1 INTRODUCTION

Moving away from conventional tethered and battery powered devices, energy harvesting devices have proven to be a major step forward in the field of wireless sensor networks. The self-sufficient and self-sustainable operation of these devices make them useful to deploy in remote terrains with virtually unlimited lifetimes. These devices utilize energy harvested from alternative energy resources such as solar, RF, vibrations, etc. However, keeping time on intermittent batteryless devices is a challenging task, despite being critical for synchronization and communication between the devices.

In order to track time on energy harvesting systems when the device is powered off, there are two main approaches: ultra low power (ULP) real time clocks (RTCs) and persistent clocks based on remanence decay. The Time and Remanence Decay in SRAM (TARDIS) [3] is a software-based technique that calculates the time elapsed during a power failure based on the percentage of decayed SRAM cells. The TARDIS divides the SRAM cell's decay curve in three stages: stage 1 denotes that no decay has occurred, stage 2 is when actual cell decay occurs, and stage 3 is when all SRAM cells has been decayed. In Custom Time and Remanence Decay (CusTARD) [3], a capacitor is used to estimate the time based on the discharge curve. However, this approach requires a dedicated pin and ADC to read the capacitor voltage. During periods when the batteryless device does not have sufficient power to be on, even state-of-the-art research RTCs cannot keep time as long as basic TARDIS-like approaches.

In this paper, we revisit TARDIS-like time remanence clocks, identify current challenges faced by such clocks, and propose possible solutions.

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2 A CASE FOR SRAM-BASED TIME REMANENCE DECAY CLOCKS

To compare RTCs and SRAM-based time remanence decay clocks, we mathematically modeled a system with a capacitor of 1μF that acts as an energy store during off periods and a load of either an active RTC or SRAM leakage of an time remanence clock. All clocks start below the minimum operating voltage of the microcontroller which is 1.8V for MSP430G2553. The RTC consumes power according to the RTCs in [2]. From the Figure 1, the 1.5nW, and 0.55nW RTC can work for 3880 and 7580 seconds respectively.

For modeling of SRAM, we used CACTI-P, configured to keep leakage power to minimum, which gives the total leakage power of SRAM structure while retaining data. We assume a conservative baseline data retention voltage (DRV) of 250mV [3] (i.e., all cells retain data at 250mV under typical conditions). Under these conditions, a 64-byte SRAM at the 65nm technology node retains data for at least 10600 seconds with 0.604 nW leakage power. We observe that an unoptimized time remanence clock built in 65nm technology could measure 39.84% longer than best research clock. Additionally, the time remanence decay clock will also be more resilient to fluctuations in voltage since RTCs can have catastrophic errors if voltage dips below Vmin while time remanence clocks will have errors proportional to voltage noise.

3 TIME REMANENCE CLOCK CHALLENGES

Retention curve variations: For SRAM cell decay time measurement similar to TARDIS, we have written 242B (maximum safely used fraction of SRAM) to SRAM before a node loses power, and read the 242B back when device starts again. This experiment was done on 15 different MSP430G2553 boards to see the effect of retention curve variations as shown in Figure 2. Each board's power was controlled by another microcontroller board supplying power through a diode. The temperature value of each measurement was recorded

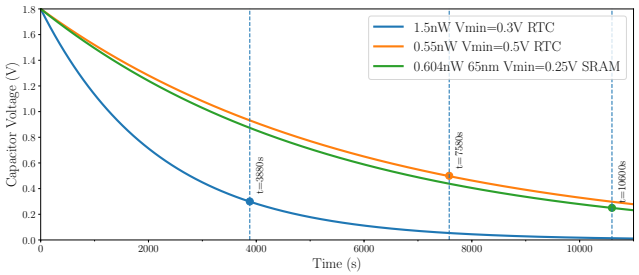

Figure 1: A 1μF capacitor discharging through state-of-the-art ULP RTCs and an SRAM-based time remanence clock. State-of-the-art research RTCs cease to reliably work before an SRAM-based time remanence approach.

by the on-board temperature sensor and was always within a degree of 78F. We observed variation in the start and end time of stage 2 (i.e., the active clock stage). This means that individual boards in a system cannot even measure the same time ranges for synchronization. Additionally, we can see that there are often cases where the decay percentage does not monotonically increase with increased power-off time making a basic TARDIS-like approach more inaccurate in stage 2. We observe that this is a function of interactions between the PCB board and the MCU chip since Figure 2 also shows results for the same chips inserted into different PCB boards resulting in qualitatively different retention curves.

Limited, fixed active clock range: TARDIS-like systems provide the most time information in the stage 2. Unfortunately, for a given chip and board (i.e., amount of capacitance) this active clock period is fixed and can be proportionally small relative to the size of stage 1. If the desired application constraints do not align well with this window or the boards have significant variation (e.g. different devices are deployed in different temperature conditions), a basic remanence clock will not be able to provide enough timing information for communication.

4 OVERCOMING CHALLENGES

Bit-cell-aware decay encoding and decoding: The MCU and board variations come from the individual cells decay behavior. Some cells start to decay early and then show no decay later, others show random variations after decay starts, while others show random behavior even when they are fully decayed (stage 3). To overcome this problem, we can create bins of cells that have similar distributions and use the vector of bin decay fractions as the index into the time table, resulting in a more reliable stage 2 time value.

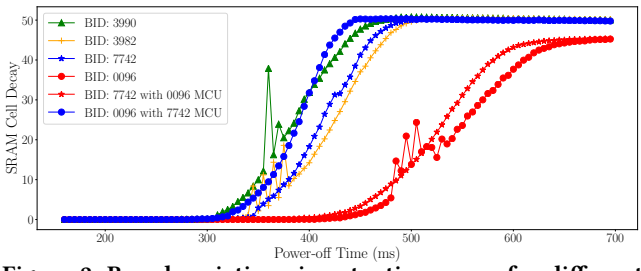

Figure 2: Board variations in retention curve for different MSP430 chips and different PCB boards. Board retention time varies both by chip and by PCB board.

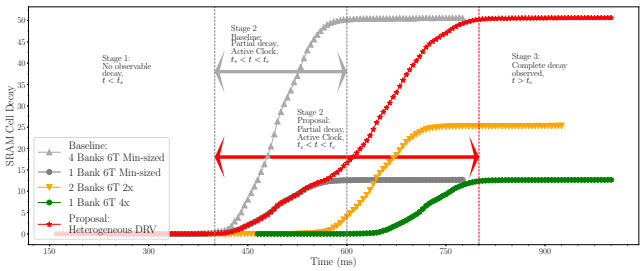

Figure 3: Fraction of total SRAM cells observed as decayed. Homogeneous four bank 6T min-sized SRAMs have half the stage 2 (i.e., active clock) period as a heterogeneous approach.

Programmable capacitor arrays: To adjust the start time and duration of stage 2 (i.e., active clock) period in time remanence clocks, we propose using an array of runtime programmable capacitors such as those presented by [1]. Although the maximum retention time is dictated by the maximum capacitance of the programmable array, this approach allows a knob to adapt to the variation between devices by reducing the start of stage 2 of devices that naturally have longer decay time. This adaptation can be used to adjust the clock dynamically in software as changing harvesting conditions or device temperatures impact the duration of time that can be accurately measured. This change can be based on the limited information of whether previous readings were in stage 1 or stage 3. Interestingly, this approach is also effective for CusTARD-like clocks.

Heterogeneous DRV SRAM banks: As an approach to increase the duration of stage 2, we propose to have SRAM memory consisting of banks of cells where each bank has a different distribution of DRVs so that cells in some banks will decay sooner and some will decay later. Effectively this widens the aggregate distribution of cell retention times which will increase the range of stage 2. In Figure 3, we show a baseline four-banked SRAM with a retention distribution same as the 7742. We then upsize two banks to 2x 6T SRAM cells and one bank to 4x 6T SRAM cells which decreases the DRV distribution of those banks [4] and, thus, increases their retention time distribution. The result is stage 2 length that is twice as long as the original TARDIS approach.

5 CONCLUSION

This paper argued that time remanence clocks can tolerate a longer power loss than state-of-the-art RTCs. Unfortunately, time remanence clocks come with less precision, board variations, and a *fixed*, relatively limited window of time measurement. Therefore, we proposed solutions to reduce/tolerate variation and extend the active clock period of time remanence clocks.

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