CprE 281: Digital Logic
Midterm 1: Friday Sep 25, 2015

Student Name:                      Student ID Number:

Lab Section:  Mon 9-12(N)  Mon 12-3(P)  Mon 5-8(R)  Tue 11-2(U)
(circle one) Tue  2-5(M)  Wed 8-11(J)  Wed 6-9(Y)  Thur 11-2(Q)
                 Thur  2-5(L)  Thur 5-8(K)  Fri 11-2(G)

1. True/False Questions (10 x 1p each = 10p)

(a) I forgot to write down my name, student ID, and lab section. TRUE / FALSE
(b) It is possible to build a NOT gate with a 2-to-1 multiplexer. TRUE / FALSE
(c) It is possible to build an AND gate with a 2-to-1 multiplexer. TRUE / FALSE
(d) It is not possible to build an OR gate with a 2-to-1 multiplexer. TRUE / FALSE
(e) It is possible to build a NOT gate with an XOR gate. TRUE / FALSE
(f) $\overline{a} \cdot \overline{c} + a \cdot c = 1$ TRUE / FALSE
(g) $x \cdot y + \overline{x} = x + y$ TRUE / FALSE
(h) $(\overline{x + y}) \cdot (\overline{x + y}) = \overline{x}$ TRUE / FALSE
(i) $x + (y + z) = (x + y) + z$ TRUE / FALSE
(j) $x + y = \overline{x + y}$ TRUE / FALSE

2. Three-Variable K-map (5p)

Draw the K-map and derive the minimum SOP expression for $f(a,b,c) = \Sigma m(0, 1, 3, 5)$
3. Truth Tables \((5p + 10p = 15p)\)
(a) Draw the truth table for the Boolean function that has the following K-map

(b) Draw the truth table for the Boolean function \(F = A \cdot C + B \cdot \overline{D} + C \cdot D\)
4. Number Conversions (4 x 5p each = 20p)

(a) Convert $10011011_2$ to decimal

(b) Convert $178_{10}$ to binary

(c) Convert $156_7$ to octal:

(d) Convert $6253_8$ to hexadecimal
5. Verilog Module (10p)

Write a Verilog module for the 4-to-1 multiplexer shown below.

Hint: \[ F = \overline{X} \overline{Y} A + \overline{X} Y B + X \overline{Y} C + X Y D \]
6. Circuit to Circuit Conversion (3 x 5p = 15p)

(a) Write the expression for the function $F$ given by this circuit (don't simplify it yet).

(b) Use the theorems of Boolean algebra to simplify the expression from part (a).

(c) Draw the circuit for your expression from part (b). Label all inputs and outputs.
7. Derive the minimum SOP expression using a K-map (3 \times 5p = 15p)

(a) Draw the K-map for the following function

\[ F(a,b,c,d) = \Sigma m(0, 6, 8, 13) + D(3, 5, 7, 11, 15) \]

(b) Use the K-map to derive the minimum-cost SOP expression for the function F.

(c) Draw the circuit diagram for the minimum expression from part (b).
8. NAND/NOR Logic (5p + 5p = 10p)
(a) Using only NAND gates, draw the logic circuit that corresponds to the truth table shown below. Hint: Start by writing and then modifying the expression for F.

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
<th>F</th>
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<tr>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
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</tbody>
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(b) Redraw the following logic circuit using only NOR gates.
9. Joint Optimization (3 x 5p = 15p)
The outputs f and g of a two-output circuit are specified with the following expressions:

\[ f(a, b, c, d) = \Sigma m(0, 2, 5, 7, 8, 12, 15) + D(4, 10, 13) \]
\[ g(a, b, c, d) = \Sigma m(2, 7, 8, 9, 10, 13, 15) + D(0, 6, 14) \]

(a) Draw the K-map for f and the K-map for g

(b) Derive the jointly optimized SOP expressions for f and g such that the two expressions share two implicants. Note that these are not necessarily prime implicants.

(c) Draw the diagram for the jointly optimized circuit. Indicate which logic gates are shared by drawing arrows that point to them. Label all inputs and outputs.
10. More K-maps (3 x 5p = 15p)
(a) Draw the K-map for the function \( F(A,B,C,D) = BD + BCD + ABC + ABCD + BD \)

(b) Derive the minimal sum-of-products (SOP) expression for \( F \).

(c) Redraw the K-map from (a). Derive the minimal product-of-sums (POS) expression for \( F \).
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<tr>
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<th>Max</th>
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<tr>
<td>2. Three-variable K-map</td>
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<tr>
<td>3. Truth Tables</td>
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<tr>
<td>4. Number Conversions</td>
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<td>5. Verilog Module</td>
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<td>6. Circuit to Circuit</td>
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