CprE 281: Digital Logic
Midterm 1: Monday Sep 30, 2013

Student Name:                   Student ID Number:

Lab Section: Mon 9-12(N), Tue 2-5(M), Wed 8-11(J), Thu 2-5(L), Thu 5-8(K), Fri 11-2(G) (circle one)

1. True/False Questions (10 x 1p each = 10p)
   (a) I forgot to write down my name and student ID number. TRUE / FALSE
   (b) A NOT gate can have two but not three inputs. TRUE / FALSE
   (c) A NAND gate can have four inputs. TRUE / FALSE
   (d) AND followed by NOT is equivalent to a NAND. TRUE / FALSE
   (e) NOR followed by NOT is equivalent to XOR. TRUE / FALSE
   (f) VHDL is the same as Verilog HDL. TRUE / FALSE
   (g) Minimization with a K-map always produces a unique solution. TRUE / FALSE
   (h) It is possible to build a NOT gate with a NOR gate. TRUE / FALSE
   (i) It is possible to build an AND gate with two NOT gates. TRUE / FALSE
   (j) It is possible to build a NOR gate with 6 CMOS transistors TRUE / FALSE

2. Boolean Expressions (5 x 1p each = 5p)

Write the value (0 or 1) for each Boolean expression, given the initial conditions.

\( X = 1 \)
\( Y = 0 \)
\( Z = 1 \)

   (a) \((X + Y)Z\)
   (b) \((ZX + YZ)X\)
   (c) \((XX + YY + ZZ)(XY + XZ + YZ)\)
   (d) \((XY + YX)(YZ + ZY)\)
   (e) \((X + Y + Z)(XYZ)\)
3. Truth Tables (5p + 10p = 15p)
Use a truth table to show that the following Boolean expressions are equivalent.

(a) \( b \cdot c + a \cdot b + \overline{a} \cdot c = \overline{a} \cdot c + a \cdot b \)

(b) \( (a \cdot b + a \cdot c)(a \cdot b + a \cdot d) = a(b + c \cdot d) \)
4. Number Conversions  (4 x 5p each = 20p)

(a) Convert $123_{15}$ to decimal

(b) Convert $312_4$ to binary

(c) Convert $\text{CAFE}_{16}$ to octal

(d) Convert $134_{10}$ to binary:
5. Chip Implementation (10p)

Implement the Boolean function $f = (a + b + \overline{d})(b + \overline{c})$ using the three chips shown below. Add the necessary wires and labels to get the desired result.
6. From Logic Circuit to Verilog Code (10p)

Write a Verilog module for the following logic circuit.
7. Derive the minimum **POS** expression using a K-map (10p + 5p = 15p)

(a) Use a K-map to derive the minimum-cost POS expression for \( f = \overline{x} (y + z) + x \cdot y \)

(b) Draw the circuit diagram for the minimum expression.
8. Derive the minimum SOP expression using a K-map (10p + 5p = 15p)

(a) Use a K-map to derive the minimum-cost SOP expression for the following function
\[ f = \Sigma m(1, 3, 5, 7, 9, 14) + D(2, 11, 12, 13) \]

(b) Draw the circuit diagram the minimum expression.
9. NAND/NOR Logic \( (5p + 10p = 15p) \)

(a) Redraw the following logic circuit using only NAND gates.

(b) Redraw the original logic circuit from (a) using only NOR gates.
10. Boolean Logic (15p)
Use the theorems of Boolean algebra to simplify the following expression:
\[
\overline{x_1} \overline{x_2} x_3 + \overline{x_1} x_2 \overline{x_3} + x_1 x_2 x_3 + x_1 \overline{x_2} x_3 + x_1 \overline{x_2} x_3 + x_1 x_2 x_3 + x_1 x_2 x_3 + x_1 x_2 x_3
\]