Name and Std No.: ____________________________  Lab Section: ____

Date: ________________

PRELAB:
Refer to Chapter 5 in your textbook and the lab instructions to complete your pre-lab. Please read all the material and complete the circuit diagrams before you come to the lab.

Q1. Draw the circuit diagram for the SR Latch using NOR Gates for Section 2.0 in the space below.

Q2. Draw the circuit diagram for the SR Latch using NAND Gates for Section 2.0 in the space below.
Q3. Draw the circuit diagram for the D Latch using NAND Gates and a NOT gate for Section 3.0 in the space below.

Q4. Draw the circuit diagram for the Master-Slave D Flip-Flop for Section 4.0 using the D latches you built in the previous step in the space below. The flip-flop should be triggered by the negative edge of the clock.
Q5. Draw the circuit diagram for the Positive-Edge-Triggered D Flip-Flop using NAND gates for Section 4.0 in the space below.

LAB:

2.0 Complete the characteristic table for both versions of the SR latch. Do both versions function properly as a latch?

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Keep State</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( Q = )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( Q = )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Restricted Combination</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>( Q = )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>( Q = )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>( Q = )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Hardware results demonstrate a good circuit. TA Initials: NOR_____ NAND_______
3.0 Complete the timing diagram below for your Gated D Latch. What is the difference between this gated latch and the previous basic latches?

\[
\begin{array}{c}
\text{Clk} \\
\text{D} \\
\text{Q} \\
\hline
\end{array}
\]

Hardware results demonstrate a good circuit. TA Initials: ______

4.0 Complete the timing diagram below for your Negative-Edge-Triggered D Flip-Flop.

\[
\begin{array}{c}
\text{Clk} \\
\text{D} \\
\text{Q} \\
\text{~Q} \\
\hline
\end{array}
\]

Hardware results demonstrate a good circuit. TA Initials: ______

Complete the timing diagram below for your Positive-Edge-Triggered D Flip-Flop.

\[
\begin{array}{c}
\text{Clk} \\
\text{D} \\
\text{Q} \\
\text{~Q} \\
\hline
\end{array}
\]

Hardware results demonstrate a good circuit. TA Initials: ______