

NAME: Pooja Nitin Mhapsekar
DEGREE: M.S.
MAJOR: Computer Engineering
DATE: January 14, 2013 4:00 p.m.
PLACE: 2222 Coover Hall
MAJOR PROFESSOR: Phillip Jones

Title: FPGA-based acceleration of the RMAP short read mapping tool.

Abstract:

Bioinformatics is a quickly emerging field. Next generation sequencing technologies are producing data up to several gigabytes per day, making bioinformatics applications increasingly computationally intensive. In order to achieve greater speeds for processing this data, various techniques have been developed. These techniques involve parallelizing algorithms and/or spreading data across many computing nodes composed of devices such as Microprocessors, Graphics Processing Units (GPUs), and Field Programmable Gate Arrays (FPGAs).

In this thesis, an FPGA is used to accelerate a bioinformatics application called RMAP, which is used for Short-Read Mapping. The most computationally intense function in RMAP, the read mapping function, is implemented on the FPGA's reconfigurable hardware fabric. This is a first step in a larger effort to develop a more optimal hardware/software co-design.

The platform used to develop this design is the Convey HC-1 Computer System, with the short-read mapping functionality implemented in hardware on one of the four Xilinx Virtex 5 FPGAs available in the system. The hardware design was evaluated by varying different input parameters, such as genome size, and number of reads. The implementation results show a speed-up of up to 5x for the short-read mapping function of RMAP.