Title:

Lagrangian Relaxation Based Multi-threaded Discrete Gate Sizer For Resistive Inteconnects

Abstract:

Accurate delay analysis with distributed RC delay can be computationally expensive, and can contribute the majority of the total runtime for gate sizers. Recent works have shown that Lagrangian relaxation based gate sizers have produced designs with the lowest power on average. But they are also very slow due to a large number of expensive timing updates spread across several tens of iterations. In this paper we develop a Lagrangian relaxation based discrete gate sizer for fast timing and power reduction by swapping the gate sizes and the threshold voltages.

Our gate sizer is multi-threaded and is equipped with parallelization enabling techniques, namely, mutual exclusion edge (MEE) assignment and directed acyclic graph (DAG) based netlist traversal. MEE are dummy edges assigned to reduce dependencies among gates sharing one or more common fan-ins. DAG based netlist traversal facilitates simultaneous resizing of gates belonging to different topological levels. Our Lagrange multiplier update strategy enables rapid convergence of our timing recovery and power recovery algorithms. To reduce the runtime of timing updates, we propose a simple and fast-to-compute effective capacitance model, and use existing fast-to-compute models for delay and slew. We further propose mechanisms to calibrate each one of these models to improve their accuracy. By calibrating the internal timing models only twice, our proposed gate sizing flow facilitates extremely fast design optimization.

We benchmark our gate sizer using the ISPD 2012 and 2013 gate sizing contest benchmark suites. Compared to the state-of the-art gate sizer, our proposed gate sizer is on average 15x faster and the optimized designs have 2.5% higher leakage power. Since we trade-off timing accuracy for larger runtime speedup, our optimized designs have small timing violations.