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Techniques suitable for on chip implementation and ADC Built-in Self-test solutions for low cost and accurate ADC testing

Abstract

As the development of System on Chip (SoC) technique, more different functions are integrated on a single chip. Testing such complex devices needs more complex and expensive measurement instruments and long testing time. Specifically, test cost of analog and RF circuits is considered as one of the challenges in the International Technology Roadmap for Semiconductors (ITRS) reports. Analog to digital converter (ADC) is one of the most important analog and mixed signal (AMS) blocks in SoC. Accurate and cost-effective testing of ADCs becomes significantly more challenging, as more functions are implemented in SoC and as customers demanding higher performance. In addition, lack of access to internal analog nodes, difficulty in maintaining signal integrity driving accurate signals on and off chip make testing of these every harder. Therefore, rising test cost and testability of deeply embedded ADCs and other analog and AMS circuits are two of challenges.

Instrumentation cost and test time are the two most significant contributors of the total ADC test cost. Researches on new techniques for reducing either part of the test cost are valuable. In addition to reducing the cost of traditional ADC testing procedure, practical low-cost Built-In Self-Test (BIST) is another way to reduce test cost. Not only reduce test cost, BIST can also address the testability problem of deeply embedded ADCs.

This work presents new techniques for reducing ADC test cost and a practical low cost BIST solution. The first technique is testing ADC spectral performance without dedicated hardware and data acquisition, which almost eliminates test cost of spectral performance test while maintaining the accuracy. The second technique is testing ADCs' noise performance from DNL existing test data, which also greatly reduce the noise test cost. The third technique is testing ADC spectral performance in real time with data acquisition, which dramatically reduces computation complexity and test time. All these techniques were developed from rigorous theory analysis and validated with experiments. Although these techniques are validated with stand alone ADC measurements, they all have potentials to be implemented on chip for ADC BIST. In the proposed BIST solution, low overhead stimulus generators and control scheme are designed with small transistor count. The BIST is implemented in transistor level. Combined Cadence and Matlab simulation results showed the BIST was able to test a 16-bit ADC to 16 bit accuracy level. These results demonstrate that accurate BIST of deeply embedded AMS blocks may be practically implemented on chip with very low overhead.