**Power Conversion Techniques in Nanometer CMOS Technologies for Low-Power Applications**

**Abstract**

As System-on-Chip (SoCs) in nanometer CMOS technologies grow larger, the power management process within these SoCs becomes very challenging. In the heart of this process lies the challenge of implementing energy-efficient and cost-effective DC-DC power converters. To address this challenge, this thesis studies in details three different aspects of DC-DC power converters and proposes potential solutions. First, to maximize power conversion efficiency, loss mechanisms must be studied and quantified. For that purpose, we provide comprehensive analysis and modeling of the various switching and conduction losses in low-power synchronous DC-DC buck converters in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operation, including the case with non-rail gate control of the power switches. Second, a DC-DC buck converter design with only on-chip passives is proposed and implemented in 65-nm CMOS technology. The converter switches at 588 MHz and uses a 20-nH and 300-pF on-chip inductor and capacitor respectively, and provides up to 30-mA of load at an output voltage in the range of 0.8–1.2 V. The proposed design features over 10% improvement in power conversion efficiency over a corresponding linear regulator while preserving low-cost implementation. Finally, a 40-mA buck converter design operating in the inherently-stable DCM mode for the entire load range is presented. It employs a Pulse Frequency Modulation (PFM) scheme using a Hysteretic-Assisted Adaptive Minimum On-Time (HA-AMOT) controller to automatically adapt to a wide range of operating scenarios while minimizing inductor peak current. As a result, compact silicon area, low quiescent current, high efficiency, and robust performance across all conditions can be achieved without any calibration.