**ABSTRACT**

Modern mixed-signal SoCs integrate a large number of sub-systems in a single nanometer CMOS chip. Each sub-system typically requires its own independent and well-isolated power supply. However, to build these power supplies requires many large off-chip passive components, and thus the bill of material, the package pin count, and the printed circuit board area and complexity increase dramatically, leading to higher overall cost. Conventional (single-frequency) Single-Inductor Multiple-Output (SIMO) power converter topology can be employed to reduce the burden of off-chip inductors while producing a large number of outputs. However, this strategy requires even larger off-chip output capacitors than single-output converters due to time multiplexing between the multiple outputs, and thus many of them suffer from cross coupling issues that limit the isolation between the outputs.

In this thesis, a Dual-Frequency SIMO (DF-SIMO) buck converter topology is proposed. Unlike conventional SIMO topologies, the DF-SIMO decouples the rate of power conversion at the input stage from the rate of power distribution at the output stage. Switching the input stage at low frequency (~2 MHz) simplifies its design in nanometer CMOS, especially with input voltages higher than 1.2 V, while switching the output stage at higher frequency enables faster output dynamic response, better cross-regulation, and smaller output capacitors without the efficiency and design complexity penalty of switching both the input and output stages at high frequency. Moreover, for output switching frequency higher than 100 MHz, the output capacitors can be small enough to be integrated on-chip. A 5-output 2-MHz/120-MHz design in 45-nm CMOS with 1.8-V input targeting low-power microcontrollers is presented as an application. The outputs vary from 0.6 to 1.6 V, with 4 outputs providing up to 15 mA and one output providing up to 50 mA. The design uses single 10-H off-chip inductor, 2-nF on-chip capacitor for each 15-mA output and 4.5-nF for the 50-mA output. The peak efficiency is 73%, Dynamic Voltage Scaling (DVS) is 0.6 V/80 ns, and settling time is 30 ns for half-to-full load steps with no observable overshoot/undershoot or cross-coupling transients. The DF-SIMO topology enables realizing multiple efficient power supplies with faster dynamic response, better cross-regulation, and lower overall cost compared to conventional SIMO topologies.