**Design for Manufacturability in Advanced Lithography technologies**

Abstract

As the technology nodes keep shrinking following Moore's law, lithography becomes increasingly critical to the fabrication of integrated circuits. The 193nm ArF immersion lithography (193i) has been a common technique for manufacturing integrated circuits. However, the 193i with single exposure has finally reached its printability limit at the 28nm technology node. To keep the pace of Moore's law, design for manufacturability (DFM) is demonstrated to be effective and cost-efficient. The concept of DFM is to modify the design of integrated circuits in order to make them more manufacturable. Tremendous efforts have been made for DFM in advanced lithography technologies. In general, the progress can be summarized in four directions. (1) Advanced lithography process by novel patterning techniques and next-generation lithography; (2) High performance lithography simulation approach in mask synthesis; (3) Physical design methodology with lithography manufacturability awareness; (4) Robust design flow integrating emerging PD challenges.

Accordingly, we propose our research topics in those directions.

(1) Throughput optimization for self-aligned double patterning (SADP) and e-beam lithography based manufacturing of 1D layout. In this work, we solve the problem of e-beam shot minimization subject to bounded line-end extension constraints. Compared with the previous work, 1000x speedup is demonstrated in the experiments.

(2) Design of efficient rasterization algorithm for all-angle mask patterns in inverse lithography technology. In this work, a look-up table based rasterization algorithm is developed, which has good shift-invariant property and 500x speedup compared with conventional approach.

(3) SADP-aware detailed routing. In this work, a color pre-assignment is applied for our SADP-aware detailed routing framework, which offers routing with the best QoR compared with other state-of-the-art academic lithography-aware detailed routers.

(4) SADP-aware detailed routing with consideration of double via insertion and via manufacturability. In this work, we extend our SADP-aware detailed routing to further consider double via insertion and via manufacturability. The overheads of these extra considerations are kept minimal.

(5) Pin accessibility driven detailed placement refinement. In this work, the problem of pin access in detailed routing is solved in the earlier design stage, i.e., detailed placement. A detailed placement refinement is proposed to refine placement by cell flipping, adjacent cell swap, and cell shifting to improve pin access. The two-phase refinement is solved by dynamic programming and linear programming.