The title is "High performance algorithm for large scale placement problem".

The abstract is:

"Placement is one of the most important problems in electronic design automation.  An inferior placement assignment will not only affect the chip's performance but might also make it nonmanufacturable by producing excessive wirelength, which is beyond available routing resources. Although placement has been extensively investigated for several decades,  it is still a very challenging problem mainly due to that design scale has been dramatically increased by order of magnitudes and the increasing trend seems unstoppable. In modern design, chips commonly integrate millions of gates that require over tens of metal routing layers. Besides, new manufacturing techniques bring out new requests leading to that multi-objectives should be optimized simultaneously during placement.

Our research provides high performance algorithms for placement problem.  We propose (i) a core wirelenght-driven engine called POLAR, which is  the fastest one among its competitors and can produce competitive solution quality;  (ii) an efficient routability-driven placer called POLAR 2.0, which is built on POLAR; (iii) an ultra-fast wirelength-driven engine called POLAR 3.0, which is also built on POLAR and can make full use of multi-core system; (iv) some simple and  efficient triple patterning lithography (TPL) aware detailed placement algorithms."