Title- LowLEAC: Low Leakage Energy Architecture for Caches

Abstract-

With the ever-decreasing feature sizes, static power dissipation has become a major concern in computing devices. On-chip memories are a major contributor towards the processor's leakage power dissipation due to their large transistor count. This thesis proposes Low Leakage Energy Architecture for Caches (LowLEAC) to minimize the static or leakage power dissipation in caches made of CMOS SRAM cells. This technique is based on turning off  lines of the L1 data cache that are not used in the recent past to avoid leakage power dissipation in them. The cache memory is implemented using CMOS compatible non-volatile SRAM cell called cNVSRAM. The cNVSRAM cell works as a conventional SRAM in the regular mode and saves the data in a non volatile back up when a cache line is turned off  or put in the sleep mode. The non-volatile back up mode helps improve the dependability of the cache and also avoids the penalty occurred due to loss of data from the inactive cache lines. With a minimal area penalty, LowLEAC achieves around 18% reduction in leakage power with almost no compromise in the performance. LowLEAC is a suitable architecture for cache memory in mobile computing devices with limited battery size as well as a means to reduce cooling costs incurred large server systems.